VITELIC

V51C64 FAMILY
HIGH PERFORMANCE LOW POWER
65,536 x 1 BIT
CMOS DYNAMIC RAM

	V51C64-10	V51C64L-10	V51C64-12	V51C64L-12	V51C64-15	V51C64L-15
Maximum Access Time (ns)	100	100	120	120	150	150
Minimum Cycle Time (ns)	160	160	190	190	245	245
Maximum Column Address Access Time (ns)	35	35	45	45	55	55

Features

- Low power dissipation for the V51C64-12
  - Operating current—35 mA (max.)
  - Standby current, TTL—1.5mA (max.)
- Extended refresh and CMOS standby current for the V51C64L
  - Refresh period, Standby Mode—64 ms (max.)
  - Standby current, CMOS—50 μA (max.)
- Average soft error rate less than 10 FITs (0.001%/1000 hours)
- Ripplemode operation for a sustained data rate up to 15.3 MHz
- Low input/output capacitance
- High reliability plastic 16-pin DIP
- VICMOS III Technology

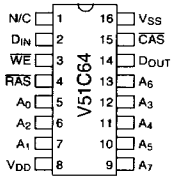
The Vitelic V51C64 is a high speed 65,536 bit CMOS Dynamic Random Access Memory. Fabricated with Vitelic's VICMOS III technology, the V51C64 offers features not provided by an NMOS technology: Ripplemode, fast usable speed, low power, and an average soft error rate of less than 10 Failures In Time (FITs). The V51C64 is ideally suited for applications such as graphic display terminals, battery operated systems, and any application where high performance is required.

Featuring Ripplemode Operation

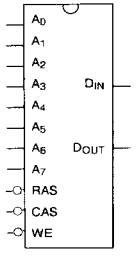
Ripplemode operation allows access of up to 256 bits at a 50 ns/bit rate with random or sequential addresses within a single row. Thus, a continuous data rate of over 15 million bits per second can be achieved. The V51C64 offers high performance with relaxed system timing requirements for fast usable speed. In addition, the fast $\overline{RAS}$ and $\overline{CAS}$ access times are compatible with high performance microprocessors without using WAIT state operation.

The V51C64L offers a standby current of 8 μA when $\overline{RAS} \geq V_{DD} - 0.5V$. During a $\overline{RAS}$-only refresh cycle, the V51C64L extends the refresh period to 64 ms to reduce power consumption to typically 116 μW for data retention. The V51C64 comes in a 16-pin plastic dual-in-line package. All inputs, outputs and control signals are TTL compatible. The input and output capacitances are significantly lowered to reduce system drive requirements.

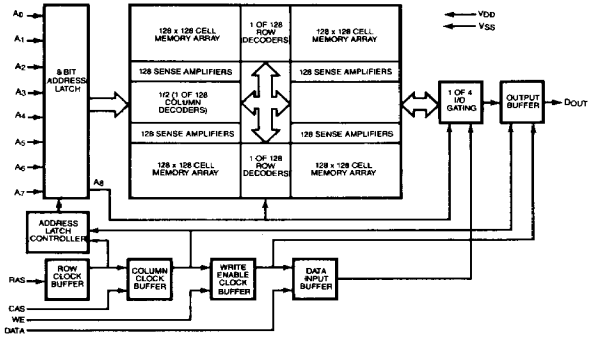
PIN CONFIGURATION
(Top View)



LOGIC SYMBOL



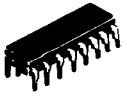
BLOCK DIAGRAM



PIN NAMES

A_{0-7}	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	Power +5V
V_{SS}	Ground

DP-16



Absolute Maximum Ratings *

Ambient Temperature Under Bias	−10° to +80°C
Storage Temperature Plastic	−55°C to +125°C
Voltage on Any Pin except V_{DD} Relative to V_{SS}	−2.0V to 7.5V
Voltage on V_{DD} Relative to V_{SS}	−1.0V to 7.5V
Data Out Current	50 mA
Power Dissipation	1.0 W

D.C. and Operating Characteristics[1]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Speed	V51C64 Limits			V51C64L Limits			Unit	Test Conditions	Notes
			Min.	Typ[2]	Max.	Min.	Typ[2]	Max.			
$\|I_{LI}\|$	Input Load Current (any input)				1			1	µA	V_{IN} = V_{SS} to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State				10			10	µA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IH}, D_{OUT} = V_{SS} to V_{DD}	
I_{DD1}	V_{DD} Supply Current, Operating	−10		27	37		27	37	mA	t_{RC} = t_{RC}(min)	3,4
		−12		23	35		23	35			
		−15		20	30		20	30			
I_{DD2}	V_{DD} Supply Current, TTL Standby			0.4	1.5		0.4	0.8	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}, all other inputs ≥ −0.5V	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Cycle	−10		24	37		24	37	mA	t_{RC} = t_{RC}(min)	4
		−12		20	35		20	35			
		−15		18	30		18	30			
I_{DD4}	V_{DD} Supply Current, Ripplemode	−10		18	37		18	37	mA	t_{PC} = t_{PC}(min)	3,4
		−12		17	35		17	35			
		−15		16	30		16	30			
I_{DD5}	V_{DD} Supply Current, Standby Output Enabled			1	3		1	2	mA	$\overline{CAS}$ and V_{IL}, $\overline{RAS}$ at V_{IH}, all other inputs ≥ −0.5V	3
I_{DD6}	V_{DD} Supply Current, CMOS Standby				2		0.008	0.05	mA	$\overline{RAS}$ ≥ V_{DD} −0.5V, $\overline{CAS}$ at V_{IH}, all other inputs ≥ −0.5V	
V_{IL}	Input Low Voltage (all inputs)		−1.0		0.8	−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)		2.4		V_{DD+1}	2.4		V_{DD+1}	V		
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	6
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = −5 mA	6

NOTES:

1. All voltages referenced to V_{SS}.
2. Typical values are at T_A = 25°C and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max) is measured within a maximum of two transitions per address input per random cycle, one transition per access cycle for Ripplemode.
5. Specified V_{IL} (min) is steady state operation. During transitions, the inputs may overshoot to −2.0V for periods not to exceed 20 ns.
6. Test conditions apply only for D.C. Characteristics. A.C. parameters specified with a load equivalent to two TTL loads and 100 pF.

* Operations at or above the absolute maximum ratings may effect device reliability.

Capacitance[1]

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, Data In	—	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	5	pF
C_{OUT}	Data Out	—	5	pF

NOTE:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V}$$

with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. Characteristics[1, 2, 3]

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

Read, Write, Read-Modify-Write and Refresh Cycles

JEDEC Symbol	Standard Symbol	Parameter	V51C64(L)-10		V51C64(L)-12		V51C64(L)-15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{REL1DOV}$	t_{RAC}	Access Time From $\overline{RAS}$		100		120		150	ns	4,5
$t_{CEL1DOV}$	t_{CAC}	Access Time From $\overline{CAS}$		20		25		30	ns	5,6,7
t_{CAVDOV}	t_{CAA}	Access Time From Column Addresses		35		45		55	ns	
t_{DR}	t_{REF}	Time Between Refresh		4		4		4	ms	8
$t_{REH2REH1}$	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		85		ns	
$t_{CEH2CEH1}$	t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		20		ns	
$t_{CEH2REH1}$	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	–20		–20		–20		ns	
$t_{REL1CEL1}$	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	80	30	95	35	120	ns	9
$t_{REL1CEL2}$	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		ns	
$t_{RAVREH1}$	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
$t_{REL1RAV}$	t_{RAH}	Row Address Hold Time	15		20		25		ns	
$t_{CAVCEH1}$	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
$t_{CEL1CAV}$	t_{CAH}	Column Address Hold Time	15		20		25		ns	
t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	10
$t_{CEH2DOZ}$	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	0	25	ns	

NOTES:
1. All Voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as a $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms for the V51C64, and greater than 64 ms for the V51C64L).
3. A.C. Characteristics assume t_T = 5 ns.
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If $t_{RCD} > t_{RCD}$ (max) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Load = 2 TTL loads and 100 pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max).
7. If $t_{ASC} < [t_{CAA}$ (max) – $t_T]$, then access time is defined by t_{CAA} rather than by t_{CAC}.
8. The V51C64L extends the refresh period to 64 ms during $\overline{RAS}$-only refresh cycles.
9. t_{RCD} (max) is specified for reference only.
10. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. Characteristics (cont'd.)

Read and Refresh Cycles

JEDEC Symbol	Standard Symbol	Parameter	V51C64(L)-10		V51C64(L)-12		V51C64(L)-15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{REH1REH1}$	t_{RC}	Random Read Cycle Time	160		190		245		ns	
$t_{REL1REL2}$	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	ns	
$t_{CEL1CEL2}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width (Read Cycle)	20	75000	25	75000	30	75000		
$t_{CEL1REL2}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		30		ns	
$t_{WEH2CEH1}$	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
$t_{CEH2WEH1}$	t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0		0		0		ns	11
$t_{REH2WEH1}$	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	20		20		20		ns	11
$t_{CAVREL2}$	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	35		45		55		ns	

Write Cycle

JEDEC Symbol	Standard Symbol	Parameter	V51C64(L)-10		V51C64(L)-12		V51C64(L)-15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{REH1REH1}$	t_{RC}	Random Write Cycle Time	160		190		245		ns	
$t_{REL1REL2}$	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	150	75000	ns	
$t_{CEL1CEL2(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width (Write Cycle)	30	75000	35	75000	40	75000	ns	
$t_{CEL1REL2(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	30		35		40		ns	
$t_{WEL1CEH1}$	t_{WCS}	Write Command Set-up Time	0		0		0		ns	12
$t_{CEL1WEL2}$	t_{WCH}	Write Command Hold Time	20		25		30		ns	
$t_{WEL1WEH2}$	t_{WP}	Write Command Pulse Width	20		25		30		ns	
$t_{WEL1REL2}$	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		40		ns	
$t_{WEL1CEL2}$	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		40		ns	
$t_{DIVCEH1}$	t_{DS}	Data-In Set-Up Time	0		0		0		ns	
$t_{CEL1DIV}$	t_{DH}	Data-In Hold Time	20		25		30		ns	

NOTES:

11. Either t_{RCH} or t_{RRH} must be satisfied.
12. t_{CWD}, t_{WCS}, t_{RWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If none of the above conditions are satisfied, the condition of the data out is indeterminate.

A.C. Characteristics (cont'd.)

Read/Modify/Write Cycle

JEDEC Symbol	Standard Symbol	Parameter	V51C64(L)-10		V51C64(L)-12		V51C64(L)-15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{REH1REH1}$ (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	195		230		280		ns	
$t_{REL1REL2}$ (RMW)	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	135	75000	160	75000	185	75000	ns	
$t_{CEL1CEL2}$ (RMW)	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	50	75000	60	75000	70	75000	ns	
$t_{REL1WEH1}$	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns	12
$t_{CEL1WEH1}$	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		30		ns	12
$t_{CAVWEH1}$	t_{AWD}	Column Address to $\overline{WE}$ Delay	35		45		55		ns	12

Ripplemode Cycle [13]

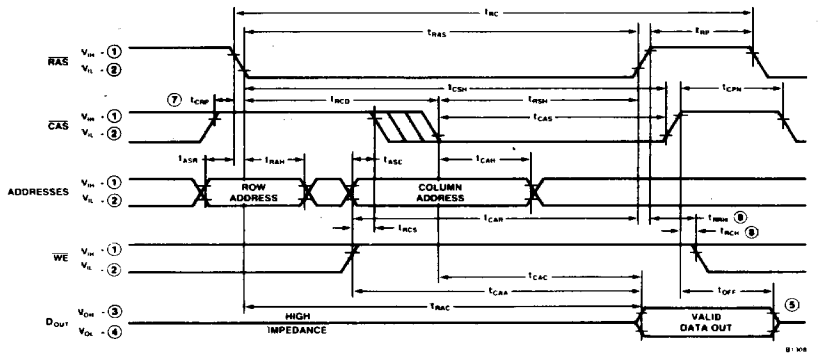
JEDEC Symbol	Standard Symbol	Parameter	V51C64(L)-10		V51C64(L)-12		V51C64(L)-15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
$t_{CEH2DOV}$	t_{CAP}	Access Time From Column Precharge		45		55		65	ns	
$t_{CEH1CEH1}$ (R)	t_{PC}	Ripplemode Read or Write Cycle Time	50		60		70		ns	
$t_{CEH2CEH1}$ (R)	t_{CP}	Ripplemode $\overline{CAS}$ Precharge Time	10		15		20		ns	
$t_{REL1REL2}$ (R)	t_{RPM}	Ripplemode $\overline{RAS}$ Pulse Width		75000		75000		75000	ns	
$t_{CEH1CEH1}$ (RRMW)	t_{PCM}	Ripplemode Read-Modify-Write Cycle Time	85		100		115		ns	

NOTES:

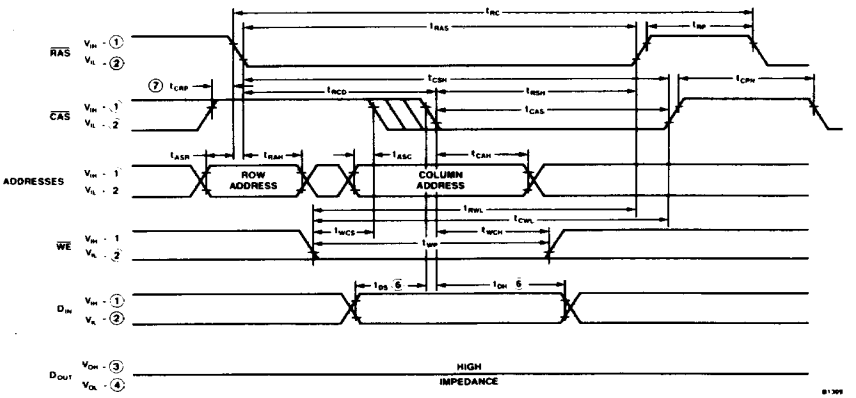
12. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If none of the above conditions are satisfied, the condition of the data out is indeterminate.
13. All previously specified A.C. characteristics are applicable.

Waveforms

Read Cycle



Write Cycle



Notes:

1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

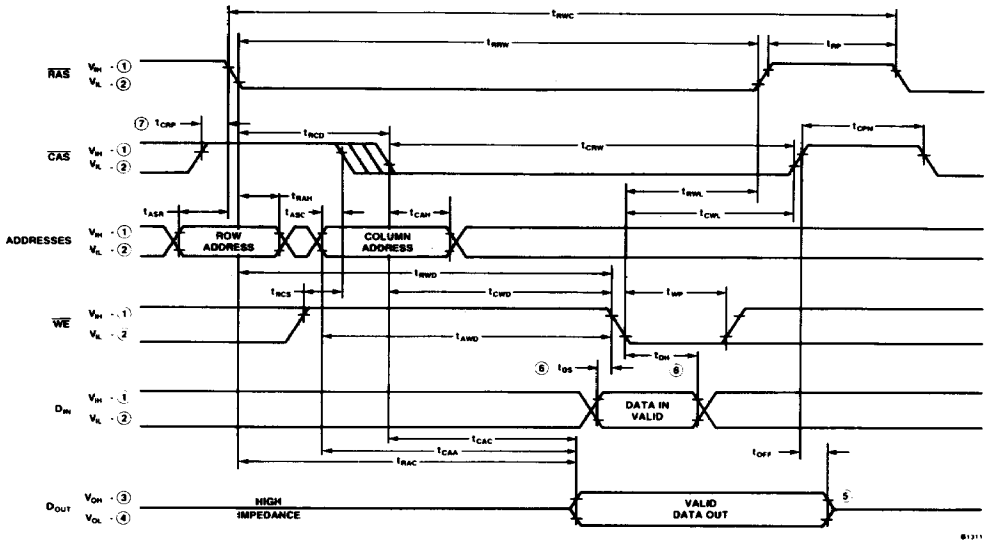
6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

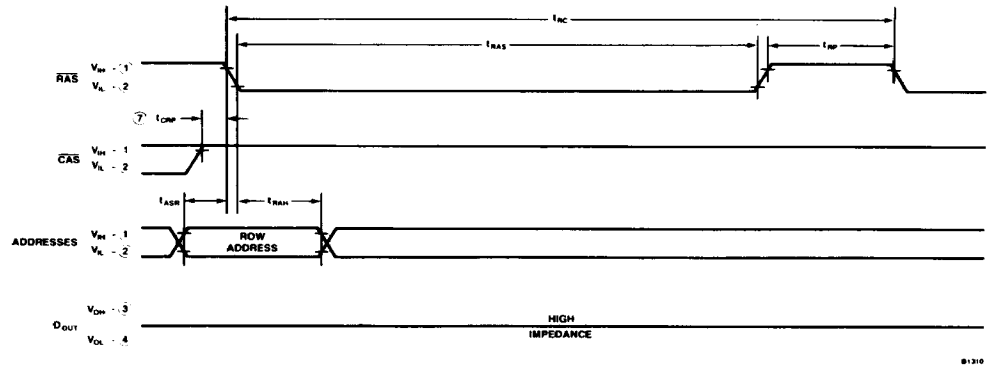
8. Either t_{RCH} or t_{RRH} must be satisfied.

Waveforms (con't)

Read-Modify-Write Cycle



RAS-Only Refresh Cycle



Notes:

1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

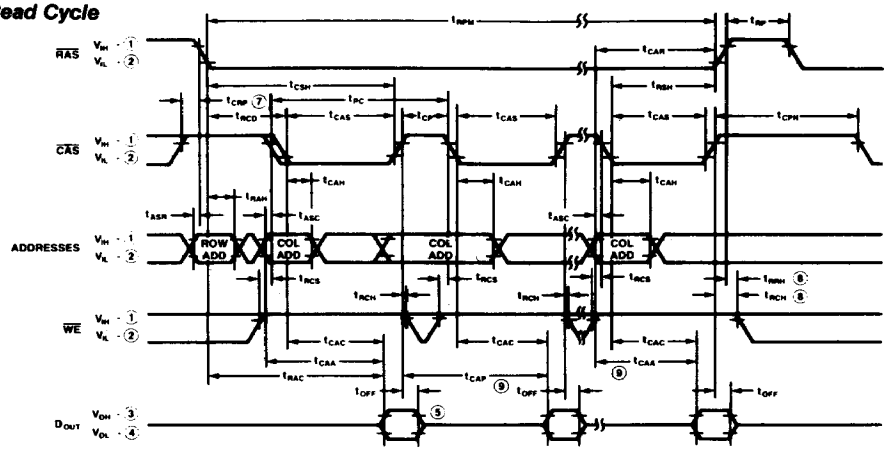
5. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

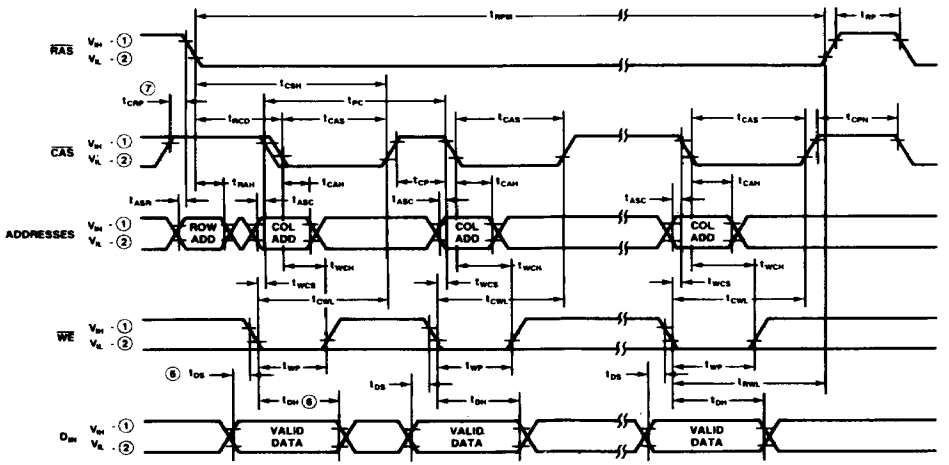
7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

Waveforms (con't)

Ripplemode Read Cycle



Ripplemode Write Cycle



Notes

1,2. $V_{IH\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

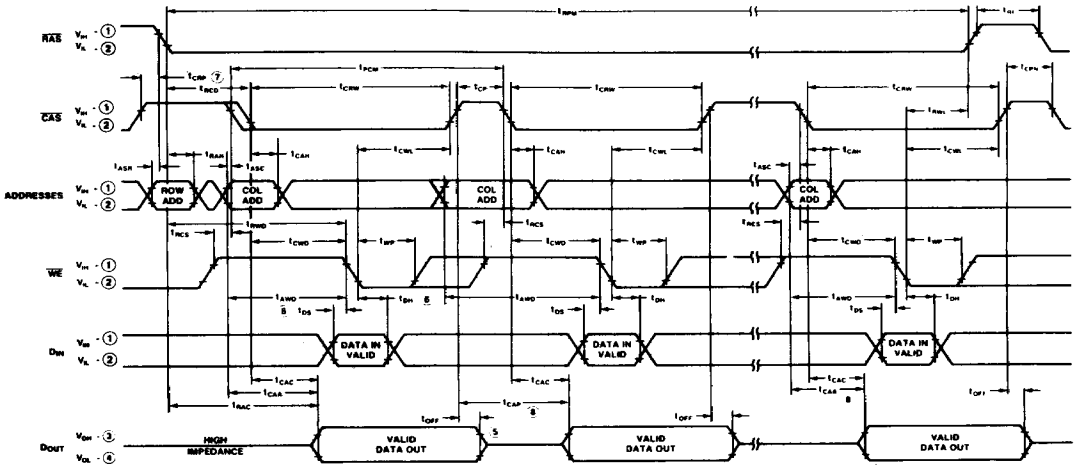
7. t_{CRP} requirement is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

8. Either t_{RCH} or t_{RRH} must be satisfied.

9. Access time is t_{CAP} or t_{CAA} dependent, see Ripplemode discussion on pages 10 and 11.

Waveforms (con't)

Ripplemode Read-Modify-Write Cycle



NOTES:

1,2. $V_{IN\ MIN}$ and $V_{IL\ MAX}$ are reference levels for measuring timing of input signals.

3,4. $V_{OH\ MIN}$ and $V_{OL\ MAX}$ are reference levels for measuring timing of D_{OUT}.

5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

6. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

7. t_{CRP} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$-only cycle (i.e., for systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).

8. Access time is t_{CAP} or t_{CAA} dependent, see Ripplemode discussion on pages 10 and 11.

Device Description

The Vitelic V51C64 is produced with VICMOS III technology, combining the scaling techniques of production proven NMOS with CMOS. VICMOS III technology together with new circuit design concepts results in fast data access, low power, fast usable speed and a soft error rate average of less than 10 FITs.

$\overline{RAS}/\overline{CAS}$ Timing

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by bringing $\overline{RAS}$ and/or $\overline{CAS}$ low, must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle cannot begin until the minimum precharge time, t_{RP}, has been met.

Read Cycle

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}/\overline{CAS}$ operation. Data Input (D_{IN}) must be valid relative to the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever transition occurs last.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. $\overline{CAS}$ may remain high (inactive) for this sequence. Any cycle, Read, Write, Read-Modify-Write, or $\overline{RAS}$-only, will refresh the memory.

Extended Refresh Cycle

The V51C64L extends the refresh cycle period to 64 milliseconds for $\overline{RAS}$-only refresh cycles. This feature reduces total power consumption to a maximum of 690 μW, and typically 235 μW for data retention, ($\overline{RAS} \geq V_{DD} - 0.5V$, $\overline{RAS}$-only refresh cycle for the V51C64L-12). The low standby power can significantly extended battery life in battery back-up applications. Power consumption is calculated from the following equation:

$$P = V_{DD}\, I_{AVG} = V_{DD}\ \frac{(t_{RC})\,(I_{Active}) + (t_{RI} - t_{RC})\,(I_{Standby})}{t_{RI}}$$

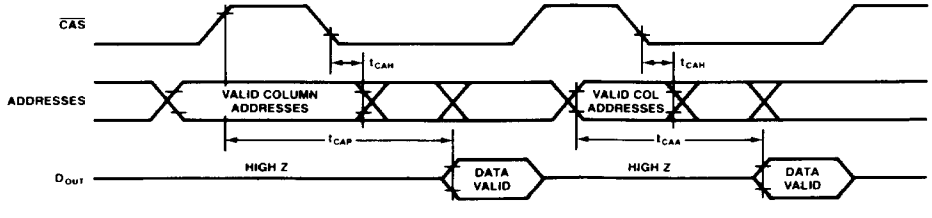
where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Ripplemode

Ripplemode operation permits all 256 columns within the selected row of the selected device to be accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent latch while $\overline{CAS}$ is high. Access begins from valid column addresses rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the addresses into the column address buffer and serves as an output enable.

During this operation, Read, Write, or Read-Modify-Write cycles are possible at random or sequential addresses within the row. Following the entry cycle into Ripplemode operation, access time is t_{CAA} or t_{CAP} dependent. If the column addresses are valid prior to or coincident with the rising edge of $\overline{CAS}$, then the access time is determined by the rising edge of $\overline{CAS}$ specified by t_{CAP} (see Figure 1.) If the column addresses are valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column addresses specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the addresses and enables the output.

Figure 1. Ripplemode Access Time Determination



Ripplemode operation provides a sustained data rate beyond 15 MHz for applications that require high data bandwidth, such a bit mapped graphics. The following formula can be used to calculate the data rate:

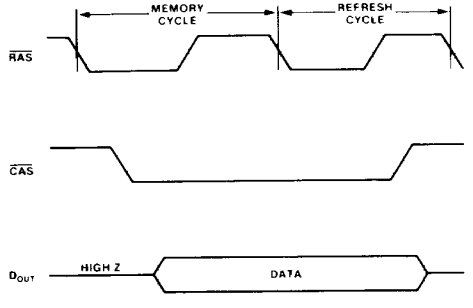
$$\text{Data Rate} = \frac{256}{t_{RC} + 255\, t_{PC}}$$

Hidden Refresh

A standard feature of the V51C64 is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and, after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure 2).

This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability. The part will be internally refreshed at the row addressed at the time of the second $\overline{RAS}$.

Figure 2. Hidden Refresh Cycle



Vitelic V51C64 Data Output Operation for Various Types of Cycles

Type of Cycle	D_{OUT} State
Read Cycle	Data from Addressed Memory Cell
Early Write Cycle	Hi-Z
$\overline{RAS}$-Only Refresh Cycle	Hi-Z
$\overline{CAS}$-Only Cycle	Hi-Z
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Delayed Write Cycle	Indeterminate

Data Output Operation

The V51C64 Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}), the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms for the V51C64, and greater than 64 ms for the V51C64L). The V_{DD} current (I_{DD}) requirement of the V51C64L during power on is, however, dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$.

If $\overline{RAS}$ = V_{SS} during power on, the device will go into an active cycle and I_{DD} will show current transients similar to those shown for the $\overline{RAS}/\overline{CAS}$ timings. It is required that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.