MOSTEK 16,384 × 1 Bit Dynamic Ram | MK 4116P-2/3

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 150ns access time, 375ns cycle (MK 4116-2)
  200ns access time, 375ns cycle (MK 4116-3)
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles

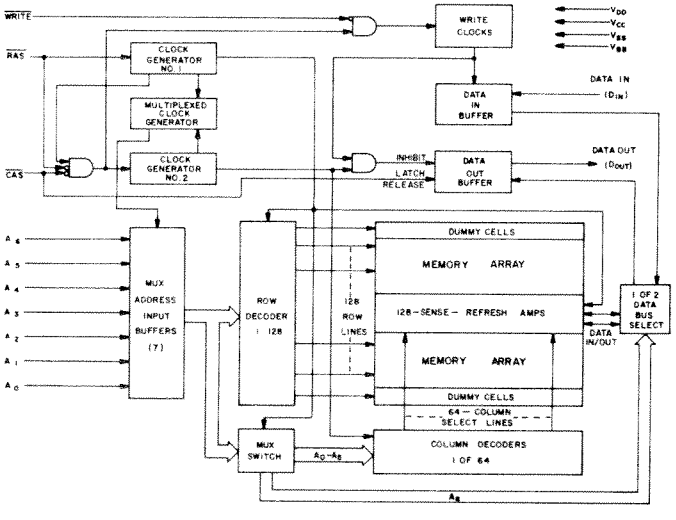
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

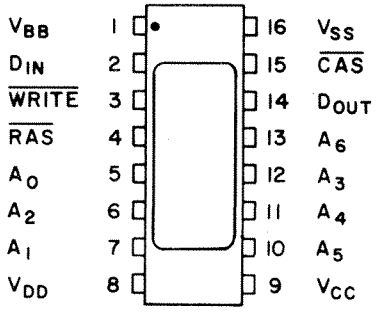
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
V_{BB}−V_{SS} (V_{DD}−V_{SS} >0V) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) ..... −55°C to + 150°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
($0°C \leq T_A \leq 70°C$)[1]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.5	Volts Volts Volts Volts	2 2,3 2 2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; V_{BB} = −5.0V ±10%; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375ns)	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	4 5
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 100	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375ns)	I_{DD3} I_{CC3} I_{BB3}	 −10 	25 10 200	mA µA µA	4
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225ns)	I_{DD4} I_{CC4} I_{BB4}		27 200	mA µA	4 5
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = −5.0V ±10%)

PARAMETER	SYMBOL	MK 4116-2		MK 4116-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	375		375		ns	9
Read-write cycle time	t_{RWC}	375		375		ns	9
Page mode cycle time	t_{PC}	170		225		ns	
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	10,12
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	11,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	ns	8
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	32,000	200	32,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row Address set-up time	t_{ASR}	0		0		ns	
Row Address hold time	t_{RAH}	20		25		ns	
Column Address set-up time	t_{ASC}	−10		−10		ns	
Column Address hold time	t_{CAH}	45		55		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	60		80		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	60		80		ns	
Data-in set-up time	t_{DS}	0		0		ns	15
Data-in hold time	t_{DH}	45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60		80		ns	
Refresh period	t_{REF}		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−40		−40		ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	70		95		ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	120		160		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

7. AC measurements assume t_T = 5ns.

8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

9. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.

10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

12. Measured with a load equivalent to 2 TTL loads and 100pF.

13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

17. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with ΔV = 3 volts and power supplies at nominal levels.

18. $\overline{CAS}$ = V_{IHC} to disable D_{OUT}.

AC ELECTRICAL CHARACTERISTICS

$(0°C \leq T_A \leq 70°C)$ $(V_{DD} = 12.0V \pm 10\%; V_{SS} = 0V; V_{BB} = -5.0V \pm 10\%)$

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

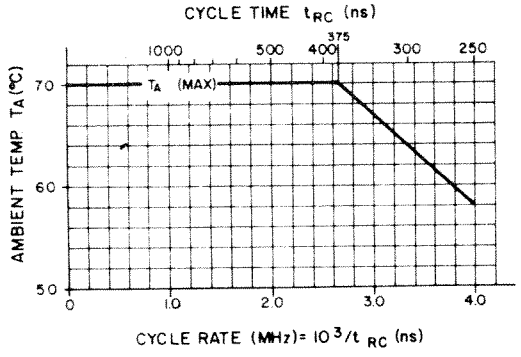


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ns) is determined by T_A (max) [°C] = 70–9.0 x (cycle rate [MHz] –2.66).

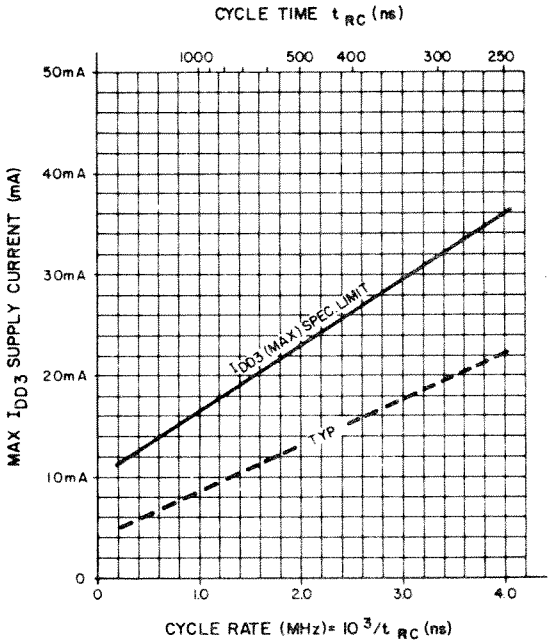


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:
I_{DD3} (max) [mA] = 10 + 6.5 x cycle rate [MHz] .

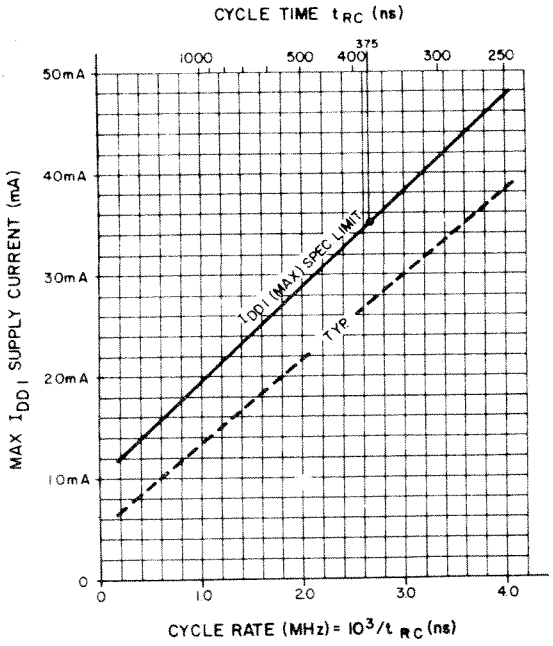


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:
I_{DD1} (max) [mA] = 10 + 9.4x cycle rate [MHz]

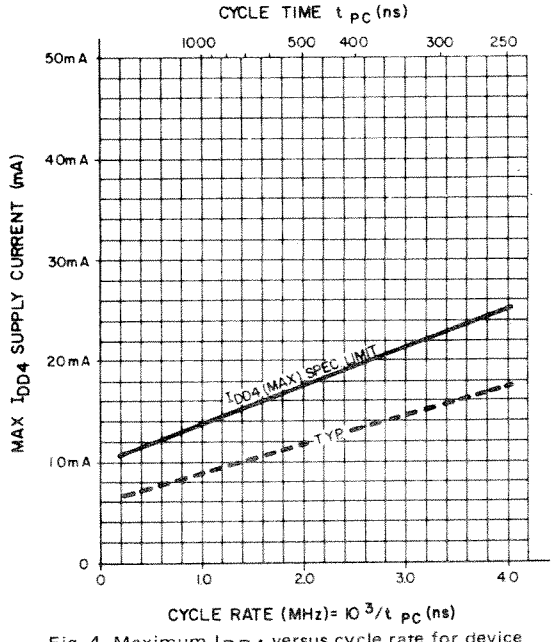
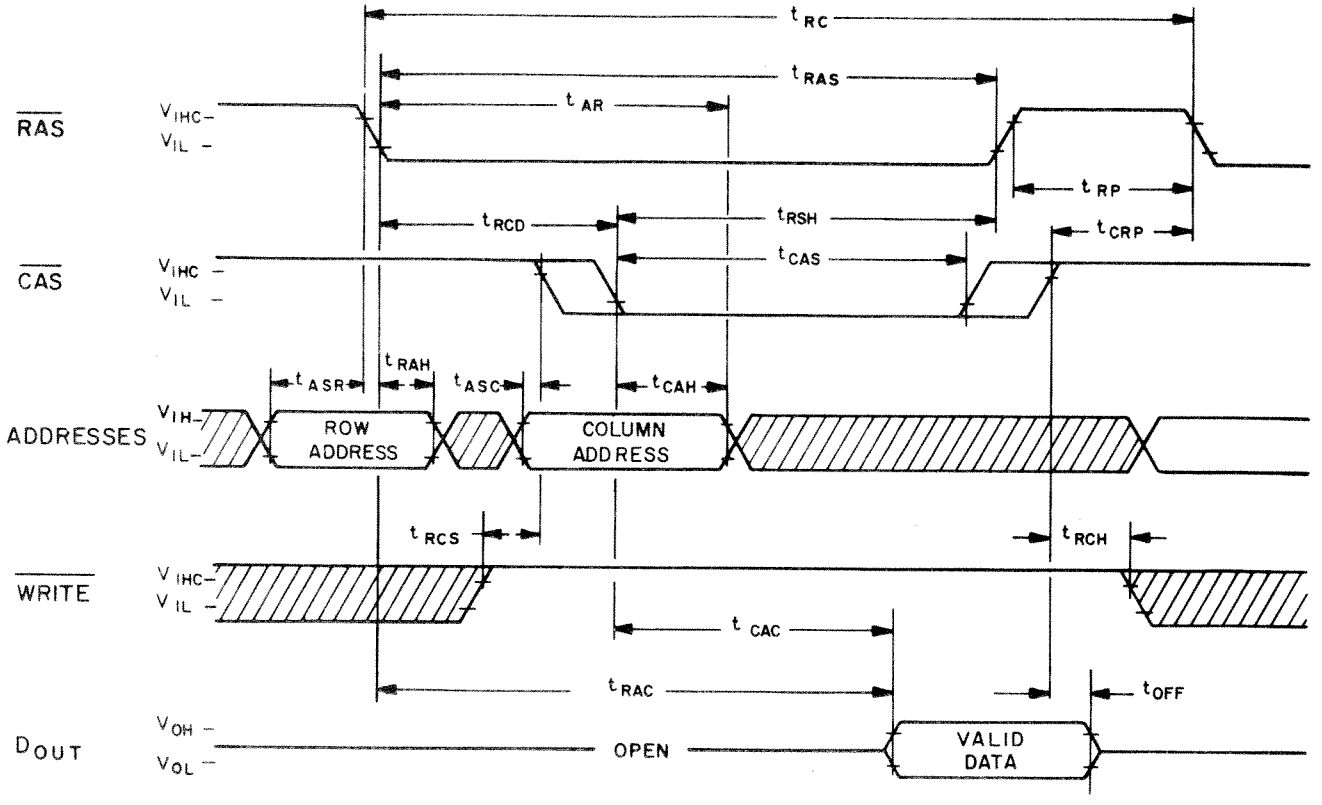
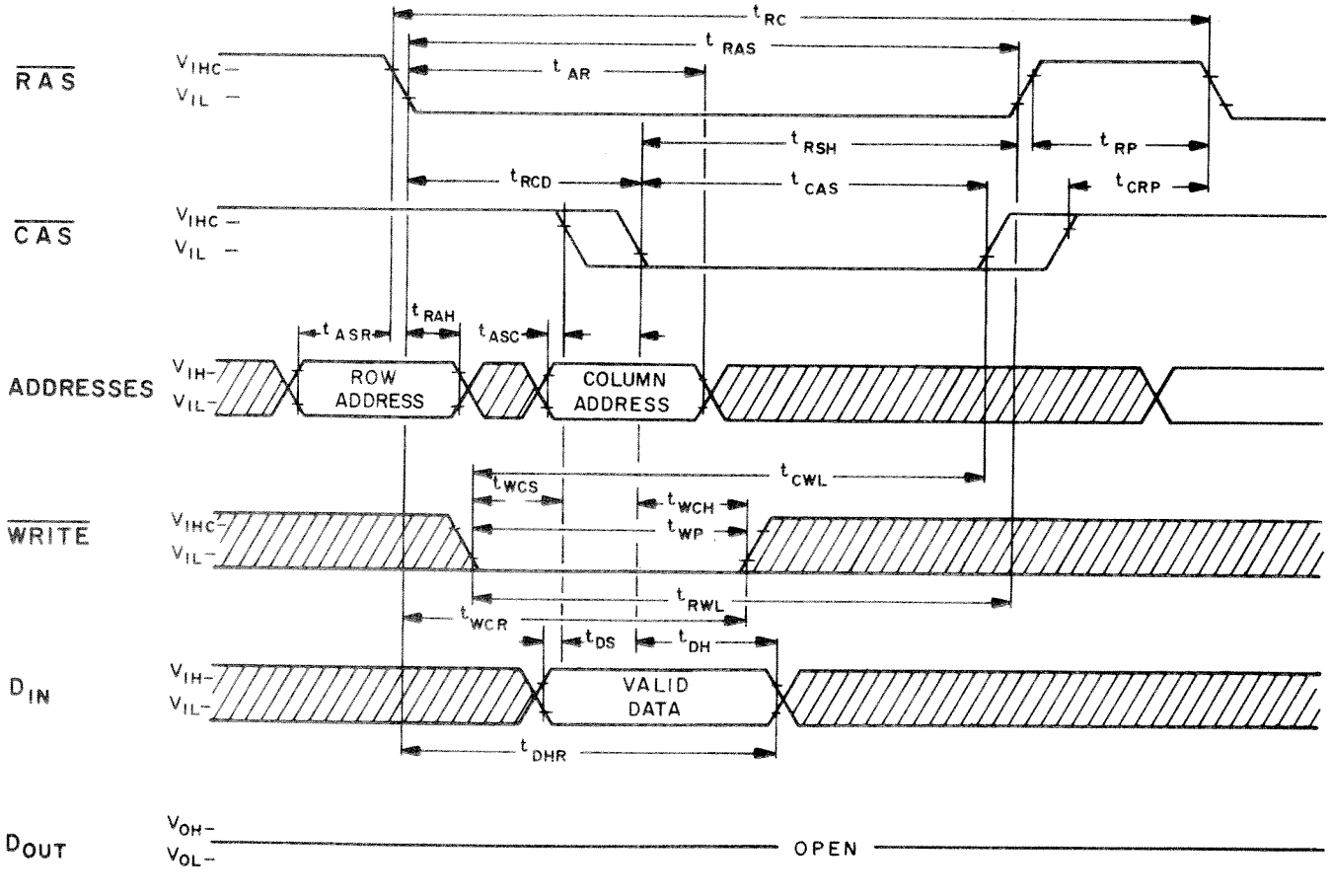


Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation
I_{DD4} (max) [mA] = 10 + 3.75 x cycle rate [MHz]

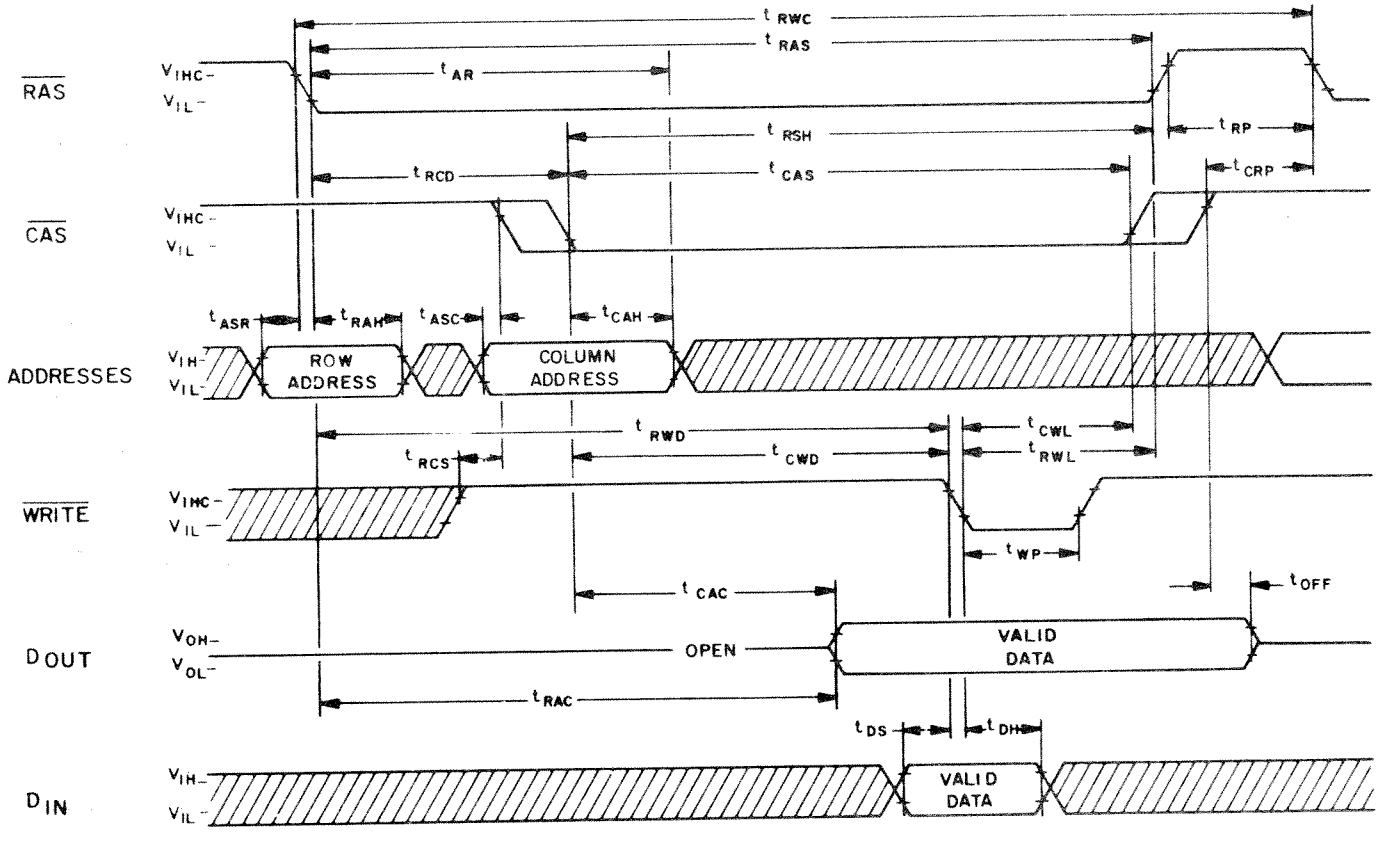
READ CYCLE



WRITE CYCLE (EARLY WRITE)

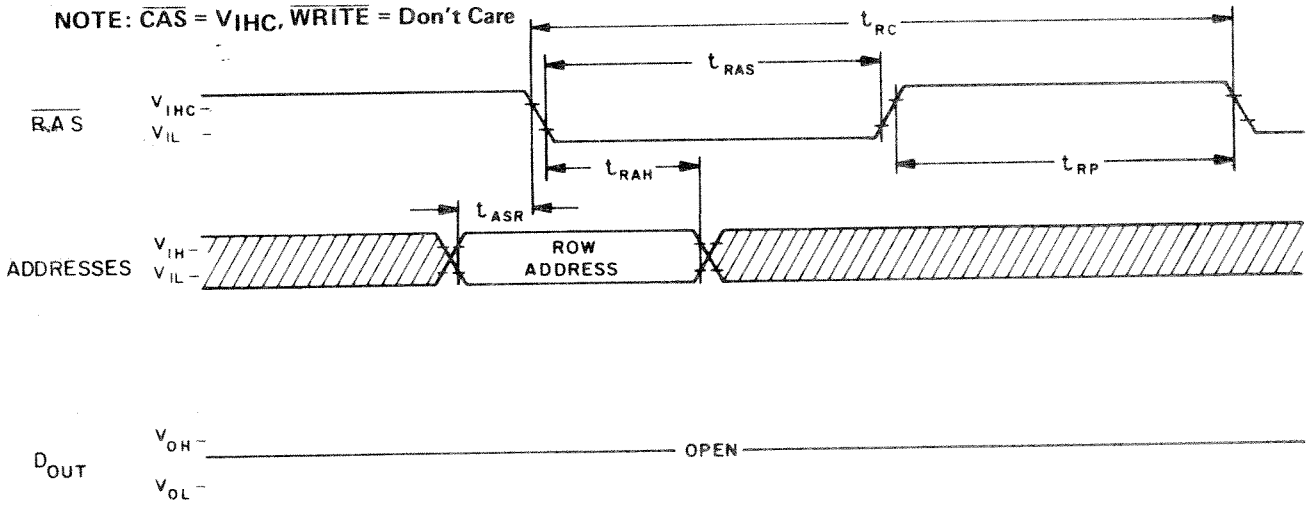


READ–WRITE/READ–MODIFY–WRITE CYCLE

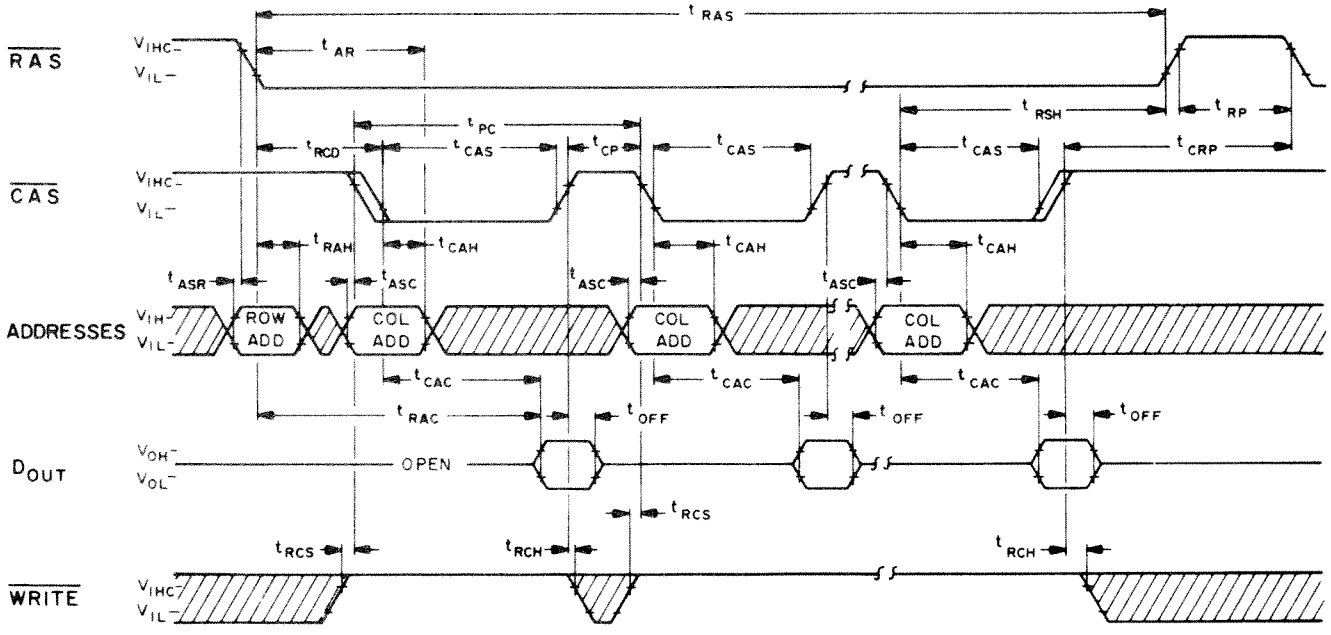


"RAS–ONLY" REFRESH CYCLE

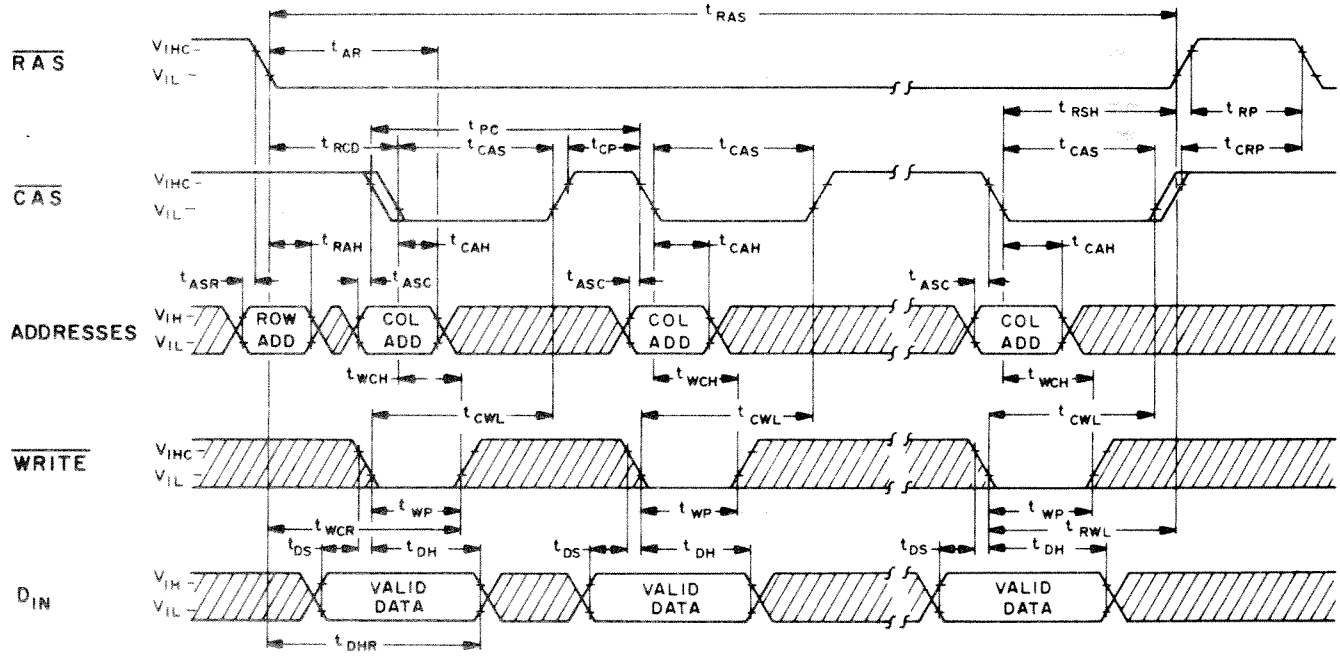
NOTE: CAS = V_{IHC}, WRITE = Don't Care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs(RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe (RAS), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 7 column address bits into the chip. Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of CAS which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS, the D_{IN} is strobed by CAS, and the set-up and hold times are referenced to CAS. If the input data is not available at CAS time or if it is desired that the cycle be a read-write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, D_{IN} is referenced to WRITE in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to CAS).

Data is retrieved from the memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime CAS is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until CAS is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state,whether or not RAS goes into precharge.

If the cycle in progress is an "early-write" cycle (WRITE active before CAS goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of WRITE command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation — If all write operations are handled in the "early write" mode,then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control — D_{OUT} will remain valid during a read cycle from t_{CAC} until CAS goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.

Two Methods of Chip Selection — Since D_{OUT}

is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary — Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns cycle with an ambient temperature range from 0°to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20mA with an ambient temperature range from 0°to 70°C.

It is possible to operate certain versions of the MK 4116 family (the −2 and −3 speed selections for example) at frequencies higher than 2.66 MHz (375ns cycle), provided all AC operating parameters are met. Operation at shorter cycle times (< 375ns) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to figure 1 for derating curve.

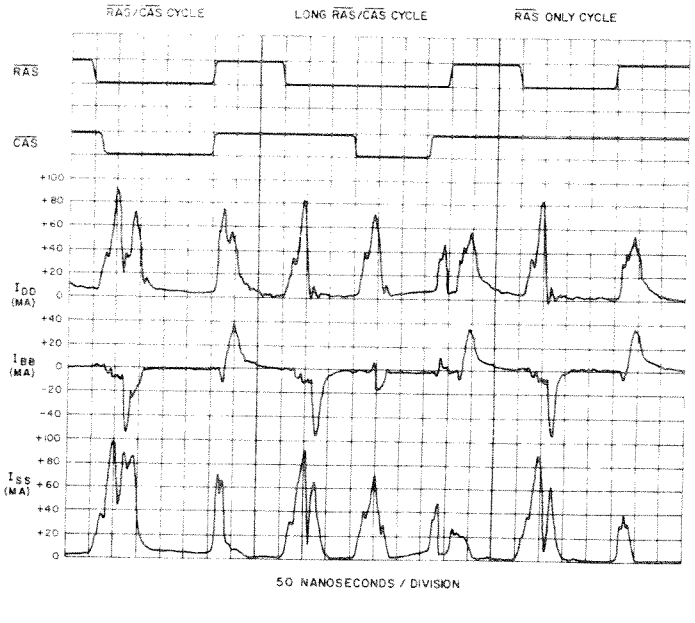


Fig. 5 Typical Current Waveforms

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

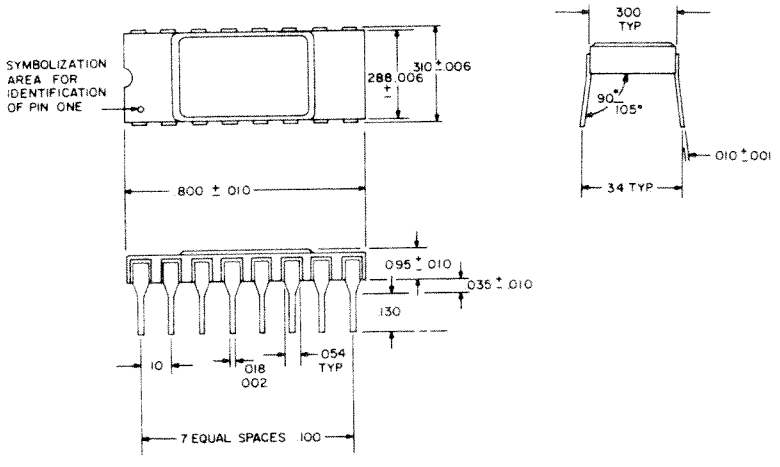
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

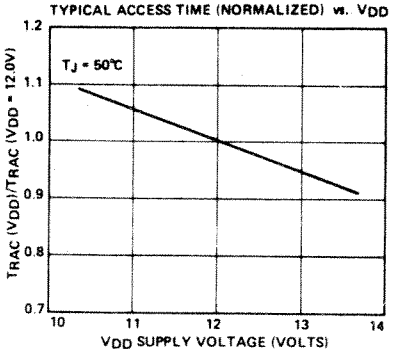
PACKAGE DESCRIPTION

16-lead side-brazed ceramic dual-in-line hermetic package

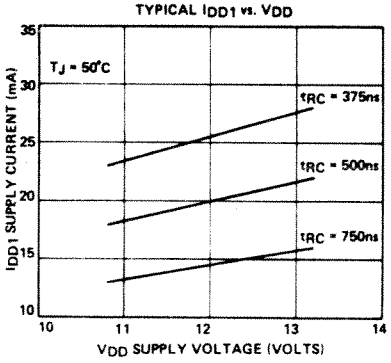


TYPICAL CHARACTERISTICS

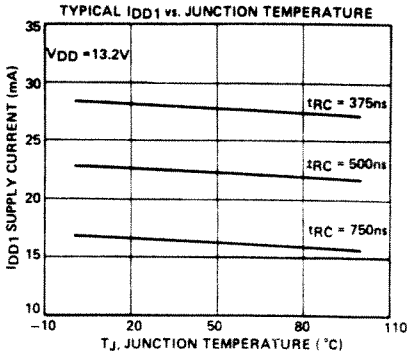
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



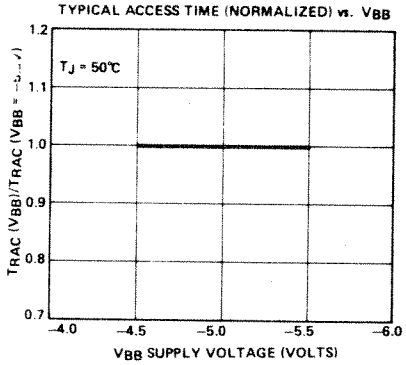
TYPICAL I_{DD1} vs. V_{DD}



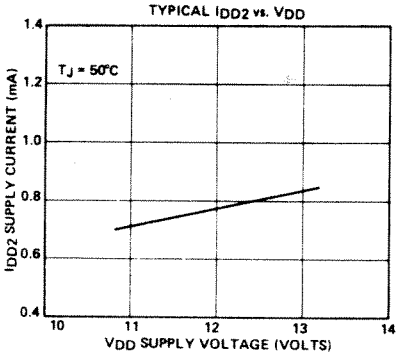
TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



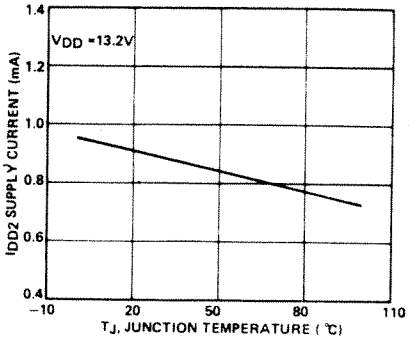
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



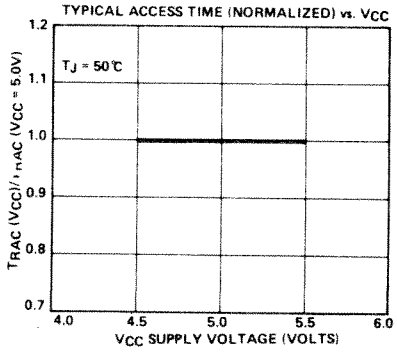
TYPICAL I_{DD2} vs. V_{DD}



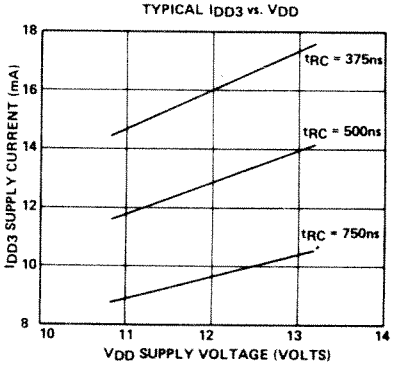
TYPICAL I_{DD2} vs JUNCTION TEMPERATURE



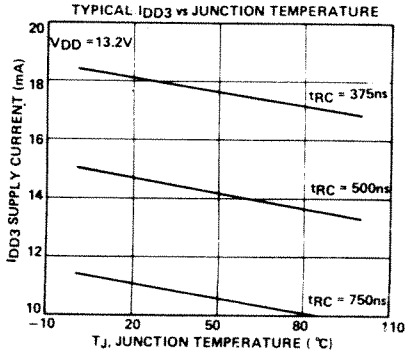
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



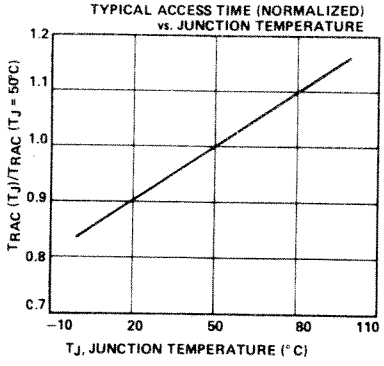
TYPICAL I_{DD3} vs. V_{DD}



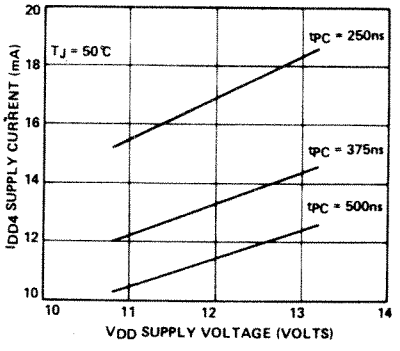
TYPICAL I_{DD3} vs JUNCTION TEMPERATURE



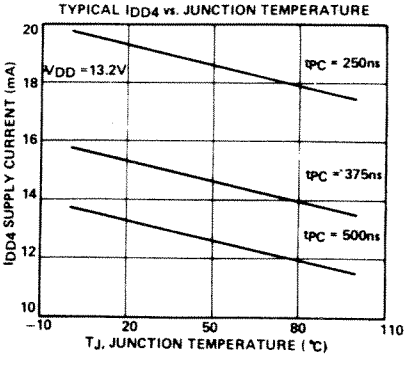
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



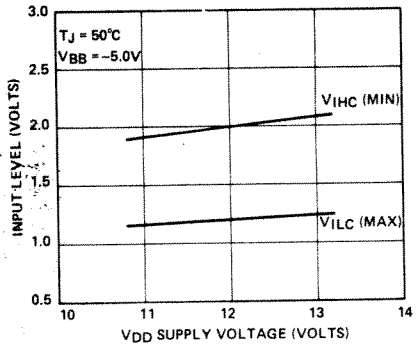
TYPICAL I_{DD4} vs V_{DD}



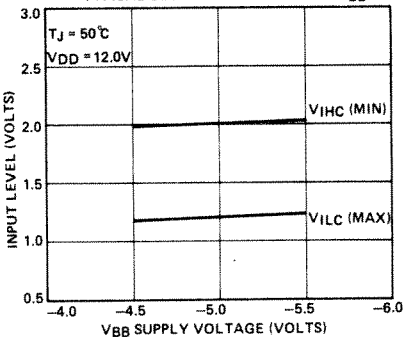
TYPICAL I_{DD4} vs. JUNCTION TEMPERATURE



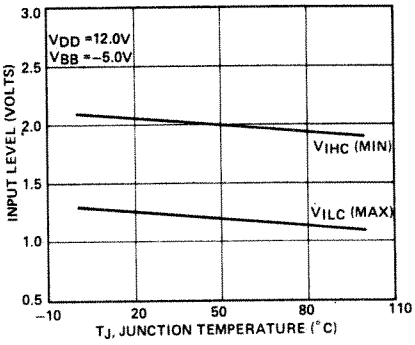
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



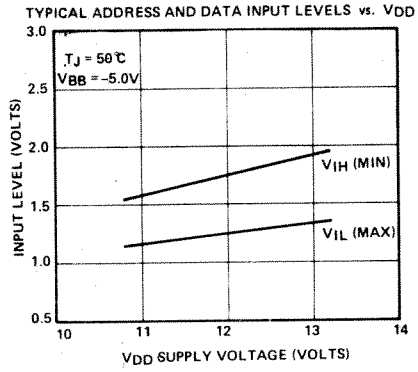
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



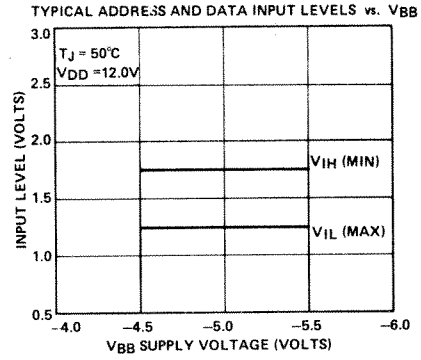
TYPICAL CLOCK INPUT LEVELS vs. T_J



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J