ST225
OEM MANUAL

PLEASE NOTE

SPECIFICATIONS OF THE ST213 HALF HEIGHT
10MB DRIVE CAN BE FOUND AT THE BACK OF
THIS MANUAL.

Seagate

ST225 OEM MANUAL

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INTRODUCTION

The Seagate ST225 disc drive provides OEMs and system integrators with over 20 megabytes of formatted capacity in a shock-resistant half-height package. The ST225 is designed for single-user desk-top systems, local storage in network or multi-user systems, or as an add-in upgrade for PCs. The low-power ST225 design is ideal for these applications in either rugged industrial or quiet office environments. The ST225 supports the industry-standard ST412 interface and has the same voltage requirements for ease of integration.

High reliability is assured through the use of LSI, a single printed circuit board, mini-monolithic heads and proven oxide media. Seagate's proprietary helical-band rotary-actuator features simplicity and ease of manufacture with excellent thermal stability. A dedicated head shipping zone assures data integrity during shipping and handling. The ST225 offers a low-cost, rugged and reliable disc drive with an MTBF of 20,000 hours.

Our manufacturing facilities have been designed and located exclusively for high volume production and testing of disc drives. Seagate's ongoing commitment to vertical integration assures availability of the latest technology at the same consistent quality and lowest possible cost. Seagate inspects every assembly at every stage of the production process. A proprietary test system continuously verifes our goals of volume production with rigorous quality control.

ST213

Oct. 29, 1985

This manual may be used to install and configure Seagate's ST213. The ST213 is a half-height, single-disc, 10 Megabyte (formatted) Winchester. It employs the same efficient helical-band rotary-actuator as the ST225 and also supports the industry-standard ST412 interface.

Voltage requirements, interface connectors and mounting requirements are identical to the ST225. Please refer to page 40, Appendix number 3 for specifications.

1.0 SPECIFICATION SUMMARY

PERFORMANCE SPECIFICATIONS 1.1

Capacity	Unformatted	Formatted	
Per Drive:	25.62 MB	20.15 MB	21.42 MB
Per Surface:	6.41 MB	5.04 MB	5.35 MB
Per Track:	10,416 Bytes	8,192 Bytes	8,704 Bytes
Per Sector:	NA	256 Bytes	512 Bytes
Sectors per Track:	NA	32 Sectors	17 Sectors

ACCESS TIME DEFINITION AND TIMING 1.1.1

Access time is defined as the time from the leading edge of the last Step pulse received to SEEK COMPLETE (including carriage settling). The period between Step pulses must be between 5μsec and 200μsec.

Average access time is measured over a 205-track seek (one-third stroke.[1] The calculation assumes the following:

1. Nominal temperature and power
2. The average is taken from an inward one-third stroke, plus an outward one-third stroke.

Track-to-Track:	20.0msec max.
Average:	65.0msec max. [1]
Maximum Seek:	150.0msec max. [1]

FUNCTIONAL SPECIFICATIONS 1.2

Rotational Speed:	3,600 RPM ± 1%
Latency:	8.33msec nominal
Recording Density:	9,827 BPI (Cylinder 614)
Flux Density:	9,827 FCI (Cylinder 614)
Track Density:	588 TPI
Cylinders:	615
Tracks:	2,460
Read/Write Heads:	4
Discs:	2
Data Transfer Rate:	5.0 Megabits/second
Recording Scheme:	MFM

PHYSICAL SPECIFICATIONS 1.3

Height:	1.63 inches max. (41.4mm)
Width:	5.75 $^{+.02}_{-.03}$ inches (146.05 $^{+0.5}_{-0.8}$ mm)
Depth:	8.00 inches max. (203.2mm)
Weight:	2.75 lbs (1.25Kg)

1. Buffered-Seek

1.4 RELIABILITY SPECIFICATIONS

MTBF:	20,000 Power-on hours [2]
PM:	Not required
MTTR:	30 minutes
Service Life:	5 years

1.4.1 READ ERROR RATES

Recoverable Read Errors:	1 per 10^{10} bits read [3]
Nonrecoverable Read Errors:	1 per 10^{12} bits read [4]
Seek Errors:	1 per 10^{6} seeks

1.4.1.1 BIT JITTER

Bit jitter reduction determines the relationship between the leading edge of READ DATA and the center of the data window.

The specified Read error rates are based on the following bit jitter specification. The data separator must provide at least −40 dB of bit jitter reduction at 2F with an offset error of less than 1.5nsec shift from the center of the data window.

1.4.2 MEDIA DEFECTS

A media defect is a Read error when data, which has been correctly written, cannot be recovered within 16 retries.

A printout will be provided with each drive listing the location of any defect by head, cylinder, sector and byte. It will also specify the number of bytes from the Index pulse. [5]

There will be no more than eight (8) defects per surface for a maximum total of thirty-two (32) per drive. Cylinder Zero will be free of defects.

1.5 ENVIRONMENTAL SPECIFICATIONS

1.5.1 AMBIENT TEMPERATURE

Operating:	50°F to 113°F (10°C to 45°C)
Nonoperating:	−40°F to 140°F (−40°C to 60°C)

1.5.2 TEMPERATURE GRADIENT

Operating:	18°F/hr (10°C/hr) max.
Nonoperating:	Below condensation

2. Typical usage at 25°C, at sea level. Calculated per *Mil. Spec. Handbook 217.*
3. Recoverable within 16 retries
4. Not recoverable within 16 retries
5. Based on a 32-sector, 256 byte/sector format

RELATIVE HUMIDITY 1.5.3

Operating:	8 to 80% noncondensing
Maximum Wet Bulb:	78.8°F (26°C) noncondensing
Nonoperating:	5 to 95% noncondensing

ALTITUDE LIMITS 1.5.4

Operating:	− 1,000 ft to 10,000 ft
Nonoperating:	− 1,000 ft to 30,000 ft

OPERATING SHOCK 1.5.5

Maximum permitted shock without incurring physical damage or degradation in performance: 10 G's [6,7]

OPERATING VIBRATION 1.5.6

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance: [7]

Frequency	Vibration
5 – 22 Hz	.010" double amplitude
22 – 300 Hz	.25 G amplitude (peak)
300 – 22 Hz	.25 G amplitude (peak)
22 – 5 Hz	.010" double amplitude

NONOPERATING SHOCK 1.5.7

Maximum permitted shock without incurring physical damage or degradation in performance: 40 G's [6,7,8]

NONOPERATING VIBRATION 1.5.8

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance: [7,8]

Frequency	Vibration
5 — 22 Hz	.010" double amplitude
22 — 300 Hz	.50 G amplitude (peak)
300 — 22 Hz	.50 G amplitude (peak)
22 — 5 Hz	.010" double amplitude

DC POWER REQUIREMENTS 1.6

The ST225 is listed in accordance with UL 478 and CSA C22.2 (0-M1982), and meets all applicable sections of IEC 380 and VDE 0806/08.81, as tested by *TUV-Rheinland, North America.*

6. 11msec half-sine wave shock pulse
7. Input levels at the drive mounting screws. Unit mounted in an approved orientation. See *Section 1.7*
8. Heads positioned to the shipping zone

Power may be applied or removed in any sequence without loss of data or damage to the drive.

+12 Volts DC:	
Voltage Tolerance (including ripple):	± 5%
Maximum Current at Power-on:	2.2 Amp
Typical Current:	.9 Amp
+5 Volts DC:	
Voltage Tolerance (inc. ripple):	± 5%
Typical Current:	.8 Amp
Power	14.8 typical[9]

1.6.1 INPUT NOISE RIPPLE

The maximum permitted ripple is 100mV (peak-to-peak) on either +12 Volts or +5 Volts measured on the host system power supply across the following equivalent resistive loads:

+12 Volts DC 16Ω
+ 5 Volts DC 5Ω

1.6.2 INPUT NOISE FREQUENCY

20MHz max. on both the +12 and +5 Volt lines

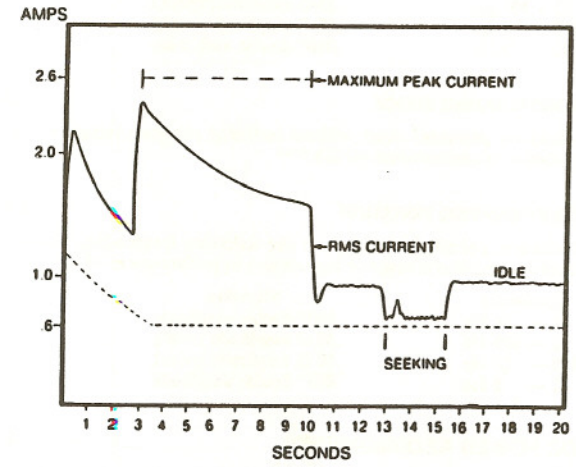
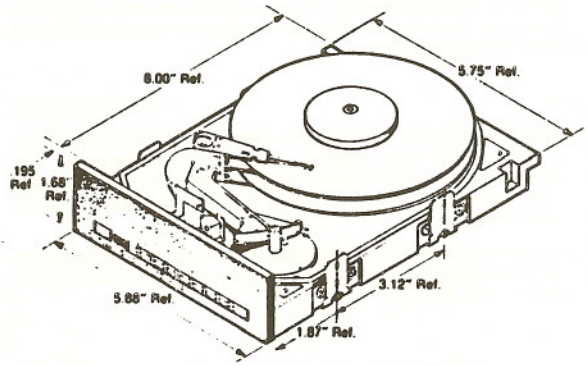


FIGURE 1: Typical RMS +12 Volt DC Start-Up Current Plot

9. Measured under the following standard operating conditions:
   25°C ambient temperature
   Sea level
   Nominal voltages applied
   Spindle rotating, drive not seeking

FIGURE 2:
Reference Dimensions



Dimensions are in inches.

Axis for shock specification

MOUNTING REQUIREMENTS 1.7

The ST225 may be mounted in the following orientations:

Horizontal:	Spindle motor down
Sides:	Left or right

The drive should not be tilted front to back, in any position, by more than ± 5°. Refer to *Figures 2* and *3* for reference and mounting dimensions.

For optimum performance the drive should be formatted in the same orientation as it will be mounted in the host system.

SHOCK MOUNTING RECOMMENDATION 1.7.1

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25Hz or lower.

A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive for cooling airflow and motion during mechanical shock or vibration.

1.7.2 HANDLING AND STATIC-DISCHARGE PRECAUTIONS

After unpacking and prior to system integration, the drive is exposed to potential handling and ESD hazard.

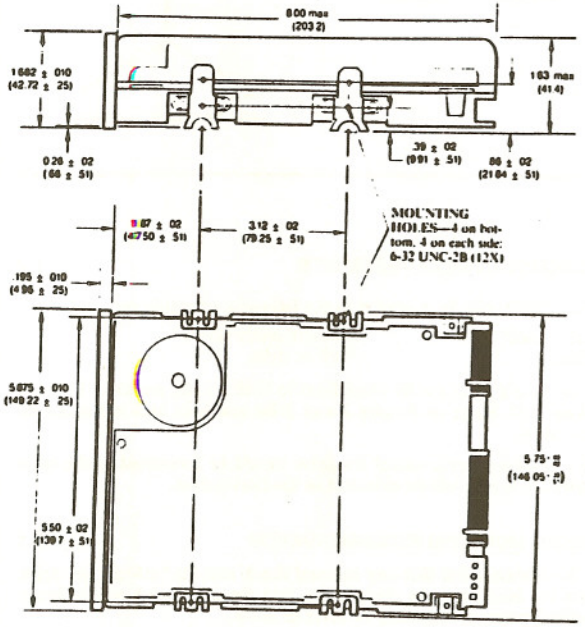
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

It is strongly recommended that the drive always rest on a padded surface, with the heads parked over the shipping zone, until the drive is mounted in the host system.

1.7.3 SHIPPING ZONE

The ST225 employs a shipping zone, located from Cylinders 615 to 670, to preserve data integrity during shipping/transport. The Read/Write heads may be parked in the shipping zone by issuing a seek to any cylinder between 615–670. The drive may then be powered-down.

Upon power-up, the drive will recalibrate to Track Ø. If the heads are parked while power is still applied, any Step pulse will cause the unit to recalibrate to Track Ø.



Dimensions are in inches (mm).

NOTE: Mounting screws must not extend more than .25 inch inside the drive.

FIGURE 3: Mounting Dimensions

2.0 ST225 HOST/DRIVE INTERFACE

This section details the physical specifications of the host/drive interface connectors. Connector dimensions and pin assignments follow under each section. Refer to *Figure 9* for an overall view of the drive and the interface connectors.

CONTROL/STATUS SIGNALS

PCB EDGE-CONNECTOR, J1 2.1

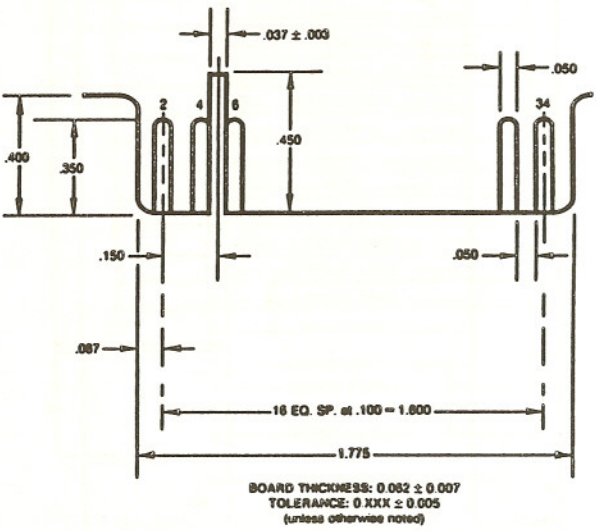
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Control and status signals between the host and the drive are transmitted through a 34-pin PCB edge-connector, J1. *Figure 4* indicates connector dimensions and *Table 1* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 5*.

With the drive resting on a padded surface, oriented with the PC Board up and the edge-connectors toward you, J1 is to your left and J2 is on the right. Refer to *Figure 9* for position and other interface option connectors.

J1 pins are numbered 1 through 34 with the even pins located on the solder side of the PCB. All odd pins are ground. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J1 is AMP ribbon connector, part number 88373-3.

FIGURE 4: J1 Connector Dimensions



GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-HEAD SELECT 2^3
3	4	-HEAD SELECT2^2
5	6	-WRITE GATE
7	8†	-SEEK COMPLETE
9	10	-TRACK Ø
11	12†	-WRITE FAULT
13	14	-HEAD SELECT 2^0
15	16	-RECOVERY MODE
17	18	-HEAD SELECT 2^1
19	20†	-INDEX
21	22†	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN

†STATUS ENABLED WITH DRIVE SELECT

TABLE: 1
J1 Host/Drive Pin Assignments

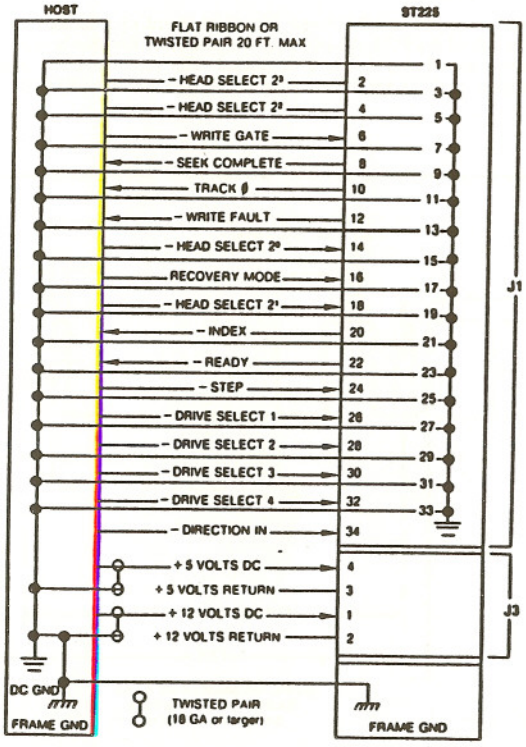


FIGURE 5:
Control/Status Signals

DATA SIGNALS
PCB EDGE-CONNECTOR, J2 2.2

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Read/Write data signals are received and transmitted over a 20-pin PCB edge-connector, J2. *Figure 6* below indicates connector dimensions and *Table 2* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 7*.

With the drive resting on a padded surface, oriented with the PC Board up and the edge-connectors toward you, J2 is to your right and J1 is on the left. Refer below to *Figure 9*.

J2 pins are numbered 1 through 20 with the even pins located on the solder side of the PCB. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J2 is AMP ribbon connector, part number 88373-6.

FIGURE 6: J2 Connector Dimensions

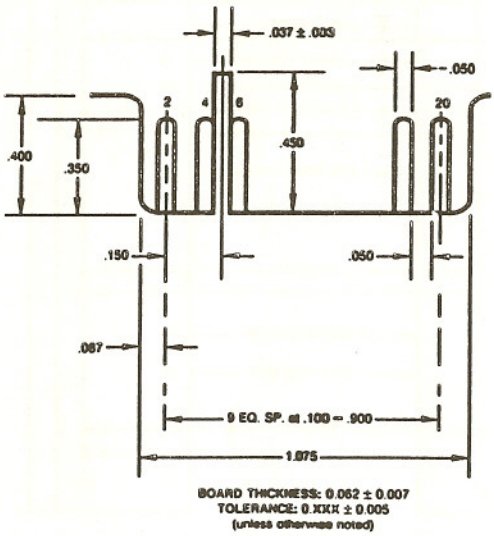
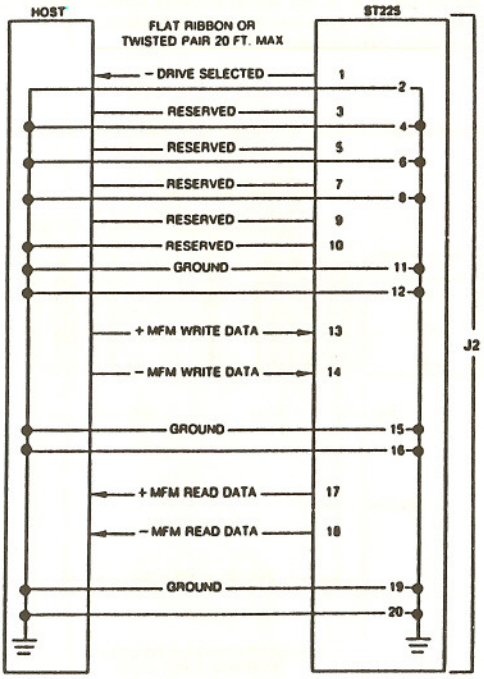


TABLE: 2
J2 Host/Drive Pin Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
10	9	RESERVED
12	11	GROUND
	13	+ MFM WRITE DATA
	14	– MFM WRITE DATA
16	15	GROUND
	17	+ MFM READ DATA
	18	– MFM READ DATA
20	19	GROUND

FIGURE 7:
Data Signals



DC POWER CONNECTOR, J3 2.3

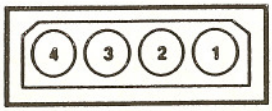
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

DC Power is transmitted from the host to the drive via the power connector J3. J3 is a 4-pin AMP "Mate-N-Lock" connector, AMP part number 350211-1. J3 is directly to the left of J1 and mounted on the component side of the PCB. The recommended mating connector is AMP part number 1-480424-0.

Applications using cable lengths less than five feet may use #18AWG wire and AMP 61314-4 strip pins.

For applications requiring cable lengths greater than five feet, #14AWG wire is recommended using AMP 61117-4 strip pins.

FIGURE 8: J3 Connector



PIN	POWER
1	+ 12 VOLTS
2	+ 12 VOLTS RETURN
3	+ 5 VOLTS RETURN
4	+ 5 VOLTS

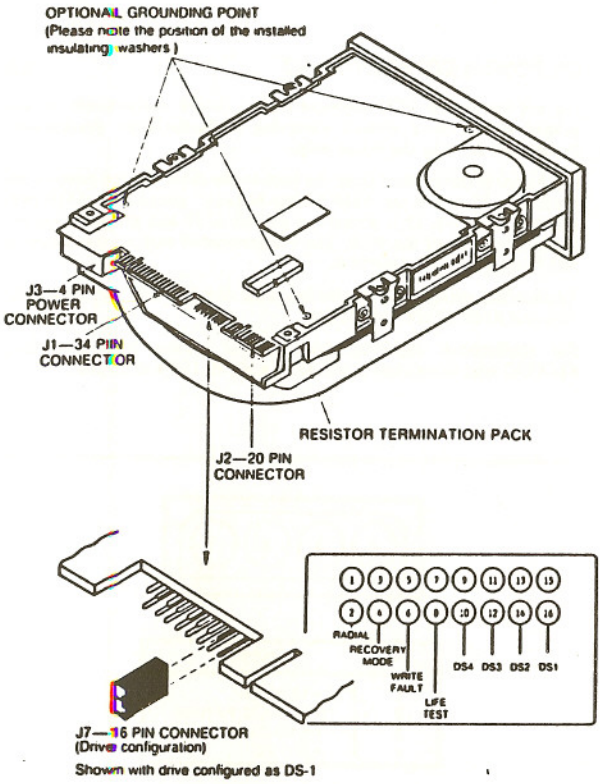


FIGURE 9:
Host/Drive Interface and Drive Configuration

3.0 DRIVE CONFIGURATION

The ST225 may be configured to specific host system requirements. *Sections 3.1* through *3.6* detail the options.

DRIVE CONFIGURATION SHUNT, J7 3.1

J7 is a 16-pin right angle shunt located midway between J1 and J2. Use the provided shorting blocks to enable the DRIVE SELECT lines and the desired options. *Figure 9* illustrates J7 and indicates Pin 1.

DRIVE SELECT CONFIGURATION 3.2

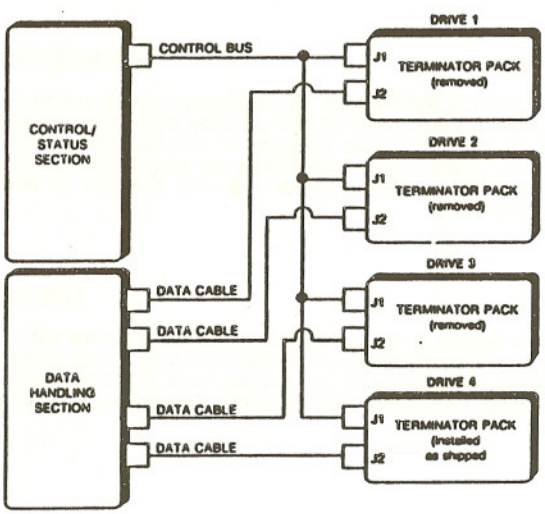
The DRIVE SELECT line enables the controller to select and address the drive. Control cable interface options use either a Daisy-Chain or Radial configuation.

Pins 15–16 shorted enables DRIVE SELECT 1
Pins 13–14 shorted enables DRIVE SELECT 2
Pins 11–12 shorted enables DRIVE SELECT 3
Pins 9–10 shorted enables DRIVE SELECT 4

DAISY-CHAIN 3.2.1

Each drive in the chain must be configured as either DRIVE 1,2,3 or 4, so that only one DRIVE SELECT line activates a device, The last drive in the chain must have a 220/330Ω resistor termination pack installed on the PCB. Refer to *Figure 9* above for resistor pack location.

FIGURE 10: Daisy-Chain Configuration



3.3 RADIAL

The Radial option is enabled by shorting pins 1 and 2 at the J7 shunt. Drives configured to this option are always selected and respond to all control signals issued on the attached control cable. The 220/330Ω resistor termination pack must remain installed on each radially-connected drive. *Figure 11* illustrates a host/drive Radial interconnection.

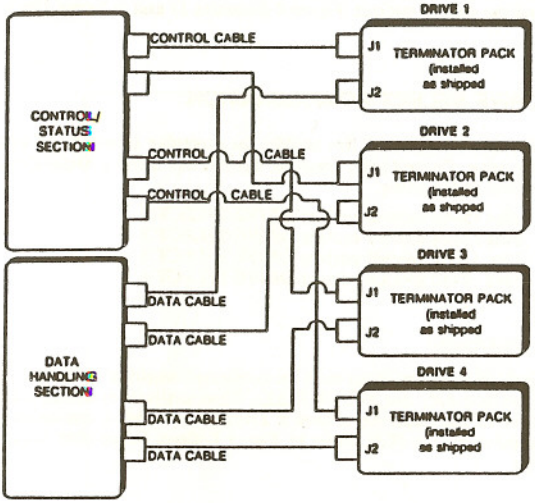


FIGURE 11:
Radial Configuration

3.4 WRITE FAULT

The WRITE FAULT signal may be internally latched. This latch may be cleared when DRIVE SELECT goes false (if pins 5 and 6 are shorted at J7). The standard configuration, with the shorting block removed, causes WRITE FAULT to go false when WRITE GATE goes false. Refer to *Section 5.7* for a detailed discussion of WRITE FAULT.

3.5 LIFE TEST

This function is used during the manufacturing process and is not recommended for field use. When pins 7 and 8 are shorted, the stepper motor will continuously seek between Track 0 and the maximum cylinder. When in this mode the drive will ignore control signals sent via the interface.

RECOVERY MODE 3.6

The ST225 may be configured to the RECOVERY MODE option by shorting pins 3 and 4 at J7. This option enables the Read/Write heads to microstep. This repositioning option may be used after the controller has completed its retry options on a read error.

RECOVERY MODE is initiated by the controller asserting the RECOVERY MODE line low (true) at the interface. This changes the STEP line to a microstep function after 100nsec. A Step pulse will now cause SEEK COMPLETE to go false 100nsec after the drive receives the pulse. The drive then microsteps off-track using the optimum algorithm, allowing 8msec for the heads to settle, and then takes the SEEK COMPLETE line true.

The controller may then attempt to read data. If data is not read correctly, the controller may issue an additional Step pulse. Up to eight separate microstep algorithms may be accessed before the sequence is repeated.

When data is read correctly, the controller exits RECOVERY MODE by taking the RECOVERY MODE line false at the interface. The drive then returns the heads to the nominal position by taking SEEK COMPLETE false, waiting 8msec for the heads to settle and reasserting SEEK COMPLETE.

Note: All writing is inhibited while the RECOVERY MODE signal is true.

4.0 CONTROL INPUT SIGNALS

The control signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing.

The signals to be multiplexed are WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, DIRECTION IN, RECOVERY MODE and STEP. These lines are terminated with a removable 220/330Ω resistor pair.

The multiplexing signals are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4. These lines are terminated in a single fixed 220/330Ω resistor pair.

Control signals are transmitted across the driver/receiver combination illustrated below in *Figure 12*. Control input signals are activated in accordance with the following specifications:

True: 0.0 Volts DC to 0.4 Volts DC at I = −48mA max.
False: 2.5 Volts DC to 5.25 Volts DC at I = +250μA (open collector)
Termination: A 220/330Ω resistor pack

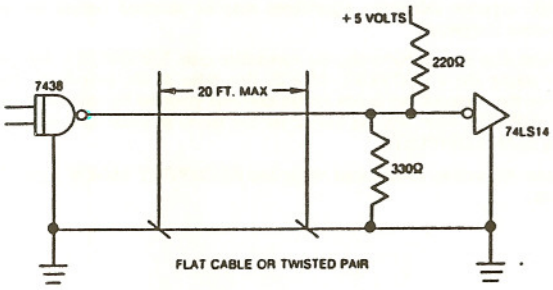


FIGURE 12: Control Signals Driver/Receiver Combination

4.1 HEAD SELECT 2^0, 2^1, 2^2, 2^3

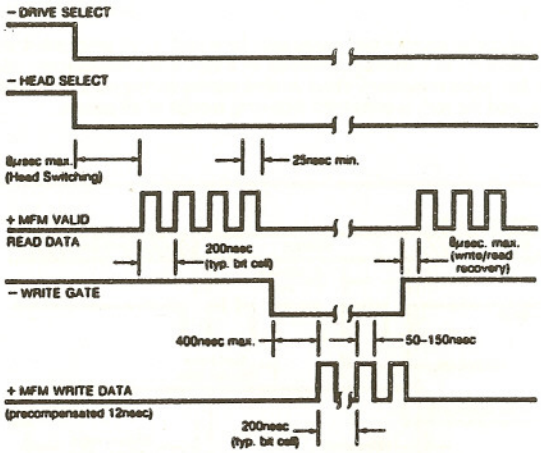
These signals allow the selection of each Read/Write head in a binary code sequence. The heads are numbered 0 through 3. HEAD SELECT 2^0 is the least significant line. When all HEAD SELECT lines are high on the interface, head 0 is selected. Refer below to *Figure 13* below for HEAD SELECT timing.

Note that both HEAD SELECT 2^2 and 2^3 are invalid signals for the ST225. These lines *are* present on the interface, but are terminated. The drive will not respond to these input signals.

4.2 WRITE GATE

The active state of this signal, or low level, enables data to be written to the disc and inhibits carriage motion if WRITE FAULT is active on the receipt of the first Step pulse. When inactive, or high, this signal enables data to be transferred from the drive and enables Step pulses to move the heads.

FIGURE 13:
Read/Write Timing



NOTE: Heads may not be switched while WRITE GATE is active.

STEP 4.3

The STEP signal is a 500nsec (minimum width) pulse that intitiates Read/Write head motion. The number of pulses issued determines distance traveled. Pulses are edge-detected on the leading edge of the pulse.

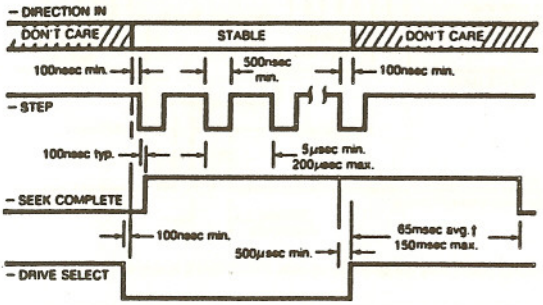
The rate of Step pulses determines the access method. If the period between pulses is from 5µsec to 200µsec, the access method will be Buffered-Seek. Slow-Step is employed if the period between pulses is greater than or equal to 3msec.

DIRECTION IN must be stable 100nsec before the leading edge of the first step pulse and remain stable for 100nsec after the last pulse in a string of Step pulses. Step pulses issued between 200µsec and 3msec may be lost.

If excessive Step pulses are issued which would cause a seek inward beyond Cylinder 670 or outward beyond Cylinder Zero, the drive will enter the Auto-Truncation mode. Refer to *Section 4.3.3.*

4.3.1 BUFFERED SEEK

To minimize access time, pulses may be issued at an accelerated rate and buffered in a counter. Initiation of a seek starts immediately after the first pulse is received. Head motion occurs during pulse accumulation, and the seek is completed following receipt of all pulses.



*Time is from start of head actuation to SEEK COMPLETE.

FIGURE 14: Buffered-Seek Timing

4.3.2 SLOW-STEP (Track-to-Track)

In single-track Slow-Step mode, the Read/Write heads move at the rate of the incoming Step pulses. The minimum pulse period is 3msec. The stepper motor is settled and SEEK COMPLETE is issued 20msec max. after the leading edge of the last pulse.

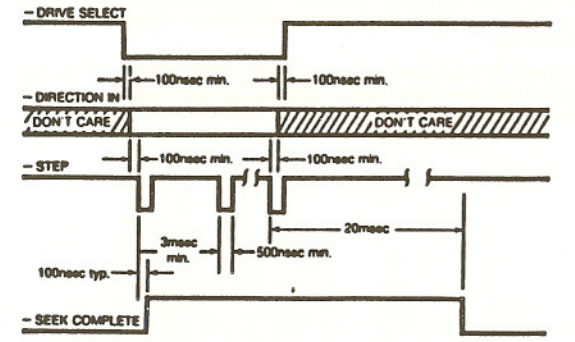


FIGURE 15: Slow-Step Timing

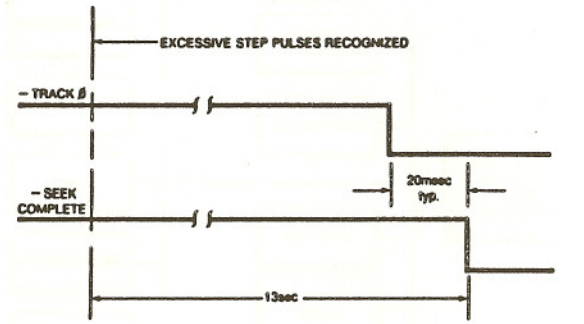
AUTO-TRUNCATION 4.3.3

The drive will enter the Auto-Truncation mode if the controller issues an excessive number of Step pulses, which would place the Read/Write heads outward beyond Track 0 or inward beyond Cylinder 670.

With Auto-Truncation active, the drive will ignore additional pulses, take control of the stepper motor and recalibrate the heads to Track 0. Refer below to *Figure 16*.

CAUTION: If the controller is still issuing Slow-Step pulses after the ST225 issues SEEK COMPLETE from Auto-Truncation mode, the drive will either reenter Auto-Truncation mode with DIRECTION IN false, or step the remaining cylinders with DIRECTION IN true.

FIGURE 16: Auto-Truncation Timing



DIRECTION IN 4.4

DIRECTION IN defines the direction the Read/Write heads will move when the STEP line is pulsed. With DIRECTION IN true, each pulse causes the heads to move one cylinder inward toward the spindle.

When DIRECTION IN is false, each pulse causes the heads to move one cylinder outward toward Track 0.

4.5 DRIVE SELECT

The DRIVE SELECT line is activated by the controller to select and address the drive.

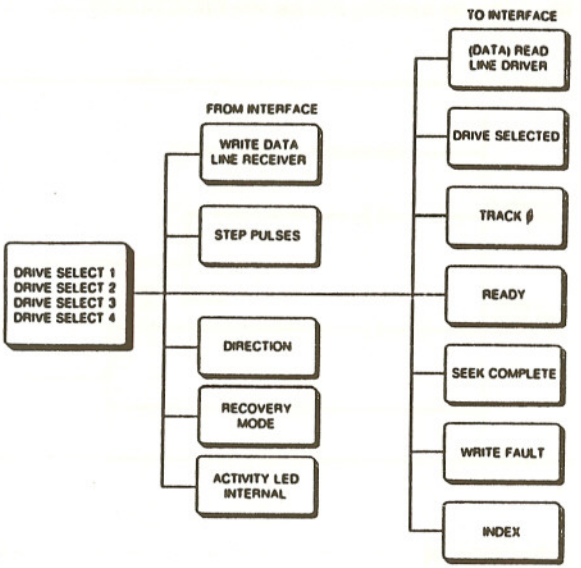
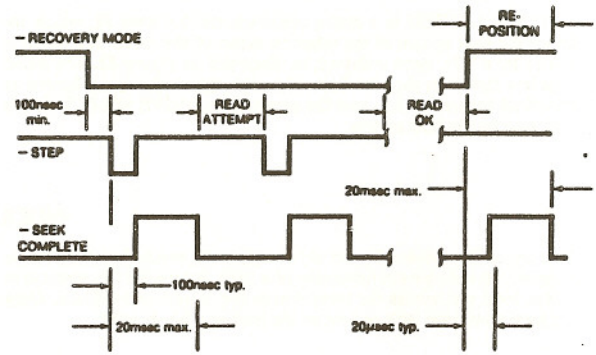


FIGURE 17: Drive Select

RECOVERY MODE 4.8

The RECOVERY MODE line provides a micropositioning option that may be used after the controller has completed its retry options on a Read error. *Section 3.6* above details this option.

FIGURE 18:
Recovery Mode Timing



5.0 CONTROL OUTPUT SIGNALS

The control output signals are gated to the interface when selected. The control output signals are DRIVE SELECTED, INDEX, TRACK ∅, READY, SEEK COMPLETE and WRITE FAULT.

5.1 DRIVE SELECTED

DRIVE SELECTED is a status signal transmitted over J2, which informs the host system of the selection status of the drive. The signal is driven by a TTL open collector, as illustrated in *Figure 12*. The signal goes low (true) on the interface only when the device is configured as described in *Section 3.2*, and the appropriate DRIVE SELECT line is activated by the host system.

5.2 INDEX

This signal is provided by the drive once each revolution (16.67msec nominal) to indicate the beginning of a track. Normally this signal is at a high level and makes the transition to low to indicate INDEX. Only the transition from high to low, or the leading edge, is valid.

5.3 TRACK ∅

This signal is active (true) only when the Read/Write heads are positioned at Cylinder Zero.

Track ∅ is the only cylinder that provides interface recognition. The drive is designed to recalibrate to Track ∅ during power-on and Auto-Truncation operations.

Track ∅ may also be accessed via conventional Buffered-Seek and Slow-Step modes. After Track ∅ is true, no action may be taken by the controller until SEEK COMPLETE is also true.

5.4 INDEX AND TRACK Ø SENSING

The ST225 does not use either an Index or Track Ø sensor. The drive accesses the Index tracks on power-up for reference information. When the drive has reached proper speed, the stepper motor IC is set to phase minus A and minus B. The MPU then seeks in multiples of eight tracks until it finds Track 617 and Track minus 1. These are the reference tracks that are written on all four surfaces.

The MPU uses these tracks to set its internal track counter. The drive then steps in one track from track minus 1 and sets the Track Ø signal on the interface. The MPU will maintain the track count until a recalibration or Auto-Truncation triggers the set-up routine.

The Index tracks, written on Cylinder 617 and Cylinder minus 1, are written with a unique data pattern which generates the Index/Track Ø interface signals. The drive has a simple data discriminator which the MPU samples during initialization. By discriminating the unique data pattern on the Index/Track Ø reference tracks, the MPU can set a divide by two circuit. This circuit allows reliable Index from the spindle motor Hall signal.

READY 5.5

This signal, when true together with SEEK COMPLETE, indicates that the drive is ready to Read, Write or Step and that all control input signals are valid. When this line is high, all reading, writing and stepping are inhibited. The maximum time after power-on for READY to be true is 24 seconds.[10]

During the power-up sequence, READY remains false until:

1. The recalibration to Track Ø is complete
2. Spindle speed is stable within ± 1% of nominal
3. Drive initialization routines are complete
4. DC voltages are within tolerance

SEEK COMPLETE 5.6

This signal goes to a low level (true) on the interface when the Read/Write heads have settled on the final track at the end of a seek. Seeking, reading or writing should not be attempted when SEEK COMPLETE is false. SEEK COMPLETE will go false in the following cases:

1. When a recalibration sequence is initiated (by drive logic) at power-on
2. 100nsec typical after the leading edge of a Step pulse
3. If either + 5 Volts or + 12 Volts are detected as unsafe
4. At the beginning and end of a RECOVERY MODE operation

WRITE FAULT 5.7

This signal notifies the host system that a condition exists which, if not corrected, may cause an incorrect Write operation.

WRITE FAULT SIGNAL GENERATION 5.7.1

With DRIVE SELECT active, and any one of the following conditions true, the WRITE FAULT signal will be issued to the interface and Write Current will be inhibited.

1. Write Gate true with no Write Current to the heads
2. Write Current to the heads with no Write Gate
3. An attempt to Write with RECOVERY MODE active
4. SEEK COMPLETE false
5. A Step pulse is received

WRITE FAULT remains true until the condition which triggered the fault is corrected and the reset is completed.

WRITE CURRENT INTERRUPTION 5.7.1.1

Any one of the following conditions will cause Write Current to be inhibited when Write Gate is true:

1. Multiple heads selected
2. No head selected
3. READY false

10. The 24 second maximum time interval is calculated from the point that the host system power supply maintains the specified ± 5% voltage tolerances.

5.8 FAULT DETECTION

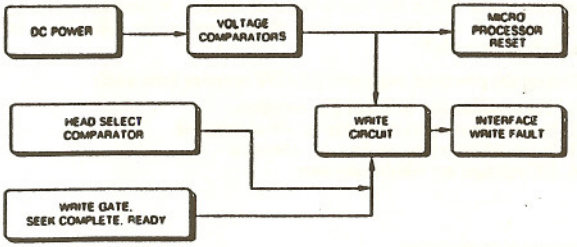


FIGURE 19: Fault Detection Flow

5.8.1 DC-UNSAFE SIGNAL

A DC-Unsafe condition will cause a microprocessor reset. This will prohibit writing, but will not directly cause a WRITE FAULT. If Write Gate remains true, while the MPU resets from a DC-Unsafe condition, a WRITE FAULT will be triggered through the loss of READY and SEEK COMPLETE.

5.8.1.1 VOLTAGE COMPARATOR

The Read/Write LSI (IC 5H) continually monitors the +5 and +12 VDC lines for low voltage conditions. If +5 Volts is > 15% low or +12 Volts is > 20% low, Write Current will be disabled and the MPU will be reset.

5.8.2 HEAD SELECT COMPARATORS

During normal operations a single head will be selected, and the Voltage Center Tap (VCT) will be high (IC 5H, pin-27).

If multiple heads are selected, the voltage will increase at Voltage Head Safe (VHS, IC 5H, pin-26) forcing its output low. Less than one head selected will decrease the voltage at pin-4, forcing its output low. Write Current will then be disabled and the MPU will reset.

6.0 POWER-ON SEQUENCE

The application of DC power inititates a sequence that starts the spindle motor, regulates its speed, steps the Read/Write heads to Track 0 and issues READY and SEEK COMPLETE sequentially to terminate the sequence.

READY and SEEK COMPLETE are issued to the interface when the drive is available to accept commands. Upon power-up the drive is available to accept commands 24 seconds max. after the power supply voltages maintain the specified ± 5% voltage tolerances.

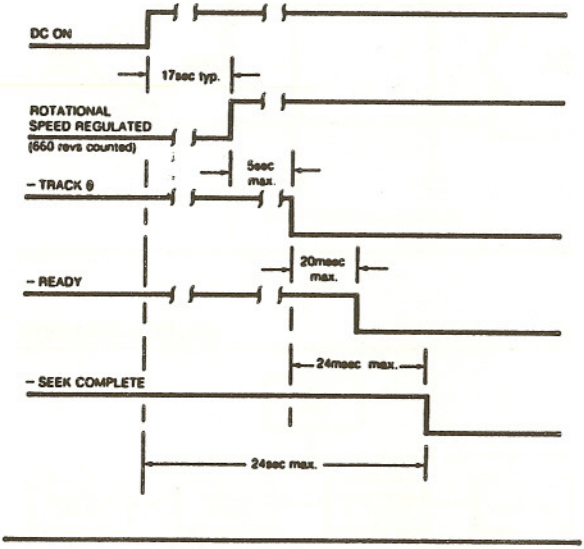


FIGURE 20: Power-On Sequence Timing

7.0 DATA TRANSFER LINES

Two pairs of balanced signals are employed for data transfer: MFM WRITE DATA and MFM READ DATA. Data transfer lines between the host system and the drive are differential in nature and may not be multiplexed. Refer above to *Table 2* for data transfer pin assignments and *Figure 7* for a host/drive interconnection example.

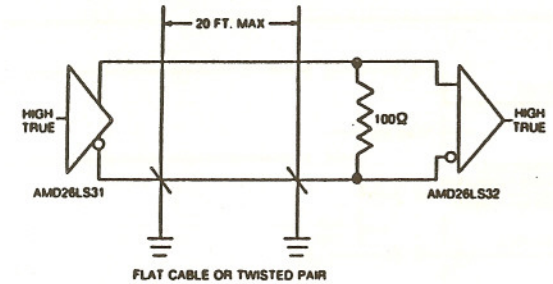


FIGURE 21: Data Signal Driver/Receiver Combination

7.1 WRITE OPERATION

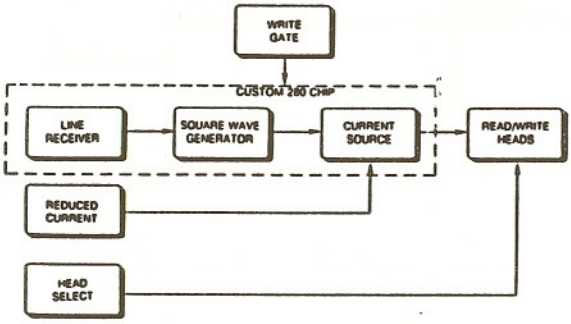


FIGURE 22: Write Operation

In order to Write, the following conditions must be true:

1. DRIVE SELECT active
2. READY active
3. SEEK COMPLETE active
4. Write Gate active
5. WRITE FAULT inactive
6. RECOVERY MODE inactive

MFM WRITE DATA 7.1.1

WRITE DATA is transmitted by a differential pair which defines the transitions to be written on the disc. The + MFM WRITE DATA line going more positive than the − MFM WRITE DATA line is the active transition. This signal must be driven to an inactive state when in the Read mode.

WRITE GATE 7.1.2

A Write sequence is initiated when Write Gate is activated, which causes the Read/Write LSI to apply + 12 Volts to the center tap of the selected lead; concurrently data is sent to the line receiver.

LINE RECEIVER 7.1.3

Differential Write data, which is precompensated MFM, is received from the controller and changed to single line. It is then fed into the pulse generator, which changes pulse data to square wave data.

Pin-5, at IC 5H, will be activated if plus data is to be written. Pin-9 will be activated for minus data.

PRECOMPENSATION 7.1.4

Precompensation is recommended on Tracks 300 through 614. The optimum amount of precompensation is 12nsec for both early and late bits. *Table 3* below indicates the bit patterns and the direction to be compensated. An X denotes a "don't care state."

As the Read/Write heads travel inward, the track circumference of course decreases, and the data bits are necessarily written closer together. The Write Current is therefore reduced to preclude any pulse crowding.

The ST225 does not require the host to specify a cylinder(s) to begin applying reduced Write Current. This function is managed internally by the microprocessor.

TABLE 3: Precompensation Pattern

PREVIOUS		SENDING	NEXT	TIMING
X	0	1	1	WRITE DATA LATE
X	1	1	0	WRITE DATA EARLY
1	0	0	0	WRITE CLOCK LATE
0	0	0	1	WRITE CLOCK EARLY

ALL OTHER PATTERNS NOMINAL

7.2 READ OPERATION

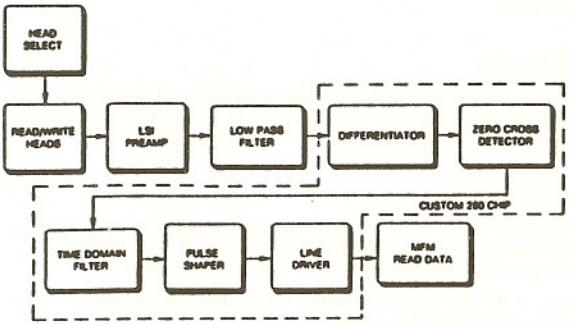


FIGURE 23: Read Operation

7.2.1 MFM READ DATA

The data recovered by reading a track is transmitted to the host system via a differential pair of MFM READ DATA lines. The transition of the + MFM READ DATA line going more positive than the − MFM READ DATA line, represents a flux reversal on the track of the selected head.

7.2.2 HEAD SELECT

The binary decoder (IC 4H) selects the desired head based on the status of the Head Select lines. If the DC voltages are too low, possibly causing an inaccurate Read operation, the decoder (pin-12) will select a nonexistent head. By referencing 0 to +5 Volts actual ground appears as −5 Volts, which eliminates the necessity of a negative power source normally required by the LSI preamp.

7.2.3 LSI PREAMP

With the Head Center Tap (HCT) active, data from the selected head will flow into the preamp (9E), which amplifies the Read signal and also acts as a high-pass filter.

The HCT voltages are monitored and controlled by the custom Read/Write LSI (5H). This chip monitors the Write Gate line and sets the appropriate level on its Voltage Center Tap (VCT) for Read or Write mode.

7.2.4 LOW-PASS FILTER

This filter network attenuates high frequency noise, which is outside the normal data signal range.

7.2.5 PHASE SHIFTER

Amplified data enters the circuit and is shifted 90° so peak data, which was detected over a fairly broad range, is now moved to a highly sloped accurately detectable position at the zero crossing point.

ZERO-CROSS DETECTOR 7.2.6

This element detects bit positions as the slope of the Read Data signals crosses the zero threshold. At this point analog data are changed to digital.

TIME DOMAIN FILTER 7.2.7

When a high resolution head reads a low frequency data pattern, there is a tendency for the head signal to decay between bits. If the signal decays below the zero cross threshold, a spurious data bit will be generated. Such false bits are ignored by delaying the clocking bit past the potential point of highest drop.

LINE DRIVER 7.2.8

This element changes raw digital data to a differential data, providing immunity to common mode noise during transmission.

8.0 THEORY OF OPERATIONS

8.1 MICROPROCESSOR

The microprocessor monitors and controls the internal drive functions and the host interface lines. The MPU has only three active modes: Initializing, Waiting, or Seeking.

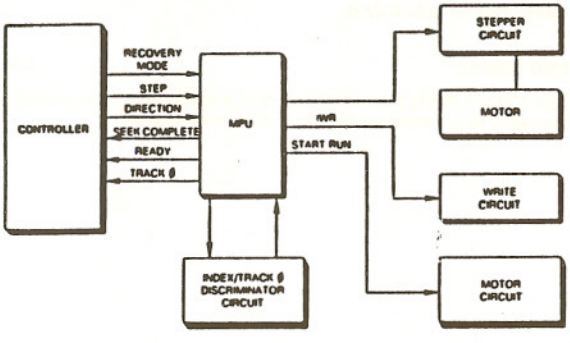


FIGURE 24: Microprocessor Operation

8.1.1 MPU INITIALIZING

At power-on, the MPU initializes the stepper circuit to phase minus A and minus B, and resets all interface lines under its control.

As the drive spins-up, the MPU switches from bipolar to unipolar after approximately 40 revolutions. The processor will measure the period of the index signal to assure that the drive is up-to-speed before the recalibration routine is initiated.

The MPU sets phase minus A and minus B on the stepper chip (IC 8D) and then executes the Seek and Discriminator routines, which recalibrates the Read/Write heads to Track Ø, divides Index, and gives READY and SEEK COMPLETE. The drive is available to accept commands 24 seconds max. after power-up.

8.1.2 MPU-IDLE

When in the idle mode, the MPU loops, waiting for Step pulses. The custom Read/Write LSI chip monitors the power inputs and, on transients, resets the MPU which will reinitialize the drive.

SEEKING 8.1.3

Upon receiving a Step pulse, the MPU pauses for 250μsec to allow for additional pulses before executing the seek operation. Every incoming pulse resets the 250μsec timer. The seek will not begin until the last pulse is received.

When seeking, the MPU counts the number of tracks to be covered, and employs the optimum step algorithm to reach the target track.

While seeking, the MPU controls the direction and mode of the custom stepper IC. Pulses are sent to the stepper chip, which does the actual phase commutations. Acceleration/deceleration are determined by the varied frequency of the pulses and the use of the Motor IC Direction line. This IC provides both a current source and sink to motor windings.

With READY and SEEK COMPLETE true, the MPU returns to the Idle mode.

SPINDLE MOTOR CONTROL 8.2

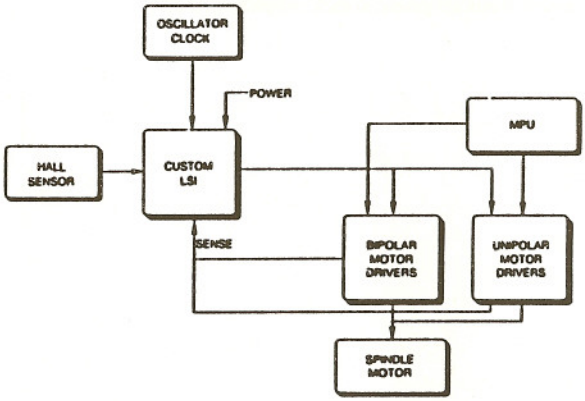


FIGURE 25: Spindle Motor Control

To insure sufficient starting power, the spindle motor circuit is run with a set of biploar motor drivers. Once the spindle motor has started running, the MPU switches the motor circuit from bipolar to unipolar drivers; which significantly lowers the required running current.

The primary functions, listed below, are incorporated within the custom spindle motor IC (IC 4B).

1. Monitors the Hall signal from the spindle motor and uses the Hall transistions to commutate the motor phases. It regulates the motor speed by measuring the Hall period and comparing it to the oscillator clock period.
2. Employs a sense line to regulate the start current and execute a current limit shut-off.
3. Monitors the power supply for output driver shut-off,. When the power is off, the output drivers become self-biases on, which brakes the motor using back-EMF.
4. Locked-Rotor Protection: IC 4B monitors the time from the first Hall transition. If the motor does not spin-up, the drivers will be disabled to avoid overheating the circuit. This Hall signal is generated by a transducer located in the motor hub. Two complete square waves are generated each complete revolution.

9.0
FIELD SERVICE

The ST225 does not require preventative maintenance. The PC Board may be exchanged in the field. Refer below to *Section 9.1* for this procedure.

PC BOARD REMOVAL 9.1

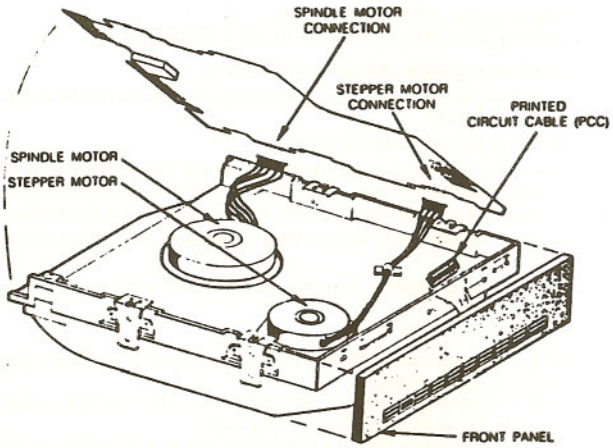
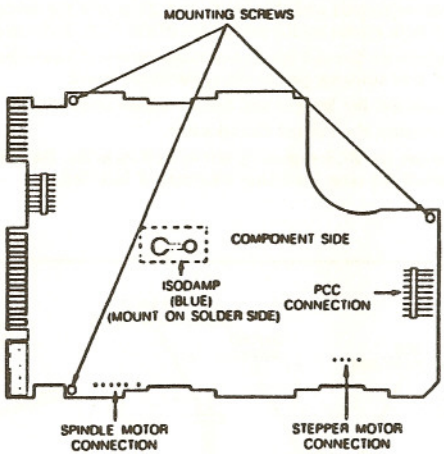


FIGURE 26:
PC Board Removal



It is mandatory that approved ESD precautions be observed during this procedure. This includes anti-static wrist-straps.

Note: Earlier revisions of this PCB, Seagate part number 20301, required the PROM (7D) to be transferred to the replacement PCB. This is no longer required and the replacement board is downward compatible for all versions.

Parts Required: PC Board 20301-004
Tools Required: Torque driver, T-10 and T-5 Torx bits

1. Secure a padded anti-static work surface.
2. Remove the two front panel screws (or if installed, the printed circuit cable shield.)
3. Orient the drive with the PCB up.
4. Remove and retain the three PCB mounting screws. There may be a clear insulating washer installed at one or more of the mounting points. Be sure to replace at the same point(s) during reassembly.
5. Locate and carefully free the Printed Circuit Cable. Do not crease the cable.
6. Locate and carefully free the spindle motor and stepper motor connections.
7. Lift out the PCB.
8. Your replacement PCB will be shipped to you with a kit containing two ground springs.
   a. If the spindle motor has a steel ball in the center of its hub, mount the spring with the graphite button (1).
   b. If the spindle motor has a short post at the center of the hub, mount the bare copper spring (2).
9. Verify that the Ground Spring assembly is aligned and will make positive contact with the spindle hub. Note that the washer and hex nut both mount on the solder side of the PCB. Refer to *Figure 27.*
10. Tighten the Ground Spring mounting screw to 2.5 inch/lbs. Transfer the blue Isodamp pad to the replacement board.
11. Reconnect the Stepper and Spindle motor connections.
12. Reconnect the Printed Circuit cable.
13. Torque the PCB mounting screws to 9 inch/lbs. Do not forget to replace the clear insulating washer(s), if installed.

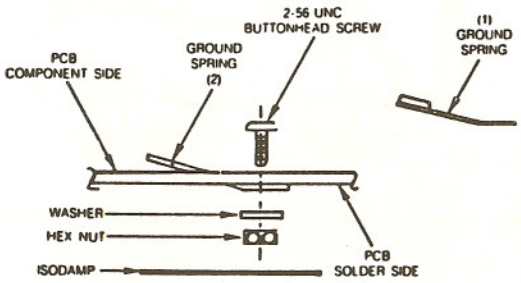
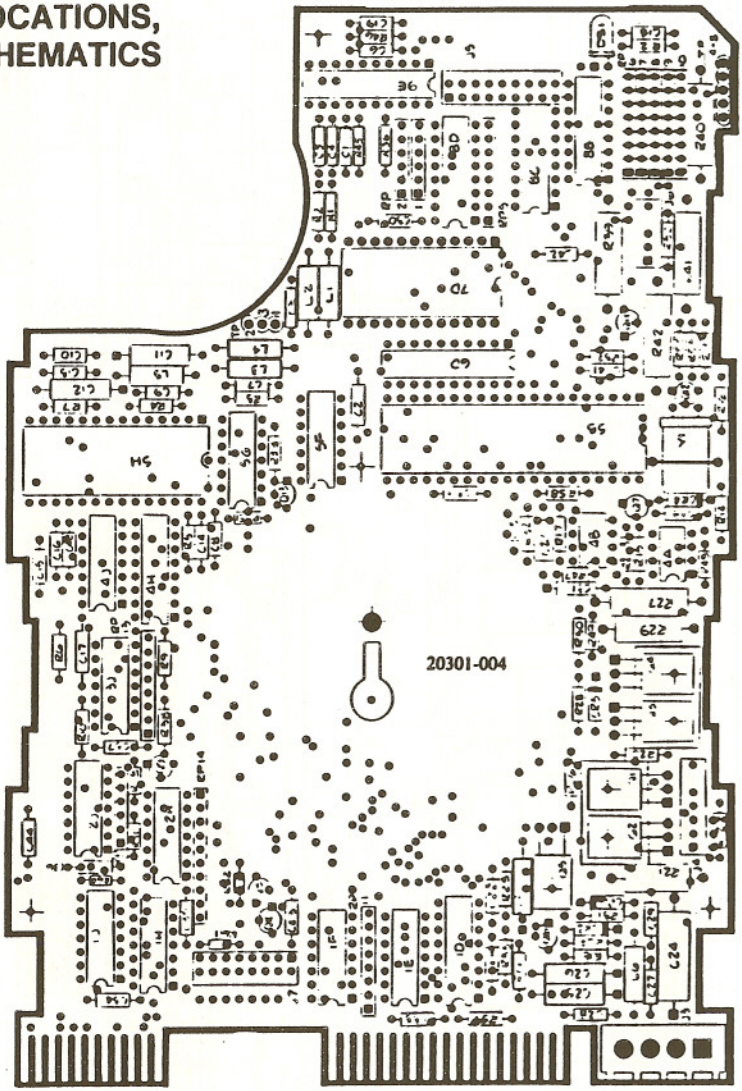
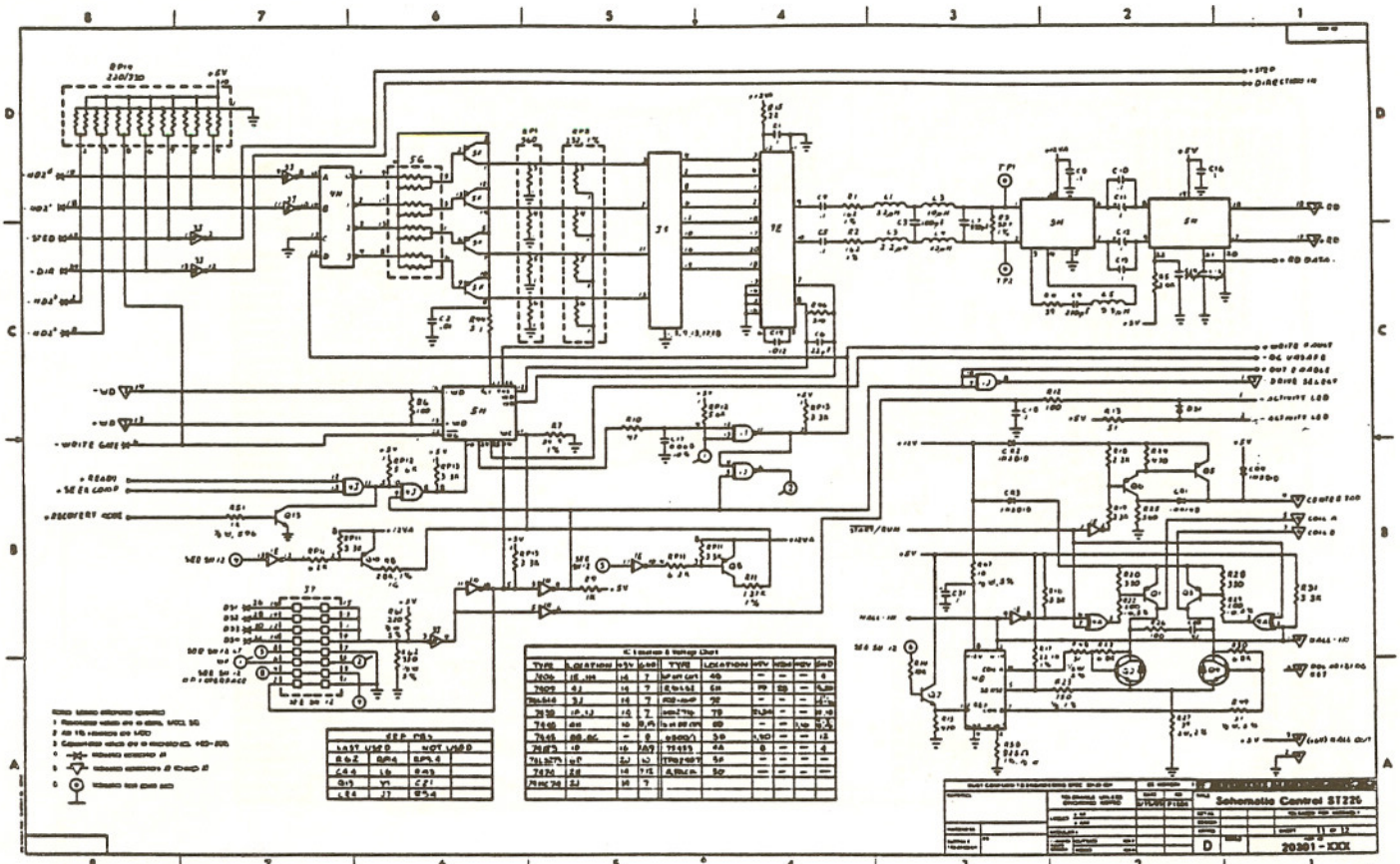
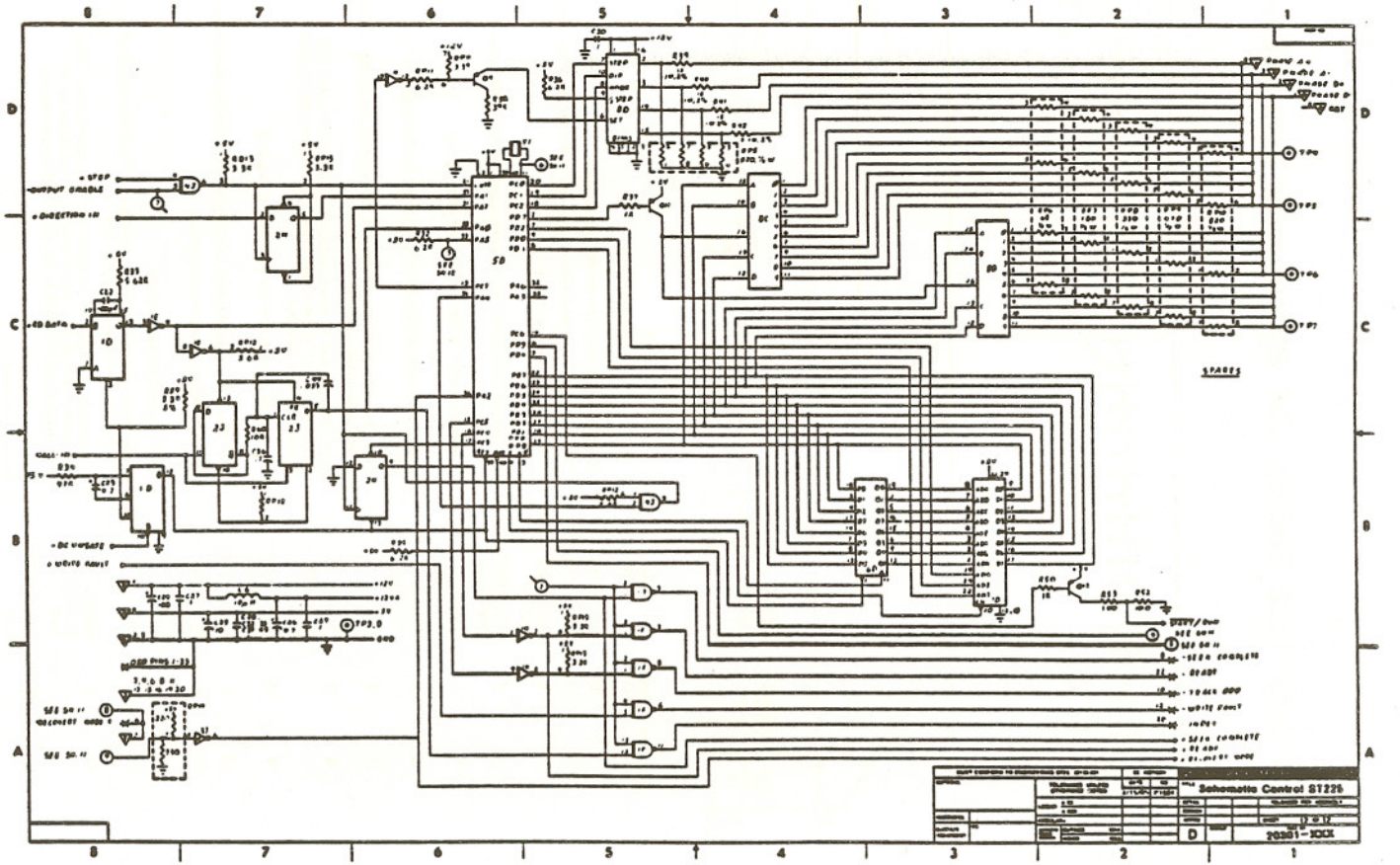


FIGURE 27: Ground Spring Assembly

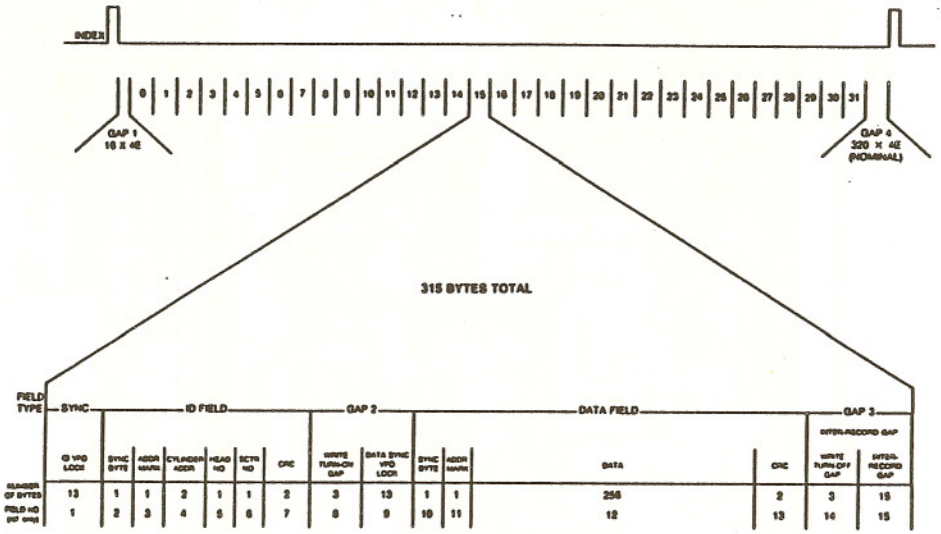
10.0 COMPONENT LOCATIONS, SCHEMATICS




Schematic Control ST225
20381-XXX


SPARES
Schematic Control ST225
20301-XXX

Appendix 1:32 Sector, 256 Byte/Sector Format Example



Reference Number	Number of Bytes	Field Name	Field Description
1	13	ID VFO LOCK	A field of all zeros to sync the VFO for the ID
2	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows
3	1	ADDRESS MARK	"FE" Hex defining that ID field data follows
4	2	CYLINDER ADDRESS	A numerical value in Hex defining the detent position of the acuator
5	1	HEAD NUMBER	A numerical value in Hex defining the head selected
6	1	SECTOR NUMBER	A numerical value in Hex defining the sector for this section of the rotation
7	2	CRC	Cyclic Redundancy Check information used to verify the validity of the ID field information just read
8	3	WRITE TURN-ON GAP	Zeros written during format to isolate the write splice created. This field assures valid reading of field number 7 and allows the 13 bytes required for Data VFO lock.
9	13	DATA SYNC VFO LOCK	A field of all zeros to sync the VFO for the data field
10	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows
11	1	ADDRESS MARK	"F8" Hex defining that user data follows
12	256	DATA	This area available for user data
13	2	CRC	Cyclic Redundancy Check information used to verify the validity of the user data field information just read
14	3	WRITE TURN-OFF GAP	Zeros written during update to isolate the write splice created. This field assures valid reading of field number 13 and allows the 13 bytes required for VFO lock for the ID field of the next sector.
15	15	INTER-RECORD GAP	A field of all zeros which acts as a buffer between sectors to allow for speed variation

Appendix 2: Standard Spares List

Front Panel, half-height:	**58838-001**
Front Panel, full-height:	**50449-001**
Shunt:	**10027-001**
Main Control PC Board:	**20301-004**

Appendix 3: ST213

Specifications

UNFORMATTED CAPACITY

Per Drive:	12.81 Megabytes
Per Cylinder:	20,832 Bytes
Per Track:	10,416 Bytes

FORMATTED CAPACITY

Per Drive:	10.71 Megabytes
Per Cylinder:	17,408 Bytes
Per Track:	8,704 Bytes
Per Sector:	512 Bytes
Sectors per Track:	17

PHYSICAL ORGANIZATION

Tracks:	1,230
Cylinders:	615
Read/Write Heads:	2
Discs:	1

FUNCTIONAL SPECIFICATIONS

Rotational Speed:	3,600 RPM ± 1%
Recording Scheme:	MFM
Recording Density:	9,827 BPI
Flux Density:	9,827 FCI
Track Density:	588 TPI
Interface:	ST412
Data Transfer Rate:	5.0 Megabits/sec

ACCESS TIME (Incl. settling)

Track-to-Track:	20msec
Average:	65msec
Full Stroke:	150msec
Latency:	8.33msec nominal

ERROR RATES

Recoverable Read Errors:	1 per 10^{9} bits read *
Nonrecoverable Read Errors:	1 per 10^{12} bits read **
Seek Errors:	1 per 10^{6} seeks

* Recoverable within 10 retries
** Not recoverable within 10 retries

RELIABILITY SPECIFICATIONS

MTBF:	20,000 Power-on Hours
PM:	Not Required
MTTR:	30 Minutes
Service Life:	5 Years

OPERATIONAL ENVIRONMENT

Ambient Temperature:	10°C to 45°C (50°F to 113°F)
Temperature Gradient:	10°C/hr. (18°F/hr.)
Relative Humidity:	8 to 80% noncondensing
Maximum Wet Bulb:	26°C (78.8°F) noncondensing

DC POWER REQUIREMENTS

+12VDC ± 5%	.9 Amps typ.
	2.2 Amps max. at power-up
+5VDC ± 5%	.8 Amps typ.
Power:	14.8 Watts typ.

PHYSICAL SPECIFICATIONS

Height:	1.63 inches max. (41.4mm)
Width:	5.75 inches (146.05 mm)
Depth:	8.00 inches max. (203.2mm)
Weight:	2.75 lbs. (1.25 Kg)

920 Disc Drive, Scotts Valley, CA 95066-4544, USA ■ 408/438-6550