12 MHz Zero-Wait 80286 Turbo Main Board

MBVLSI-168 (V.2)

The information in this manual is subject to change without notice.

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WHAT WE POSSESSIVE THAT OTHERS WITHOUT !

* 5 chips set full CMOS process low power consumption
* Zero wait state read operations
* One wait state write operations
* 20 mA, 200pF slot drive (system bus) capability
* 8 mA, 150pF DRAM drive capability
* Four layer implementation for low noise operation.
* Most powerful memory combination available:
  –Using 44256/41256 memory chip, up to 512K/1024K
  –Using 4164/41256/1M bit memory chip, up to 512K/640K/1024K/2048K/4096K
  –Using RAM Modular, UP TO 512K/1024K/2048K/4096K

NOTE: In this manual,
80286: means Personal Computers that use 80286 CPU

I. GENERAL SPECIFICATION

* Fully compatible with 80286 system
* 8/12 MHz speed hardware and software selectable
* RAM access time 0-wait and 1-wait switchable
* Up to 4 mega byte memory on board
* 16 mega byte expandable memory in the protect, virtual address mode
* 2 sockets for BIOS.
* 8 I/O expansion slots
* Socket for 80287 math processor
* CMOS clock and calendar circuit with rechargable battery support
* 24-bit addressing and 16-bit data path capabilities
* 16-level interrupts
* 7-channel DMA (Direct memory access)
* 3-programmable timers
* 1/0 speed: 8MHz
* Most powerful memory combination available:
  –Using 44256/41256 memory chip, up to 512K/1024K
  –Using 4164/41256/1M bit memory chip, up to 512K/640K/1024K/2048K/4096K
  –Using RAM Modular, UP TO 512K/1024K/2048K/4096K

II. MAIN BOARD JUMPER SELECTION

CONNECTORS AND JUMPERS:

Jumper No.	Function
PS1/PS2	– Power supply connector
KB1	– Keyboard connector
JP1	– Hardware reset switch
JP2	– Keylock/Power LED
JP3	– Speaker connector
JP4	– Turbo hardware switch
JP5	– Turbo LED indicator
JP6	– Memory speed Jumper
JP7/JP8/JP9	– Memory size select
JP10	– Zero wait/One wait select
JP11	– EPROM size select
JP12	– Display adapter select
*JP13/JP14/JP15/JP18	– Keyboard controller select
JP16	– Power good select
JP17	– External battery connector

*: Jumper JP13/JP14/JP15/JP18 is default-set for software speed change, which according to the "BIOS" used in this board.
It is not necessary for user to adjust the jumper setting, unless user would like to change the "BIOS".
More technical information, please refer to "ATTACHMENT I"

JP1: Hardware reset switch
It's a reset button

JP4: Turbo hardware switch
It's a Turbo button

JP5: Trubo LED indicator
LED lights on for Turbo mode

JP6: Memory speed select
Short Pin 1 & Pin 2 of Jumper JP6:
using 100ns speed memory chips (DEFAULT)

JP7/JP8/JP9: Memory size select

JP7/JP8/JP9	Amount memory	(Base memory	/Expansion memory)
open/short/short	4096K (4MB)	640K	/3456K)
short/open/open	2048K (2MB)	(640K	/1408K)
short/open/short	1024K (1MB)	(640K	/384K))
short/short/open	640K	(640K	/0)
short/short/short	512K	(512K	/0)

JP10: Zero wait/One wait select
Short JP10: Zero wait
Open JP10: One wait

JP11: EPROM size select
Short JP11: Using 256K EPROM
Open JP11: Using 128K EPROM

JP12: Display adapter select
Short JP12: Using Color display adapter
Open JP12: Using Monographics display adapter

JP16: Power good select
Short Pin 1 & Pin 2 of JP16: Power good provided by Mother Board (default)
Short Pin 2 & Pin 3 of JP16: Power good provided by Power supplier itself

JP17: External battery connector
The connector is for connecting for size "AA" batteries instead of the blue barrel shaped rechargable battery. Pin assignments as followings:

PIN	ASSIGNMENT
1	6Vdc
2	Not used
3	GND
4	GND

JP13/JP14/JP15/JP18: Keyboard controller

Jumper JP13/JP14/JP15/JP18 is default-set to change speed via software, and which according to the "BIOS" used in this board.

Unless you would like to change the "BIOS", it is not necesory for you to adjust the Jumper setting. More technical information, please refer to "ATTACHMENT I".

III MEMORY COMBINATION

III-1: Using 44256/41256 memory chip combination:

Memory size	Jumper setting	Bank 0 socket position	Bank 1 socket position
512K	JP7/JP8/JP9 short/short/short	44256 x 4 pcs (U47-U50) 41256 x 2 pcs (U29 & U38)	————
1024K (1MB)	short/open/short	44256 x 4 pcs (U47-U50) 44256 x 4 pcs (U29 & U38)	44256 x 4 pcs (U41-U44) 41256 x 2 pcs (U11 & U20)

III-2: Using 4164/41256/1Mbbyte memory chip combination:

Memory size	JP7/JP8/JP9	Bank 0	Bank 1
512K	short/short/short	41256 x 18 pcs (U21-U38)	————
640K	short/short/open	41256x18 pcs (U21-U38)	4164 x 18 pcs (U3-U20)
1024K (1MB)	short/open/short	41256 x 18 pcs (U21-U38)	41256 x 18 pcs (U3-U20)
2048K (2MB)	short/open/open	1M byte x 18 pcs (U21-U38)	————
4096K (4MB)	open/short/short	1M byte x 18 pcs (U21-U38)	1M byte x 18 pcs (U3-U20)

III-3 Using RAM MODULAR Chip combination:

Memory size	JP7/JP8/JP9	Bank 0	Bank 1
512K	short/short/short	256K x 2 sets (U1 & U2)	———
1024K (1MB)	short/open/short	256Kx2 sets (U1 & U2)	256K x 2 sets (U39 & U40)
2048K (2MB)	short/open/open	1MB x 2 sets (U1 & U2)	———
4096K (4MB)	open/short/short	1MB x 2 sets (U1 & U2)	1MB x 2 sets (39 x& U40)

NOTE: User cannot combinate each of Item III-1/III-2/III-3 for total amount memory.
Each item III-1/III-2/III-3 works independently.

IV HOW TO CHANGE THE SYSTEM SPEED BY SOFTWARE

This mother board has two system clock i.e. 8MHz and 12MHz, User can change speed via hardware or software controller.

IV–1 Hardware controller:
Hardware controller: refer to JP4, press "Turbo switch button" for Turbo/Normal mode

IV-2 Software controller:

IV-2-1 When the equipment of mother board used "AMI BIOS" Press and hold down 〈CTRL〉 & 〈ALT〉 key and hit the 〈+〉or 〈–〉key for Turbo/Normal speed change.

IV-2-2 When the equipment of mother board used "AWARD BIOS" Press and hold down 〈CTRL〉 & 〈ALT〉 key and hit the 〈+〉 or 〈–〉 key for Turbo/ Normal mode.

IV-2-3 When the equipment of mother board used "PHONIX BIOS" Press and hold down 〈CTRL〉 & 〈ALT〉 key and hit the 〈\ 〉 key for Turbo/Normal mode.

Due to different version of PHONIX BIOS, user may press and hold down 〈CTRL〉 & 〈ALT〉 key and hit the 〈+〉 or 〈–〉 key for Turbo/Normal mode.

V. SYSTEM MEMORY MA)

ADDRESS RANGE	START-END	NAME	FUNCTION
000000-03FFFF	000K-256K	Bank 0	System memory (256K)
040000-07FFFF	256K-512K	Bank1	System memory (256K)
080000-09FFFFF	512K-640K	Bank2	System memory (128K)
0AFFFF-0BFFFF	640K-768K	Video	Display card buffer (128K)
0C0000-0DFFFF	768K-869K	I/O ROM	Expansion ROM (128K)
0E0000-0EFFFF	896K-960K	ROM	System usage (64K)
0F0000-0FFFFF	960K-1024K	ROM	BIOS (64K)
100000-11FFFF	1024K-1152K	Bank 2	System memory (128K)
120000-15FFFF	1152K-1408K	Bank 3	System memory (128K)
160000-FDFFFF	1408K-16146K	RAM	Expansion RAM (14870K)
FE0000-FEFFFF	16146K-16210K	ROM	System usage (64K)
FF0000-FFFFFF	16210K-16274K	ROM	BIOS (64K)

VI. I/O CHANNEL SLOTS

The I/O channel supports:

* I/O address space hex 100 to hex 3FF
* 24-bit memory addresses (16MB)
* Refresh of system memory from channel microprocessors
* Selection of data accesses (eigher 8 bit or 16 bit)
* Interrupt
* DMA channels
* I/O wait-state generation
* Open-bus structure (allowing multiple microprocessors to share the system's resources, including memory)

I/O ADDRESS MAP

HEX RANGE	DEVICES	USAGE
000-01F	DMA controller 1	System
020-03F	Interrupt controller 1	System
040-05F	Timer	System
060-06F	8042 (Keyboard)	System
070-07F	Real time clock, NMI mask	System
080-09F	DMA page register	System
0A0-0BF	Interrupt controller 2	System
0C0-0DF	DMA controller 2	System
0F0	Clear Math Coprocessor busy	System
0F1	Reset Math Coprocessor	System
0F8-0FF	Math Coprocessor	System
1F0-1F8	Fixed disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel printer port 2	I/O
2F8-2FF	Serial port 2	I/O
300-31F	prototype card	I/O
360-36F	Reserved	I/O

I/O ADDRESS MAP

HEX RANGE	DEVICES	USAGE
378-37F	Parallel printer port 1	I/O
380-38F	SDLC, bisynchronus 2	I/O
3A0-3AF	Bisynchronus 1	I/O
3B0-3BF	Monochrome display and printer adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/graphic monitor adapter	I/O
3F0-3F7	Floppy diskette controller	I/O
3F8-3FF	Serial port 1	I/O

Numbering of the I/O slots is as follows:

REARPANEL

GND	B1	A1	–I/O CH CK
RESET DRV	B2	A2	SD7
+5Vdc	B3	A3	SD6
IRQ2	B4	A4	SD5
–5Vdc	B5	A5	SD4
DRQ2	B6	A6	SD3
–12Vdc	B7	A7	SD2
0WS	B8	A8	SD1
+12Vdc	B9	A9	SD0
GND	B10	A10	–I/O CH RDY
–SMEMW	B11	A11	AEN
–SMEMR	B12	A12	SA19
–IOW	B13	A13	SA18
–IOR	B14	A14	SA17
–DCK3	B15	A15	SA16
DRQ3	B16	A16	SA15
–DACK1	B17	A17	SA14
DRQ1	B18	A18	SA13
–REFRESH	B19	A19	SA12
CLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
–DACK2	B26	A26	SA5
T/C	B27	A27	SA4
BALE	B28	A28	SA3
+5Vdc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0

I/O CHANNEL J1 – J8

REARPANEL

Signal	Pin	Pin	Signal
–MEM CS16	D1	C1	SBHE
I/O CS16	D2	C2	LA23
IRQ16	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
–DACK0	D8	C8	LA17
DRQ0	D9	C9	–MEMR
–DACK5	D10	C10	–MEMW
DRQ5	D11	C11	SD08
–DACK6	D12	C12	SD09
DRQ6	D13	C13	SD10
– DACK7	D14	C14	SD11
DRQ7	D15	C15	SD12
+5Vdc	D16	C16	SD13
–MASTER	D17	C17	SD14
GND	D18	C18	SD15

I/O CHANNEL J2 – J7

VII. HARDWARE COMPATIBILITY

SYSTEM TIMERS

The system has three programmable timer/counters controlled by an Intel 8254-2 timer/counter chip. These are channels 0 through 2, defined as follows:

Channel 0	System Timer
GATE 0	Tied on
CLK IN 0	1.190 MHz OSC
CLK OUT 0	8259A IRQ

Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190MHz OSC
CLK OUT 1	Request Refresh Cycle

Note: Channel 1 is programmed to generate a 15 microsecond period signal.

Channel 2	Tone Generation for Speaker
GATE 2	Controlled by bit 0 of port hex 61 PPI bit
CLK IN 2	1.190 MHz OSC
CLK OUT 2	Used to drive the speaker

SYSTEM INTERRUPTS

Sixteen levels of system intrrupts are provided by the 80286 NMI and two 8259A Interrupt Controller chips. The following shows the interrupt-level assignments in decreasing Priority:

LEVEL		FUNCTION
Microprocessor NMI		Parity or I/O channel check
Interrupt controllers		
CTLR 1	CTLR 2	
IRQ 0		Timer output 0
IRQ 1		Keyboard (Output buffer full)
IRQ 2		Interrupt from CTLR 2
	IRQ8	Realtime clock interrupt
	IRQ9	Software redirected to INT 0Ah (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed disk controller
	IRQ15	Reserved
IRQ 3		Serial port 2
IRQ 4		Serial port 1
IRQ 5		Parallel port 2
IRQ 6		Diskette controller
IRQ 7		Parallel port 1

DIRECT MEMORY ACCESS

Eight DMA channels are supported by the system. Two Intel 8237-5 DMA controller chips (four channels in each chip) are used. DMA channels are assigned as follows:

CTLR1	CTLR2
Ch 0 – Spare	Ch 4 – Cascade for CTRL 1
Ch 1 – SDLC	Ch 5 – Spare
Ch 2 – Diskette	Ch 6 – Spare
Ch 3 – Spare	Ch 7 – Spare

Channels 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB blicks throughout the 16-megabyte system address space.

Channel 4 through 7 are contained in DMA conroller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfers of 16-bit data between 16-bit adapters and 16-bit system memory are supported by channels 5, 6, 7. DMA channels 5 through 7 will transfer data in 128KB blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The addresses for the page register are as follows:

PAGE REGISTER	I/O HEX ADDRESS
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows:

* For DMA channels 3 through 0

SOURCE	DMA PAGE REGISTERS	8237A-5
Address	A23 – A16	A15 – A0

Note: To generate the addressing signal "byte high enable" (BHE) invert address line A0.

* For DMA channels 7 through 5

SOURCE	DMA PAGE REGISTERS	8237A- 5
Address	A23 – A17	A16 – A1

Note: The BHE and A0 addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries (64KB for channels 0 throught 3 and 128KB for channels 5 through 7).

REAL TIME CLOCK AND NONVOLATILE RAM

The real time clock MC146818 and its 64 bytes of RAM information are backed up by 6V DC battery. the internal colock circuitry uses 14 bytes while the rest is allocated to system configuration.

ADDRESS	DESCRIPTION
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown
10	Diskette drive type byte-driver A and B
11	Reserved
12	Fixed disk type byte – driver C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte

ADDRESS	DESCRIPTION
19 – 2D	Reserved
2E – 2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34 – 3F	Reserved

ATTACHMENT I FUNCTION OF JUMPER JP13/JP14/JP15/JP18

In this mother board, Jumper setting of JP13/JP14/JP15/JP18 is provide to enable user to change speed via software. As different "BIOS" and "keyboard controller" makes different Jumper setting of JP13/JP14/JP15/JP18. Before you choose the specific "BIOS" for this mother board, be sure that the keyboard controller (8042 controller) is compatible with this "BIOS".

Once the "BIOS" and "Keyboard controller" are selected, it is necessary to short one of these Jumper JP13/JP14/JP15/JP18 for software speed change, and which according to the "controller pin" that this specific "BIOS" and "keyboard controller" supported.

a) Short JP13: menas keyboard controller is set on "PIN 30"
b) Short JP14: means keyboard controller is set on "PIN 23"
c) Short JP15: means keyboard controller is set on "PIN 27"
d) Short JP18: means keyboard controller is set on "PIN 32"

While the Jumpers JP13/JP14/JP15/JP18 is set correctly, you can change the system speed by software.

ATTACHMENT II