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IBM PC*jr* Speech Attachment Technical Reference

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Description

The Speech Attachment adds speech capability to the PC*jr*™. It uses a 32K by 8-bit ROM module, which contains the standard vocabulary and BIOS support. This module appears as normal system memory at hex CE000 through CFFFF.

The Speech Attachment provides two technologies for speech reproduction:

- Speech synthesis using linear predictive coding (LPC).
- Speech encoding (speech-to-data) and decoding (data-to-speech), using a continuously variable slope delta (CVSD) modulation technique.

LPC

LPC synthesizes speech from compressed speech data on the internal ROM module. Speech data in LPC format may also be placed in RAM from a diskette or other storage devices. LPC contains a vocabulary of words, phrases, and sound effects.

CVSD

CVSD allows the user to encode speech using a microphone and store the resulting uncompressed speech data in system memory or on diskette. The stored speech data can then be decoded with the resulting speech output available on the audio channel. The microphone jack is at the rear of the attachment.

PC*jr* is a trademark of the International Business Machines Corporation.

The following is a block diagram of the Speech Attachment:

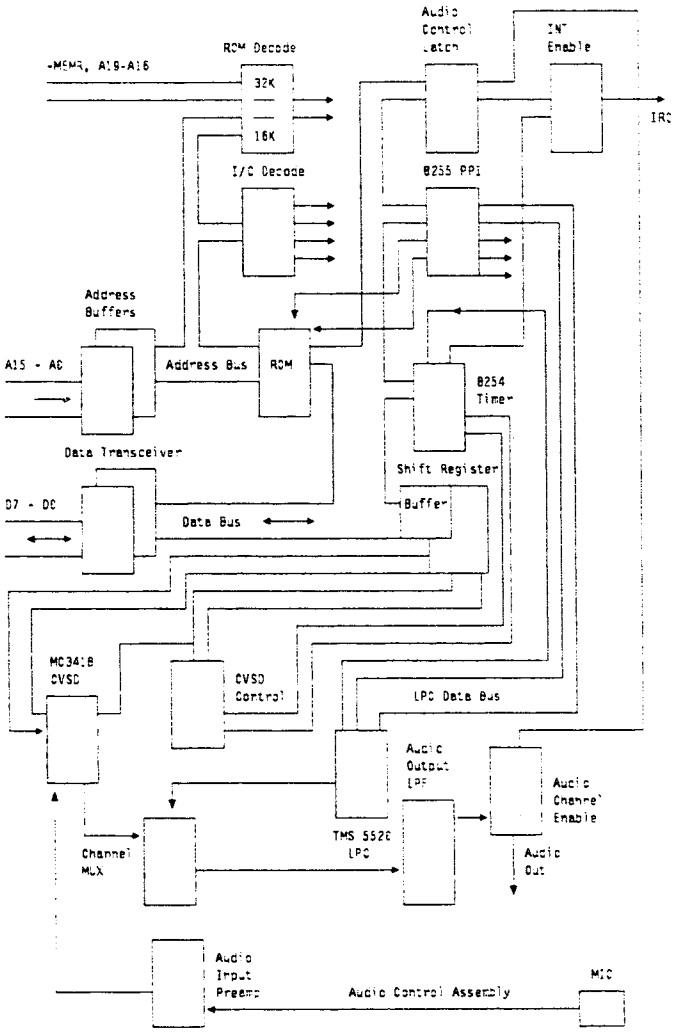

Figure 1. Block Diagram

Vocabulary

The following is a list of the standard vocabulary containing 196 words, phrases, and sound effects.

1 danger	2 time has expired	3 laughing
4 get ready	5 go	6 up
7 down	8 left	9 right
10 warning	11 well done	12 gotcha
13 zero	14 one	15 two
16 three	17 four	18 five
19 six	20 seven	21 eight
22 nine	23 ten	24 a
25 b	26 c	27 d
28 e	29 f	30 g
31 h	32 i	33 j
34 k	35 l	36 m
37 n	38 o	39 p
40 q	41 r	42 s
43 t	44 u	45 v
46 w	47 x	48 y
49 z	50 an	51 again
52 alt	53 add	54 am
55 are	56 a.m.	57 ahead
58 answer	59 back	60 by
61 brake	62 at	63 as
64 and	65 code	66 computer
67 cent	68 control	69 date
70 disk	71 day	72 dollar
73 down	74 do	75 excellent
76 eleven	77 -ez	78 -ed (past tense)
79 echo	80 equals	
81 enter	82 end	83 first
84 from	85 false	86 file
87 fif-	88 function	89 go
90 green	91 good	92 hundred
93 hold	94 hour	95 home
96 is	97 it	98 key
99 last	100 lose	101 list
102 less	103 left	104 ok
105 or	106 period	107 plus
108 please	109 program	110 press
111 p.m.	112 per	113 point
114 run	115 read	116 red
117 right	118 release	119 start
120 stop	121 -s (plural)	122 save
123 second	124 sorry	125 screen
126 score	127 select	128 -th

Figure 2 (Part 1 of 2). Standard Vocabulary

129 third	130 thir-	131-teen
132 true	133 to	134 -ty
135 this	136 twelve	137 thousand
138 that	139 than	140 then
141 time	142 type	143 thing
144 try	145 turn	146 the
147 twenty	148 word	149 white
150 wait	151 wrong	152 what
153 yes	154 you	155 yellow
156 year	157 your	158 space
159 delete	160 page	161 cursor
162 name	163 letter	164 board
165 any	166 sign	167 spell
168 win	169 pause	170 bar
171 insert	172 look	173 lock
174 3 frames of silence	175 minus	176 million
177 month	178 minute	179 move
180 no	181 negative	182 number
183 not	184 alternate	185 up
186 -ing	187 chime	188 bat hitting ball
189 ball being caught	190 gunshot	191 laser
192 phaser	193 buzz	194 tic
195 toc	196 fast chime	

Figure 2 (Part 2 of 2). Standard Vocabulary

I/O Address Registers

The Speech Attachment uses the following registers:

Device	Address	Register
8255 PPI	FB98	Port A
	FB99	Port B
	FB9A	Port C
	FB9B	Mode
8254 Timer	FB9C	Channel 0
	FB9D	Channel 1
	FB9E	Channel 2
	FB9F	Control Word
Shift Register	FF98	Shift
Audio Control Latch	FF9F	Audio Control Latch

Figure 3. I/O Address Map

Programmable Peripheral Interface

The Speech Attachment uses an 8255 programmable peripheral interface (PPI) for control and status. The mode is set to hex 83 to read LPC status. For all other operations, the mode should be hex 81. The 8255 modes are defined as follows:

Mode	Function	Port Description
81	Normal Open	A=Output B=Output C0-C3=Input C4-C7=Output
83	LPC Status	A=Output B=Input C0-C3=Input C4-C7=Output

Note: All output signals of the 8255 are reset when the mode is changed.

Figure 4. Modes

The following figures show the bit definition for ports A, B, and C of the PPI.

Port A

Bit	Write Function
7	LPC in progress
6	Reserved
5	Reserved
4	Reserved
3, 2	ROM Page
1, 0	Channel MUX

Figure 5. Port A Register

Bit 7 When set to 1, this bit indicates that LPC is currently running in the background.

Bits 6-4 Reserved.

Bits 3-2 Setting the ROM page should be done after a Mode change. These bits select the different pages within ROM as shown in the following figure:

Bits 3-2	ROM Page Selected
0 0	Page 0 (default)
0 1	Page 1
1 0	Page 2
1 1	Page 3

Bits 1-0 These bits select the audio channel source as shown in the following figure:

Bits 1-0	Channel MUX Selected
0 0	LPC
0 1	CVSD
1 0	Reserved (Audio Test)
1 1	Reserved

Port B

Port B is used as the LPC data bus. Its direction (input or output) is changed by issuing Mode commands to the Mode register.

Bit	Read Function	Write Function
7	Talk Status	LPC Data Bus
6	Buffer Low	LPC Data Bus
5	Buffer Empty	LPC Data Bus
4	—	LPC Data Bus
3	—	LPC Data Bus
2	—	LPC Data Bus
1	—	LPC Data Bus
0	—	LPC Data Bus

Figure 6. Port B Register

Bits 7-0 Bits 7 through 0 are used to send commands and data to the LPC chip. LPC status is returned in bits 7 through 5.

Port C

Port C is used as a control port for CVSD timing and LPC timing.

Bit	Read Function	Write Function
7	—	Reserved
6	—	CVSD E/D
5	—	LPC WS
4	—	LPC RS
3	-CVSD Clock	—
2	-CVSD Frame	—
1	-LPC INT	—
0	-LPC RDY	—

Figure 7. Port C Register

Bit 7 Reserved.

Bit 6 When cleared to 0, this bit selects CVSD decode (playback); when set to 1, this bit selects CVSD encode (record).

Bit 5 When set to 1, the 'LPC write' signal is active.

Bit 4 When set to 1, the 'LPC read' signal is active.

Bit 3 This bit is the inverted form of the clock signal used by CVSD read to clock serial data into and out of the Shift register from channel 0.

Bit 2 This bit indicates the state of the CVSD frame signal.

Bit 1 When cleared to 0, this bit indicates an interrupt.

Bit 0 When set to 1, this bit indicates a busy state. When cleared to 0, this bit indicates a completed state.

Timer

The Speech Attachment uses an 8254 timer to create the various clock signals. CVSD circuits use channels 0 and 1. Channel 2 generates the interrupt pulses used during LPC. Channel 2 can also be gated onto the audio channel for audio channel test purposes.

All clock signals are derived from the system clock.

The following are bit definitions for the Control Word register:

Bit	Function
7	Counter Select
6	Counter Select
5	Read/Write
4	Read/Write
3	Mode
2	Mode
1	Mode
0	Counter Mode

Figure 8. Control Word Register

Channel 0 (CVSD CLOCK)

The speech attachment initializes channel 0 in the square wave mode and holds the channel 0 gate active.

Channel 0 has the following functions:

- Divides the system clock to provide the CVSD bit-sample rate. The positive edge of this signal is used by the CVSD modulator to latch the digital serial data. The Shift register uses the positive edge of the inverted CVSD clock signal to clock the serial data.
- Provides the inverted channel 0 output used by channel 1 to generate the 'CVSD frame' signal.

Channel 1 (CVSD Frame)

The BIOS initializes the channel 1 divisor to 8. It also initializes channel 1 in the rate generator mode and holds the channel 1 gate active.

This channel divides the inverted CVSD clock by 8. It counts the CVSD clock periods and drives CVSD frame inactive for one period every eight clocks. BIOS uses the positive edge of this signal to write data to the Shift register during CVSD decoding. BIOS polls this channel for synchronization signals during both CVSD encoding and decoding.

Channel 2 (Clock)

Channel 2 has two functions: LPC interrupt and Audio Test.

These functions:

- Generate the interrupt pulse during LPC operations.
- Can be routed to the audio channel to test the channel output.

When the interrupt is enabled, Channel 2 generates the interrupt pulse during LPC operation. When the interrupt is disabled and the channel enabled, the Channel 2 output is active. The output can then be multiplexed onto the audio channel by selecting the source as audio test in Port A.

These functions are selected by the state of the interrupt enable bit in the Audio Control Latch.

Audio Test Mode: The channel 2 output can be multiplexed onto the audio channel. When the channel is enabled, the channel 2 gate is held active.

Shift Register

The Speech Attachment uses the Shift register to serialize and deserialize CVSD data. The Shift register is a tri-state device capable of both serial-to-parallel and parallel-to-serial conversions.

Audio Control Latch (ACL)

Audio control gating and local interrupt control is provided by the Audio Control Latch.

Bit	Function
7-2	Reserved
1	Interrupt Enable
0	Channel Enable

Figure 9. ACL Bit Functions

Bits 7-2 Reserved.

Bit 1 When this bit set to 1, the interrupt is enabled. Bit 1 is inverted when read.

Bit 0 When this bit is set to 1, the channel is enabled.

Programs that use the Speech Attachment are responsible for sharing the audio channel. Before using the audio channel, the BIOS:

1. Disables each of the possible 32 audio channels. See Figure 10 on page 12 for a listing of control latch addresses.
2. Reads the Audio Control Latch to determine if the channel is disabled.
3. Enables the audio channel.

The possible audio channel addresses are shown in the following figure:

Device	ACL	Device	ACL
1	079F	17	879F
2	0F9F	18	8F9F
3	179F	19	979F
4	1F9F	20	9F9F
5	279F	21	A79F
6	2F9F	22	AF9F
7	379F	23	B79F
8	3F9F	24	BF9F
9	479F	25	C79F
10	4F9F	26	CF9F
11	579F	27	D79F
12	5F9F	28	DF9F
13	679F	29	E79F
14	6F9F	30	EF9F
15	779F	31	F79F
16	7F9F	32	FF9F

Figure 10. ACL Address

Programs should read bit 0 of the ACL each time the channel is required. If the channel is not enabled, another device has control, and the program should either post an error, or regain control of the channel.

Audio Multiplexer

Before the attachment begins speech synthesis, BIOS performs the following:

- The audio multiplexer points to the speech source.
- The audio channel is enabled in the ACL.
- The PC*jr*'s Multiplexer points to the I/O channel (PB bits 5 and 6).

Audio Filters

The Speech Attachment has two audio circuits: output and input. The audio output low-pass filter provides a signal compatible with the systems audio channel. The input preamp provides the amplification and filtering needed to attach a low level microphone to the attachment.

Programming Considerations

Linear Predictive Coding (LPC)

The Speech Attachment uses a TMS 5520 for LPC synthesis. This device operates at an 8 kHz sample rate.

There are two possible modes of LPC speech synthesis: interrupt driven (background) and polled (foreground).

Background Mode

The interrupt signal is enabled and is used to generate interrupts.

This mode returns control to the calling program while speech synthesis is in progress with the following restrictions:

- The system cannot perform diskette or other operations that disable hardware interrupts during speech synthesis.
- The system must not change environments when in the background mode; for example, changing DOS to BASIC.

Foreground Mode

In this mode, the interrupt signal is disabled, and control is not returned to the system until after the speech synthesis is completed.

Note: The BIOS continuously polls the system during speech synthesis and updates when necessary.

Continuously Variable Slope Delta (CVSD) Modulation

The attachment uses a Motorola MC3418 CVSD Modulator for CVSD recording and playback. This device, along with two low-pass filters, a Shift register, and appropriate clock signals provides for encode and decode functions.

Decode (Playback) Mode

The following is a typical programming procedure:

- Set CVSD E/ in Port C to 0 (decode).
- Set the audio channel source to CVSD.
- For all bytes:
  - Wait for positive edge of CVSD Frame
  - Output data byte to the Shift register
  - Do any "housekeeping" needed.
- End do.

Encode (Record) Mode

The following is a typical programming procedure:

- Set CVSD E/D high (encode).
- For all bytes:
  - Wait for the negative edge of CVSD FRAME
  - Input data byte from the Shift register
  - Do any "housekeeping" needed.
- End Do.

BIOS

The attachment uses a 32K by 8-bit ROM module that contains the standard vocabulary and BIOS support. This module appears as normal system memory at hex CE000 through CFFFF.

BIOS Interface

Interrupt 4DH

Software interrupt hex 04D provides low-level BIOS support for CVSD and LPC. The following shows the interrupt interface. All registers except AX are preserved.

For all functions of interrupt 04D, the following is returned:

```
ON RETURN:
      (AL) = STATUS
            0 - Everything O.K.
            1 - Undefined command
            2 - LPC speak in progress
            3 - ACL error (stuck)
            4 - LPC index out of range
            5 - CVSD speed out of range
            6 - Time out waiting for LPC ready
```

(AH) = 00H Reset Card

(AH) = 01H CVSD (Continuously Variable Slope Delta)

(AL) = 00H - CVSD Record (Using Speed Table)

```
      (DS:SI)  - Segment:offset
         (BL)  - Table speed
               0 = 1800 bytes/sec
               1 = 2400 bytes/sec
               2 = 3000 bytes/sec
               3 = 3600 bytes/sec
               4 = 4200 bytes/sec
               5 = 4800 bytes/sec
         (CX)  - Byte count
```

(AL) = 01H - CVSD Playback (Using Speed Table)

(DS:SI) - Segment:offset
(BL) - Table speed
0 = 1800 bytes/sec
1 = 2400 bytes/sec
2 = 3000 bytes/sec
3 = 3600 bytes/sec
4 = 4200 bytes/sec
5 = 4800 bytes/sec
(CX) - Byte count

(AL) = 02H - CVSD Record (Using User Speed)

(DS:SI) - Segment:offset
(BX) - User speed divisor
(CX) - Byte count

(AL) = 03H - CVSD Playback (Using User Speed)

(DS:SI) - Segment:offset
(BX) - User speed divisor
(CX) - Byte count

(AH) = 02H LPC (Background)

Interrupt driven LPC

(AL) = 00H - LPC Status

(AL) = 01H - LPC Speak - Index

(BX) - Word number from index
(BX = 01 or greater)

(AL) = 02H - LPC Speak - Buffer

(DS:SI) - Start of buffer (seg:offset)
(CX) - Number of bytes in the LPC word to be spoken. (CX) must be 4096 or less.

(AH) = 03H - LPC (Foreground)

Polled LPC

(AL) = 00H - LPC Status

(AL) = 01H - LPC Speak - Index

```
(BX)  - Word number from index
      (BX = 01 or greater)
```

(AL) = 02H - LPC Speak - Buffer

```
(DS:SI)  - Start of bfr (seg:offset)
  (CX)   - Number of bytes in the LPC
           word to be spoken.  (CX) must be
           4096 or less.
```

Specifications

The following are specifications of the attachment:

Size

- Length: 239 mm (9.4 in.)
- Height: 99 mm (3.9 in.)

Power

- +5Vdc with 453 mA maximum current
- +12Vdc with 60 mA maximum current
- −12Vdc with 20 mA maximum current

Microphone Input

- 1/8 inch phone jack
- 500 ohm nominal impedance

Headphone

- 1/4 inch phone jack
- 16 ohm impedance.