

# SERVICE MODULE

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# Power Supply

**Z-100 PC Series Computers**

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## Record of Service Bulletins

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# Abbreviations

CSA	Canadian Standards Association
FCC	Federal Communications Commission
KHz	Kilohertz
ms	millisecond
mV	millivolt
PSG	Power Supply Good
TTL	Transistor-Transistor Logic
UL	Underwriters Laboratories
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VDE	German Engineers Association



# Introduction and Specifications

## Introduction

**WARNING:** Do not attempt to service the power supply. Serious or fatal injury may result.

This module provides information on the power supply. The power supply as a unit is **NOT SERVICEABLE**. The power supply contains proprietary information. Therefore, there is no disassembly, parts list, reassembly, or schematic included with this module. The specifications for the power supply are listed below.

## Specifications

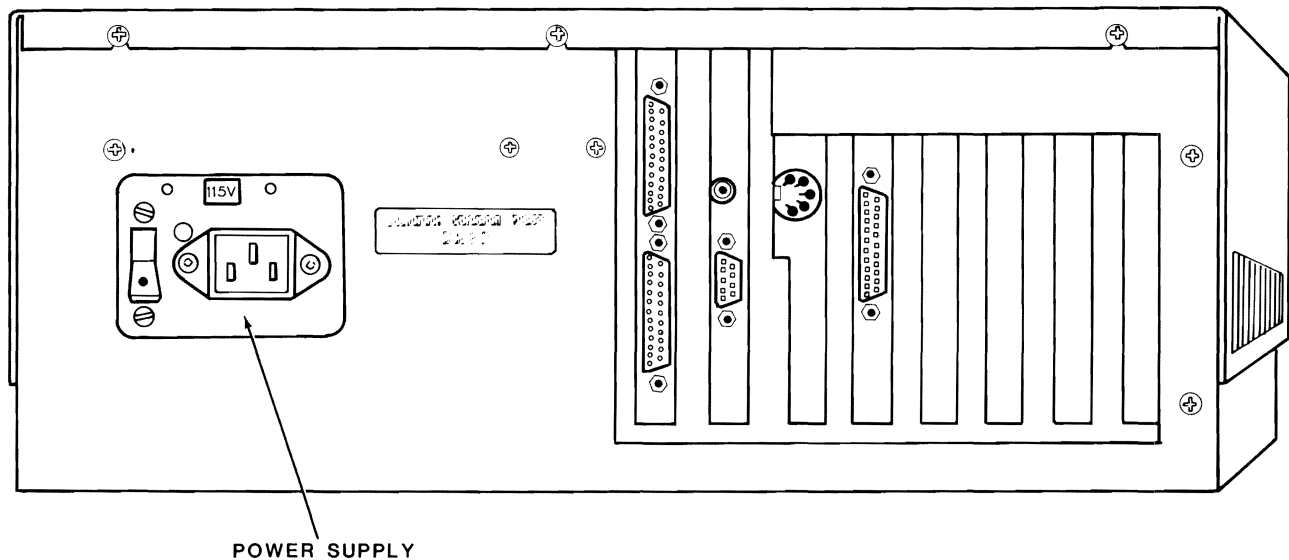
<b>Part Number:</b>	HE 234-434.
<b>AC Input:</b>	100-130 VAC, 60 Hz. 200-260 VAC, 50 Hz. Switch selectable.
<b>DC Outputs:</b>	+ 5 V ( $\pm 3\%$ ), + 12 V (+ 5, - 4%), - 12 V (+ 5, - 4%).
<b>Temperature Range:</b>	10 to 32°C. 47 to 89°F.

## Chapter 2

# Configuration

Refer to Figure 2.1 while reading the following.

The voltage switch at the rear of the computer is located through the small window on the power supply that is covered with plastic. The voltage switch is normally set for 115 VAC. If this computer is to be operated on 240 VAC line voltage, use a small-bladed screwdriver and break the plastic window over the 115 VAC position of the switch. Then slide the switch so that 240 VAC is visible on the switch. Connect the appropriate line cord.



**Figure 2.1. Power Supply Rear View**

# Theory of Operation

## Introduction

Refer to Figure 3.1 while reading the following.

The power supply provides regulated voltages used by the various components within the Z-100 PC Series Computers. The power supply is located toward the rear and to the right of the chassis, and uses a quasi square wave switching regulator to produce three regulated output voltages. This unit complies with FCC, VDE, CSA, and UL regulations.

## Outputs

All outputs from the precision-regulated power supply are electrically isolated from the main voltage and share a common ground, which is the chassis of the power supply.

The voltages output to disk drive connectors P1 and P2 have special requirements for output ripple frequency components in the frequency range of 60 to 120 KHz. To obtain these low levels, a low pass filter is added to the regular output leads of P1 and P2. The output ripple is measured with an oscilloscope with a bandwidth of 3 KHz. Component frequency of the output ripple of the 5-volt or 12-volt outputs should **NOT** exceed 2 mV peak between the frequencies of 60 KHz to 120 KHz. Connector P3 supplies the output voltages to the backplane board.

Theory of Operation

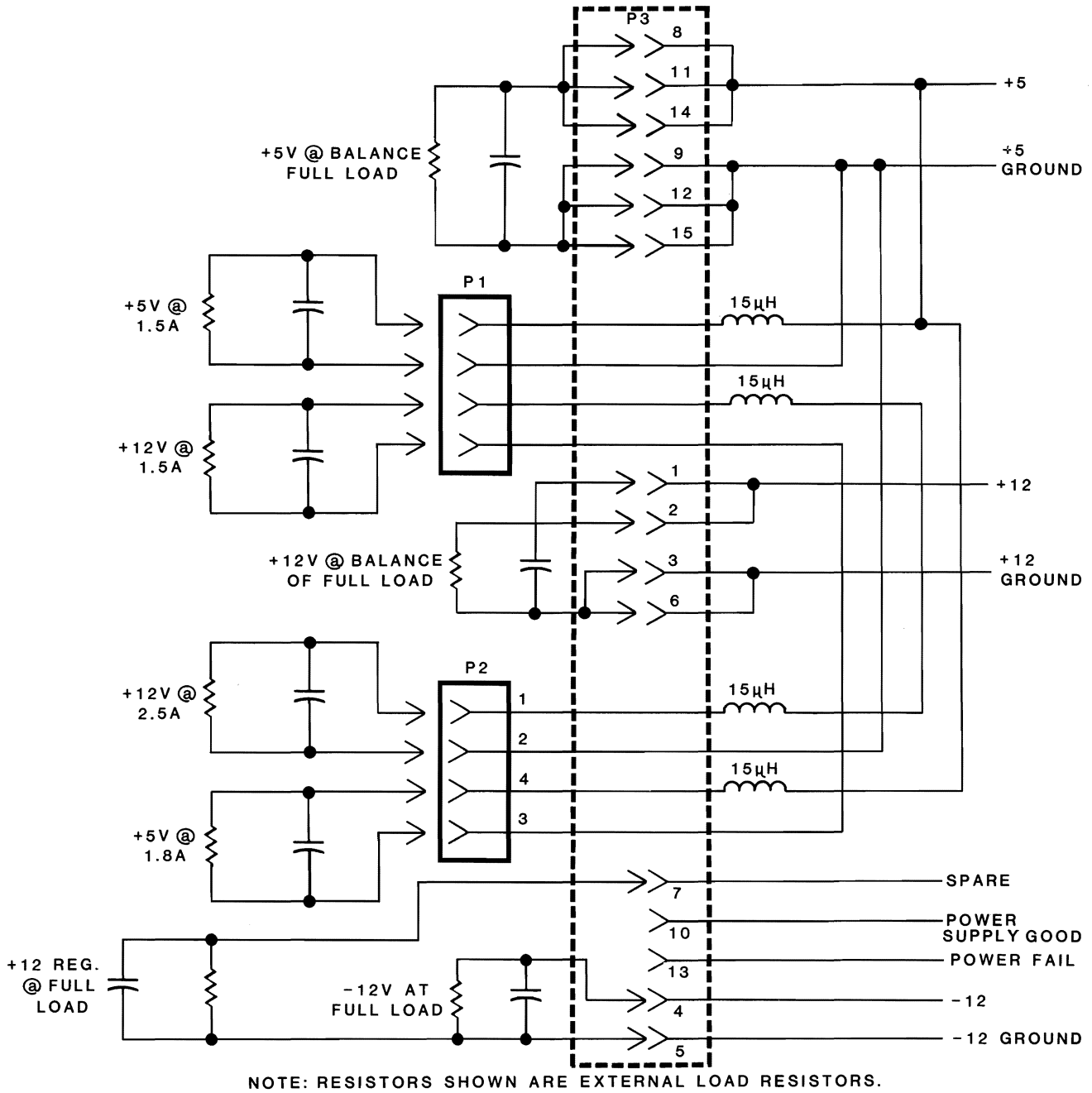


Figure 3.1. Power Supply Output

## **Power Supply Good (PSG) Signal**

The PSG logic signal is an open collector TTL-compatible output which is used by external circuits to determine if the output voltages are valid and within specification. Upon power up, PSG shall remain high until all the DC output voltages stay within specification for a minimum of 70 to 130 ms, after which time PSG will go low. If any voltage is not within this normal limit plus 1% of nominal voltage (refer to Specifications), PSG will go high. PSG will not return to a low condition until outputs have met the same conditions as those required at initial power application.

## **Operation at No Load**

The power supply is capable of operating under the adverse condition of no load without damage. If the power supply shuts down, it will require a manual reset by turning the power supply off, waiting 5 seconds, and then turning it back on. The output voltage may seek a value between ground and 50% over nominal. Output voltages will not exceed the peak rating of the output circuit components.

# Troubleshooting

Refer to Figure 4.1 while reading the following.

Measure the power supply outputs with the disk drive connectors disconnected, and connector P3 connected to the backplane board. Measure the voltages at the test points on the backplane board, and refer to Figure 4.1 for the power supply voltages.

Measure the ripple voltage with an oscilloscope. If the power supply voltages are normal, measure the voltage with the disk drives connected. This will indicate if the circuit cards or disk drives are loading down the power supply.

**WARNING:** The load resistors listed below generate heat. Use caution to avoid burns.

**NOTE:** Voltages may not be within tolerance. The correct loads for the output voltages are: + 5 V at 4 Amps (1.25-ohm resistor rated at 20 watts or greater), + 12 V at 1 Amp (12-ohm resistor rated at 12 watts or greater), and - 12 V at 250 mA (50-ohm resistor rated at 3.5 watts or greater).

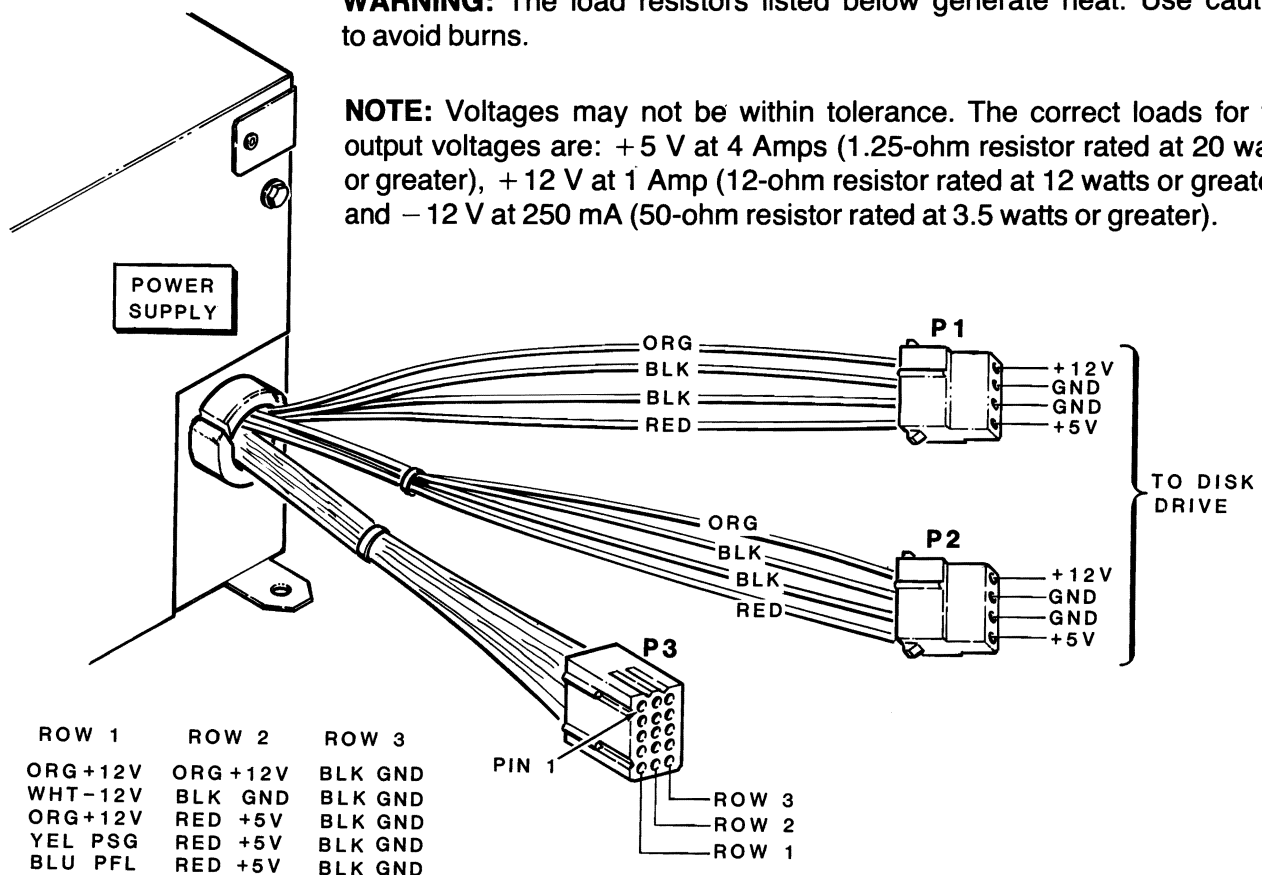


Figure 4.1. Power Supply Connectors

# SERVICE MODULE

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# Backplane Board

**Z-100 PC Series Computers**

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# Abbreviations

CLK	Clock
CPU	Central Processing Unit
DC	Direct Current
DMA	Direct Memory Access
GND	Ground
I/O	Input/Output
LED	Light-Emitting Diode
mA	Milliamperes
MHz	Megahertz
NMI	Non-Masked Interrupt
ns	nanosecond
PSG	Power Supply Good
ROM	Read-Only Memory
VDC	Volts Direct Current

# Introduction and Specifications

## Introduction

The backplane board in the Z-100 PC Series Computer contains five supply voltage diagnostic LEDs, a  $-5$  VDC regulator, and the eight IBM®-compatible bus connectors, P101 through P108, into which the remainder of the computer's cards are inserted for intersystem communication. A power supply interface connector, P110, and a  $+12$  VDC connector, P109, also are contained on this board. P109 supplies  $+12$  VDC to an internal video monitor on some models.

## Diagnostics

The LEDs on the backplane board aid the user in determining whether or not a fault lies in the DC power generation circuits. The five LEDs on this board indicate the overall integrity of the power supply, and the presence or absence of the four individual operating supply voltages:  $+12$  VDC,  $-12$  VDC,  $+5$  VDC, and  $-5$  VDC.

## — 5 Volt Regulator

The only supply voltage actually generated on this board is the  $-5$  VDC. The specifications for this supply are as follows:

- **Input:**  $-7.3$  to  $-25$  VDC, filtered by  $2.2 \mu\text{F}$ .
- **Output:**  $-4.8$  to  $-5.2$  VDC, at  $100$  mA, filtered by  $47 \mu\text{F}$ .
- **Load:**  $1$  mA to  $100$  mA, short-circuit protected.
- **Ambient Temperature:**  $0$  to  $+70^\circ\text{C}$ .  
 $32$  to  $158^\circ\text{F}$ .

## Introduction and Specifications

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### Signal Bus

The eight-connector array on this board is basically an input/output (I/O) extension of the microprocessor bus. The bus interface is implemented via a 62-pin edge connector on the card or device which plugs into one of the eight backplane sockets. The bus supplies the following:

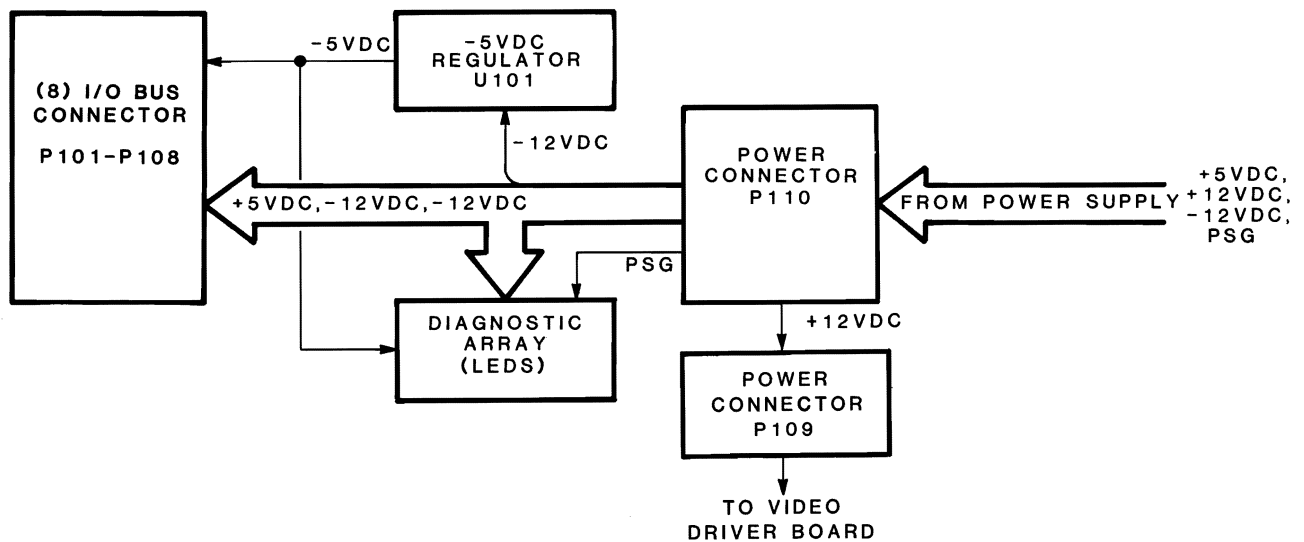
- Eight bits of bidirectional data;
- Twenty address lines to access up to 1 megabyte of memory. The maximum user memory is 640K of 64K devices, or 768K using 256K devices;
- Six levels of interrupt;
- Control lines for memory and I/O read and write;
- Clock and timing control lines;
- A channel check line for device error reporting or parity error reporting by existing and add-on memory. A non-masked interrupt (NMI) is supplied to the central processing unit (CPU) when this line is active;
- Operating power consisting of + and - 5 VDC, + and - 12 VDC, and ground;
- An I/O CH RDY line for use by slow acting peripherals;
- Capability of addressing up to 64K I/O ports;

A complete listing of the signal names and their functions is presented in the "Detailed Circuit Description," Chapter 3.

## Chapter 2

# Theory of Operation

Refer to Figure 2.1, the backplane board block diagram, for the following description.



**Figure 2.1. Backplane Board Block Diagram**

## Power Connector

P110 from the power supply delivers the operating supply voltages for the cards which plug into the backplane board connectors, and for the diagnostic LED array contained on the backplane board. System ground, +5 VDC, +12 VDC, and -12 VDC are routed to the backplane board by this connector. To increase the current carrying capability on the heavier loaded supply busses and the ground return, more than one pin on the connector is used for the same supply bus. Ground and +5 VDC are contained in the middle layer of the printed circuit board.

P109 supplies +12 VDC to the video driver board.

## Theory of Operation

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### **– 5 Volt Regulator**

The –5 volt supply is derived from –12 VDC from the power supply, which is applied to a solid-state voltage regulator, U101. The –5 VDC is then applied to the parallel bus connectors, and to its respective diagnostic LED circuit.

### **Diagnostic LEDs**

Five green light-emitting diodes (LEDs) are incorporated to indicate the power supply is good, and the presence or absence of +5 VDC, –5 VDC, +12 VDC, and –12 VDC. Suitable current-limiting resistors are connected inline with the LEDs to provide the appropriate operating voltage and current to the devices. The LEDs are on (lit) when the parameter associated with a device is at or near its stated value, and off when the associated parameter is deficient.

### **Backplane I/O Connectors**

Eight 62-pin edge-type socket connectors are provided by the backplane board to interconnect the CPU card, the memory card, the video card, and the disk controller card with the appropriate edge connector, as well as any other cards which may be added for system enhancement or expansion. The optional connectors are identical and are wired in parallel so that, functionally, any card may be inserted at any connector location.

# Detailed Circuit Description

Refer to the backplane board schematic for the following circuit description.

## Power Distribution

P110, the backplane power connector, connects +5 VDC, +12 VDC, –12 VDC, the power supply good (PSG) signal, and ground to the backplane board. Ground is connected to pins 3, 5, 6, 9, 12, and 15. +5 VDC comes in on pins 8, 11, and 14. –12 VDC appears on pin 4. +12 VDC is applied to pins 1 and 2. The PSG signal is on pin 10. Pins 7 and 13 are not used.

+5 VDC, +12 VDC, and –12 VDC are fed through to B3, B9, and B7, respectively, on the parallel signal bus connectors, P101 through P108, and also are applied to their respective LEDs. –12 VDC also is fed to the input, pin I of U101, the –5 VDC regulator. Ground (GND) is routed to the signal bus, pins B1, B10, and B31. The PSG signal is connected to the cathode of D104, the PSG LED.

## –5 VDC Regulation

U101, the –5 volt regulator, accepts the –12 VDC on its input, drops and regulates it, and sends the –5 VDC output, pin O, to bus pin B5, and to R101, the dropping resistor for the –5 volt LED. The G pin of U101 connects to system ground to serve as a return path for the regulator circuit. C119 and C117 filter and decouple the –12 VDC input. C118 filters the –5 VDC output to reduce the ripple to an acceptable level.



## Detailed Circuit Description

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### Diagnostic Circuitry

The diagnostic LEDs, D101 through D105, indicate the integrity of the four DC voltages and the PSG signal. R101 through R105 act as voltage-dropping and current-limiting resistors to obtain the 2.5 volts, 20 mA required for safe illumination of the LEDs. R101 and R102 connect to the cathodes of D101 and D102, while the anodes are returned to ground, the proper configuration for sensing of negative-polarity voltages. R103 and R105 connect to D103 and D105 anodes, and the cathodes return to ground, to properly sense the +5 and +12 VDC signals.

+5 VDC is connected to R104, which is, in turn, series-connected to the anode of D104, the PSG LED. Upon power up, a few hundred milliseconds are allowed to stabilize the power supply outputs. Up until this point, pin 10 of P110, which is also the cathode of D104, is at approximately +5 VDC, keeping the LED extinguished. If at the end of the delay time all the supply voltages are normal, sensing circuitry in the power supply pulls pin 10 nearly to ground potential, lighting D104 to indicate proper power supply operation.

### Signal Bus

The signal bus consists of eight identical 62-pin edge connector sockets, P101 through P108. The connectors are arranged with 31 pins labeled A1 through A31 on one side, and 31 pins labeled B1 through B31 on the other. There is a one-to-one electrical correspondence between identical pin numbers on each connector.

Capacitors C101, C103, C105, C107, C110, C112, C114, and C116 are connected between +5 VDC and ground as filtering. They are physically located between every other pair of backplane signal connectors at the top and bottom of the board.

Table 3.1 defines the signals which appear on the backplane signal bus connectors.

## Detailed Circuit Description

**Table 3.1. I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
A1	I/O CHCK*	I/O channel check. Provides the CPU with parity error status for memory or other I/O devices. Active-low indicates error.
A2	D7	Data bit 7
A3	D6	Data bit 6
A4	D5	Data bit 5
A5	D4	Data bit 4
A6	D3	Data bit 3
A7	D2	Data bit 2
A8	D1	Data bit 1
A9	D0	Data bit 0
A10	I/O CHRDY	I/O channel ready. Used by slower peripherals to ensure data is not lost during read and write operations. May be held low (not ready) up to 10 CLK cycles (2.1 $\mu$ s).
A11	AEN	Address enable. Assigns control of read and write operations to the DMA controller.
A12	A19	Address bit 19
A13	A18	Address bit 18
A14	A17	Address bit 17
A15	A16	Address bit 16
A16	A15	Address bit 15
A17	A14	Address bit 14
A18	A13	Address bit 13

Continued . . .

## Detailed Circuit Description

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**Table 3.1 (Continued). I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
A19	A12	Address bit 12
A20	A11	Address bit 11
A21	A10	Address bit 10
A22	A9	Address bit 9
A23	A8	Address bit 8
A24	A7	Address bit 7
A25	A6	Address bit 6
A26	A5	Address bit 5
A27	A4	Address bit 4
A28	A3	Address bit 3
A29	A2	Address bit 2
A30	A1	Address bit 1
A31	A0	Address bit 0
B1	GND	Ground
B2	RESET	When high, resets, or initializes system logic devices.
B3	+5 VDC	+5 VDC bus
B4	IRQ2	Interrupt request 2. Not used, but available for assignment to a user-selected device.
B5	-5 VDC	-5 VDC bus
B6	DRQ2	DMA request 2. Assigned to floppy disk controller.

Continued . . .

## Detailed Circuit Description

**Table 3.1 (Continued). I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
B7	- 12 VDC	- 12 VDC bus
B8	N.C.	No connection
B9	+ 12 VDC	+ 12 VDC bus
B10	GND	Ground
B11	MEMW*	Memory write. When low, causes data on data bus to be stored in memory.
B12	MEMR*	Memory read. When low, causes memory to drive data onto the data bus.
B13	IOW*	I/O write. When low, instructs an I/O device to read the data on the data bus.
B14	IOR*	I/O read. When low, instructs an I/O device to drive its data onto the data bus.
B15	DACK3*	DMA acknowledge 3. Assigned to the Winchester drive controller.
B16	DRQ3	DMA request 3. Assigned to the Winchester drive controller.
B17	DACK1*	DMA acknowledge 1. Not used. Available for user assignment.
B18	DRQ1	DMA request 1. Available.
B19	DACK0*	DMA acknowledge 0. Assigned to timer #1. Initiates memory refresh cycle.
B20	CLK	System clock 4.77 MHz.
B21	IRQ7	Interrupt request 7. Assigned to parallel interface.
B22	IRQ6	Interrupt request 6. Assigned to floppy disk controller.

Continued . . .

## Detailed Circuit Description

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**Table 3.1 (Continued). I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
B23	IRQ5	Interrupt request 5. Assigned to Winchester drive controller.
B24	IRQ4	Interrupt request 4. Assigned to serial port #1 (fixed).
B25	IRQ3	Interrupt request 3. Assigned to serial port #2 (configurable).
B26	DACK2*	DMA acknowledge 2. Assigned to floppy disk controller.
B27	T/C	Terminal count. Goes high when terminal count for any DMA channel is reached.
B28	ALE	Address latch enable. Generated by bus controller to indicate valid processor addresses to the I/O channel.
B29	+5 VDC	+ 5 VDC bus.
B30	OSC	Oscillator. A high-speed clock: 14.31818 MHz. Provides the basic timing for the system.
B31	GND	Ground.

# Chapter 4

## Troubleshooting

### General Troubleshooting

If you have encountered problems with the computer and indications point to the backplane board as the source of the difficulty, proceed to isolate the fault in the following manner.

If a spare backplane board is available, attempt to clear the problem by direct substitution of the board. If the difficulty does not reappear, the removed backplane board is at fault.

If a backup backplane board is not available, attempt to isolate the fault by the step-by-step checks which follow. Fault-isolation is divided into two categories: power supply related problems, and signal bus problems.

### DC Voltages and Diagnostics

If one or more of the backplane LEDs is extinguished, it may indicate a power supply or  $-5$  volt regulator problem, or that the LED itself is defective.

If you suspect that one or more of the DC voltages is absent or deficient, use a voltmeter and make the following checks. The computer must be on, and the meter set to a suitable range for the voltage being measured.

### DC Voltage Checks

Turn the computer on and perform the following:

1. Connect the common lead of the voltmeter to ground by connecting it to one of the ground pins on P110: pin 3, 6, 5, 9, 12, or 15.

## Troubleshooting

---

2. Set the polarity of the meter to positive and probe pin 1 of P110. Meter should read +12 VDC (+5%, -4%).
3. Probe pin 10 of P110. Voltage should be +5 VDC ( $\pm 3\%$ ).
4. Set the polarity of the meter to negative and probe pin 4 of P110. Voltage should be -12 VDC (+5%, -4%).

If any of the voltages are missing or low, the power supply is suspect. Refer to the troubleshooting section of the power supply module.

If a voltage is present, but its LED is not lit, perform the following steps:

1. Turn off the computer, and set the meter to read ohms. Check the value of the resistor associated with the LED that was out. R102 and R103 should read approximately 1500 ohms, and R105 should read 560 ohms.
2. If the resistor checks good, replace the LED in question.

If the previous checks do not indicate a problem, perform the following checks:

1. Set the voltmeter to read negative polarity, and turn the computer back on.
2. Probe pin O (output) of U101. Meter should read approximately -5 VDC ( $\pm 5\%$ ). If it does not, replace U101. If replacing U101 does not restore -5 VDC, check the other components associated with U101: C117, C118, and C119.
3. If -5 VDC is present but D101 is not lit, perform LED checks as outlined previously.

Check the PSG signal. If the power supply is functioning properly, there should be approximately zero volts on pin 10 of P110, and D104 should be lit. If zero volts is indicated but PSG LED is not lit, turn off the computer and check the resistance of R104 with an ohmmeter. It should read 560 ohms. If the resistor checks good, replace D104.

If the power supply checked good and one or more of the voltages is now deficient, the supply is, more than likely, being loaded down by one of the cards. Remove the cards one at a time until the deficient voltage returns to normal, then refer to the troubleshooting section for that card.

## **Backplane Connector Fault Isolation**

If you have reason to suspect a defective backplane signal bus connector of causing a problem, perform the following:

1. Turn off the computer, and swap cards in the suspect location; e.g., remove the video card and replace it with the CPU card.
2. Turn the computer back on and perform several operations to determine if the problem still is present, or has changed in nature.

If the same problem still is present, it is probable that the cause is on a card whose function is related to the nature of the problem. Consult the troubleshooting section for the affected card.

If the nature of the difficulty has changed, try to relate the symptoms to the particular cards used in a given location to pinpoint the defective backplane connector.

Once the suspect location has been determined, turn off the computer and visually inspect the edge connector in that location for physical damage, poor solder connections, corroded contacts, etc. If no discrepancy is noted, connector replacement is indicated.



# Chapter 5

## Parts List

### Introduction

Contained in this chapter are a component view of the backplane boards, part numbers HE 181-4656 and HE 181-4936, and the related parts list. Refer to Figure 5.1 for location of parts and components.

This chapter also includes a Semiconductor Identification Index for additional information on the semiconductor devices.

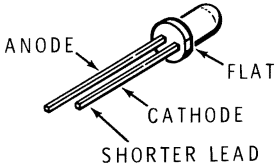
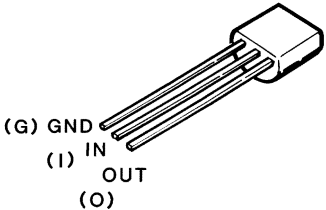
### Component Parts List

<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>	<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
<b>Capacitors</b>			<b>Integrated Circuits</b>		
C101	HE 25-928	33 $\mu$ F electrolytic	U101	HE 442-665	Regulator, voltage, - 5 V
C102	Not Used		<b>Interfaces</b>		
C103	HE 25-928	33 $\mu$ F electrolytic	P101	HE 432-1351	Connector, edge, 62-pin
C104	Not Used		P102	HE 432-1351	Connector, edge, 62-pin
C105	HE 25-928	33 $\mu$ F electrolytic	P103	HE 432-1351	Connector, edge, 62-pin
C106	Not Used		P104	HE 432-1351	Connector, edge, 62-pin
C107	HE 25-928	33 $\mu$ F electrolytic	P105	HE 432-1351	Connector, edge, 62-pin
C108	Not Used		P106	HE 432-1351	Connector, edge, 62-pin
C109	Not Used		P107	HE 432-1351	Connector, edge, 62-pin
C110	HE 25-928	33 $\mu$ F electrolytic	P108	HE 432-1351	Connector, edge, 62-pin
C111	Not Used		P109	HE 432-943	Connector, 2-pin
C112	HE 25-928	33 $\mu$ F electrolytic	P110	HE 432-1376	Connector, power, 15-pin
C113	Not Used		<b>Resistors</b>		
C114	HE 25-928	33 $\mu$ F electrolytic	R101	HE 6-561-12	560 $\Omega$ , film
C115	Not Used		R102	HE 6-152-12	1500 $\Omega$ , film
C116	HE 25-928	33 $\mu$ F electrolytic	R103	HE 6-152-12	1500 $\Omega$ , film
C117	HE 21-769	.01 $\mu$ F ceramic	R104	HE 6-561-12	560 $\Omega$ , film
C118	HE 25-883	47 $\mu$ F electrolytic	R105	HE 6-561-12	560 $\Omega$ , film
C119	HE 25-924	2.2 $\mu$ F electrolytic			
<b>Diodes</b>					
D101	HE 412-642	LED, 2.5 V, 20 mA			
D102	HE 412-642	LED, 2.5 V, 20 mA			
D103	HE 412-642	LED, 2.5 V, 20 mA			
D104	HE 412-642	LED, 2.5 V, 20 mA			
D105	HE 412-642	LED, 2.5 V, 20 mA			

## Parts List

## Semiconductor Identification Index

This section will aid you in identifying the semiconductor devices installed on the backplane board by cross referencing, where applicable, the Zenith/Heath part numbers with generic device numbers. The components are listed in numerical order, along with any applicable device number and device lead configuration.

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
412-642	SG205D	D101-D105 Green LED 2.5 V, 20 mA	
442-665	79L05	U101 Voltage regulator -5 VDC	

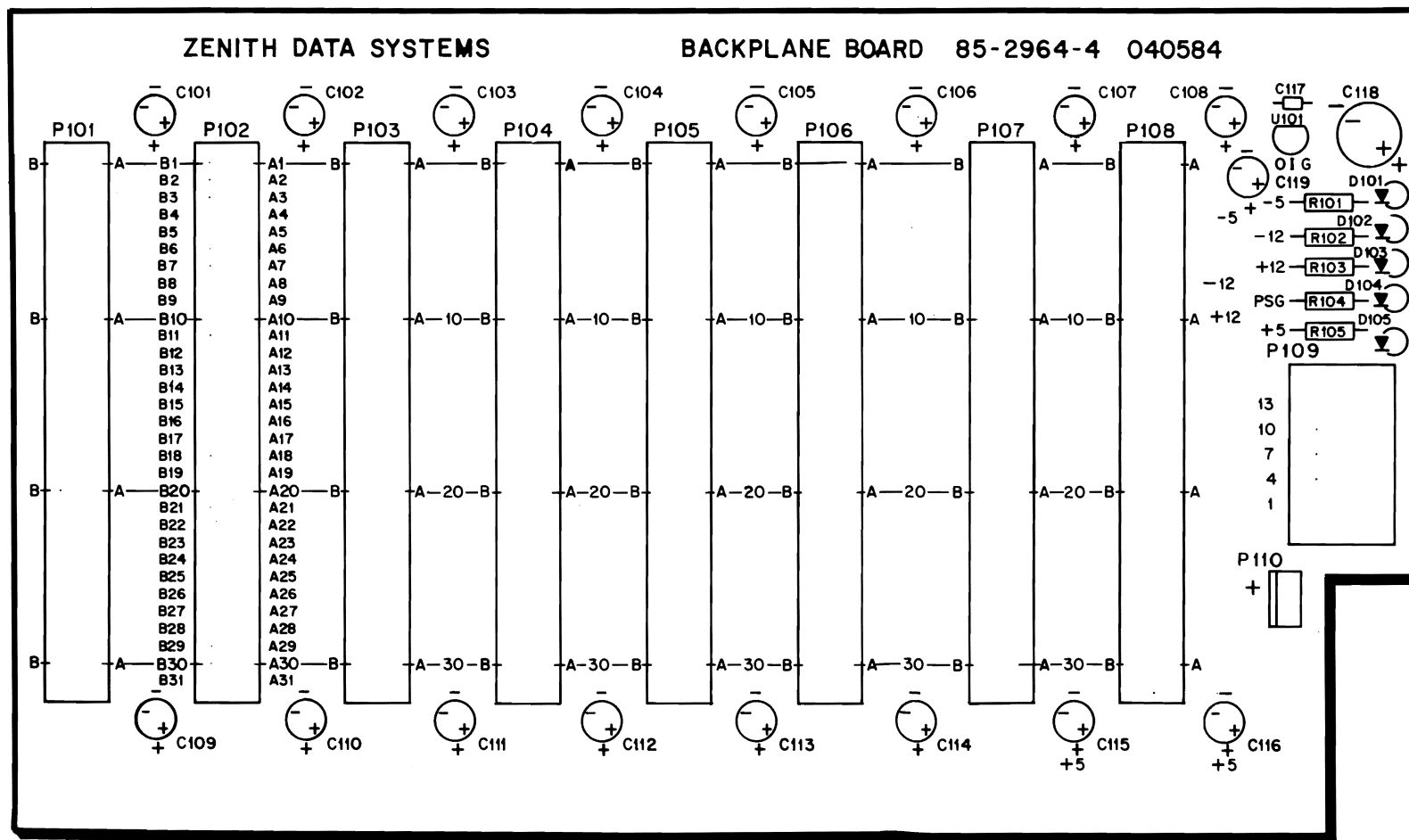
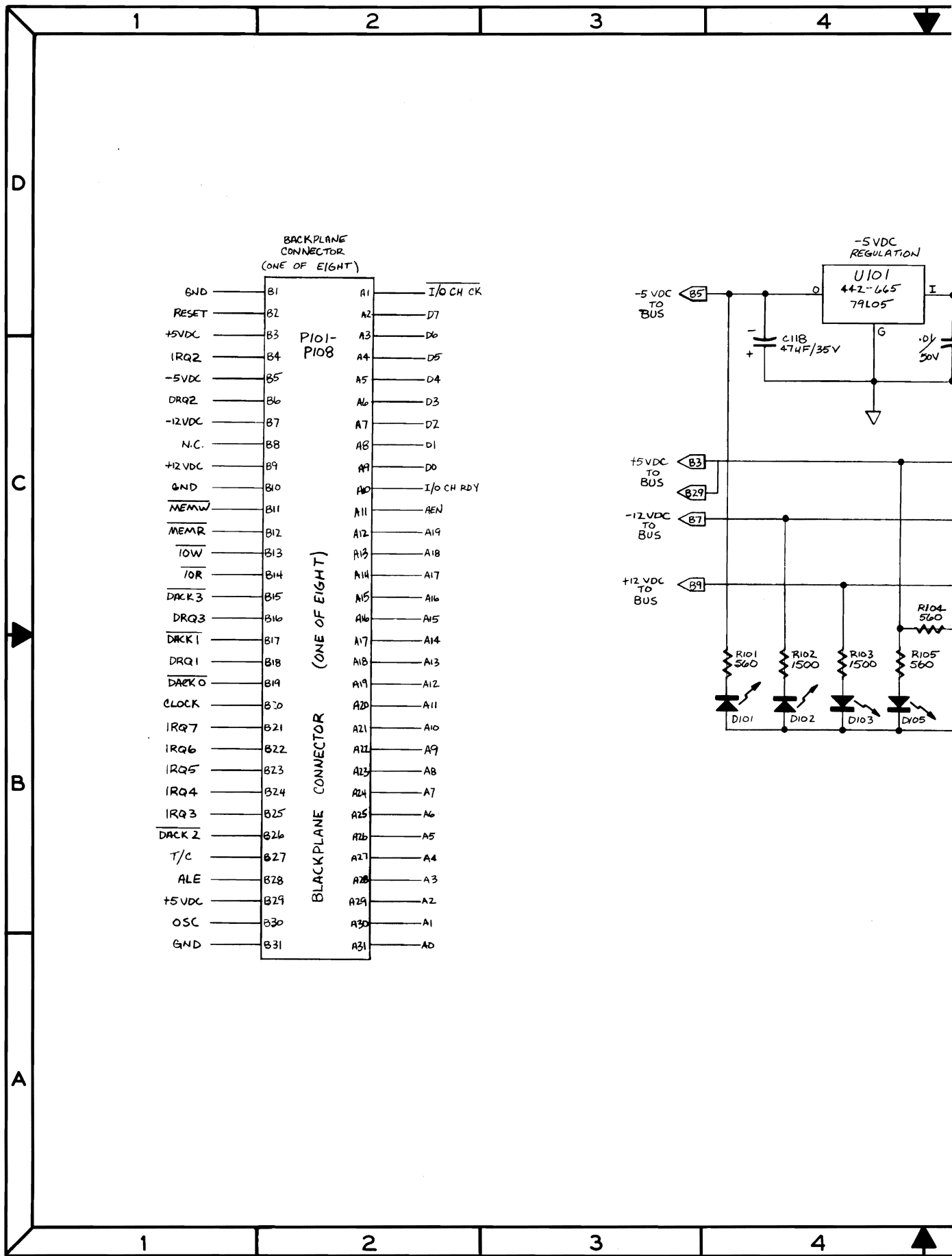
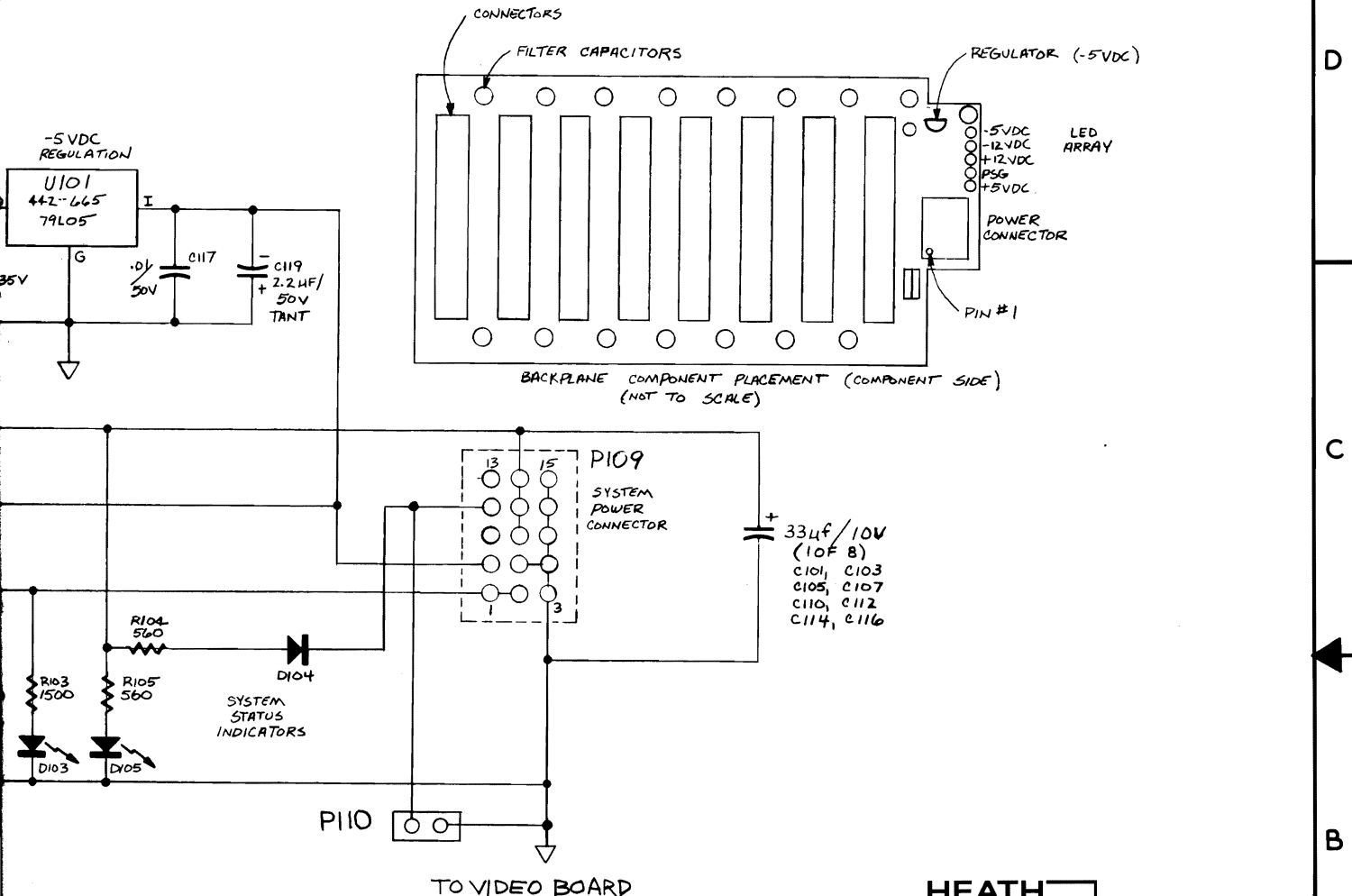


Figure 5.1. Backplane Board Component Layout





**NOTES:**

- ALL RESISTOR VALUES ARE IN OHMS (K = 1,000, M = 1,000,000) ALL RESISTORS ARE 1/4-WATT, 5% UNLESS OTHERWISE SPECIFIED.
- ALL CAPACITOR VALUES ARE IN µF (MICROFARADS), UNLESS OTHERWISE SPECIFIED.
- REFER TO THE CIRCUIT BOARD COMPONENT VIEW FOR THE PHYSICAL LOCATION OF PARTS.

**LEGEND:**

- CIRCUIT BOARD GROUND
- +5V
- BUS SIGNAL
- MECHANICAL CONNECTION
- DIRECTION TO
- DIRECTION FROM
- NO CONNECTION
- CONNECTION

**PARTS ORDERING INFORMATION:**

If you order a part from Zenith Data Systems, use the (HE) prefix. Example:  
HE 443-730

If you order a part from Heath Company, DO NOT use the (HE) prefix. Example:  
443-730

For semiconductor type numbers (Example: 74LS153), refer to the "Semiconductor Identification Chart."

**INDEX:**

Sheet 1 of 1  
BACKPLANE BOARD

585-84-01  
BACKPLANE BOARD  
**SHEET 1 OF 1**

# SERVICE MODULE

---

# Keyboard

**Z-150 PC Desktop Computers**  
**Z-160 PC Portable Computers**

---

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

## Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Zenith Data Systems Corporation  
St. Joseph, Michigan 49085

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# Abbreviations

ASCII	American Standard Code for Information Interchange
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
Hex	Hexadecimal
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least-Significant Bit
mA	Milliampere
MSB	Most-Significant Bit
RAM	Random Access Memory
ROM	Read-Only Memory
VDC	Volts Direct Current

# Description and Specifications

## Introduction

This service module provides keyboard information for the Z-150 PC Desktop Computer and the Z-160 PC Portable Computer. This chapter includes the description and specifications of the keyboard.

## Description

Refer to Figure 1.1. The keyboard is packaged in a low-profile enclosure with a tilt adjustment for 5-degree (Z-150 only) or 15-degree orientations.

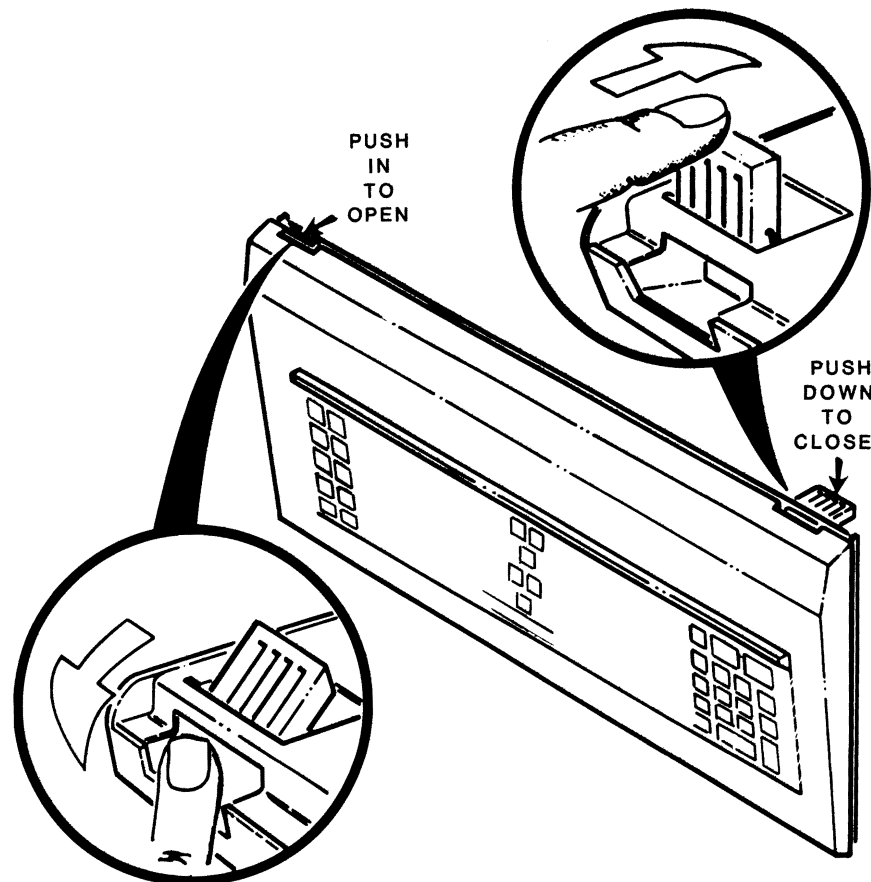
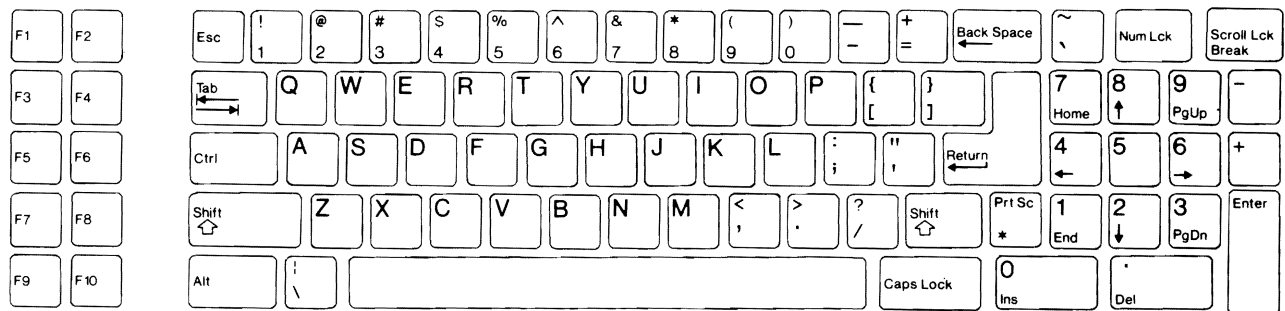


Figure 1.1. Z-150 Desktop Computer Keyboard

## Description and Specifications

Refer to Figure 1.2. The keyboard contains 83 keys laid out in three major groupings. The central portion of the keyboard consists of a standard (QWERTY) typewriter keyboard layout. On the left side, arranged as a  $2 \times 5$  block, are 10 function keys. These keys are user-defined by software. On the right side is a 16-key keypad area. This area also is defined by software, but contains legends for the functions of numeric entry, cursor control, and calculator pad screen edit.



**Figure 1.2. Keyboard Key View**

## Description and Specifications

---

The keyboard interface is defined so system software has the maximum flexibility in defining keyboard operation. This is accomplished by having the keyboard return specific hexadecimal (hex) codes rather than ASCII codes. In addition, all keys except control keys can be event driven and generate both make and break codes. For example, key 1 produces hexadecimal 01 when pressed and hexadecimal 81 when released. The keyboard input/output (I/O) driver can produce code either with or without control keys (SHIFT, CTRL, ALT) pressed, or under event driven conditions, as required by the application.

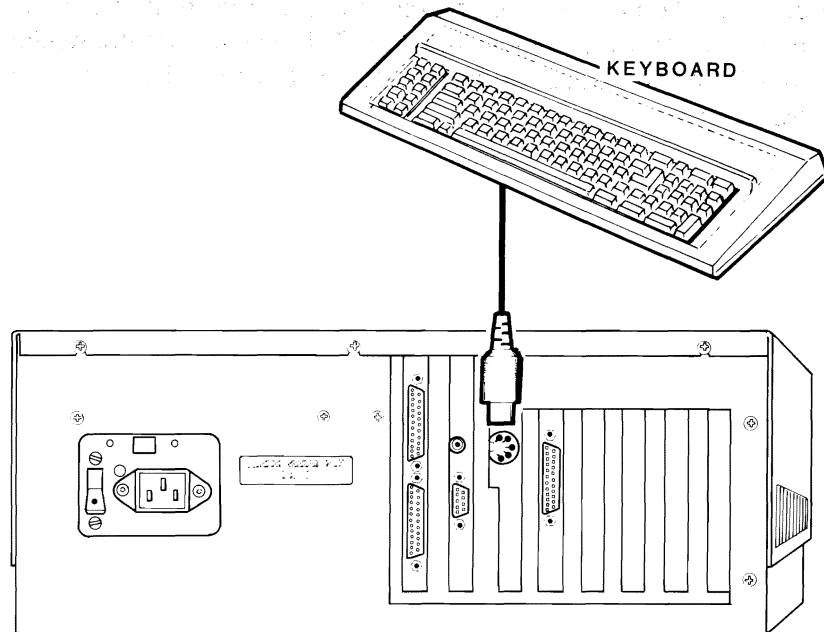
## Specifications

<b>Keys:</b>	84 keys
<b>Modes:</b>	Extended function capabilities
<b>Microprocessor:</b>	8748 microcomputer or 8048 or 8031 (8048 emulator)
<b>Operating Environment:</b>	60° to 90°F (16° to 32°C) 10 to 80% relative humidity
<b>Contacts:</b>	Single-pole, single-throw
<b>Maximum Ratings:</b>	+ 5 VDC, 100 mA

# Installation and Configuration

## Installation

Refer to Figure 2.1. The keyboard is attached to the Z-100 PC Series Computers via a coiled serial interface cable connected to the rear of the CPU card.



**Figure 2.1. Keyboard Installation**

### NOTES:

1. The floppy disk serial I/O card may or may not have two serial connectors as shown in Figure 2.1.
2. The three-card computer design combines the floppy disk serial I/O card with the video card and will have one serial connector, one RGB connector, and one composite-monochrome video out jack (not illustrated).
3. The two-card computer design combines the memory-parallel output card with the CPU card. This new card (also not illustrated) will have the parallel connector and the keyboard connector on it.

## Configuration

The keyboard cable is a coiled, shielded, five-wire cable. The cable interface contains power (+ 5 VDC), ground, two bidirectional signal lines, and a keyboard reset line (disabled). The cable is either permanently attached at the keyboard end and plugs into the CPU via a DIN connector, or is separate from the keyboard depending on the model (refer to "Parts List," Chapter 9).

# Chapter 3

## Operation

### Keyboard Codes

The keyboard sends hex codes to the CPU card. Refer to Table 3.1 for the list of hex codes corresponding to the key(s) pressed.

For most keys, the value received will be the least-significant byte of the key code shown in the table. For instance, 2C7AH would be received as 7AH.

However, keys where the least-significant byte is 0 will generate two bytes, the first having a value of zero (0) to indicate a special key and the second being the code of the key itself. Thus, function key F10 (which generates 7100H in hardware) will generate 00H followed by 71H.

The table is arranged as follows: main keyboard by row, followed by function keys in order.

**Table 3.1. Keyboard Codes (Hardware)**

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
ESC	011BH	011BH	011BH	----	011BH
!					
1	0231H	0221H	----	7800H	0231H
@					
2	0332H	0340H	0300H	7900H	0332H
#					
3	0433H	0423H	----	7A00H	0433H
\$					
4	0534H	0524H	----	7B00H	0534H
%					
5	0635H	0625H	----	7C00H	0635H
↑					
6	0736H	075EH	071EH	7D00H	0736H
&					
7	0837H	0826H	----	7E00H	0837H
*					
8	0938H	092AH	----	7F00H	0938H
(					



## Operation

Table 3.1 (Continued). Keyboard Codes (Hardware)

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
9	0A39H	0A28H	----	8000H	0A39H
)					
0	0B30H	0B29H	----	8100H	0B30H
—					
-	0C2DH	0C5FH	0C1FH	8200H	0C2DH
+					
=	0D3DH	0D2BH	----	8300H	0D3DH
BACK SPACE	0E08H	0E08H	0E7FH	----	0E08H
~					
`	2960H	297EH	----	----	2960H
NUM LCK	----	----	(Note 2)	----	----
SCROLL LCK					
BREAK	----	----	(Note 3)	(Note 4)	----
TAB	0F09H	0F00H	----	----	0F09H
Q	1071H	1051H	1011H	1000H	1051H
W	1177H	1157H	1117H	1100H	1157H
E	1265H	1245H	1205H	1200H	1245H
R	1372H	1352H	1312H	1300H	1352H
T	1474H	1454H	1414H	1400H	1454H
Y	1579H	1559H	1519H	1500H	1559H
U	1675H	1655H	1615H	1600H	1655H
I	1769H	1749H	1709H	1700H	1749H
O	186FH	184FH	180FH	1800H	184FH
P	1970H	1950H	1910H	1900H	1950H
{					
[	1A5BH	1A7BH	1A1BH	----	1A5BH
}					
]	1B5DH	1B7DH	1B1DH	----	1B5DH
7					
HOME	4700H	4737H	7700H	(Note 5)	4737H
8					
(up arrow)	4800H	4838H	----	(Note 5)	4838H
9					
PGUP	4900H	4939H	8400H	(Note 5)	4939H
-	4A2DH	4A2DH	----	----	4A2DH
CTRL	----	----	----	----	----
A	1E61H	1E41H	1E01H	1E00H	1E41H
S	1F73H	1F53H	1F13H	1F00H	1F53H
D	2064H	2044H	2004H	2000H	2044H

**Table 3.1 (Continued). Keyboard Codes (Hardware)**

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
F	2116H	2146H	2106H	2100H	2146H
G	2267H	2247H	2207H	2200H	2247H
H	2368H	2348H	2308H	2300H	2348H
J	246AH	244AH	240AH	2400H	244AH
K	256BH	254BH	250BH	2500H	254BH
L	266CH	264CH	260CH	2600H	264CH
:					
;	273BH	273AH	----	----	273BH
"					
'	2827H	2822H	----	----	2827H
RETURN	1C0DH	1C0DH	1C0AH	----	1C0DH
4					
(left arrow)	4B00H	4B34H	7300H	(Note 5)	4B34H
5	----	4C35H	----	(Note 5)	4C35H
6					
(right arrow)	4D00H	4D36H	7400H	(Note 5)	4D36H
+	4E2BH	4E2BH	----	----	4E2BH
(left) SHIFT	----	----	----	----	----
Z	2C7AH	2C5AH	2C1AH	2C00H	2C5AH
X	2D78H	2D58H	2D18H	2D00H	2D58H
C	2E63H	2E43H	2E03H	2E00H	2E43H
V	2F76H	2F56H	2F16H	2F00H	2F56H
B	3062H	3042H	3002H	3000H	3042H
N	316EH	314EH	310EH	3100H	314EH
M	326DH	324DH	320DH	3200H	324DH
<					
,	332CH	333CH	----	----	332CH
>					
.	342EH	343EH	----	----	342EH
?					
/	352FH	353FH	----	----	352FH
(right) SHIFT	----	----	----	----	----
PRT SC					
*	372AH	(Note 1)	7200H	----	372AH
END	4F00H	4F31H	7500H	(Note 5)	4F31H
2					
(down arrow)	5000H	5032H	----	(Note 5)	5032H
3					
PGDN	5100H	5133H	7600H	(Note 5)	5133H
ENTER	540DH	540DH	540AH	----	540DH

## Operation

**Table 3.1 (Continued). Keyboard Codes (Hardware)**

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
ALT	----	----	----	----	----
	2B5CH	2B7CH	2B1CH	----	2B5CH
\	3920H	3920H	3920H	3920H	3920H
(space bar)	----	----	----	----	----
CAPS LOCK	----	----	----	----	----
0					
INS	5200H	5230H	----	(Note 5)	5230H
DEL	5300H	532EH	----	----	532EH
F1	3B00H	5400H	5E00H	6800H	3B00H
F2	3C00H	5500H	5F00H	6900H	3C00H
F3	3D00H	5600H	6000H	6A00H	3D00H
F4	3E00H	5700H	6100H	6B00H	3E00H
F5	3F00H	5800H	6200H	6C00H	3F00H
F6	4000H	5900H	6300H	6D00H	4000H
F7	4100H	5A00H	6400H	6E00H	4100H
F8	4200H	5B00H	6500H	6F00H	4200H
F9	4300H	5C00H	6600H	7000H	4300H
F10	4400H	5D00H	6700H	7100H	4400H

**NOTES:**

1. Pressing SHIFT-PRT SC will cause the contents of the screen to be sent to the printer.
2. Pressing CTRL-NUM LCK will temporarily halt the execution of a program.
3. Pressing CTRL-BREAK will halt the execution of a program and exit back to the system. This key sequence sends a special code of 0000H.
4. Pressing ALT-BREAK will empty the keyboard (type ahead) buffer.
5. This function is used for entering special keycodes. If you want to enter a special keycode, press and hold the ALT key, and then enter the three-digit keycode (in decimal) on the numeric (calculator) portion of the keyboard. When you release the ALT key, the desired code will be generated. For example, to generate the hexadecimal code 7B (decimal 123), press and hold the ALT key, then enter 1, 2, and 3 on the calculator portion of the keyboard, then release the ALT key. The actual code generated will be preceded by 38H, the scan code of the ALT key. Therefore, the complete generated code for ALT-123 is 387BH.

## Special Function Key Combinations

The following key combinations are used for special purposes by the computer firmware (MFM-150 monitor ROM).

CTRL-ALT-DEL:	Resets the computer.
CTRL-ALT-INS:	Returns control to the MFM-150 monitor.
CTRL-ALT-RETURN:	Enters the MFM-150 monitor debug program and displays the CPU register contents.
ESC:	Aborts booting of disk.

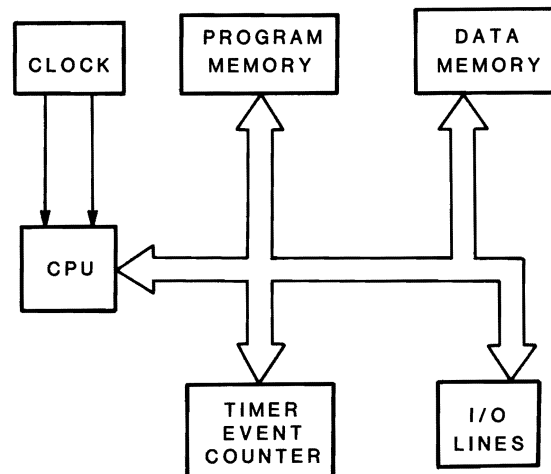
# Theory of Operation

## Introduction

This chapter includes a brief theory of operation. If a more detailed circuit description is desired, refer to Chapter 5 of this module.

## Theory of Operation

Refer to Figure 4.1. The keyboard uses a microcomputer (Intel 8048) performing the keyboard scan functions. Additional keyboard functions are: key debounce, buffering of up to 256 key scan codes, maintaining bidirectional serial communications with the CPU, and executing the handshaking protocol required by each code transfer.



**Figure 4.1. Keyboard Block Diagram**

# Detailed Circuit Description

## Introduction

This chapter provides a detailed circuit description and pin definitions of the microcomputer. Refer to the schematic while reading the following.

## Circuit Description

The keyboard is a strobe scanning keyboard, controlled by microcomputer U107. U107 performs keyboard matrix scanning, setting and resetting of LEDs, actuation of the audio transducer, and serial communication with the computer.

All keys except NUM LCK (key 69) and CAPS LOCK (key 58) are configured in a general matrix consisting of 11 scan lines and 8 sense lines. A keyswitch and diode are arranged at each crossover point. The diodes prevent the generation of phantom keys due to multiple closures.

A 6.00 MHz crystal is connected between XTAL and XTAL 2 for the internal control and timing references of U107. Capacitors C1 and C2 are used for stability purposes.

Port bits P10 (LSB) through P13 (MSB) of U107 control the scan lines. The port bits drive U105 and U106 (dual one-of-four decoders) with the selected scan line being driven low. After setting a scan line, the sense lines are checked for a key closure.

Resistors R9 through R16 are used for pull-ups of the sense lines. The active low sense lines are buffered by U103 and U104 to provide static immunity for the microprocessor which is a NMOS device. The sense lines are read by bits D0 through D7.

The outputs P23 and P24, when directed by U107, are driven by U101, lighting the NUM LCK LED (key 69) and CAPS LOCK LED (key 58). Resistors R1 and R2 are LED bias resistors.

Port bit P22 drives the audio transducer, with U101 and R4 providing the current path. Diode D1 is used as a current shunt and R3 is the bias resistor.

## Detailed Circuit Description

---

U102 buffers the input/output data and clock. Resistors R5 and R6 are pull-up resistors for U102. Capacitors C3, C4, and C5 are line filters.

The KYBRST\* line is tied high through resistor R7, thereby eliminating a keyboard hard reset.

J1 provides jumper selectability of either masked ROM (8048) or EPROM (8748) versions of U107. Production keyboards are jumpered for masked ROMs.

The filter of C6 through C14 provides the required filtering of the +5 VDC input.

Power of approximately 5 VDC is applied to the keyboard through pin 1.

**Table 5.1. 8048/8748 Pin Definitions**

DESIGNATION	PIN	DESCRIPTION
Vss	20	Circuit GND potential
Vdd	26	Low power standby pin
Vcc	40	Main power supply; +5 V during operation
PROG	25	Output strobe for I/O expander
P10 – P17 Port 1	27-34	8-bit quasi-bidirectional port
P20 – 27 Port 2	21-24	8-bit quasi-bidirectional port
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch, and serve as a 4-bit I/O expander bus for the 8243.

## Detailed Circuit Description

Table 5.1 (Continued). 8048/8748 Pin Definitions

DESIGNATION	PIN	DESCRIPTION
DB0 – DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$ , $\overline{WR}$ strobes. The port also can be statically latched. Contains the 8 low order program counter during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$ . Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ , and $\overline{WR}$ .
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low.)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.  Used as a read strobe to external data memory. (Active low.)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low.)
$\overline{WR}$	10	Output strobe during a bus write. (Active low.)  Used as a write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle. The negative edge of ALE strobes addresses into external data and program memory.



Detailed Circuit Description

---

**Table 5.1 (Continued). 8048/8748 Pin Definitions**

DESIGNATION	PIN	DESCRIPTION
$\overline{\text{PSEN}}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low.)
$\overline{\text{SS}}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low.)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high.)
XTAL1	2	One side of crystal input for internal oscillator.
XTAL2	3	Other side of crystal input.

# Disassembly

## Disassembly Procedure

The following is the disassembly sequence for the keyboard. Refer to Figure 6.1. The Z-160 disassembly sequence is similar; for an accurate representation refer to Figure 9.2.

- Place the keyboard face down on a soft cloth.
- Remove four  $6 \times 3/8$ " screws and bottom panel.
- Remove six  $6 \times 1/4$ " screws and two washers.
- Remove rubber strain relief (keyboard cable connector in the Z-160) from slot.
- Remove wired keyboard.

# Disassembly

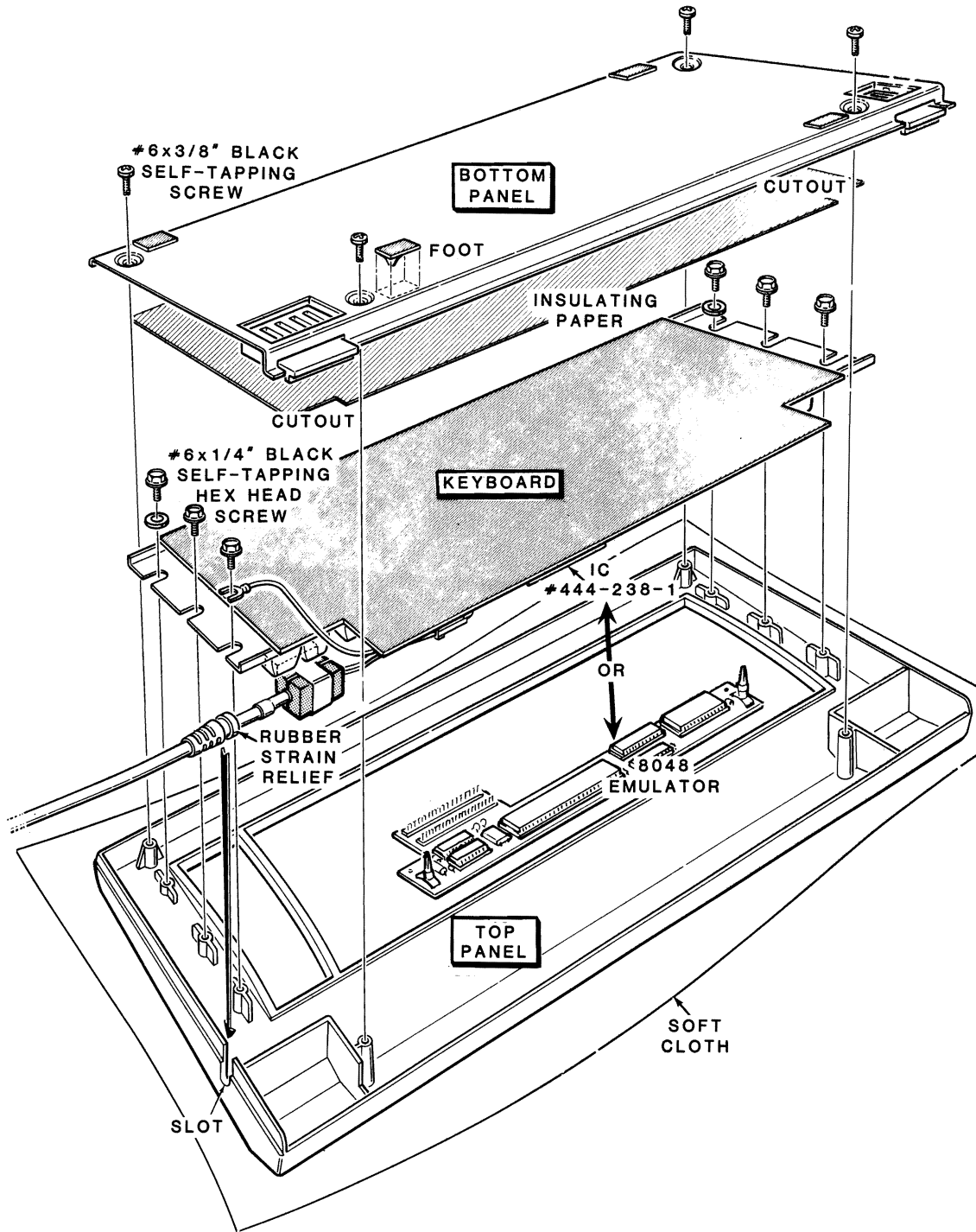


Figure 6.1. Keyboard Disassembly

# Troubleshooting

The microcomputer in the keyboard performs several functions when requested by the CPU, including a power-on self-test. This diagnostic CRC (Cyclic Redundancy Check) uses an algorithm to check the microcomputer ROM, tests memory, and checks for stuck keys. If a problem exists with the keyboard, an interrupt is generated to the CPU and a message is displayed on the video monitor.

# Reassembly

## Reassembly Procedure

The following is the reassembly sequence for the keyboard. Refer to Figure 8.1. The Z-160 reassembly sequence is similar; for an accurate representation refer to Figure 9.2.

- Place the keyboard cabinet face down on a soft cloth.
- Install rubber strain relief (keyboard cable connector in the Z-160) into slot.
- Install wired keyboard into cabinet and secure with six  $6 \times 1/4$ " screws and two washers.
- Install the bottom panel and secure with four  $6 \times 3/8$ " screws.

# Reassembly

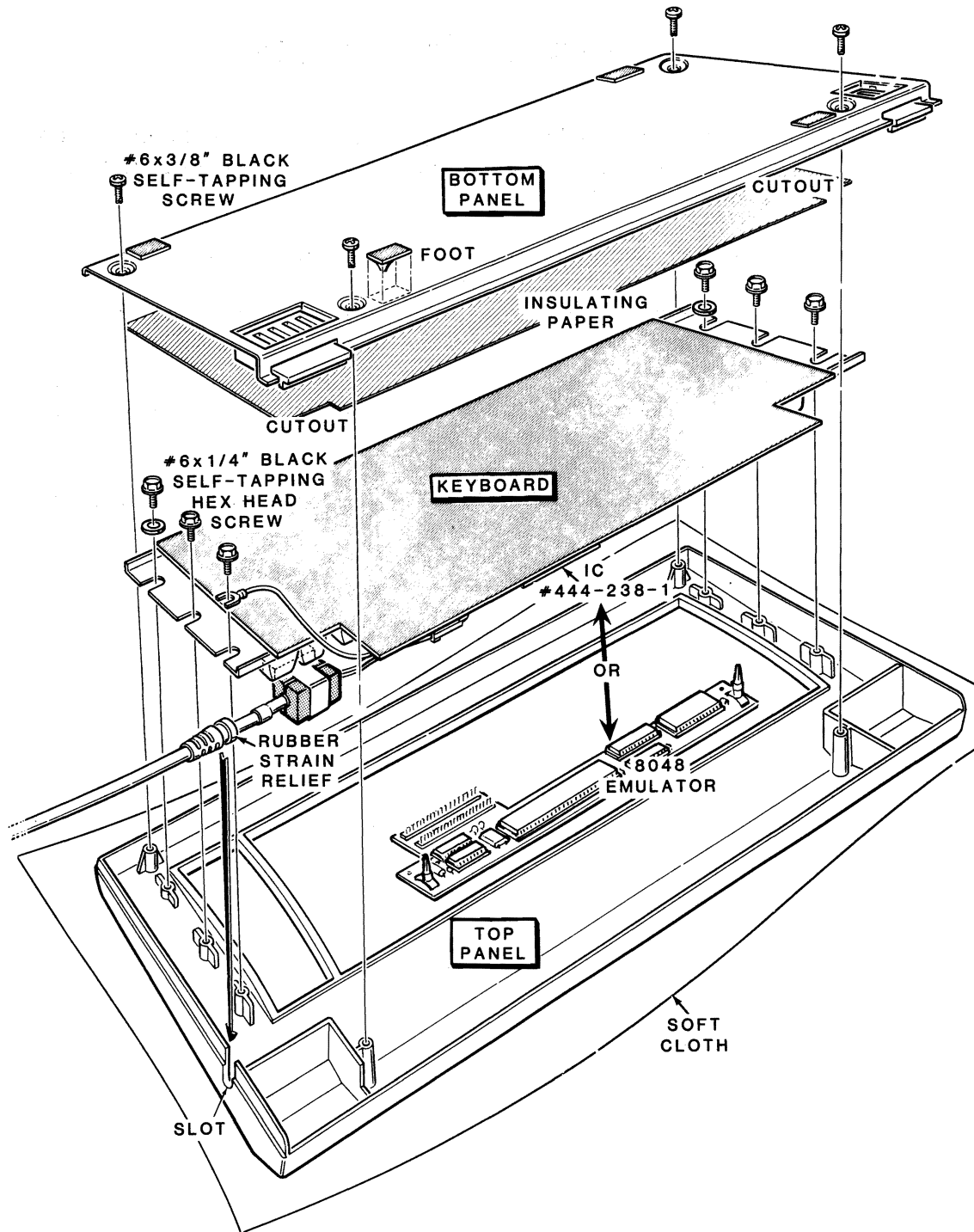


Figure 8.1. Keyboard Reassembly

# Parts List

## Replacement Parts

This chapter includes a parts list of the keyboard components supplied by Zenith Data Systems only. Refer to Figure 9.1 for Z-150 part identification. The Z-150 Desktop Computer keyboard wired and tested part number is HE 181-5599 or 181-5745. The Z-160 Portable Computer keyboard wired and tested part number is HE 181-4935-1. Refer to Figure 9.2.

**CAUTION: This board contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.**

## Parts List

**Keyboard Assembly Z-150**

<u>ITEM NUMBER</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
5	HE 205-1923-1	Bottom plate
10	HE 250-1434	Screw, pan head phillips 6-BT × .375"
15	HE 266-1220	Support leg
20	HE 258-759	Spring, leg return
25	HE 75-138	Insulator
30	HE 75-851	Insulator
35	HE 163-16	Wired keyboard
	with	
	HE 134-1473	Keyboard cable
40	HE 250-1521	Screw, slotted 6-AB × .250"
45	HE 444-238-1	Keyboard microcomputer (see Y101)
	or	
	HE 444-314	Keyboard microcomputer (see Y101)
	or	
	HE 187-5305	8048 emulator
50	HE 253-60	Washer
55	HE 260-713	Strain relief
60	HE 92-803	Molded cabinet
65	HE 485-54	Plug, button



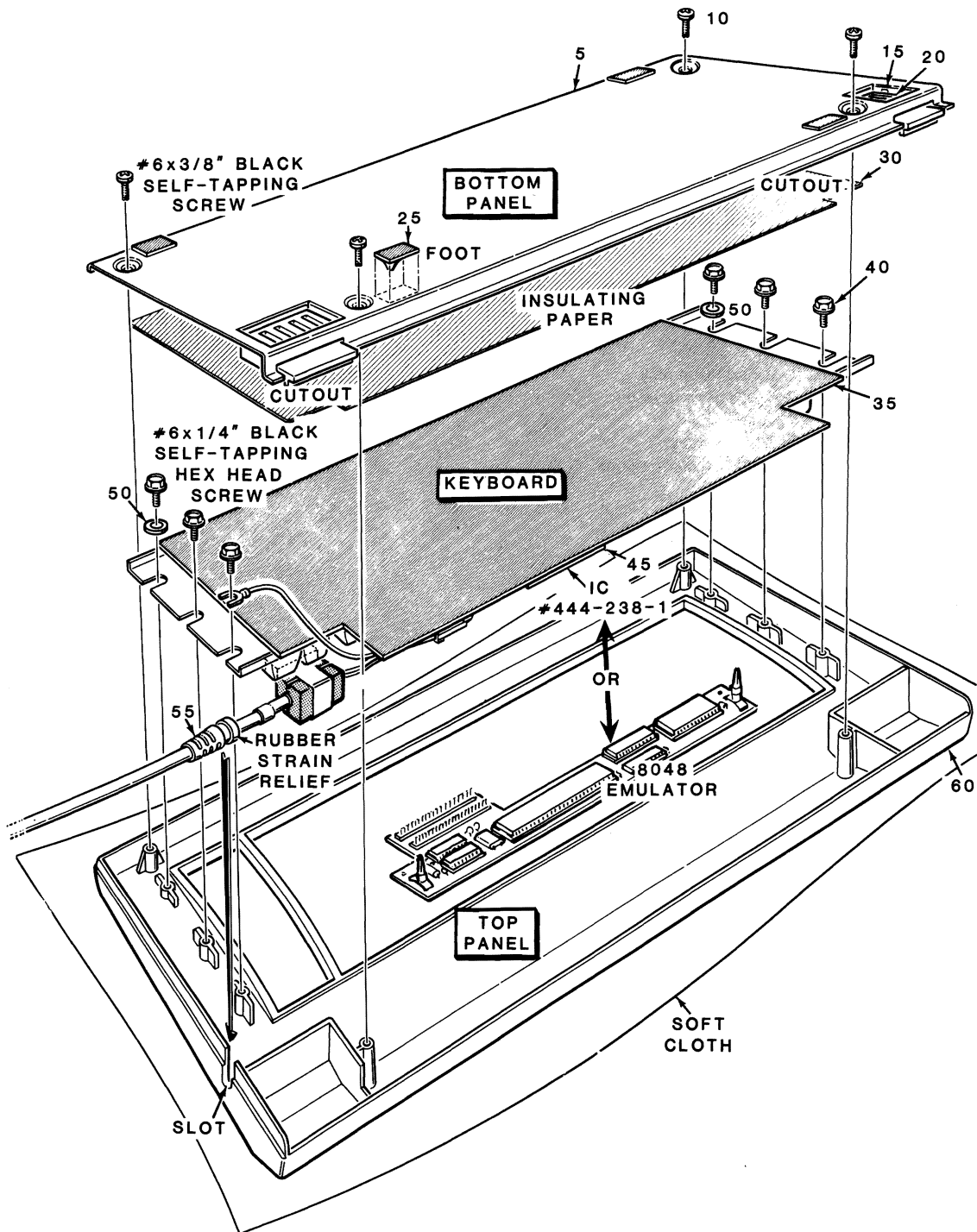


Figure 9.1. Z-150 Desktop Computer Keyboard—Exploded View

## Parts List

## Keyboard Assembly Z-160

<u>ITEM NUMBER</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
5	HE 92-823	Keyboard bottom
10	HE 250-1434	Screw, pan head phillips 6-BT × .375"
15	HE 94-643	Support leg
20	HE 453-360	Shaft
25	HE 161-16	Keyboard assembly
30	HE 250-1508	Screw, pan head slotted 6-32 × .187"
35	HE 134-1448	Cable assembly
40	HE 444-238-1	Keyboard microcomputer (see Y101)
	or	
	HE 444-314	Keyboard microcomputer (see Y101)
	or	
	HE 187-5305	8048 emulator
45	HE 92-322	Keyboard top
50	HE 94-644	Slide
55	HE 94-645	Slide latch
60	HE 252-178	Nut, push on
65	HE 134-1397	Keyboard cable assembly, coiled

Parts List

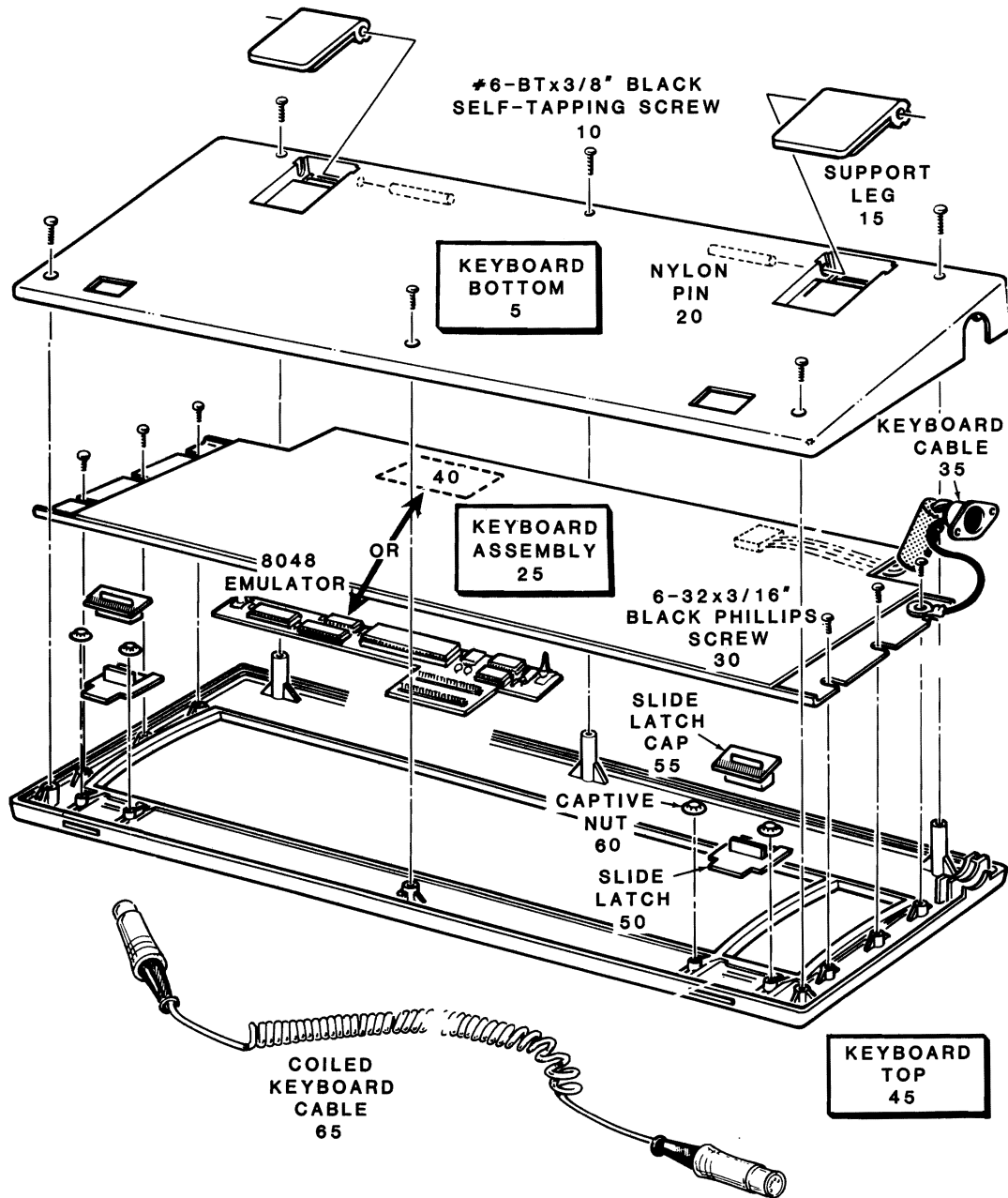


Figure 9.2. Z-160 Portable Computer Keyboard—Exploded View

## Parts List

## Keyboard Components Z-150 and Z-160

<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>	<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
<b>Capacitors</b>			<b>Integrated Circuits</b>		
C1	HE 21-705	10 pF	U101	HE 443-967	Hex inverter buffer/driver
C2	HE 21-757	22 pF	U102	HE 443-811	Buffer, tri-state
C3	HE 21-147	47 pF	U103	HE 443-991	Hex buffer/converter
C4	HE 21-147	47 pF	U104	HE 443-991	Hex buffer/converter
C5	HE 21-147	47 pF	U105	HE 443-1036	Dual one-of-four decoder
C6	HE 25-162	33 $\mu$ F	U106	HE 443-1036	Dual one-of-four decoder
C7	HE 27-73	.047 $\mu$ F	U107	HE 444-238-1 or HE 444-314	Microcomputer
C8	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C9	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C10	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C11	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C12	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C13	HE 21-95	6 $\times$ 0.1 $\mu$ F			
C14	HE 25-863	4.7 $\mu$ F			
<b>Diode</b>				HE 485-54	Dummy plug for side exit
D101	HE 56-56	IN4149		HE 473-29	Audio transducer
<b>Crystal</b>					
Y101	HE 404-647 or HE 404-689	6.000 MHz (use only with keyboard microcomputer HE 444-238) 3.58 MHz (use only with keyboard microcomputer HE 444-314)			
<b>Resistors</b>					
R1	HE 6-221-12	220 $\Omega$			
R2	HE 6-221-12	220 $\Omega$			
R3	HE 6-101-12	100 $\Omega$			
R4	HE 6-472-12	4.7 k $\Omega$			
R5	HE 6-202-12	2 k $\Omega$			
R6	HE 6-202-12	2 k $\Omega$			
R7	HE 6-202-12	2 k $\Omega$			
R8	HE 6-472-12	4.7 k $\Omega$			
R9	HE 6-472-12	4.7 k $\Omega$			
R10	HE 6-472-12	4.7 k $\Omega$			
R11	HE 6-472-12	4.7 k $\Omega$			
R12	HE 6-472-12	4.7 k $\Omega$			
R13	HE 6-472-12	4.7 k $\Omega$			
R14	HE 6-472-12	4.7 k $\Omega$			
R15	HE 6-472-12	4.7 k $\Omega$			
R16	HE 6-472-12	4.7 k $\Omega$			
R17	HE 6-472-12	4.7 k $\Omega$			

## 8048 Emulator

Part Number HE 181-5305. Refer to Figure 9.3.

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
<b>Capacitors</b>			<b>Integrated Circuits</b>		
C1	HE 21-786	.1 $\mu$ F	U1	HE 443-802	Quad, multiplexer 2-input, tri-state
C2	HE 21-786	.1 $\mu$ F		or	
C3	HE 21-786	.1 $\mu$ F		HE 443-1037	
C4	HE 21-786	.1 $\mu$ F		HE 434-299	Socket
C5	HE 21-786	.1 $\mu$ F	U2	HE 443-802	Quad, multiplexer 2-input, tri-state
C6	HE 21-786	.1 $\mu$ F		or	
C7	HE 21-707	36 pF		HE 443-1037	
C8	HE 21-707	36 pF	U3	HE 434-299	Socket
C9	HE 25-866	22 pF		HE 443-1119	Microprocessor
				HE 434-253	Socket
			U4	HE 443-872	Hex inverter
				HE 434-298	Socket
			U5	HE 443-837	8-bit tri-state latch
				HE 434-311	Socket
			U6	HE 444-320	Emulator ROM
				HE 434-312	Socket
			<b>Crystal</b>		
			Y1	HE 404-647	

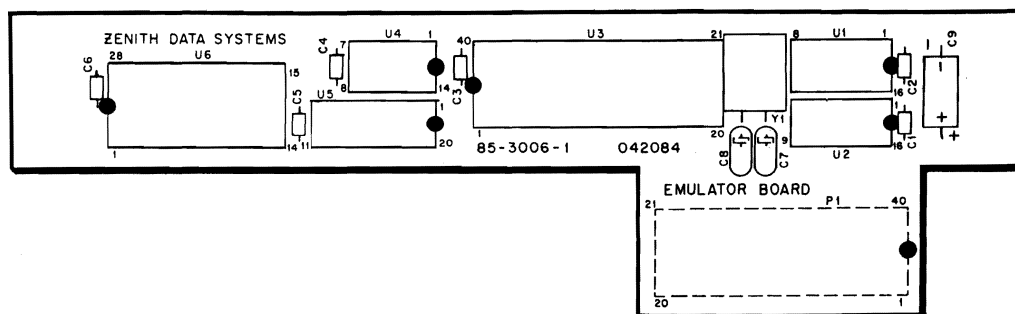


Figure 9.3. 8048 Emulator Board—Component View

Parts List

# Semiconductor Identification

This section will help to identify the various semiconductor devices installed on the keyboard. The components are listed in ascending numerical order, along with the device number (where applicable), and device lead configuration. The Zenith/Heath part numbers are cross-referenced, where applicable, with generic/alternate device numbers.

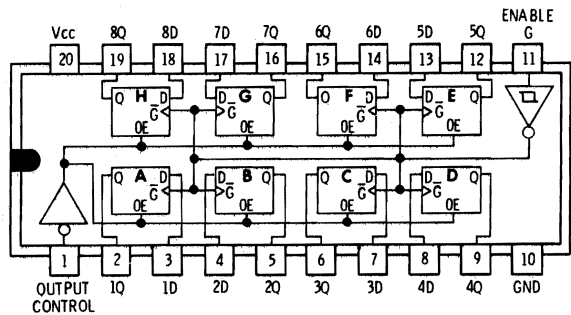
## Part Number Index

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-802 or HE 443-1037	74LS257 74ALS257	U1, U2 Quad multiplexer 2-input tri-state	
HE 443-811	74LS125	U102 Buffer tri-state	

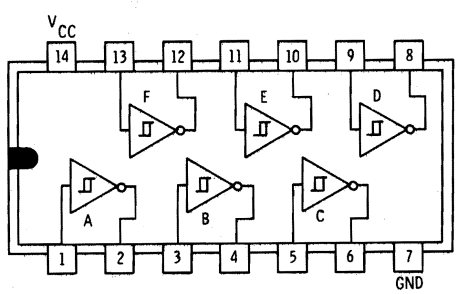
Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
-------------------	---------------	-------------	--------------------

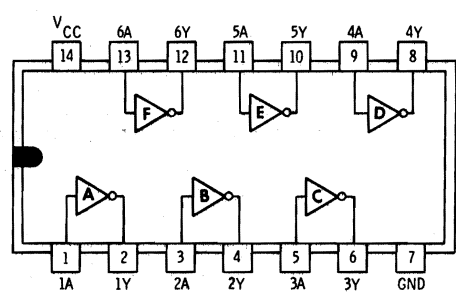
HE 443-837      74LS373      U5  
8-bit tri-state latch



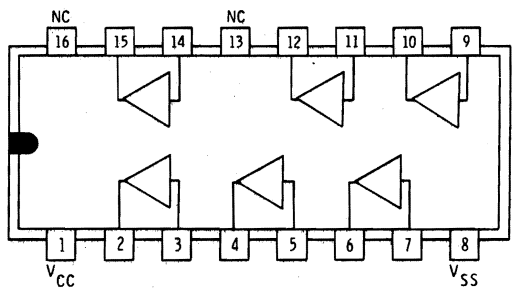
HE 443-872      74LS14      U4  
Hex inverter



HE 443-967      7406      U101  
Hex inverter buffer/driver



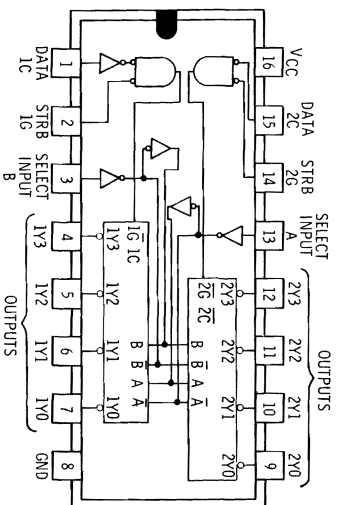
HE 443-991      MC14050B      U103, U104  
Hex buffer/convertter



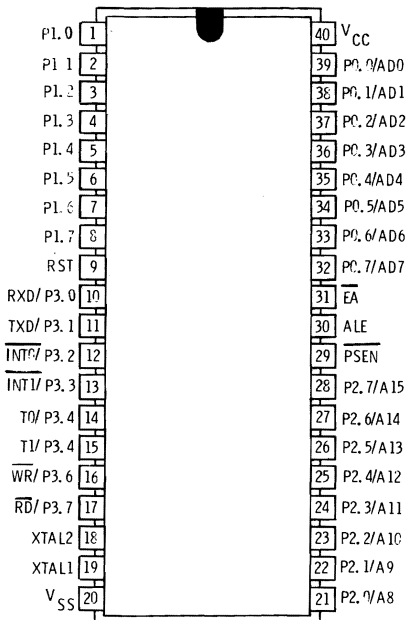
Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
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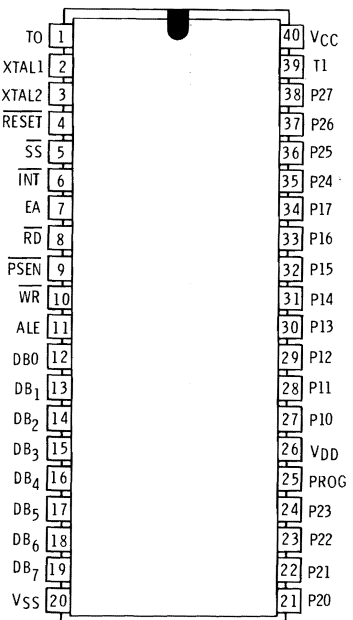
HE 443-1036      74LS156  
 U105, U106  
 Dual one-of-four decoder



HE 443-1119      8031  
 U3  
 Microprocessor



HE 444-238-1      8048/8748  
 or  
 HE 444-314      U107  
 Microcomputer



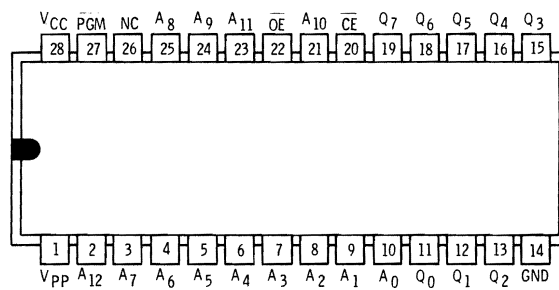


Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
-------------------------	------------------	-------------	--------------------

HE 444-320

U6  
ROM



1

2

3

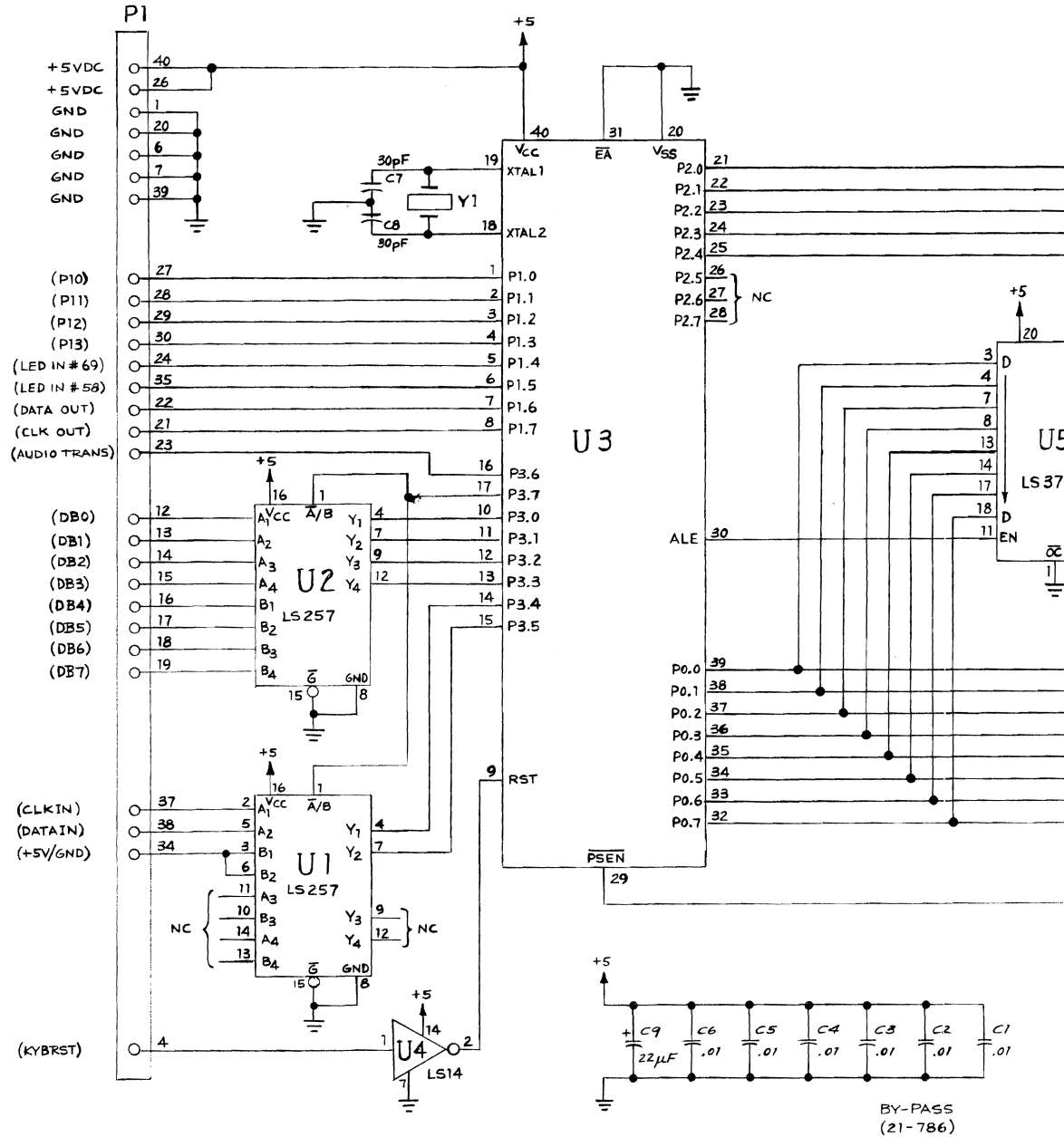
4

D

C

B

A



1

2

3

4

5

6

7

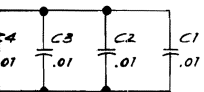
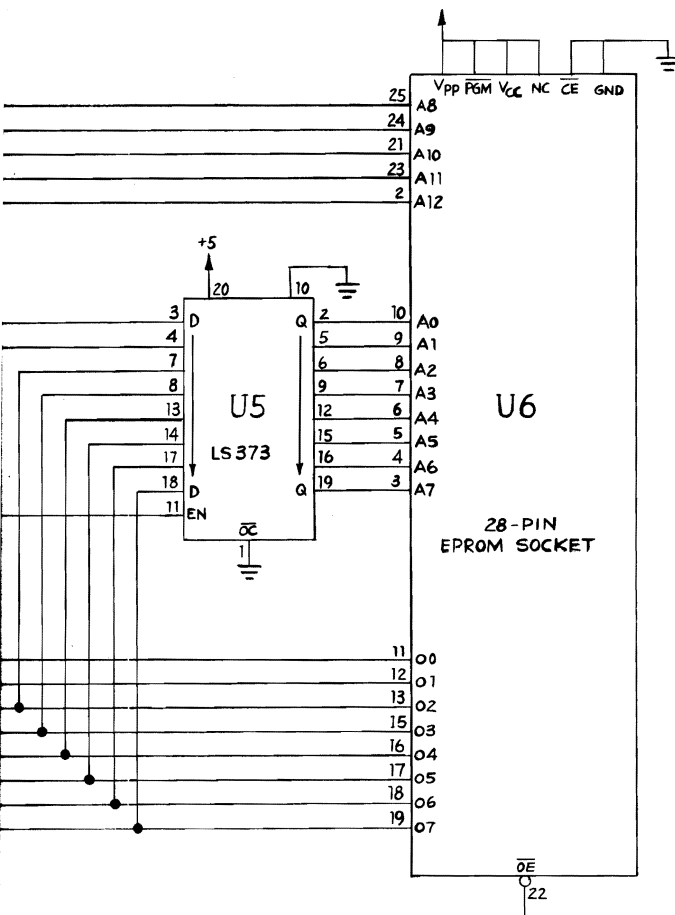
8

D

C

B

A



BY-PASS  
(21-786)



**NOTES:**

1. ALL RESISTOR VALUES ARE IN OHMS (k = 1,000, M = 1,000,000) ALL RESISTORS ARE 1/4-WATT, 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITOR VALUES ARE IN  $\mu$ F (MICROFARADS), UNLESS OTHERWISE SPECIFIED.
3. REFER TO THE CIRCUIT BOARD COMPONENT VIEW FOR THE PHYSICAL LOCATION OF PARTS.

**PARTS ORDERING INFORMATION:**

If you order a part from Zenith Data Systems, use the (HE) prefix. Example:

HE 443-730

If you order a part from Heath Company, DO NOT use the (HE) prefix. Example:

443-730

For semiconductor type numbers (Example: 74LS153), refer to the "Semiconductor Identification Chart."

**LEGEND:**

1. CIRCUIT BOARD GROUND
2. +5V
3. BUS SIGNAL
4. MECHANICAL CONNECTION
5. DIRECTION TO
6. DIRECTION FROM
7. NO CONNECTION
8. CONNECTION

585-61-05  
8048 EMULATOR  
**SHEET 1 OF 2**

5

6

7

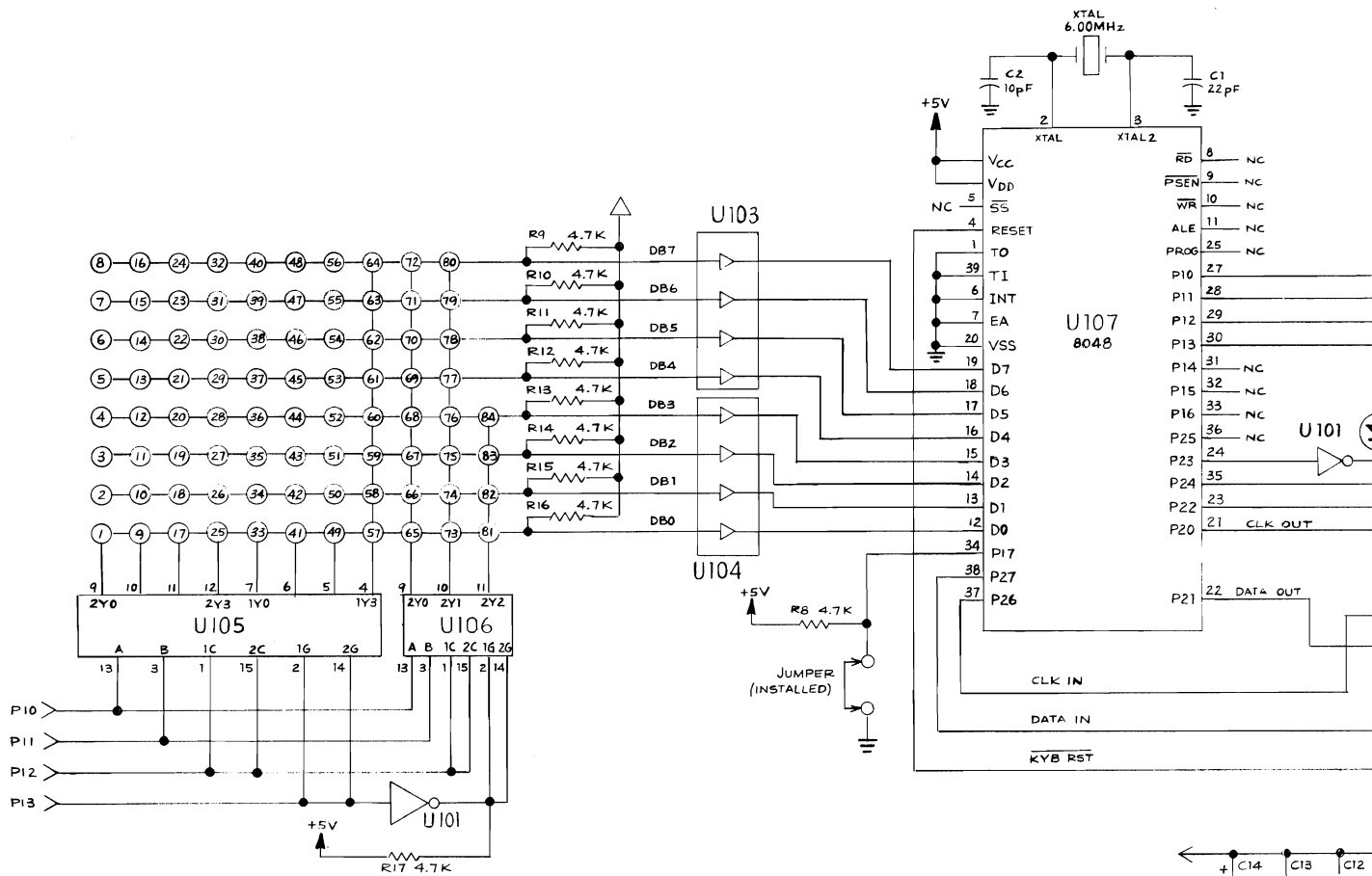
8

D

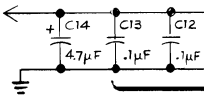
C

B

A

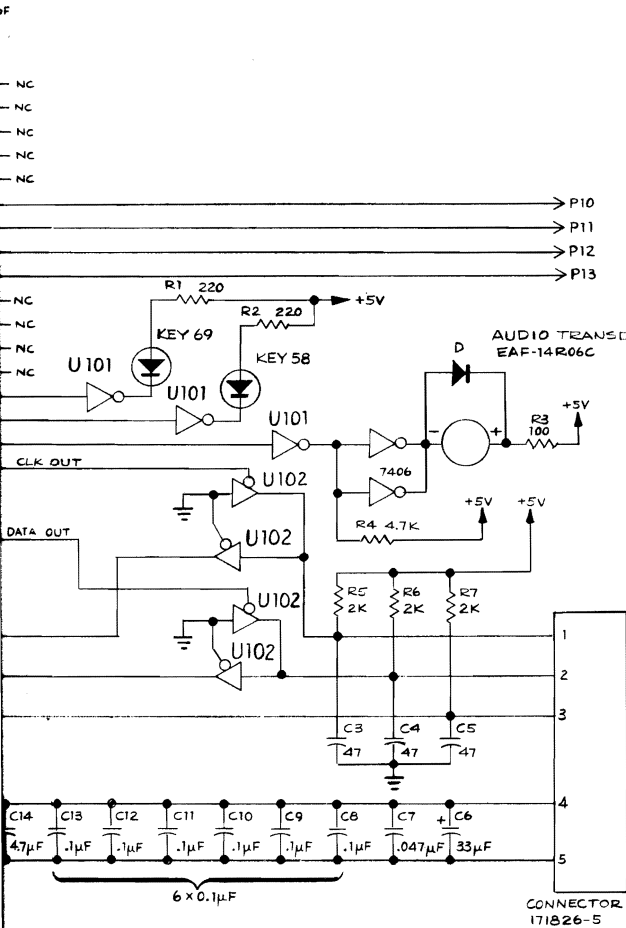
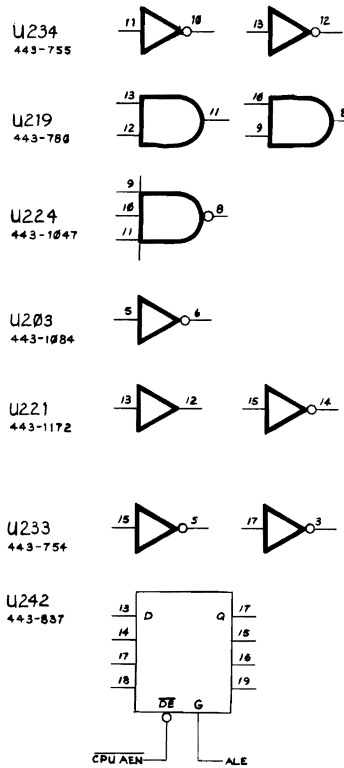


- U101 SN7406N
- U102 74LS125
- U103 MC14050BCP
- U104 MC14050BCP
- U105 74LS156
- U106 74LS156
- U107 8748/8048



EXTRA GATES:

EXTRA RESISTORS:



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS (K - 1,000, M - 1,000,000) ALL RESISTORS ARE 1/4-WATT, 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITOR VALUES ARE IN μF (MICROFARADS), UNLESS OTHERWISE SPECIFIED.
3. REFER TO THE CIRCUIT BOARD COMPONENT VIEW FOR THE PHYSICAL LOCATION OF PARTS.

PARTS ORDERING INFORMATION:

If you order a part from Zenith Data Systems, use the (HE) prefix. Example:  
HE 443-730

If you order a part from Heath Company, DO NOT use the (HE) prefix. Example:  
443-730

For semiconductor type numbers (Example: 74LS153), refer to the "Semiconductor Identification Chart."

LEGEND:

1. ▽ CIRCUIT BOARD GROUND
2. → +5V
3. □ BUS SIGNAL
4. ≧ MECHANICAL CONNECTION
5. → DIRECTION TO
6. ← DIRECTION FROM
7. + NO CONNECTION
8. • CONNECTION

585-61-05  
KEYBOARD

**SHEET 2 OF 2**

**SERVICE MODULE**  
**CPU/Memory Card with Gate Array**

---

**Z-158 Computers**

**Part Number HE-181-5445 (128K)**  
**HE-181-5857 (256K)**  
**HE-181-5601 (320K)**

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# IV

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## Introduction

This service module describes the function of the CPU/memory card used in the Z-158 model computer. Specifically, this service module describes three cards: HE-181-5445 with 128K of RAM, HE-181-5857 with 256K of RAM, and HE-181-5601 with 320K of RAM. The only difference between these cards is the number and type of RAM devices. The RAM is contained in three banks of 64- and/or 256-kilobit devices, and is expandable from 128K to 640K. For information on how to configure the CPU/memory card for different RAM sizes, refer to Chapter 2.

The CPU circuitry consists of an 8088-2 microprocessor, which makes all of the operational decisions, controls all of the functions of the computer, and communicates with all peripherals. The actions of this microprocessor are governed by machine language instructions which are contained in either the firmware (ROM), or software.

The 8088-2 can operate at clock frequencies of either 4.77 MHz or 8.0 MHz. The frequency is switch-selectable by means of a pushbutton mounted above the keyboard connector, external to the computer. The frequencies are derived by dividing the two crystal oscillator frequencies (14.31818 MHz and 24.0 MHz) by 3. Also, the CPU/memory card was designed so that an optional 8087 coprocessor may be added to speed arithmetic operations.

The 8088-2 microprocessor communicates with the rest of the system through three separate busses. The address bus determines which device is being talked to by the 8088-2. The data bus carries the actual message to or from the addressed device. The control bus determines what type of operation (such as read, write, or input/output) is to be performed and is also used to control the timing of the operation. For more information on the operation of the CPU/memory card, refer to Chapter 3.

Basically, the CPU/memory card combines the functions of CPU and RAM circuitry onto a single card. This is possible because a gate array device replaces several different components with a single IC. This gate array performs all signal generation for the computer, including all clock and control signals. It also performs all DMA functions, parity generation, and interrupt acknowledge functions for the 8088-2. Refer to Chapter 4 for more information on the gate array.

## Configuration

For instructions on removing the CPU/memory card from the computer, refer to the Z-150 PC Series Base Unit Service Module. Figure 2-1 shows the location of all switches and jumpers on the CPU/memory card.

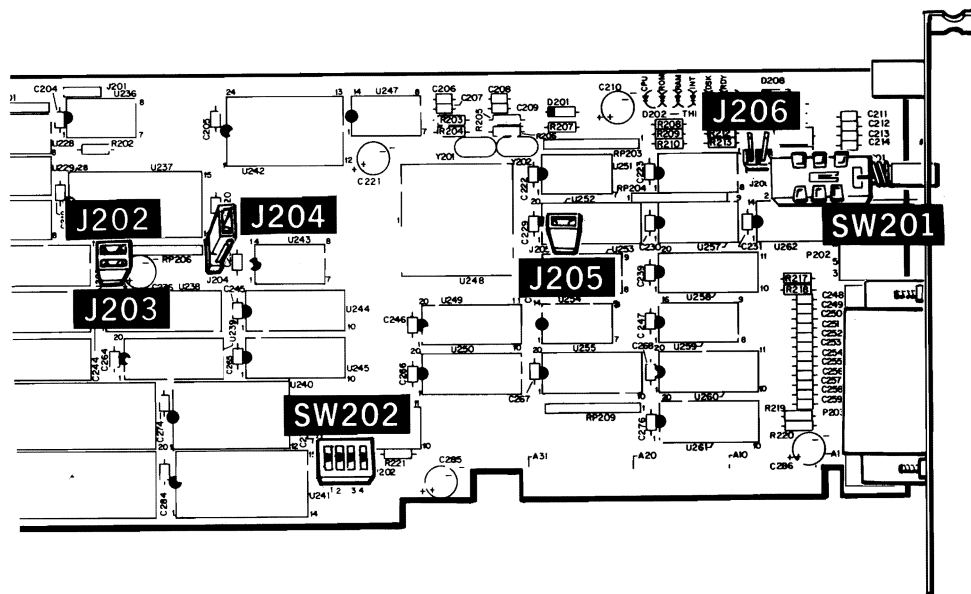


Figure 2-1: Switch and Jumper Locations

**CAUTION:** Many ICs are electrostatic-sensitive and can be damaged by static electricity if they are handled improperly. When you remove an IC or card from its mounting or from its protective packing, do not lay it down or let go of it until it is installed in the computer. Also, when you need to bend the leads of an IC, hold the device in one hand and place your other hand on the work surface before touching the IC to the work surface. This will equalize the static charges between you, the IC, and the work surface.

## Configuration

---

### Switches

Switch SW201 is a pushbutton used to select the CPU clock frequency, as explained in Table 2-1. Another way to determine the current CPU clock frequency setting is to enter **I C0** at the system's Monitor prompt and press **RETURN**. The system will respond with two hexadecimal characters. Convert these hexadecimal characters to binary. If the most-significant bit of the binary number is 1, the frequency is set at 8 MHz; if the most-significant bit is 0, the frequency is set at 5 MHz.

**Table 2-1: CPU Clock Frequency Selection**

SWITCH POSITION	CPU CLOCK FREQUENCY
IN	4.77 MHz
OUT	8.00 MHz

DIP switch SW202 configures the CPU/memory card to the specific hardware of the system. Refer to Table 2-2.

**Table 2-2: SW202 Settings**

SECTION	DEFINITION
1	Used to determine the frequency of the power supply. Normal setting is 60 Hz; do not use the 50 Hz setting. Settings are as follows:  ON = 60 Hz power supply (factory setting) OFF = 50 Hz power supply
2	Used to determine the device to be used for autoboot. Settings are as follows:  ON = Autoboot from 5.25-inch floppy disk (factory setting) OFF = Autoboot from rigid disk system

**NOTE:** This switch cannot be used to defeat the autoboot feature.

**Table 2-2 (continued): SW202 Setting**

---

SECTION	DEFINITION
3	<p>Used to determine whether or not the floppy disk controller circuitry is installed. This circuitry is contained on the video/floppy card in the Z-158 computer. Settings are as follows:</p> <p>ON = Floppy disk controller not installed OFF = Floppy disk controller installed (factory setting)</p>
4	<p>Used to determine whether color or monochrome video circuitry is installed. The video/floppy card installed in the Z-158 computer requires that this switch be ON. Settings are as follows:</p> <p>ON = Color video circuitry installed (factory setting) OFF = Monochrome video circuitry installed</p> <p><b>NOTE:</b> This switch should be OFF if an optional video card, such as the Z-329 video card, is installed. Installation of the Z-329 card does not require removal of the video/floppy card.</p>

---

## Configuration

---

### Jumpers

The jumper connection at J201 is permanently closed and cannot be altered. Jumpers J202 and J203 (Table 2-3) specify the size of the system RAM, and jumpers J204 and J205 address and enable the parallel port (Table 2-4). Jumper J206 should be left OFF (unjumpered) for RFI reasons.

**Table 2-3: Jumpers J202 and J203 Settings**

---

JUMPER	DEFINITION
J202/J203	Used to configure the CPU/memory card's memory banks in terms of how many 256-kilobit devices are installed. Settings are as follows:  ON/ON = No banks contain 256-kilobit RAM devices ON/OFF = Bank 0 contains 256-kilobit RAM devices OFF/ON = Banks 0 and 1 contains 256-kilobit RAM devices OFF/OFF = All banks contain 256-kilobit RAM devices

---

**NOTE:** Each bank must contain only one type of RAM device, and must be completely filled before devices may be installed in the next bank. If 256-kilobit devices are used with 64-kilobit devices, they must be installed in the lower-most banks.

---

**Table 2-4: Jumpers J204, J205, and J206 Settings**

---

JUMPER	DEFINTION
J204	Used to determine the base parallel port address. Settings are as follows:  Pins 1 and 2 jumpered = 378H Pins 2 and 3 jumpered = 278H
J205	Used to enable the parallel port. Settings are as follows:  ON = Parallel port enabled OFF = Parallel port disabled
J206	Should be OFF (unjumpered) for RFI reasons.

---

## Theory of Operation

This chapter explains the operation of the CPU/memory card in terms of a simplified block diagram. For more information on the operation of this card, refer to Chapter 4, "Detailed Circuit Description."

### Block Diagram

A simplified block diagram of the CPU/memory card is shown in Figure 3-1. This diagram represents only the major functions of the CPU/memory card. Refer to this block diagram while reading the descriptions in the following paragraphs.

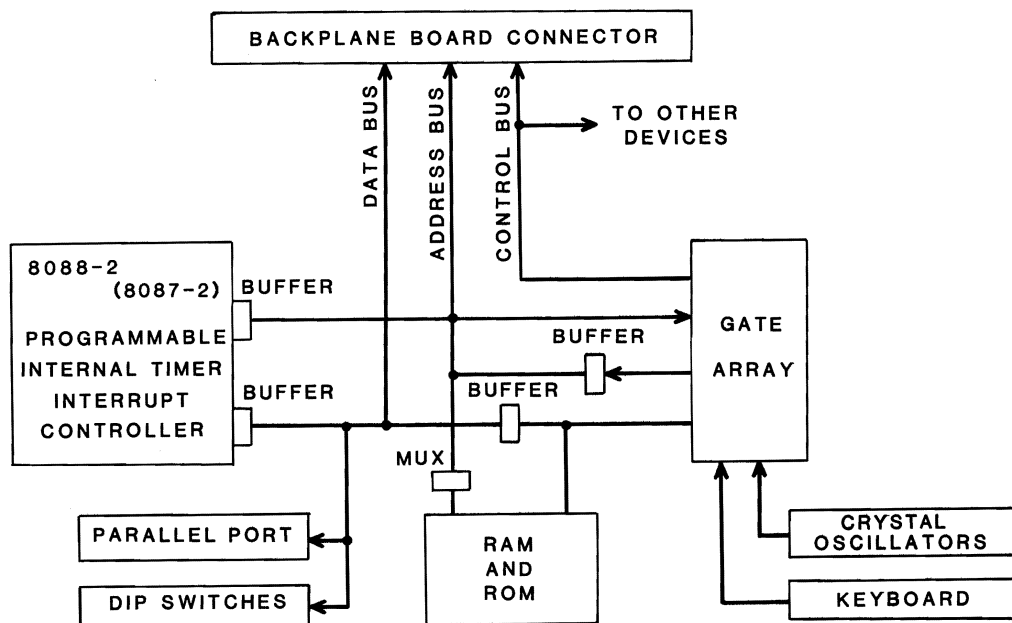


Figure 3-1: CPU/Memory Card Block Diagram

**Backplane Board Connector** -- The backplane board connector is used to connect the CPU/memory card to the rest of the system. This connector also supplies the CPU/memory card with power from the power supply.

## Theory of Operation

---

**Busses** -- The 8088-2 microprocessor and gate array communicate with the other devices on the CPU/memory card and with the rest of the computer system using three busses. Many of the transmissions over these busses are multiplexed.

The address bus is used to locate the specific device or memory byte that the microprocessor is seeking. The data bus is used to exchange information between the microprocessor and the rest of the computer system. The control bus carries commands to the rest of the system hardware. This bus carries the read and write signals for the system, the interrupts from the system, and various other timing and control signals.

The buffers shown on the busses are used to control the direction of the data flow and buffer the data so that several devices can be driven by each bus. The multiplexer on the address bus is used to multiplex the address information for the three banks of RAM on the CPU/memory card.

**8088-2 Microprocessor** -- The 8088-2 microprocessor is the heart of the computer system. It receives inputs from the peripherals and keyboard, calculates all solutions, and controls the computer system. This microprocessor is manufactured using HMOS technology and has 16-bit internal architecture. It uses an 8-bit data bus to communicate with other devices.

**NOTE:** This device is capable of operating at clock frequencies of up to 8 MHz and is therefore not interchangeable with an 8088 microprocessor.

**Optional 8087-2 Numeric Data Coprocessor** -- The 8087-2 coprocessor may be installed on the CPU/memory card as an option. The 8087-2 is an ALU processor which contains expanded 80-bit registers, an expanded instruction set, and internal logic designed to perform complex mathematical operations with fewer program instructions than would be required by the 8088-2.

**NOTE:** This device is capable of operating at clock frequencies of up to 8 MHz and is therefore not interchangeable with an 8087 numeric data coprocessor.

**Programmable Interval Timer** -- The programmable interval timer contains three independent counters which are used by the computer system to generate specific time delays. These time delays are used to update the real-time clock, refresh the dynamic RAM, and provide the frequencies used to generate tones for the speaker.



## Theory of Operation

---

**Interrupt Controller** -- The interrupt controller is used to prioritize the system interrupts. This device accepts up to eight interrupt inputs from other parts of the system, assigns each input a priority for processing, and then directs the microprocessor to the next instruction in the interrupt routine.

**Gate Array** -- The gate array on the CPU/memory card replaces many of the buffers, latches, and other devices normally required in CPU circuitry. Primarily, the gate array performs signal generation, including all control signals and clock frequencies. This device also receives all keyboard interrupts for the microprocessor and performs DMA functions. The gate array is described in more detail in Chapter 4.

**Parallel Port** -- The CPU/memory card is equipped with a Centronics-compatible, 25-pin, D-type connector to provide access to a parallel printer or other parallel device. The parallel port can be disabled by removing a jumper. Also, the port's address can be changed to a second fixed address by moving a jumper.

**DIP Switches** -- The DIP switches on the CPU/memory card inform the microprocessor of the system configuration. This allows the microprocessor to utilize the installed hardware correctly and efficiently. For more information on configuring the CPU/memory card, refer to Chapter 2.

**RAM** -- The CPU/memory card combines CPU circuitry and system RAM onto a single card. This is possible because of the gate array, which combines several functions into a single device. The RAM is contained in three banks of 64-kilobit and/or 256-kilobit devices and is expandable from 128K to 640K.

**ROM** -- The 256-kilobit ROM located on the CPU/memory card contains the instructions which control the fundamental operation of the microprocessor. These instructions tell the microprocessor how to load software, read the keyboard, and perform many other functions. The instructions for self-checks at power-up, as well as for more complete diagnostics, are also contained in the ROM.

**Oscillators** -- The microprocessor can operate at either of two clock frequencies, which are selected by means of a pushbutton switch. These frequencies are derived from two crystals, with frequencies of 14.31818 MHz and 24.0 MHz, respectively. The selected frequency is divided by 3 in the gate array to provide either 4.77 or 8.0 MHz 33% duty cycle output for the microprocessor.

## **Theory of Operation**

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**Keyboard** -- The keyboard communicates directly with the gate array. This relieves the microprocessor of the responsibility of frequently checking for keyboard entries. When a key is pressed, the gate array sends a system interrupt to the interrupt controller, which then informs the microprocessor.

## Detailed Circuit Description

This chapter describes the operation of the most important components on the CPU/memory card. Refer to the schematics while reading this chapter.

### 8088-2 Microprocessor

The 8088-2 microprocessor used in the CPU/memory card is manufactured using HMOS technology. This device is functionally identical to other 8088-type microprocessors, however, it is capable of operating at much higher clock frequencies. In the Z-158, the microprocessor can be driven at either 4.77 or 8.0 MHz clock frequencies. Figure 4-1 identifies the pinouts of this device, and Table 4-1 identifies and describes each signal.

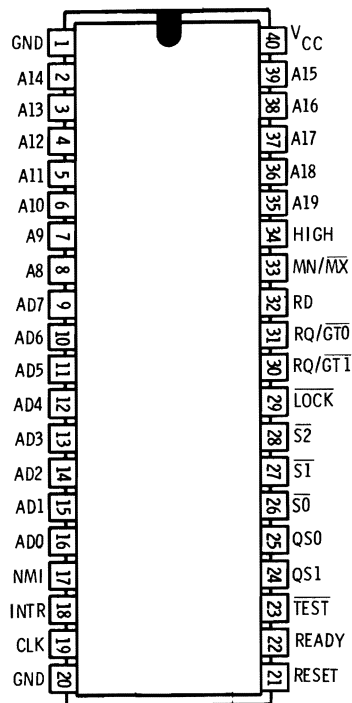


Figure 4-1: 8088-2 Microprocessor Pinouts

## Detailed Circuit Description

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The microprocessor has 16-bit internal architecture for all registers, internal data paths, instruction codes, and the ALU. It communicates with the rest of the computer system using 8-bit data lines. Twenty address outputs provide over 1,000,000 possible memory address locations and 64,000 I/O address locations.

The memory is processed internally by the 8088-2 as 16 segments of 64K each. This is possible because the microprocessor uses two separate registers to store the memory address. A 4-bit register, called the segment register, defines the most significant 4 bits of the address. The lower 16 bits of the address are stored in a separate register.

**Table 4-1: 8088-2 Microprocessor Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	GND	Ground for the 8088-2 microprocessor (U235).
2-8, 39	A8 - A15	Middle-order address lines.
9-16	AD0 - AD7	These signals are used for both the data bus and the first eight bits of the address bus. At the beginning of an instruction cycle, they are used for the low-order address. Later, these signals are used for data (refer to The Instruction Cycle section in this chapter).
17	NMI	Used by the gate array (U248) to inform the microprocessor of a nonmaskable interrupt. A low-to-high transition in this signal will direct the microprocessor to a specific location in the program instructions (refer to the Interrupt Operation section in this chapter).
18	INTR	Used by the interrupt controller (U240) to inform the microprocessor of a maskable interrupt. When the interrupt is acknowledged, the interrupt controller supplies the microprocessor with the address of the programming instructions for the interrupt (refer to the Interrupt Operation section in this chapter).

## Detailed Circuit Description

Table 4-1 (continued): 8088-2 Microprocessor Signals

PIN NUMBER	SIGNAL NAME	DESCRIPTION
19	CLK	The 4.77 MHz or 8.0 MHz clock from the gate array (U248) is connected to the 8088-2 (U235) at this pin. The clock frequency provides the basis for all timing in the microprocessor.
20	GND	Ground for the power supply (pin 40).
21	RESET	This signal originates at the gate array (U248) and causes the 8088-2 (U235) to immediately terminate its present activity and begin the power-up sequence.
22	READY	This signal is an acknowledgment from the addressed memory or I/O device that it will complete the requested data transfer. The READY signal is normally used with low-speed devices which cannot complete a data transfer in one bus cycle.
23	TEST*	This signal is used only when the 8087-2 coprocessor (U234) is installed. A high state during the "wait for test" instruction will place the 8088-2 (U235) in an idle condition until the 8087-2 returns the signal to a low state.
24	QS1	This signal is used to communicate with the 8087-2 coprocessor (U234).
25	QS0	This signal is used to communicate with the 8087-2 coprocessor (U234).
26 - 28	S0* - S2*	These signals are decoded to produce the read and write pulses for the system. Table 4-2 defines the functions of these signals.
29	LOCK*	Not connected in the Z-158.

## Detailed Circuit Description

---

**Table 4-1 (continued): 8088-2 Microprocessor Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
30	RQ*/GT1*	This signal is used by the 8087 coprocessor (U234) to gain control of the busses from the 8088-2 (U235).
31	RQ*/GT0*	Not connected in the Z-158.
32	RD*	Not connected in the Z158.
33	MN/MX*	This pin, which is grounded in the Z-158, informs the microprocessor that it is operating in a maximum system mode.
34	HIGH	This signal is in a high state in the Z-158.
35-38	A16-A19	The high-order addresses or segment addresses.
40	VCC	+5 VDC power supply.

### The Instruction Cycle

The first operation in the instruction cycle is to load the contents of the internal program counter register into the address outputs (AD0 through AD7). The program counter also keeps track of the address of the next instruction stored in memory.

When the address is stable at the output pins, the address is latched into external latches. The output pins are now free to transfer data. The program counter is incremented so that it indicates the location of the next instruction.

After the address is latched, a combination of the S0, S1, and S2 signals is used to generate the appropriate function, such as "read from memory." When this signal occurs, the data from the addressed memory location is received and decoded by the microprocessor. In cases where the instruction is more than one byte long, the cycle is repeated to load the rest of the instruction.

## Detailed Circuit Description

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The rest of the instruction cycle is determined by the content of the instruction. It may involve memory reads or writes, or internal processing which does not generate external signals. Address outputs A8 through A19 are processed the same as AD0 through AD7. Instruction cycles involving I/O devices are identical to operations involving memory, except for the state of signals S0, S1, and S2, as shown in Table 4-2.

**Table 4-2: S0, S1, and S2 Signal Decoding**

S0 STATE	S1 STATE	S2 STATE	FUNCTION
Low	Low	Low	Interrupt acknowledge
Low	Low	High	Read I/O port
Low	High	Low	Write I/O port
Low	High	High	Halt
High	Low	Low	Code access
High	Low	High	Read memory
High	High	Low	Write memory
High	High	High	Idle

### Interrupt Operation

There are two types of interrupts used with the 8088-2. The non-maskable interrupt (NMI) cannot be ignored by the device, while some instructions can tell the microprocessor to ignore maskable interrupts (INTR). In either case, the basic operation of the interrupt is the same.

When a maskable interrupt occurs, the interrupting device sends an 8-bit type number to the interrupt controller (U241), which prioritizes up to eight interrupt inputs at one time. The interrupt controller then sends an INTR signal to microprocessor at pin 18 to notify it of a waiting interrupt.

When the interrupt is acknowledged, the interrupt controller points to the location where the address of the interrupt routine is stored. As many as 64 different devices can be handled by cascading the interrupt controllers.

The microprocessor will then execute the first instruction found at that address. The interrupt program must end with a return command (RET), which causes the 8088-2 to return to the operation which was interrupted.

## Detailed Circuit Description

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If the interrupt is a non-maskable interrupt, the microprocessor is directed to the fixed address 008H. In all cases, a non-maskable interrupt has priority over a maskable interrupt. If both types of interrupts occur at the same time, the non-maskable interrupt will be processed first. Non-maskable interrupts must also end with return (RET) commands.

### System Timing

Figures 4-2 through 4-5 illustrate the timing for memory read, memory write, I/O read, and I/O write operations, respectively. These diagrams represent state changes in the signals listed in Table 4-3.

**Table 4-3: Timing Signal Locations**

LOCATION	SIGNAL
Gate Array	
pin 8	S2*
pin 9	S1*
pin 10	S0*
pin 37	CLKG
U236	
pin 6	ALEB
U244	
pin 1	DT/R*
pins 2 - 9	D0 - D7
pin 19	GM*
U249	
pins 2, 5, 6, 9, 12, 15, 16, 19	A0 - A7
U252	
pin 7	IOR*
pin 16	IOW*
RAM	
	MW*
	MA0 - MA7
	RAS*
	CAS*
U238	
pin 15	GCPU

The four states of each bus cycle are represented by the numbers T1 through T4 on the clock waveform in Figures 4-2 through 4-5. TW represents a wait state.



Detailed Circuit Description

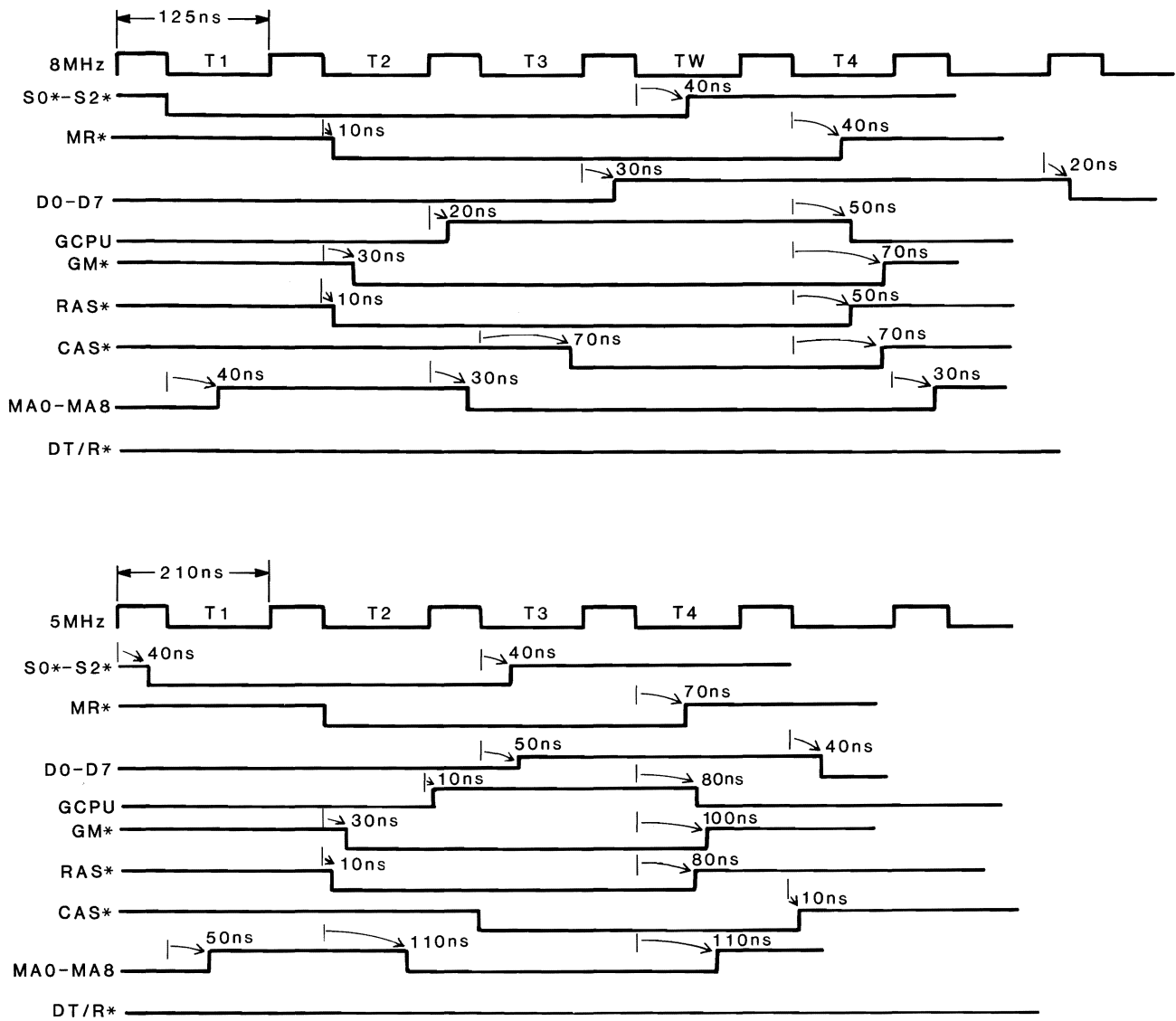
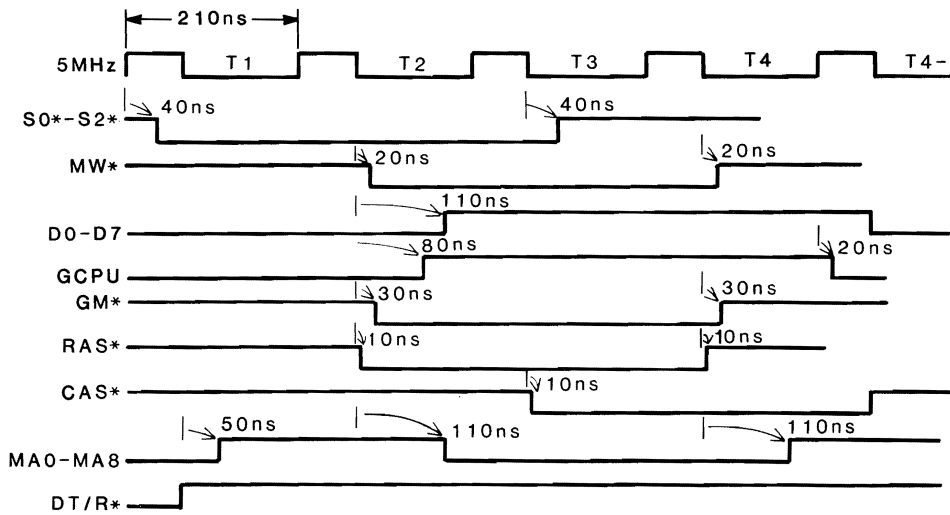
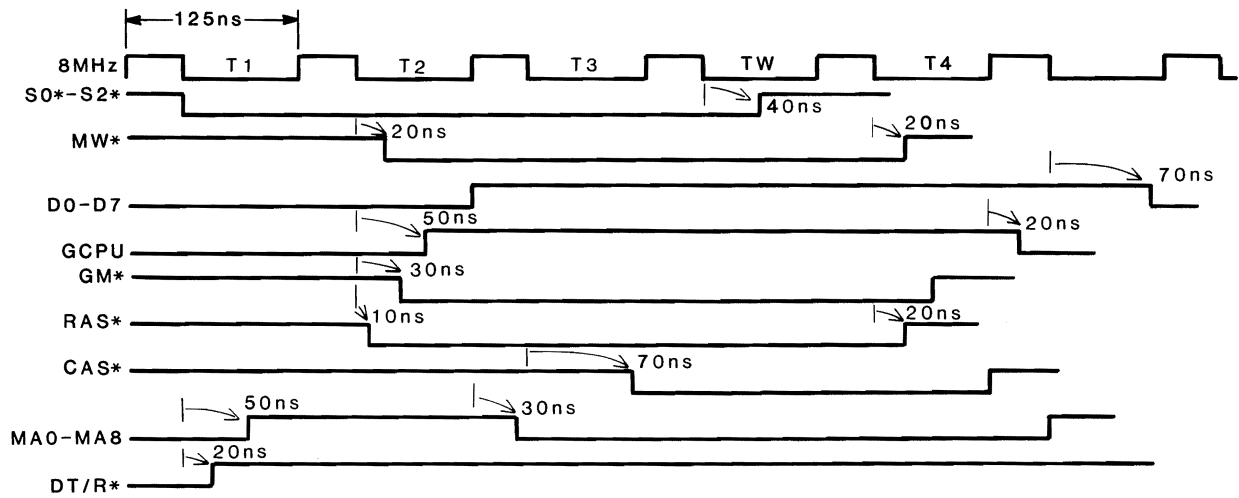


Figure 4-2: Memory Read Timing

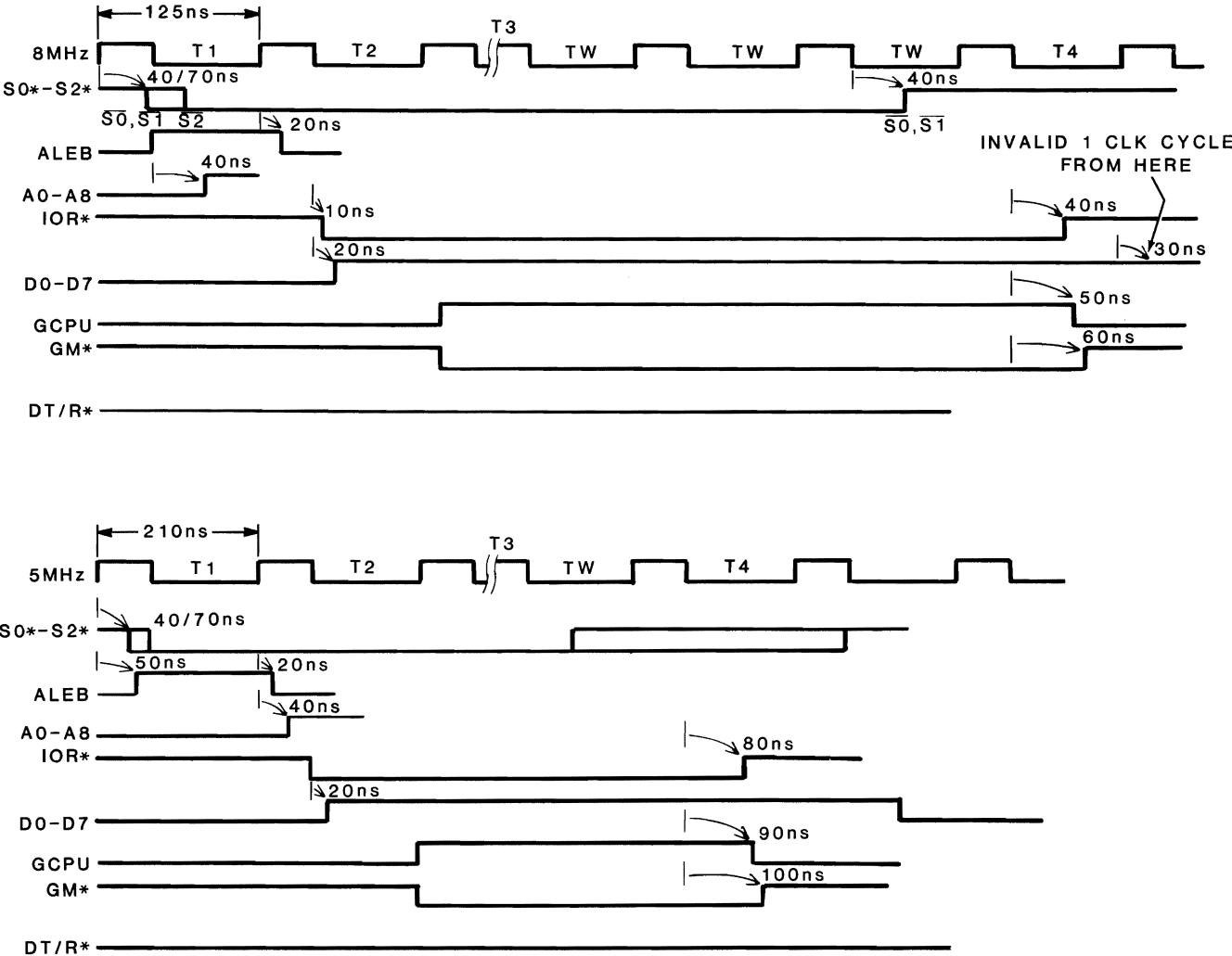
# Detailed Circuit Description



NOTE:  $\overline{MW}$  at RAM

Figure 4-3: Memory Write Timing

# Detailed Circuit Description



**NOTE:** S0\*-S2\* at gate array; IOR\* at U46; A0-A8 at U40; CLKG, ALEB, GM\* , D0-D7, and DT/R\* at U51

Figure 4-4: I/O Read Timing

# Detailed Circuit Description

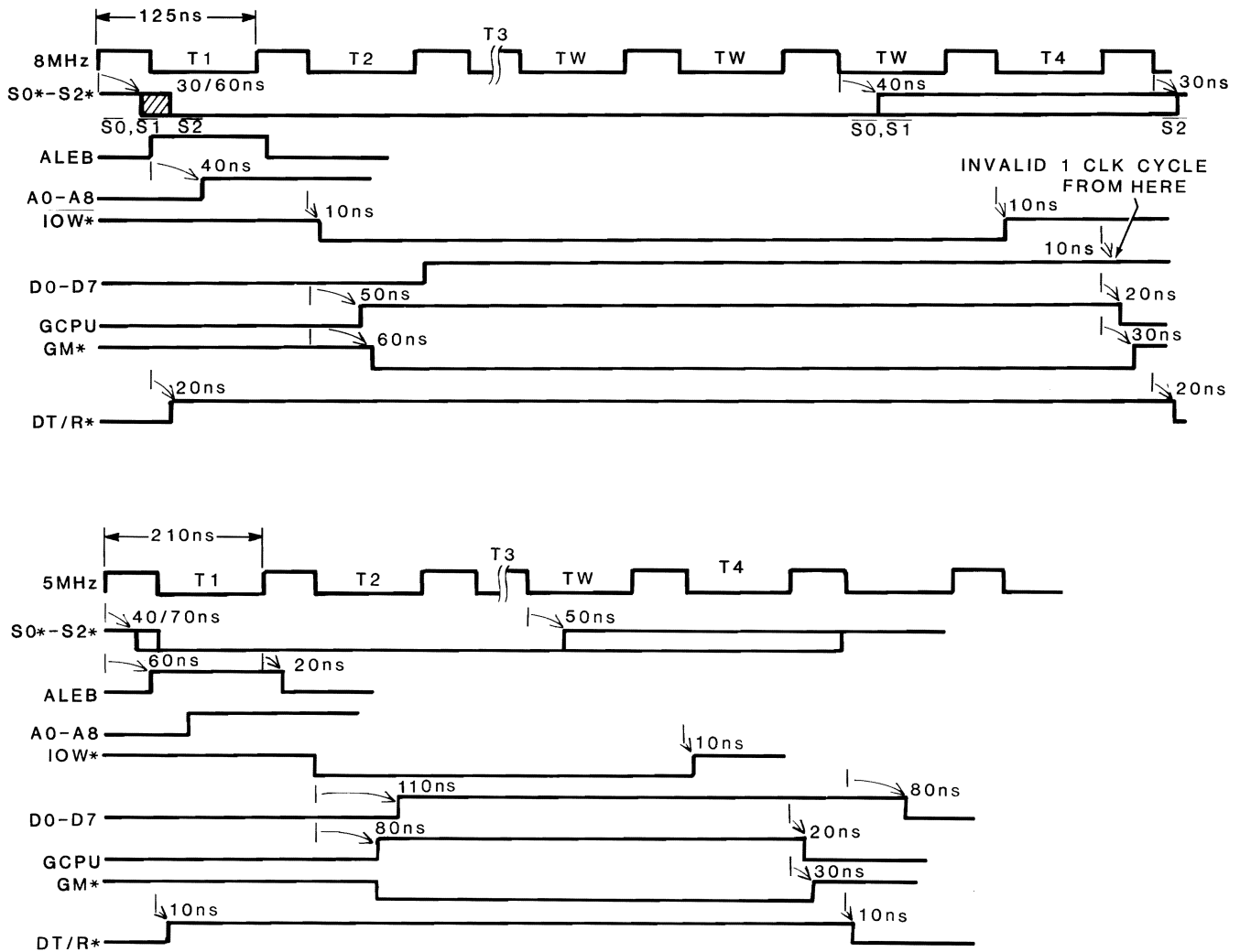


Figure 4-5: I/O Write Timing

## Programmable Interval Timer

The programmable interval timer (U240) contains three independent programmable counters, which are all connected to the TCLK input from the gate array. These counters are used to generate output which may be processed as system interrupts or may cause specific functions to occur.

For example, counter 0 causes the microprocessor to issue a memory refresh signal, counter 1 is used to update the real-time clock, and counter 2 provides frequencies for the speaker. Figure 4-6 identifies the pinouts on the programmable interval timer.

The programmable interval timer can operate in any of several modes, as determined by a control word. These modes are identified in Table 4-4. Table 4-5 identifies the programming codes for this device.

**Table 4-4: Programmable Interval Timer Operating Modes**

MODE NUMBER	DESCRIPTION
0	A terminal value is loaded into the selected counter, which then begins counting from 0. Each time the terminal value is reached, a logic high is sent out at the appropriate output. This signal remains until the terminal value is re-loaded.
1	Same as mode 0 except that the high output is sent only for a fixed time and then returns to low.
2	The incoming clock signal is divided by a predetermined value to generate output pulses.
3	Same as mode 2 except that the outgoing pulse remains high until the next count reaches 1/2 of the starting count.
4	Similar to mode 2 except that the output starts high and goes low when the terminal count is reached.
5	A hardware-triggered strobe; the count begins when a low-to-high transition occurs at one of the gate inputs.

## Detailed Circuit Description

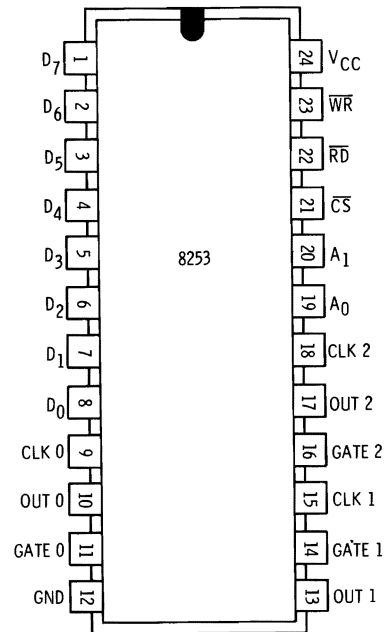


Figure 4-6: Programmable Interval Timer Pinouts

Table 4-5: Programmable Interval Timer Programming Codes

INPUT SIGNALS					FUNCTION
CS*	RD*	WR*	A0	A1	
0	1	0	0	0	Load counter 0
0	1	0	0	1	Load counter 1
0	1	0	1	0	Load counter 2
0	1	0	1	1	Write mode word
0	0	1	0	0	Read counter 0
0	0	1	0	1	Read counter 1
0	0	1	1	0	Read counter 2
0	0	1	1	1	No operation 3-state
1	x	x	x	x	Disabled 3-state
0	1	1	x	x	No-operation 3-state

## Interrupt Controller

The interrupt controller (U241) prioritizes up to eight interrupt signals to the microprocessor, stores an instruction address for each interrupt, and generates a maskable interrupt signal (INT) for the interrupt of highest priority. The microprocessor can tell the interrupt controller to ignore, or mask, all interrupts, or to change the priority of the interrupts. Maskable interrupts are acknowledged by an INTA\* signal from the gate array to the interrupt controller. Figure 4-7 illustrates the pinouts of the interrupt controller.

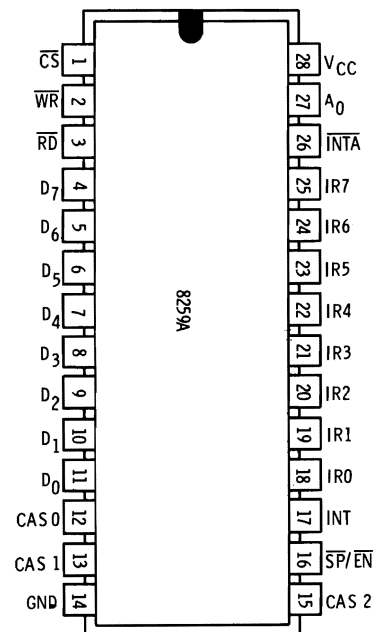


Figure 4-7: Interrupt Controller Pinouts

## Detailed Circuit Description

### Gate Array

The gate array (U248) on the CPU/memory card has several different functions, including signal generation, bus control, and DMA control. Figure 4-8 illustrates the pinouts for the gate array and Table 4-6 identifies the signals.

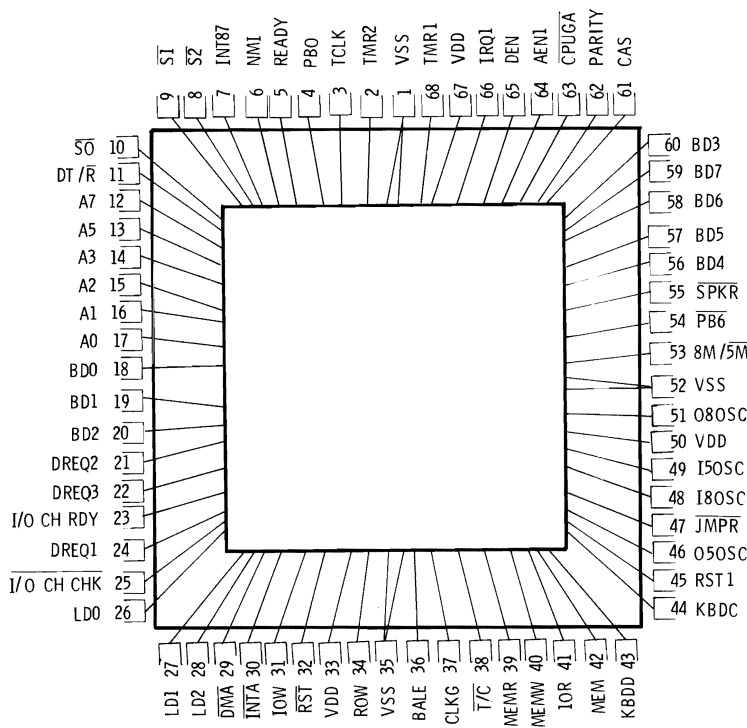


Figure 4-8: Gate Array Pinouts

As signal generator, the gate array provides either a 4.77 MHz or 8.0 MHz 33% duty cycle clock signal (CLKG) to the 8088-2, as determined by the position of switch SW201 (refer to Chapter 2). It also provides synchronization for the RDY signal, and provides the RESET signal at power-up. Additional timing signals (TCLK and CLK) are sent by the gate array to the programmable interval timer (U240), and to the busses to provide synchronization for other devices, by way of the buffer/driver (U246).



## Detailed Circuit Description

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As bus controller, the gate array decodes the status signals (S0, S1, and S2) from the microprocessor to provide the latching and enabling signal for the buffers and address latches, as well as read/write signals for the system memory and I/O devices.

As DMA controller, the gate array can transfer blocks of data from memory to peripheral device, or vice versa, more rapidly and easily than the microprocessor. This is possible because the gate array has its instructions built in, and therefore does not need to decode them before performing a data transfer operation. This also leaves the microprocessor free to perform other operations during data transfer, as long as the busses are not needed.

When a data transfer is to be performed, a DREQ signal is sent to the gate array. The gate array then assumes control of the busses from the microprocessor long enough for the data transfer to be performed under DMA control. Buffers allow the gate array to place its signals on the busses only when the busses are under DMA control. During the data transfer, the gate array generates its own address signals (A0 through A19). Refer to Table 4-6 for a description of all gate array signals.

**Table 4-6: Gate Array Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	VSS	Ground.
2	TMR2	OUT2 from programmable interval timer (U240). Refer to pin 68.
3	TCLK	Clock input to programmable interval timer (U240).
4	PB0	Enables counter 2 of programmable interval timer (U240).
5	READY	Ready signal to 8088-2 (U235) and 8087-2 (U234).
6	NMI	Non-maskable interrupt signal to 8088-2.
7	INT87	INT signal from 8087-2 (U234).

## Detailed Circuit Description

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**Table 4-6 (continued): Gate Array Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
8 - 10	S0* - S2*	S0*, S1*, and S2* signals from 8088-2 (U235) and/or 8087-2 (U234). Refer to Table 4-2.
11	DT/R*	Signal specifying transmit or receive status to data transceiver (U245).
12 - 17	A0 - A3, A5, A7	Address inputs.
18 - 20	BD0 - BD2	Data outputs (refer also to pins 56 - 60).
21 - 22	DREQ2 - DREQ3	Request for DMA channels 2 and 3 (refer also to pin 24).
23	I/O CH RDY	I/O CH ready signal from bus.
24	DREQ1	Request for DMA channel 1 (refer also to pins 21 and 22).
25	I/O CH CHK*	I/O CH check signal from bus.
26 - 28	LD0 - LD2	Signals to load data into 8-bit latches U249, U250 and U255 respectively.
29	DMA*	Signal to enable the outputs of 8-bit latches U249 and U250.
30	INTA*	Interrupt acknowledge signal to interrupt controller U241.
31	IOW	I/O write signal to gate array control (U238) and bus (IOW*), and to decoder (U253).

## Detailed Circuit Description

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**Table 4-6 (continued): Gate Array Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
32	RST*	Reset signal, including keyboard reset (KYBRST*), 8088-2/8087-2 reset (RESET), and the hex D flip-flop (U256) that drives the CPU/memory card LEDs.
33	VDD	+5 VDC.
34	ROW	ROW signal to SB input (pin 1) of quad multiplexers (U228 and U230) and to pin 11 of address decoder (U231).
35	VSS	Ground.
36	BALE	Not connected.
37	CLKG	Clock signal to 8088-2/8087-2 and to buffer/driver (U246).
38	T/C*	This signal when low indicates terminal count during DMA.
39	MEMR	Memory read signal to pin 8 of octal buffer (U252).
40	MEMW	Memory write signal to pin 11 of octal buffer (U252).
41	IOR	I/O read signal to pin 13 of octal buffer (U252).
42	MEM	Indicates memory operation.
43	KBDD	Data signal from keyboard.
44	KBDC	Clock signal from keyboard.

## Detailed Circuit Description

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**Table 4-6 (continued): Gate Array Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
45	RSTI	Used to initiate powerup sequence, based on charging of capacitor (C210) when system is switched on.
46	O5OSC	Connection, with pin 49, to 14.31818 MHz oscillator (Y202).
47	JMPR*	Enables the outputs of drivers so that the settings of DIP switches (SW202) can be read.
48	I8OSC	Connection, with pin 51, to 24.000 MHz oscillator (Y201).
49	I5OSC	Connection, with pin 46, to 14.31818 MHz oscillator (Y202).
50	VDD	+5 VDC.
51	O8OSC	Connection, with pin 48, to 24.000 MHz oscillator (Y201).
52	VSS	Ground.
53	8M/5M*	Input from dual D flip-flop (U254) determining clock frequency based on position of pushbutton switch (SW201).
54	PB6*	Used to disable the keyboard clock.
55	SPKR*	Signal to speaker via connector (P201).
56 - 60	BD3 - BD7	Data outputs (refer also to pins 18 - 20).
61	CAS	Column address strobes to RAM banks 0, 1, and 2.

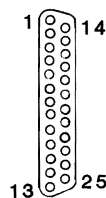
## Detailed Circuit Description

**Table 4-6 (continued): Gate Array Signals**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
62	PARITY	Parity bit for DIN inputs (pin 2) of RAM devices U201, U210, and U219.
63	CPUGA*	Input to enable the I/O addresses in the gate array.
64	AEN1	When high during DMA cycles, this signal disables the address drivers of the CPU.
65	DEN	Data enable signal to DEN input (pin 13) of gate array control (U238).
66	IRQ1	Interrupt request signal to IR1 (pin 19) input of interrupt controller (U241).
67	VDD	+5 VDC.
68	TMR1	OUT1 from programmable interval timer (U240). Refer to pin 2.

### Peripheral Interface

Table 4-7 identifies the signals at the parallel port on the CPU/memory card. Refer to Figure 4-9 for the connector pinouts.



**Figure 4-9: Peripheral Connector Pinouts**

## Detailed Circuit Description

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**Table 4-7: Peripheral Connector Signals**

CONNECTOR PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	STROBE*	Strobe signal to peripheral.
2-9	DATA 0-7	Data to peripheral device.
10	ACK*	Acknowledge from peripheral.
11	BUSY	Busy signal from peripheral.
12	PE	End-of-paper signal from printer.
13	SLCT	Select signal from peripheral.
14	AUTOFDXT*	Auto FDXT signal to peripheral.
15	ERROR*	Error signal from peripheral.
16	INIT*	Initialize signal to peripheral.
17	SLCT IN*	Select-in signal to peripheral.
18-25	GND	Ground.

## Keyboard Communication

The keyboard sends data in serial format to the gate array (KBDAT) along with a clock (KYBCLK). Table 4-8 identifies the keyboard signals. Refer to Figure 4-10 for the connector pinouts.

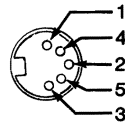


Figure 4-10: Keyboard Connector Pinouts

Table 4-8: Keyboard Signals

CONNECTOR PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	KYBCLK	Timing signal to gate array.
2	KYBDATA	Serial data to gate array.
3	KYBRST*	Reset signal from gate array.
4	KYBGND	Ground.
5	KYBPWR	+5 VDC power supply.

## Troubleshooting

Three hardware/software diagnostic aids are available for troubleshooting the CPU/memory card. These are the disk-based diagnostics (CB-5063-28), the ROM-based diagnostics, and the LEDs on the card and on the backplane board.

The LEDs can be used to isolate failures of major portions of the computer system. The ROM-based diagnostics include the power-up test (performed automatically each time the computer is turned on), and several other tests which can be selected from a menu. The use of these tests is explained in the service guide for Z-150 PC Series computers. The disk-based diagnostics are shipped automatically to service centers and kit customers, and are more thorough than the ROM-based diagnostics.

**NOTE:** Servicing the CPU/memory card with an oscilloscope is difficult. In order to obtain reliable information, it is necessary to write machine language programs that exercise the hardware so that predictable, repeatable results are obtained in desired locations. No such programs are provided in this manual.



## Troubleshooting

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### System Troubleshooting

System troubleshooting using the ROM-based diagnostics is explained in the service guide for Z-150 PC Series computers (860-81-1) and in the Z-150 PC Series Base Unit Service Module (860-136). Refer to these documents, or to the disk-based diagnostics documentation (CB-5063-28), for more information.

Whenever troubleshooting the system, first check the power supply LEDs on the backplane board (Figure 5-1). All of these LEDs should be lit when the computer is on. An unlit -5 VDC LED indicates a backplane board failure. Any other unlit LED indicates a power supply failure.

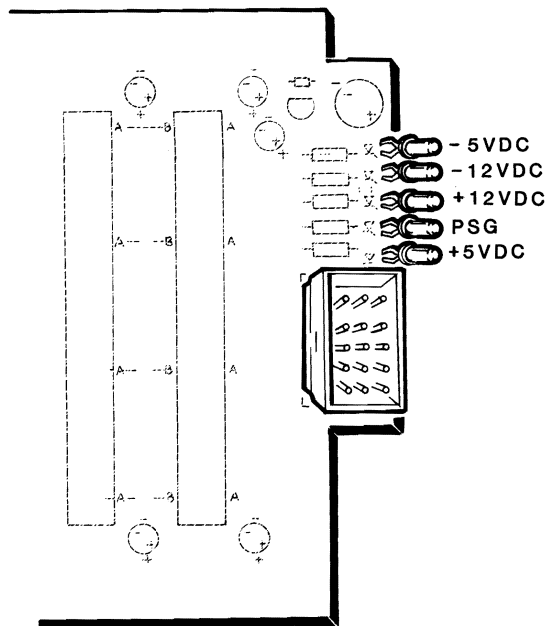


Figure 5-1: Backplane Board Power Supply LEDs

## CPU/Memory Card Troubleshooting

Because the circuitry on the CPU/memory card is essential to the operation of the entire computer, a failure on this card will usually prevent all computer operation. Many CPU/memory card problems will be indicated as error message, or by a lit LED. Table 5-1 at the end of this chapter contains a list of system error messages with their interpretations and corrections.

**NOTE:** If replacement of the gate array device is necessary, use the correct IC extractor (part number HE-490-230).

The CPU/memory card LEDs are shown in Figure 5-2. Five of the six LEDs on the CPU/memory card correspond to specific sections of the system circuitry: CPU, ROM, RAM, interrupt, and disk controller. These LEDs should light immediately when the system is powered up, and then go out sequentially as the self-tests are completed. The sixth LED (RDY) will go out when an operating system is loaded into the RAM.

A lit LED on the CPU/memory card means that there is a problem in the corresponding part of the system circuitry. When this occurs, always check for loose connectors or improper card configuration first. Refer to the service guide for Z-150 PC Series computers for a detailed diagnostic procedure.

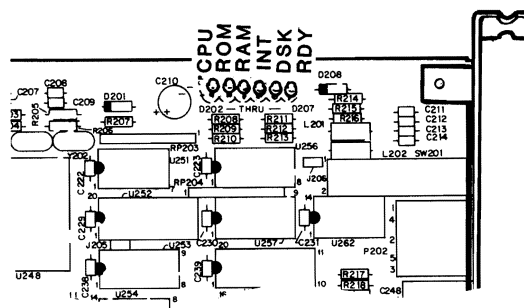


Figure 5-2: CPU/Memory Card LEDs

## Troubleshooting

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**Table 5-1: Error Messages**

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+++ ERROR: CPU failure! +++  
+++ ERROR: ROM checksum failure! +++

When either of these messages occur, the CPU circuitry has a fault. Replace the CPU/memory card.

+++ ERROR: RAM failure! Address:XXXX:YYYY, Bit: n, Chip UXXX +++  
+++ ERROR: Parity hardware failure! Address:XXXX:YYYY, Chip UXXX +++  
+++ ERROR: Parity failure! Address: XXXX:YYYY, Chip: UXXX +++

These messages indicate that the CPU is unable to read from or write to RAM or video memory. This may be caused by improper configuration of the DIP switches or jumpers. Refer to Chapter 2 and make sure that the appropriate DIP switches and jumpers are correctly set for the amount of memory installed in the computer.

If the chip number displayed is a 200 number, such as U227, the failure is on the CPU/memory card. If the chip number is a 300 number, the failure is on the video/floppy card. Replace the IC indicated in the message.

+++ ERROR: Timer Interrupt failure! +++

This error message indicates the possible failure of the interrupt control and/or timer logic in the CPU circuitry. Refer to Chapter 2 and make sure all DIP switches and jumpers are correctly set for the options that are connected to the computer. Also make sure all optional boards are set up properly. If that does not correct the problem, replace the CPU/memory card.

+++ ERROR: Invalid/No keyboard code received! +++

Normally this message is caused by the keyboard being unplugged. If the keyboard is plugged in, the problem may be in the keyboard or keyboard cable. Replace the keyboard and/or keyboard cable.

+++DISK ERROR: Drive not ready! +++

These error messages are usually caused when the system attempts to boot the operating system from the disk and no disk is in the disk drive. This may also be caused by a faulty disk or faulty disk controller circuitry. Make sure there is a disk in the drive, that it is inserted correctly, and that the drive latch is closed. If a disk is properly inserted in the drive, try another disk or try booting from the other disk drive.

No system

This message occurs when a disk does not contain an operating system. Make sure the disk is inserted properly and that it contains a valid operating system.

**Table 5-1 (continued): Error Messages**

---

+++ DISK ERROR: Bad disk controller! +++

+++ DISK ERROR: DMA overrun error! +++

These error messages usually indicate faulty disk controller circuitry, but may be caused by addressing clashes with boards that are not supplied by Zenith Data Systems. Turn off the power and disconnect the expansion chassis or remove any optional boards that are installed.

+++ DISK ERROR: Sector not found! +++

+++ DISK ERROR: CRC error! +++

+++ DISK ERROR: Invalid address mark detected! +++

These messages happen when booting the operating system from a disk. They can be the result of using a damaged disk, one that does not have the operating system on it, or from a faulty disk drive. You can usually correct this condition by using another disk. If this problem continues, try booting from the other disk drive.

+++ DISK ERROR: Seek failure! +++

This error message indicates that the computer cannot read the disk and/or cannot read track 0. This error can be caused by a damaged disk or by a failure of the disk controller circuitry. Replace the disk or try the other disk drive. If the problem still persists, replace the video/floppy card.

#### DEVICE ERROR

This message occurs only during the disk read test of the ROM-based tests. When it occurs, it indicates that the computer is unable to read the disk. Make sure that a disk is correctly installed in the drive and that the drive is closed. If a disk is installed properly, this message indicates the failure of either the disk drive or the disk controller circuitry. Try the same disk in the other disk drive. If the problem persists, replace the video/floppy card.

## Parts List

This chapter contains a component view of the CPU/memory card (part numbers HE-181-5445, HE-181-5857, and HE-181-5601) and the related parts list. Refer to Figure 6-1 for the locations of the parts described in this chapter. Table 6-1 lists all of these parts.

These cards are identical except in the arrangement of their RAM devices. Card HE-181-5445 contains two banks (0 and 1) of 64-kilobit RAM devices. Card HE-181-5857 contains one bank (bank 0) of 256-kilobit RAM devices. Card HE-181-5601 contains 1 bank (bank 0) of 256-kilobit RAM devices, and 1 bank (bank 1) of 64-kilobit RAM devices. Other RAM arrangements are also possible on these cards, as explained in Chapter 2, "Configuration."

**CAUTION:** Many ICs are electrostatic-sensitive and can be damaged by static electricity if they are handled improperly. When you remove an IC or card from its mounting or from its protective packing, do not lay it down or let go of it until it is installed in the computer. Also, when you need to bend the leads of an IC, hold the device in one hand and place your other hand on the work surface before touching the IC to the work surface. This will equalize the static charges between you, the IC, and the work surface.

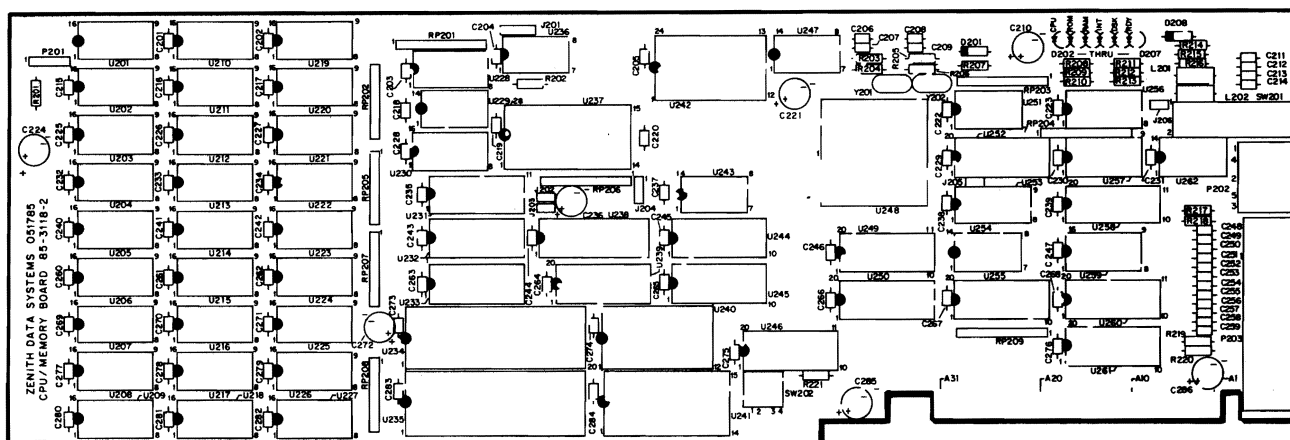


Figure 6-1: CPU/Memory Card Component Layout

## Parts List

---

**Table 6-1: CPU/Memory Card Parts List**


---

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
<b>Capacitors</b>		
C201	HE-21-811	Capacitor, ceramic, 0.33 uF
C202	HE-21-811	Capacitor, ceramic, 0.33 uF
C203	HE-21-786	Capacitor, ceramic, 0.1 uF
C204	HE-21-786	Capacitor, ceramic, 0.1 uF
C205	HE-21-786	Capacitor, ceramic, 0.1 uF
C206	(not used)	
C207	HE-21-707	Capacitor, ceramic, 15 pF
C208	(not used)	
C209	HE-21-707	Capacitor, ceramic, 15 pF
C210	HE-25-820-1	Capacitor, electrolytic, 10 uF, 10 VDC
C211	HE-21-761	Capacitor, ceramic, .01 uF
C212	(not used)	
C213	HE-21-711	Capacitor, ceramic, 470 pF
C214	(not used)	
C215	HE-21-811	Capacitor, ceramic, 0.33 uF
C216	HE-21-811	Capacitor, ceramic, 0.33 uF
C217	HE-21-811	Capacitor, ceramic, 0.33 uF
C218	HE-21-786	Capacitor, ceramic, 0.1 uF
C219	HE-21-786	Capacitor, ceramic, 0.1 uF
C220	HE-21-786	Capacitor, ceramic, 0.1 uF
C221	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
C222	HE-21-786	Capacitor, ceramic, 0.1 uF
C223	HE-21-786	Capacitor, ceramic, 0.1 uF
C224	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
C225	HE-21-811	Capacitor, ceramic, 0.33 uF
C226	HE-21-811	Capacitor, ceramic, 0.33 uF
C227	HE-21-811	Capacitor, ceramic, 0.33 uF
C228	HE-21-786	Capacitor, ceramic, 0.1 uF
C229	HE-21-786	Capacitor, ceramic, 0.1 uF
C230	HE-21-786	Capacitor, ceramic, 0.1 uF

## Parts List

Table 6-1 (continued): CPU/Memory Card Parts List

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
C231	HE-21-786	Capacitor, ceramic, 0.1 uF
C232	HE-21-811	Capacitor, ceramic, 0.33 uF
C233	HE-21-811	Capacitor, ceramic, 0.33 uF
C234	HE-21-811	Capacitor, ceramic, 0.33 uF
C235	HE-21-786	Capacitor, ceramic, 0.1 uF
C236	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
C237	HE-21-786	Capacitor, ceramic, 0.1 uF
C238	HE-21-786	Capacitor, ceramic, 0.1 uF
C239	HE-21-786	Capacitor, ceramic, 0.1 uF
C240	HE-21-811	Capacitor, ceramic, 0.33 uF
C241	HE-21-811	Capacitor, ceramic, 0.33 uF
C242	HE-21-811	Capacitor, ceramic, 0.33 uF
C243	HE-21-786	Capacitor, ceramic, 0.1 uF
C244	HE-21-786	Capacitor, ceramic, 0.1 uF
C245	HE-21-786	Capacitor, ceramic, 0.1 uF
C246	HE-21-786	Capacitor, ceramic, 0.1 uF
C247	HE-21-786	Capacitor, ceramic, 0.1 uF
C248	HE-21-763	Capacitor, ceramic, 330 pF
C249	HE-21-763	Capacitor, ceramic, 330 pF
C250	HE-21-763	Capacitor, ceramic, 330 pF
C251	HE-21-763	Capacitor, ceramic, 330 pF
C252	HE-21-763	Capacitor, ceramic, 330 pF
C253	HE-21-763	Capacitor, ceramic, 330 pF
C254	HE-21-763	Capacitor, ceramic, 330 pF
C255	HE-21-763	Capacitor, ceramic, 330 pF
C256	HE-21-763	Capacitor, ceramic, 330 pF
C257	HE-21-763	Capacitor, ceramic, 330 pF
C258	HE-21-763	Capacitor, ceramic, 330 pF
C259	HE-21-763	Capacitor, ceramic, 330 pF
C260	HE-21-811	Capacitor, ceramic, 0.33 uF
C261	HE-21-811	Capacitor, ceramic, 0.33 uF
C262	HE-21-811	Capacitor, ceramic, 0.33 uF
C263	HE-21-786	Capacitor, ceramic, 0.1 uF
C264	HE-21-786	Capacitor, ceramic, 0.1 uF
C265	HE-21-786	Capacitor, ceramic, 0.1 uF

## Parts List

Table 6-1 (continued): CPU/Memory Card Parts List

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
C266	HE-21-786	Capacitor, ceramic, 0.1 uF
C267	HE-21-786	Capacitor, ceramic, 0.1 uF
C268	HE-21-786	Capacitor, ceramic, 0.1 uF
C269	HE-21-811	Capacitor, ceramic, 0.33 uF
C270	HE-21-811	Capacitor, ceramic, 0.33 uF
C271	HE-21-811	Capacitor, ceramic, 0.33 uF
C272	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
C273	HE-21-786	Capacitor, ceramic, 0.1 uF
C274	HE-21-786	Capacitor, ceramic, 0.1 uF
C275	HE-21-786	Capacitor, ceramic, 0.1 uF
C276	HE-21-786	Capacitor, ceramic, 0.1 uF
C277	HE-21-811	Capacitor, ceramic, 0.33 uF
C278	HE-21-811	Capacitor, ceramic, 0.33 uF
C279	HE-21-811	Capacitor, ceramic, 0.33 uF
C280	HE-21-811	Capacitor, ceramic, 0.33 uF
C281	HE-21-811	Capacitor, ceramic, 0.33 uF
C282	HE-21-811	Capacitor, ceramic, 0.33 uF
C283	HE-21-786	Capacitor, ceramic, 0.1 uF
C284	HE-21-786	Capacitor, ceramic, 0.1 uF
C285	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
C286	HE-25-915	Capacitor, electrolytic, 47 uF, 16 VDC
Cxxx	HE-25-820	Capacitor, electrolytic, 10 uF, 10 VDC
Cxxx	HE-21-17	Capacitor, ceramic, 270 pF
Cxxx	HE-21-17	Capacitor, ceramic, 270 pF
Cxxx	HE-21-17	Capacitor, ceramic, 270 pF
Cxxx	HE-21-807	Capacitor, ceramic, 47 pF
Cxxx	HE-21-807	Capacitor, ceramic, 47 pF

### Diodes

D201	HE-56-56	Diode
D202	HE-412-654	LED, red
D203	HE-412-654	LED, red
D204	HE-412-654	LED, red
D205	HE-412-654	LED, red
D206	HE-412-654	LED, red
D207	HE-412-654	LED, red
D208	HE-56-56	Diode



## Parts List

Table 6-1 (continued): CPU/Memory Card Parts List

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
<b>Chokes</b>		
L201	HE-475-39	RF core
L202	HE-475-39	RF core
Lxxx	HE-475-39	RF core
Lxxx	HE-475-39	RF core
<b>Resistors</b>		
R201	HE-6-330	33 ohm
R202	HE-6-270-12	27 ohm
R203	HE-6-225-12	2.2 Megohm
R204	(not used)	
R205	HE-6-515-12	5.1 Megohm
R206	(not used)	
R207	HE-6-104-12	100 kohm
R208	HE-6-561-12	560 ohm
R209	HE-6-561-12	560 ohm
R210	HE-6-561-12	560 ohm
R211	HE-6-561-12	560 ohm
R212	HE-6-561-12	560 ohm
R213	HE-6-561-12	560 ohm
R214	HE-6-912-12	9.1 kohm
R215	HE-6-103-12	10 kohm
R216	HE-6-151-12	150 ohm
R217	HE-6-472-12	4.7 kohm
R218	HE-6-472-12	4.7 kohm
R219	HE-6-472-12	4.7 kohm
R220	HE-6-472-12	4.7 kohm
R221	HE-6-330-12	33 ohm
Rxxx	HE-6-102-12	1 kohm
RP201	HE-9-128	10 kohm resistor pack
RP202	HE-9-126	33 ohm resistor pack
RP203	HE-9-138	1 kohm resistor pack
RP204	HE-9-138	1 kohm resistor pack
RP205	HE-9-126	33 ohm resistor pack

## Parts List

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**Table 6-1 (continued): CPU/Memory Card Parts List**

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
RP206	HE-9-112	4.7 kohm resistor pack
RP207	HE-9-126	33 ohm resistor pack
RP208	HE-9-126	33 ohm resistor pack
RP209	HE-9-138	1 kohm resistor pack

### Switches

SW201	HE-64-683	Pushbutton, 2 position, DPDT
SW202	HE-60-667	DIP switch, 4-section, SPST

### Integrated Circuits

U201	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U202	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U203	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U204	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U205	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U206	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U207	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket

## Parts List

Table 6-1 (continued): CPU/Memory Card Parts List

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
U208	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U209	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U210	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U211	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U212	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U213	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U214	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U215	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U216	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U217	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket
U218	HE-443-970	64-kilobit RAM, 6665
	HE-443-1268	256-kilobit RAM, 41256-15
	HE-434-299	Socket

## Parts List

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**Table 6-1 (continued): CPU/Memory Card Parts List**

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
U219	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U220	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U221	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U222	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U223	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U224	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U225	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U226	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U227	HE-443-970 HE-443-1268 HE-434-299	64-kilobit RAM, 6665 256-kilobit RAM, 41256-15 Socket
U228	HE-443-1120 HE-434-299	Quad multiplexer, 2-input, 74F257 Socket
U229	HE-443-730 HE-434-298	Flip-flop, dual D, 74LS74 Socket

Table 6-1 (continued): CPU/Memory Card Parts List

COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
U230	HE-443-1120 HE-434-299	Quad multiplexer, 2-input, 74F257 Socket
U231	HE-444-361 HE-434-311	Address decoder, logic array, 16L8A Socket
U232	HE-443-837 HE-434-311	8-bit latch, 74LS373 Socket
U233	HE-443-791 HE-434-311	Buffer/driver, 3-state, 74LS244 Socket
U234	HE-443-1168 HE-434-253	Coprocessor, 8087-2 (optional) Socket
U235	HE-443-1187 HE-434-253	Microprocessor, 8088-2 Socket
U236	HE-443-1073 HE-434-298	Quad AND, 2-input, 74ALS08 Socket
U237	HE-444-358 HE-434-312	Monitor ROM, EPROM, 27256-30 Socket
U238	HE-444-360-1 HE-434-368	Gate array control, logic array, 14L8 Socket
U239	HE-443-837 HE-434-311	8-bit latch, 74LS373 Socket
U240	HE-443-1066 HE-434-307	Programmable interval timer, 8253-5 Socket
U241	HE-443-1012 HE-434-312	Interrupt controller, 8259A Socket
U242	HE-443-1027 HE-434-307	RAM, 200 ns, 6116-P4 Socket
U243	HE-443-755 HE-434-298	Hex inverter, 74LS04 Socket

## Parts List

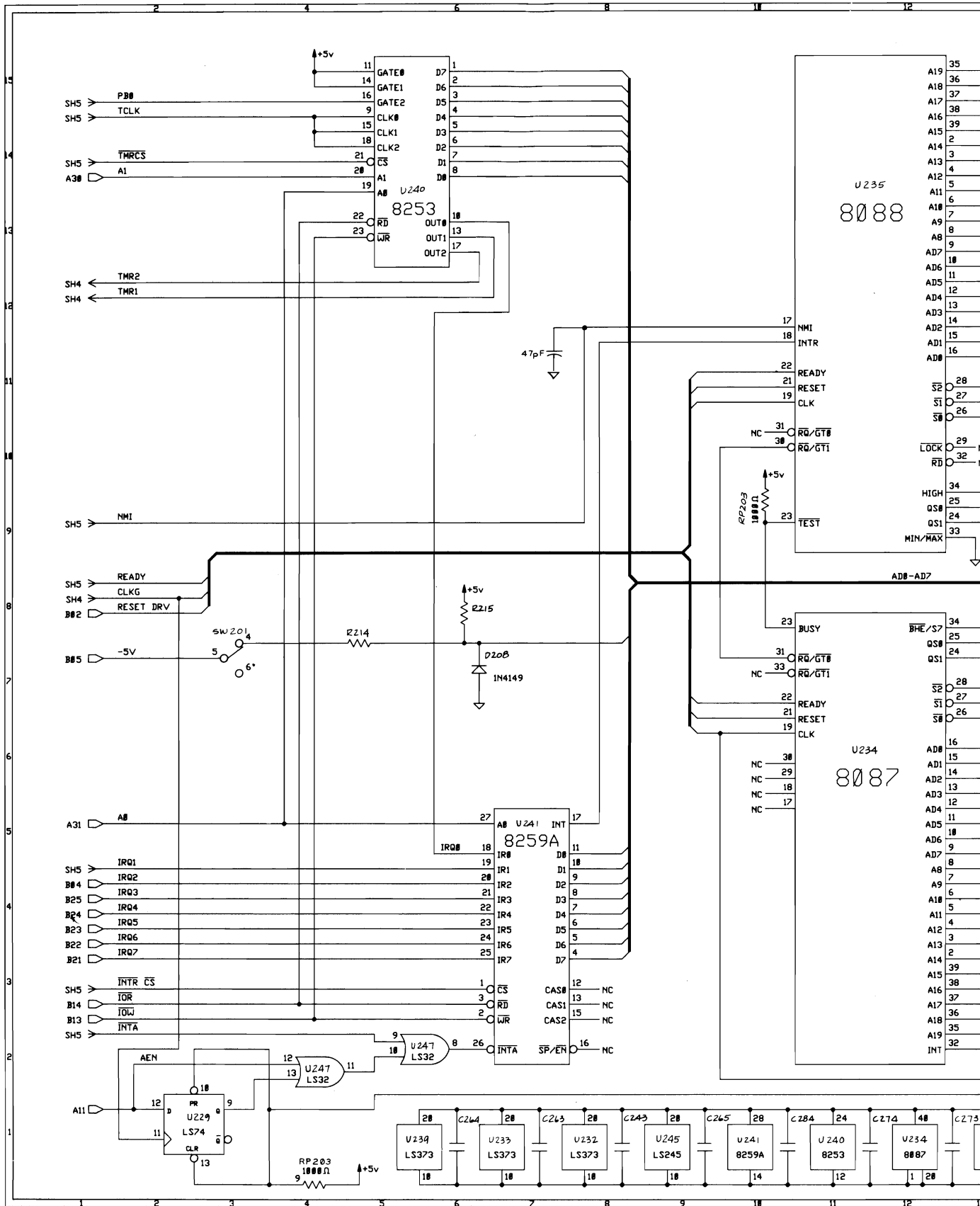
---

**Table 6-1 (continued): CPU/Memory Card Parts List**

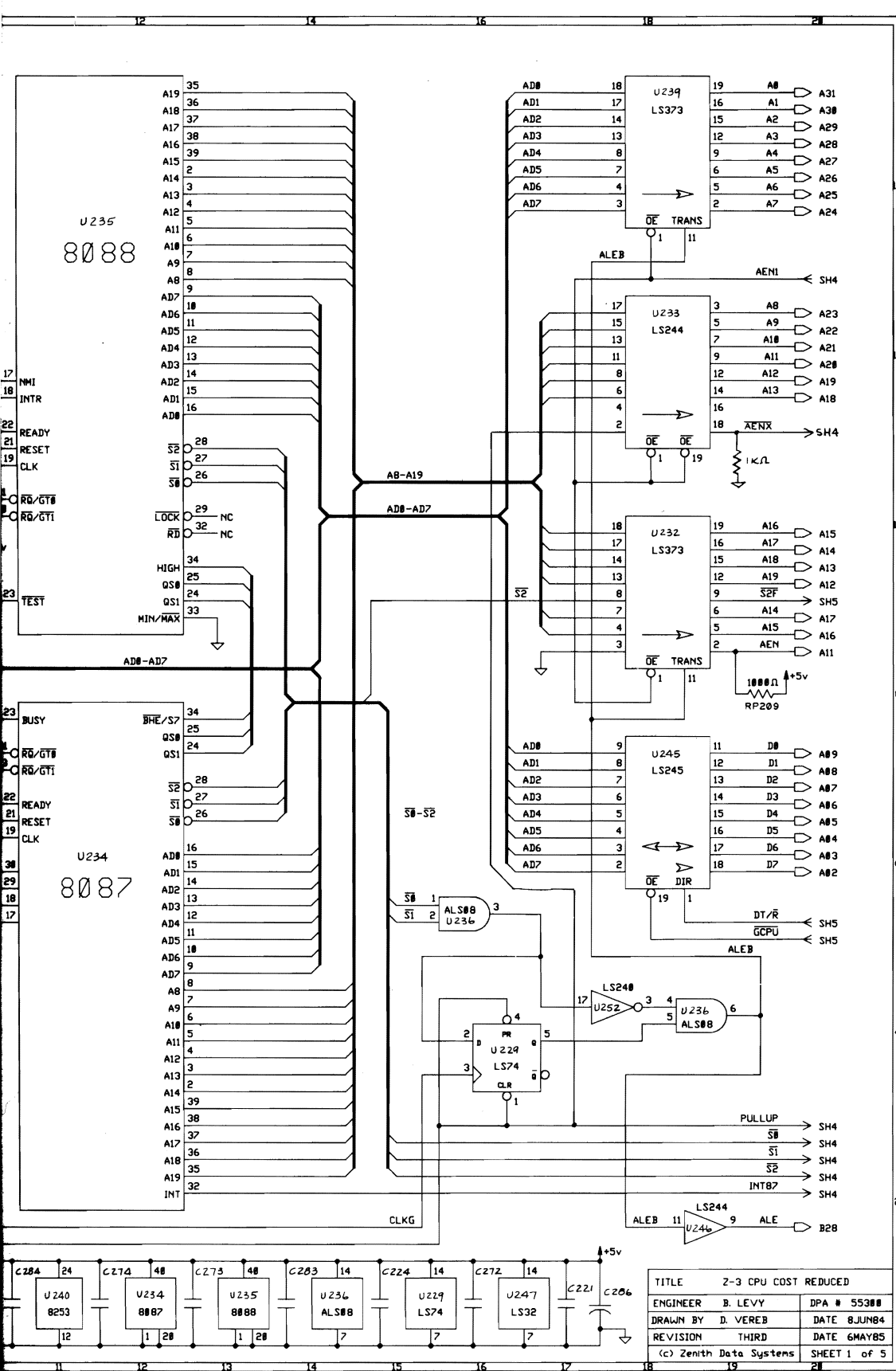
COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
U244	HE-443-885 HE-434-311	Transceiver, 74LS245 Socket
U245	HE-443-885 HE-434-311	Transceiver, 74LS245 Socket
U246	HE-443-791 HE-434-311	Buffer/driver, 3-state, 74LS244 Socket
U247	HE-443-875 HE-434-298	Quad OR, 2-input, 74LS32 Socket
U248	HE-443-321 HE-434-380	Gate array, CPU/RAM, 5320 Socket
U249	HE-443-837 HE-434-322	8-bit latch, 74LS373 Socket
U250	HE-443-837 HE-434-322	8-bit latch, 74LS373 Socket
U251	HE-443-967 HE-434-298	Hex inverter, 7406 Socket
U252	HE-443-754 HE-434-311	Octal buffer, 3-state, 74LS240 Socket
U253	HE-443-782 HE-434-299	Decoder, 74LS155 Socket
U254	HE-443-730 HE-434-298	Flip-flop, dual D, 74LS74 Socket
U255	HE-443-1182 HE-434-311	Octal latch, 74ALS373 Socket
U256	HE-443-879 HE-434-299	Flip-flop, hex D, 74LS174 Socket
U257	HE-443-879 HE-443-299	Flip-flop, hex D, 74LS174 Socket
U258	HE-443-754 HE-434-311	Octal buffer, 3-state, 74LS240 Socket

Table 6-1 (continued): CPU/Memory Card Parts List

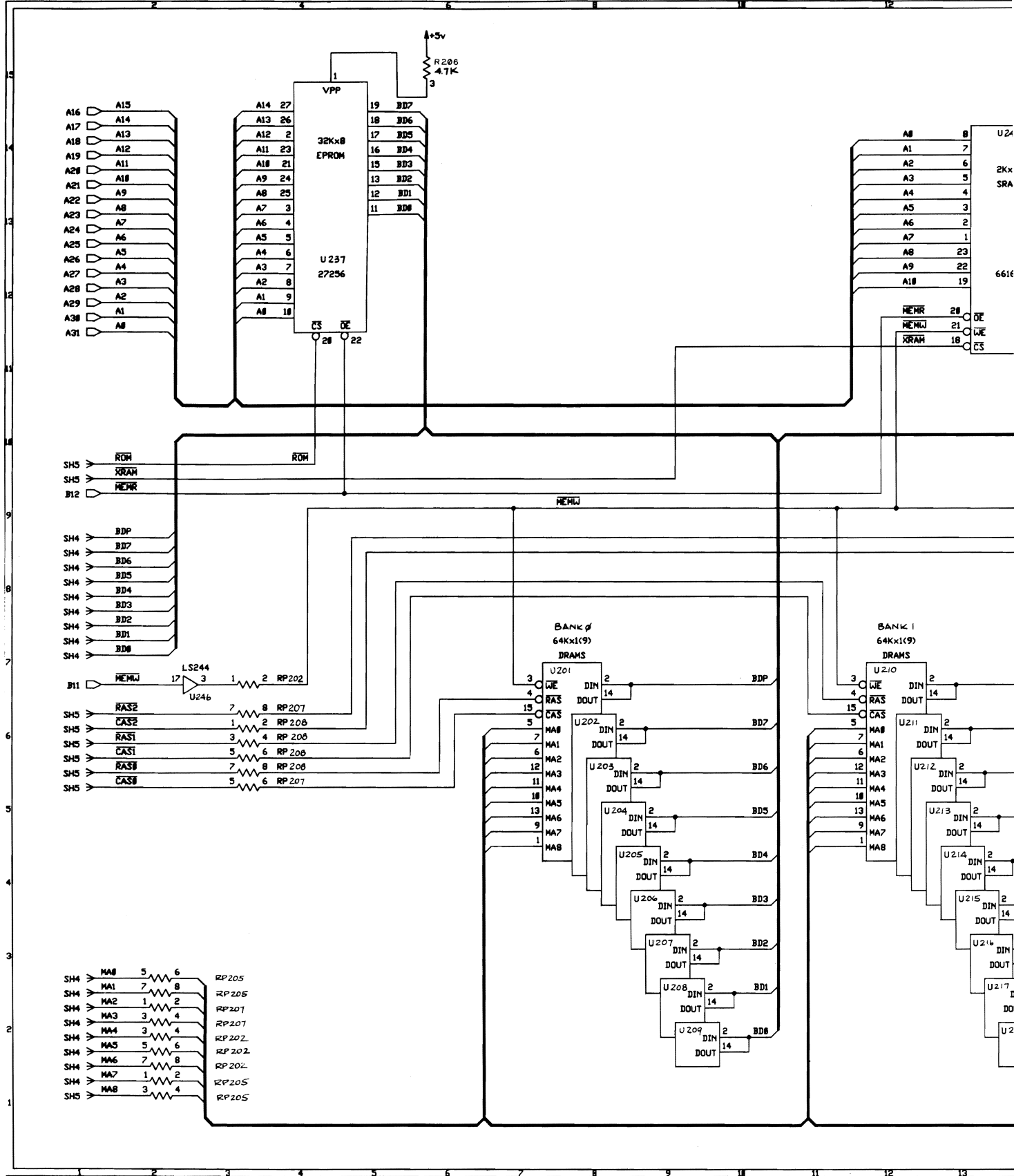
COMPONENT NUMBER	ZDS PART NUMBER	DESCRIPTION
U259	HE-443-857 HE-434-299	Hex buffer, 3-state, 74LS367 Socket
U260	HE-443-791 HE-434-311	Buffer/driver, 3-state, 74LS244 Socket
U261	HE-443-863 HE-434-311	Flip-flop, octal D, 3-state, 74LS374 Socket
U262	HE-443-967 HE-434-298	Hex inverter, 7406 Socket
<b>Oscillators</b>		
Y201	HE-404-681	Crystal oscillator, 24.0 MHz
Y202	HE-404-673	Crystal oscillator, 14.31818 MHz
<b>Jumpers</b>		
J202	HE-432-1171	2-pin, Molex
J203	HE-432-1171	2-pin, Molex
J204	HE-432-1102	3-pin, Molex
J205	HE-432-1171	2-pin, Molex
J206	HE-432-1171	2-pin, Molex
	HE-432-1041	2-connector jumper, Berg
<b>Connectors</b>		
P201	HE-432-1231	4-pin, Molex
P202	HE-432-1495	Keyboard connector
P203	HE-432-1382	25-pin, female connector
<b>Miscellaneous</b>		
	HE-75-873	Insulator
	HE-85-3118-2	Printed circuit board
	HE-204-2876	Bracket, card mounting
	HE-250-1414	Screw, pan head, phillips, 4-40 x .250"
	HE-255-757	Spacer, hex, threaded, 4-40 x 4-40 x .19"

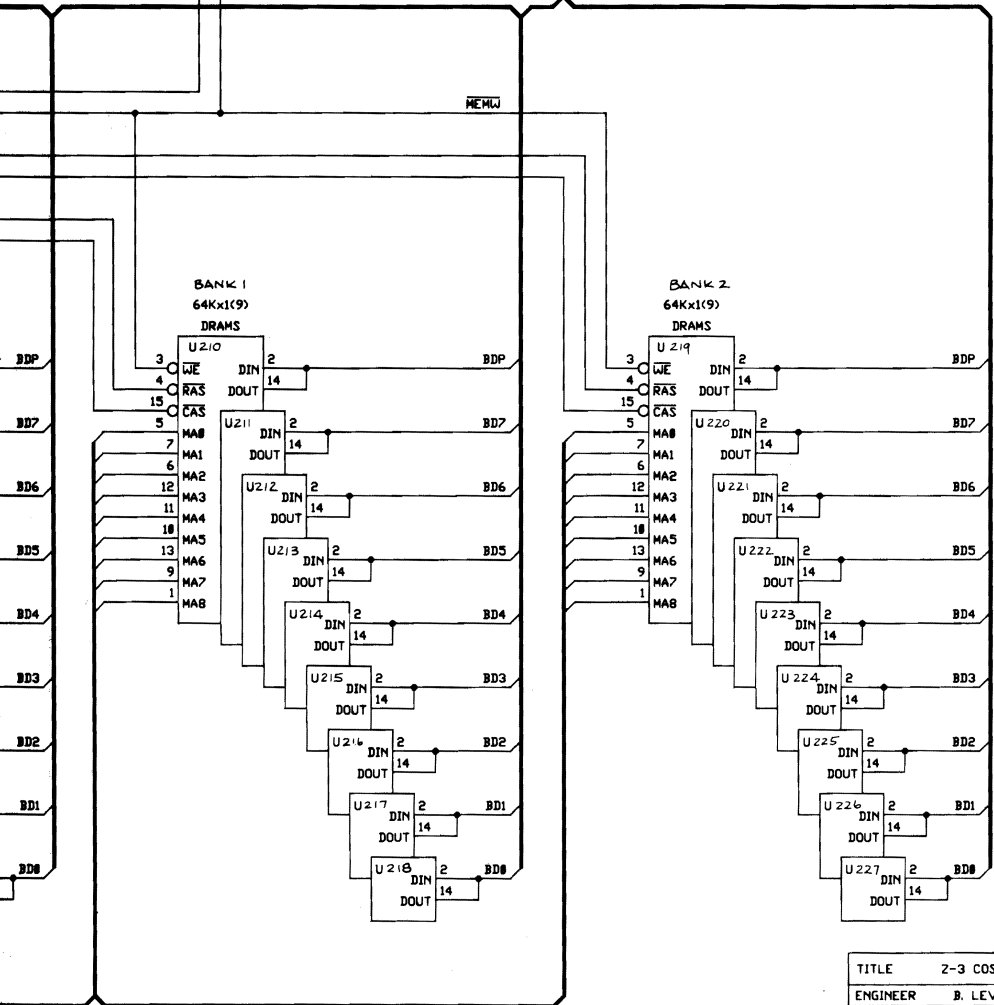
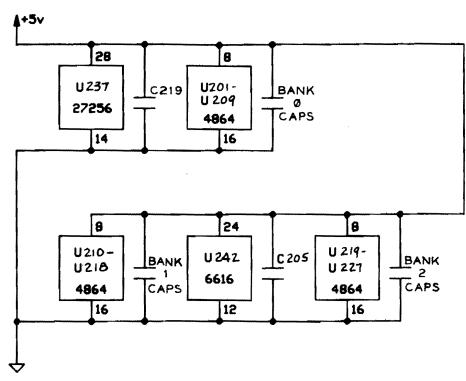
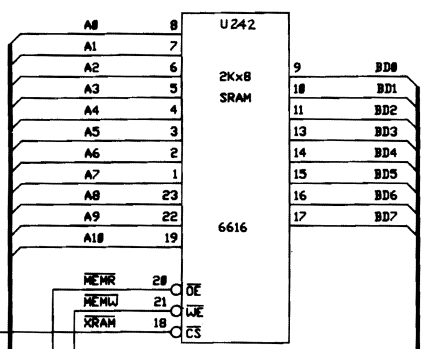




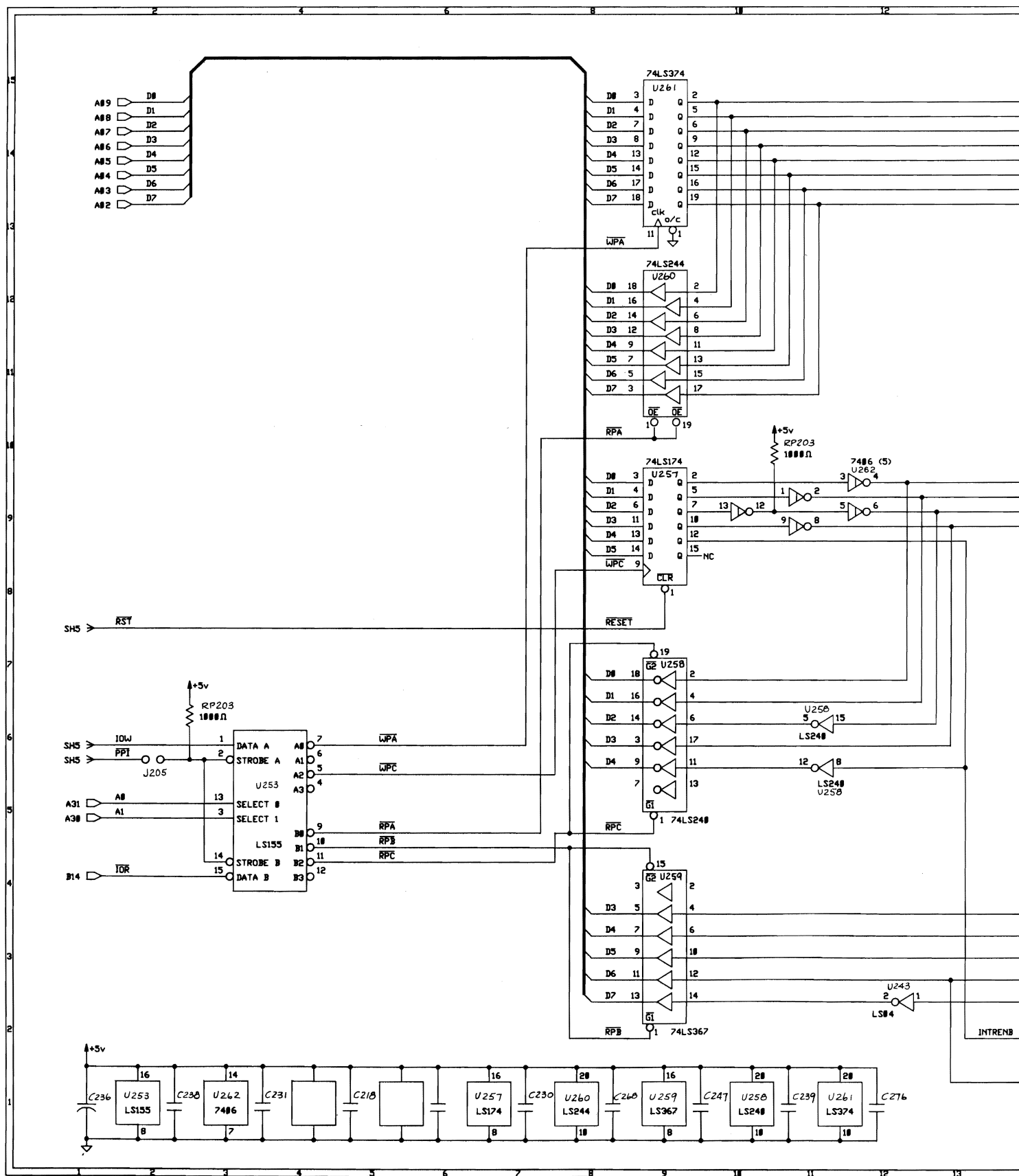


TITLE 2-3 CPU COST REDUCED		
ENGINEER	B. LEVY	DPA # 55388
DRAWN BY	D. VEREB	DATE 8JUN84
REVISION	THIRD	DATE 6MAY85
(c) Zenith Data Systems		SHEET 1 of 5





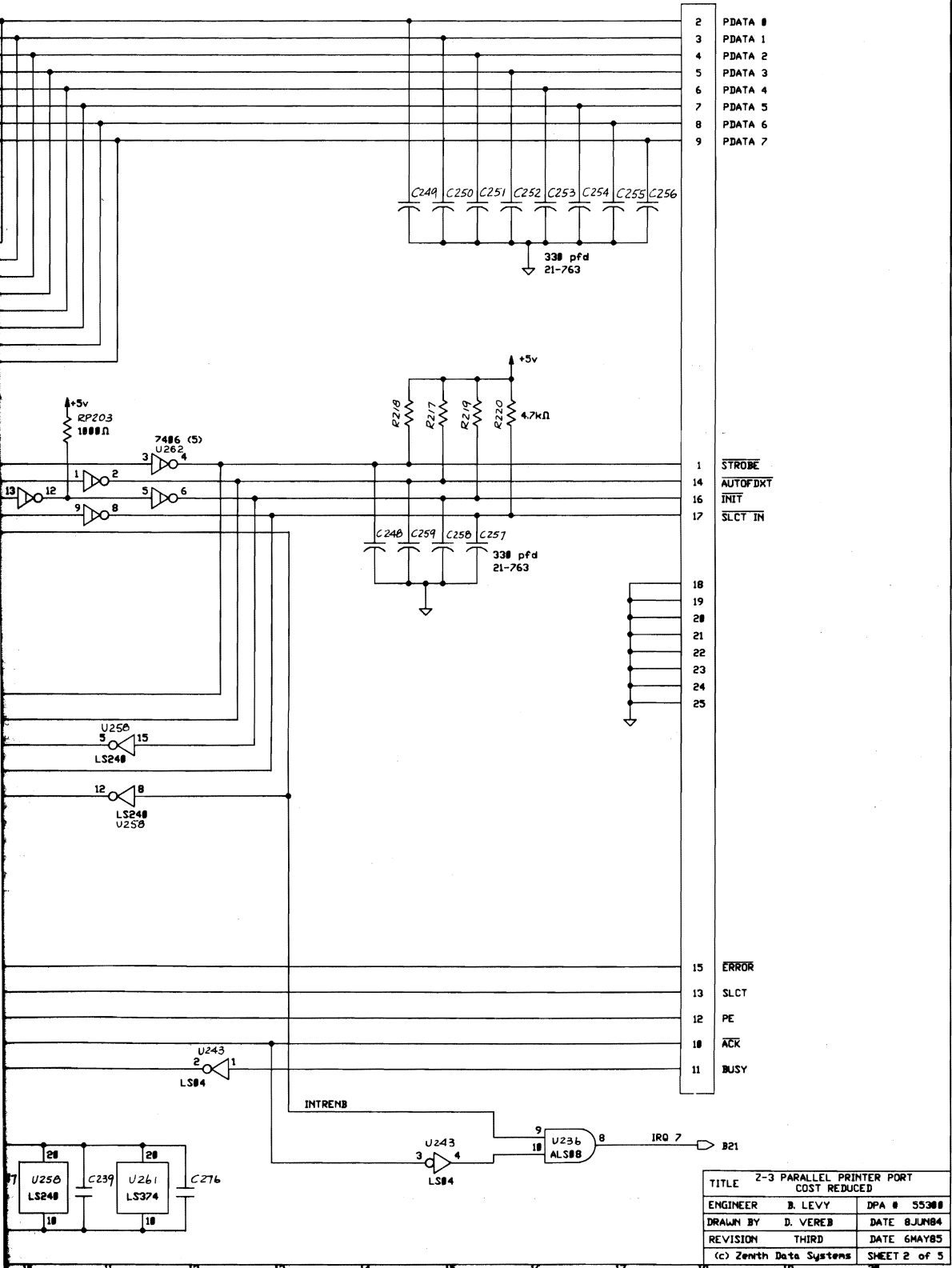
TITLE 2-3 COST REDUCED MEMORY		
ENGINEER	B. LEVY	DPA # 55388
DRAWN BY	D. VEREB	DATE 8JUN84
REVISION	THIRD	DATE 6MAY85
(c) Zenith Data Systems		SHEET 3 of 5



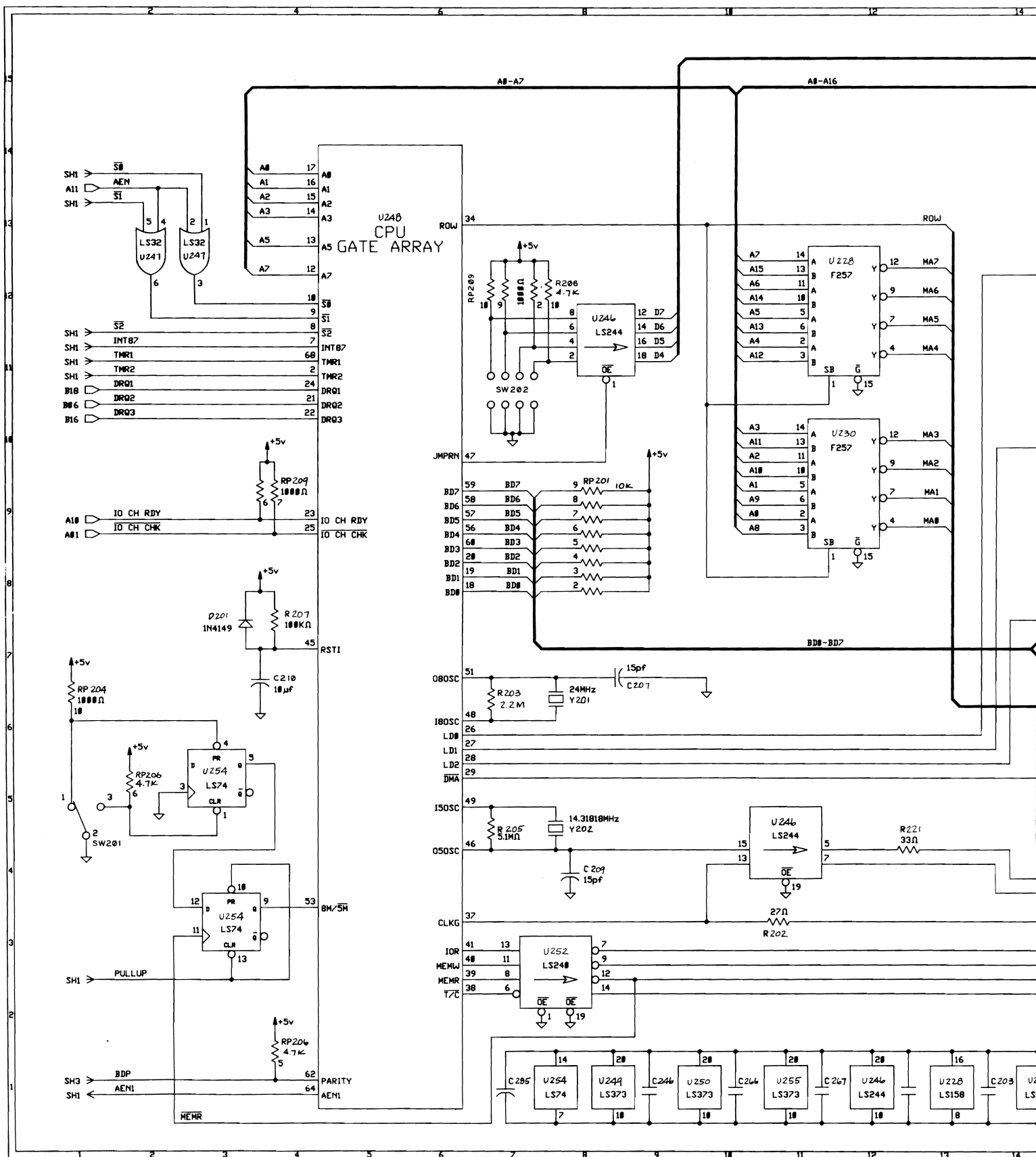
P203

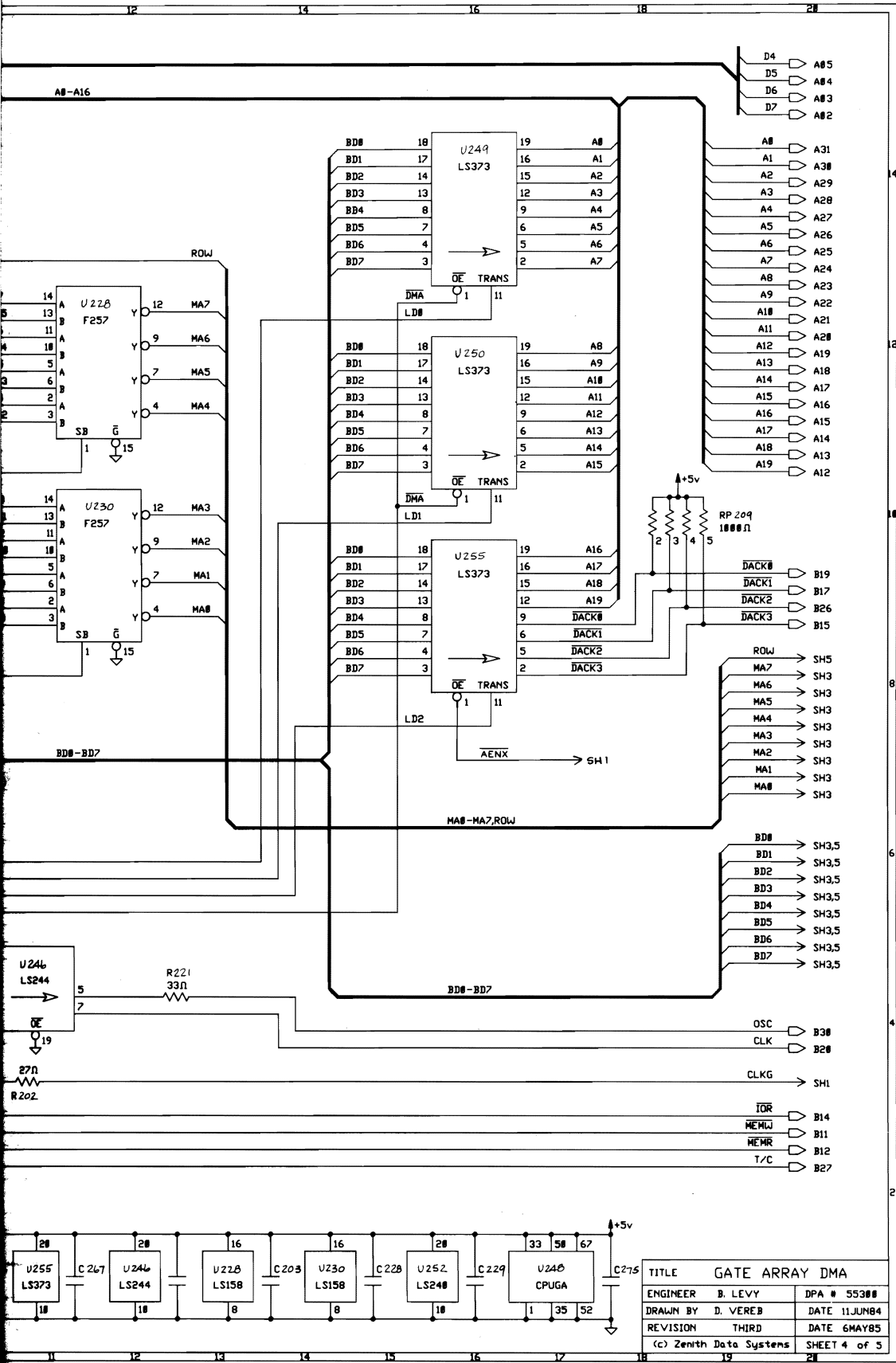
432-1195

25 PIN 'D' CONN.

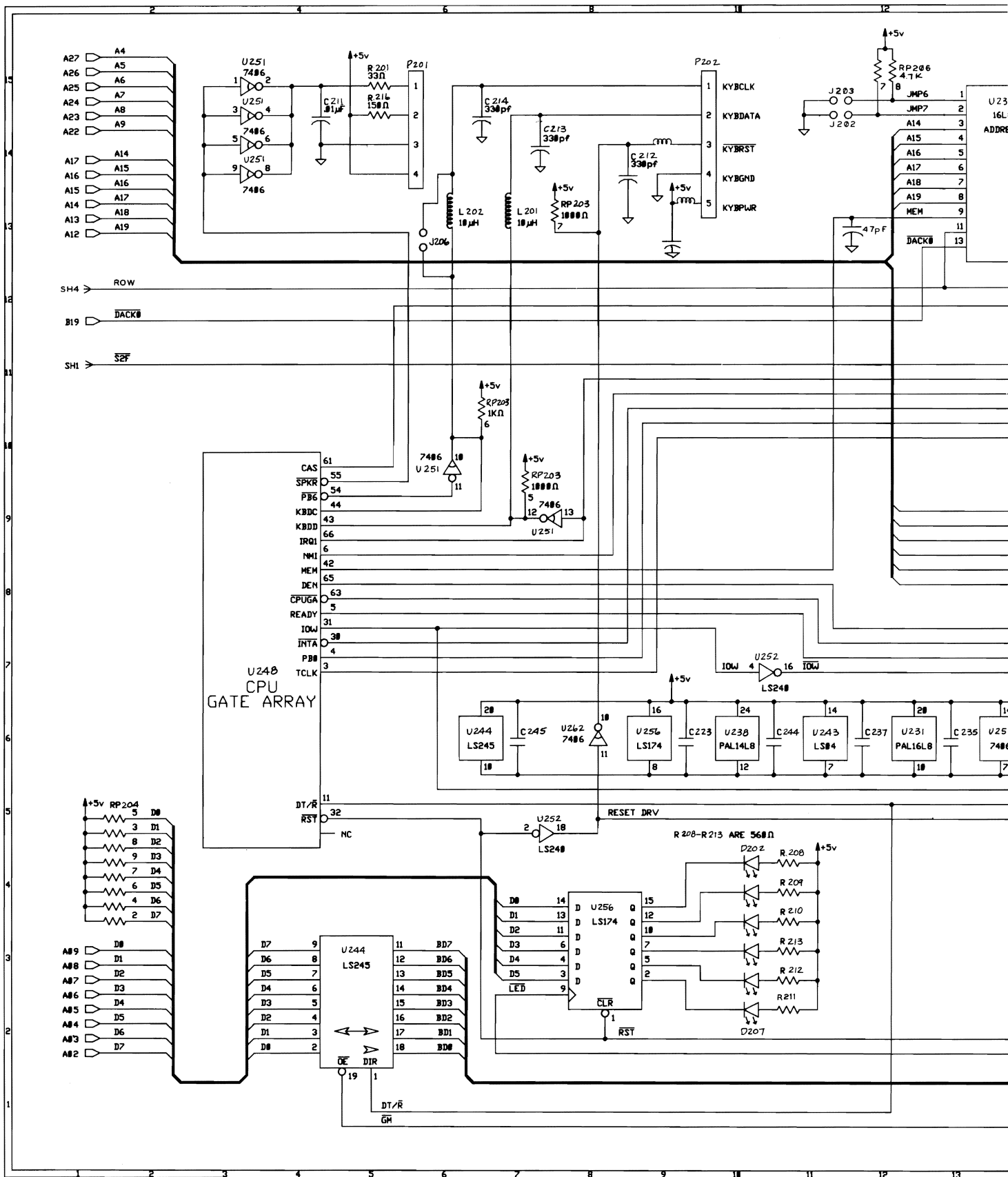


TITLE 2-3 PARALLEL PRINTER PORT COST REDUCED		
ENGINEER	B. LEVY	DPA # 55300
DRAWN BY	D. VEREB	DATE 8JUN84
REVISION	THIRD	DATE 6MAY85
(c) Zenith Data Systems		SHEET 2 of 5

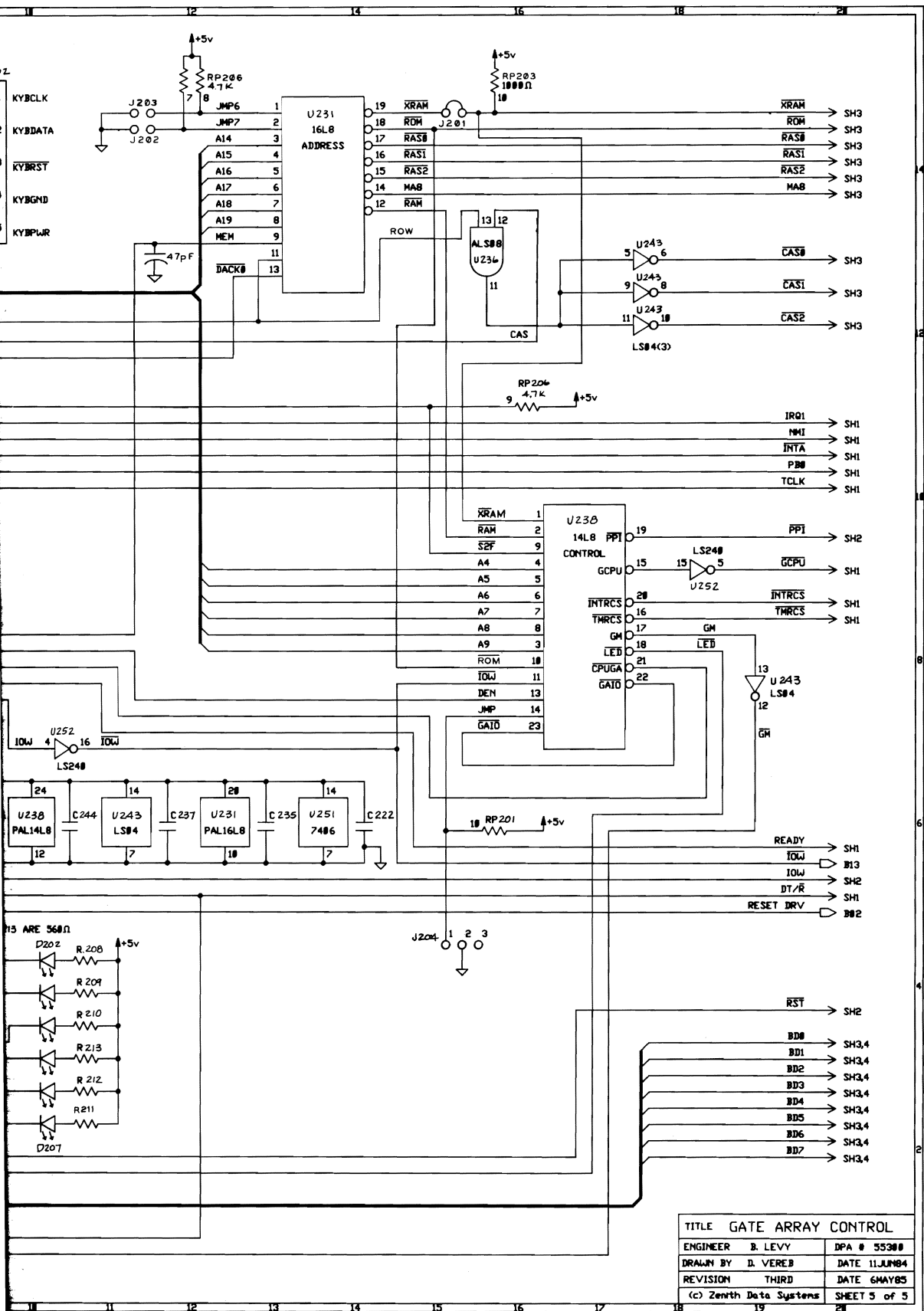




TITLE		GATE ARRAY DMA	
ENGINEER	B. LEVY	DPA #	55300
DRAWN BY	D. VEREB	DATE	11JUN84
REVISION	THIRD	DATE	6MAY85
(c) Zenith Data Systems		SHEET 4 of 5	







**TITLE GATE ARRAY CONTROL**  
 ENGINEER B. LEVY     DPA # 55300  
 DRAWN BY D. VEREB     DATE 11JUN84  
 REVISION THIRD     DATE 6MAY85  
 (c) Zenith Data Systems     SHEET 5 of 5

# SERVICE MANUAL

## Color Video Monitor

ZCM-1490



The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, mark the manual and list the information in the record below.

## Record of Field Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Zenith Data Systems Corporation  
St. Joseph, Michigan 49085

# Warnings and Cautions

## WARNING

Removing or lifting the ground from the AC power source may present a potentially lethal shock hazard. Do not use an AC two-to-three wire adapter plug with this unit.

## WARNING

The CRT anode retains a potentially lethal voltage even when the monitor is turned off. Perform repairs only after the CRT anode has been properly discharged. Refer to Figure 6-1 and the following procedure to discharge the CRT anode:

1. Connect a clip lead or heavy gauge wire to chassis ground.
2. Connect the other end of the lead to the stem of a flat-blade screwdriver that has an insulated handle.
3. Insert the blade of the screwdriver under the rubber insulation that covers the anode lead on the CRT and make contact with the anode terminal. Depending on the amount of charge present on the anode, a distinct snap may be heard as the CRT discharges.

## WARNING

The switch mode power supply contains circuits that generate dangerous high frequency, high amplitude, quasi-square wave signals that present a potentially lethal shock hazard. In the ZCM-1490, this circuitry is located on a separate, exposed circuit board located along the left side of the monitor when viewed from the back. Do not attempt to service the power supply.

## WARNING

To prevent both personal injury and equipment damage, always use an isolation transformer when troubleshooting this monitor.

## CAUTION

Under no circumstances should the original design be modified or altered without permission from Zenith Electronics Corporation. All components should be replaced only with types identical to those in the original circuit, and their physical location, wiring, and lead dress must conform to the original layout upon completion of repairs.

## CAUTION

Some components contain an X in their reference number. For safety reasons, these components must be replaced only with identical components.

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# Chapter 1

## Introduction

The Zenith Data Systems ZCM-1490 is a high-resolution analog RGB color video monitor. This monitor incorporates Zenith's patented flat technology CRT. The ZCM-1490 can be used with a computer video source that supplies an analog RGB color signal having a 31.49 kHz horizontal scan frequency. It can also display information in CGA, EGA, MDA, and Hercules video modes provided that the video source supplying the monitor is capable of delivering these modes as analog RGB color signals at a 31.49 kHz scan frequency. The ZCM-1490 is illustrated in Figure 1-1.

Related publications include the *High-Resolution Analog RGB Color Video Monitor User's Guide* (595-3924-1).

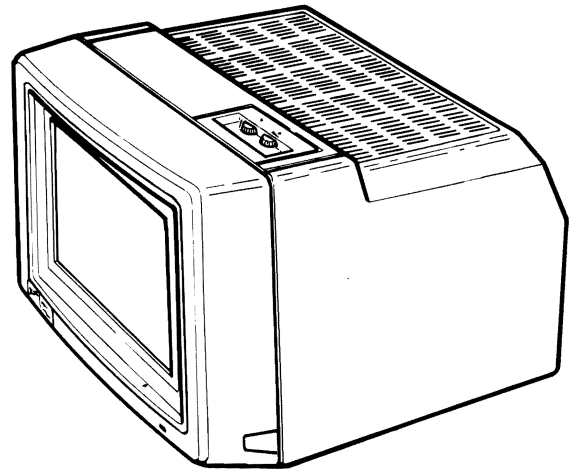


Figure 1-1. ZCM-1490 Color Video Monitor

## Specifications

Power input: .....	90-135/200-265 VAC, 48-62 Hz, switch selectable. Six-foot (1.98 m), 3-wire grounded power cord included.
Video input: .....	Analog RGB video signal, 0-0.714 V peak-to-peak (1V peak-to-peak maximum), 75 ohm resistive.
Sync input	
Horizontal: .....	31.49 kHz, $\pm 1$ kHz, positive TTL, 350-line mode, negative TTL, 400-line mode, negative TTL, 480-line mode.
Vertical: .....	70 Hz, negative TTL, 350-line mode, 70 Hz, positive TTL, 400-line mode, 60 Hz, negative TTL, 480-line mode.
Signal Connector: .....	15-pin subminiature D-type.



CRT: .....	Flat technology, 14-inch, 0.31 mm pitch, regular tint, non-glare.
Display area: .....	10.07 inches (25.6 cm) wide by 7.67 inches (19.5 cm) high (approximate). Display size remains constant with changes in video modes.
Display colors: .....	Infinite array of displayable colors. (The actual number of displayable colors is limited only by the video source supplying the monitor.)
Characters: .....	80 characters × 25 rows.
Character block: .....	8 × 19 (Zenith), 9 × 16 (VGA), 8 × 16 (MCGA), 8 × 14 (EGA), 8 × 16 (CGA, 400-line), 9 × 14 (MDA), 9 × 14 (Hercules).
<b>Active video time</b>	
Horizontal: .....	25.42 μs, all modes.
Vertical: .....	15.4 ms, 640 × 480 (Zenith, VGA), 15.2 ms, 640 × 480 (MCGA), 12.8 ms, 320 × 200 (MCGA), 12.8 ms, 640 × 350 (EGA), 12.8 ms, 320 × 200 (CGA), 12.8 ms, 720 × 350 (MDA), 11.2 ms, 720 × 350 (Hercules).
<b>Inactive video time</b>	
Horizontal: .....	6.36 μs, 640 × 480 (Zenith, VGA), 6.35 μs, 640 × 480 (MCGA), 6.36 μs, 320 × 200 (MCGA), 6.35 μs, 640 × 350 (EGA), 6.35 μs, 320 × 200 (CGA), 6.36 μs, 720 × 350 (MDA), 6.35 μs, 720 × 350 (Hercules).

Vertical: .....	1.44 ms, 640 × 480 (Zenith, VGA), 1.44 ms, 640 × 480 (MCGA), 1.56 ms, 320 × 200 (MCGA), 1.56 ms, 640 × 350 (EGA), 1.56 ms, 320 × 200 (CGA), 1.56 ms, 720 × 350 (MDA), 3.15 ms, 720 × 350 (Hercules).
Resolution: .....	640 dots × 480 lines (Zenith, VGA), 640 dots × 480 lines (MCGA), 320 dots × 200 lines (MCGA), 640 dots × 350 lines (EGA), 320 dots × 200 lines (CGA), 720 dots × 350 lines (MDA), 720 dots × 350 lines (Hercules).
Misconvergence: .....	0.68 mm maximum within display area.
User controls: .....	Power, brightness, contrast, H. CENT (horizontal centering), H. SIZE (horizontal size), V. CENT vertical centering), V. SIZE (vertical size).
Environmental	
Temperature: .....	0° to 40° C (32° to 104° F) operating, -40° to 60° C (-40° to 140° F) storage.
Humidity: .....	10% to 90%, (noncondensing) operating, 0% to 95%, (noncondensing) storage.
Altitude: .....	-1000 to 10,000 feet (-0.3 to 3.05 km) operating, 40,000 feet (12.2 km) maximum (storage).
Dimensions: .....	14.9 inches (37.9 cm) wide by 12.6 inches (32.0 cm) high by 15.5 inches (39.4 cm) deep.
Weight: .....	40 lbs (18.1 kg), approximate.

Zenith Data Systems reserves the right to discontinue products and to change specifications at any time without incorporating these changes into products previously sold.

# Chapter 2 Installation

This chapter provides basic installation and set-up information for the ZCM-1490 analog color video monitor. If further adjustment or servicing information is required, refer to the appropriate chapters which follow.

## Controls and Connections

The various monitor controls and connectors are illustrated in Figures 2-1 and 2-2. Each control and connector is explained individually in the following paragraphs.

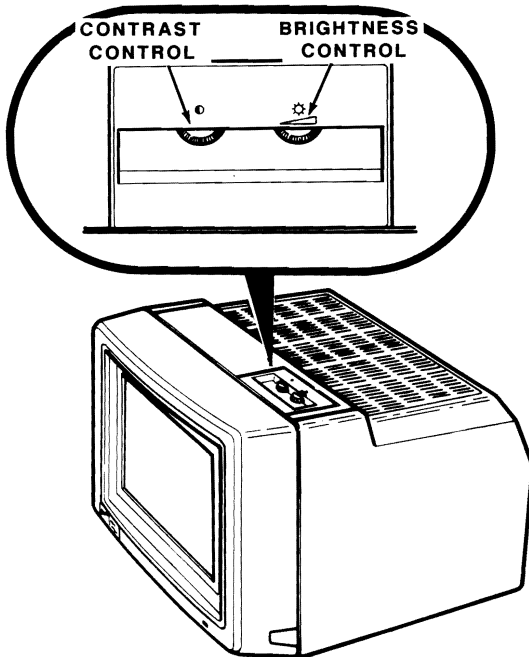


Figure 2-1. ZCM-1490 Front View

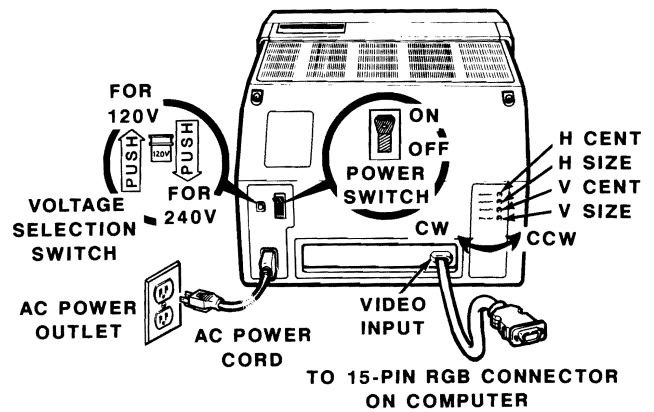


Figure 2-2. ZCM-1490 Rear View

**Power** — The rocker-type power switch located on the rear panel turns the monitor on or off.

**Power-On Indicator** — A green LED located on the front panel lights when power is applied to the monitor.

**Brightness** — The brightness control varies the overall or average intensity of illumination of the display. The average intensity in turn determines the background level in the display.

**Contrast** — The contrast control varies the difference in intensity between the black and the white areas of the display.

**Voltage Selection Switch** — The voltage selection switch configures the monitor for operation from the appropriate AC power source.

**H. CENT** — The horizontal centering control adjusts the left-to-right position of the display within the screen area. To move the display to the left, turn this control counterclockwise. To move the display to the right, turn this control clockwise.

**H. SIZE** — The horizontal size control adjusts the width of the display within the screen area. To increase the display width, turn this control counterclockwise. To reduce the display width, turn this control clockwise.

**V. CENT** — The vertical centering control adjusts the top-to-bottom position of the display within the screen area. To move the display upward, turn this control clockwise. To move the display downward, turn this control counterclockwise.

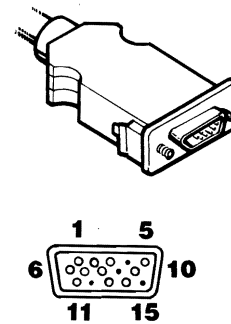
**V. SIZE** — The vertical size control adjusts the height of the display within the screen area. To increase the display height, turn this control counterclockwise. To reduce the display height, turn this control clockwise.

**Power Input Jack** — A 3-pin, grounded-type power jack is located on the rear panel.

**Power Cord** — A 6-foot (1.8 m), 3-wire grounded and shielded power cord supplies power to the monitor.

**Video Input Cable** — A 3.5-foot (1.05 m) cable, terminated with a 15-pin, subminiature D-type connector, supplies video and sync signals to the monitor. The cable is attached to the monitor and is not

detachable. Figure 2-3 illustrates the connector and Table 1-1 lists its pin configuration.



**Figure 2-3. Subminiature D-type Connector**

**Table 2-1. Video Input Cable Pin Functions**

PIN NUMBER	FUNCTION
1	Red video input
2	Green video input
3	Blue video input
4	N/C
5	Reserved (test)
6	Red video ground
7	Green video ground
8	Blue video ground
9	N/C
10	Digital/sync ground
11	Reserved (mode)
12	N/C
13	Horizontal sync
14	Vertical sync
15	N/C

# Set-Up and Operation

Perform the following steps to set up and operate the monitor.

1. Place the monitor on a flat surface near the computer and near an AC power outlet. Be certain that the ventilation slots in the cabinet are not blocked.
2. Connect the video input cable from the monitor to the computer.
3. Plug the power cord into the monitor and then into an AC outlet. Make sure the voltage selection switch on the rear panel is set to the proper position.

## WARNING

Removing or lifting the ground from the AC power source may present a potentially lethal shock hazard. Do not use an AC two-to-three wire adapter plug with this unit.

4. Turn on the computer and the monitor. The front panel power indicator should light.
5. Boot an operating system.
6. When a message is displayed on the monitor, adjust the brightness and contrast controls to obtain a comfortable display.

## Initial Tests

To assess the monitor's operation, perform the color bar test and the fill screen test. Both tests are ROM-based.

## Color Bar Test

The color bar test displays an array of colors in the form of a bar graph. To display the color bars using a Zenith Data Systems PC-compatible computer:

1. Press the CTRL, ALT, and INS keys in sequence, hold them, and then release them.
2. After the Monitor prompt appears, type C and then press RETURN. Color bars should now be displayed.

## Fill Screen Test

The ROM-based keyboard test can be used to set the brightness, contrast, dimensions, focus, convergence, and other qualities of the display to comfortable levels. To perform the fill screen test using a Zenith Data Systems PC-compatible computer:

1. Press the CTRL, ALT, and INS keys in sequence, hold them, and then release them.
2. After the prompt appears on the monitor, type TEST and press RETURN.
3. Select the keyboard test by pressing the 2 key.
4. Press any displayable key to fill the screen with that character. (The capital Z is a good character to display for assessing display characteristics.)

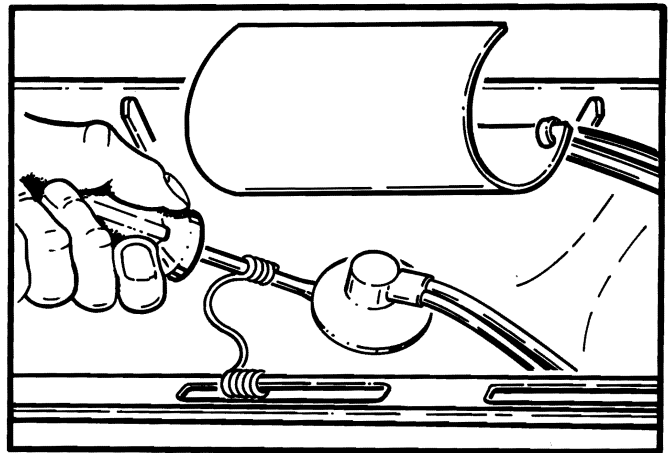
## Chapter 3

# Disassembly

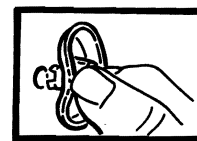
This chapter contains instructions for both disassembly and reassembly of the monitor. Step-by-step instructions are provided for disassembly. For reassembly, perform the steps in the reverse order unless instructed otherwise. Read each section (and any previous sections referred to) completely before disassembling the monitor.

Before proceeding, make sure the power cord and video cable are disconnected. The overall disassembly sequence for this monitor is as follows:

1. Remove the rear cover.
  2. Remove the rear chassis panels.
  3. Remove the video board.
  4. Remove the control board.
  5. Remove the PIN board.
  6. Remove the fan and bottom panel.
  7. Remove the support bracket and shield.
  8. Remove the deflection board assembly.
  9. Remove the deflection board.
  10. Remove the power supply/dynamic focus board assembly.
  11. Remove the power supply and dynamic focus boards.
  12. Remove the CRT.
1. Connect a clip lead or heavy gauge wire to chassis ground.
  2. Connect the other end of the lead to the stem of a flat blade screwdriver that has an insulated handle.
  3. Insert the blade of the screwdriver under the rubber insulation that covers the anode lead on the CRT and make contact with the anode terminal. Depending on the amount of charge present on the anode, a distinct snap may be heard as the CRT anode discharges.



1. CAREFULLY SLIDE A GROUNDED FLAT SCREWDRIVER TIP UNDER THE LIP OF THE ANODE LEAD.



2. AFTER DISCHARGING THE VOLTAGE, DISCONNECT THE ANODE LEAD FROM THE CRT.

**WARNING**

The CRT anode retains a potentially lethal voltage even when the monitor is turned off. After removing the monitor cover, discharge the CRT anode. Before proceeding with the disassembly. The anode is located at the top of the CRT and is shielded by a white insulating sheet. Refer to Figure 3-1 and the following procedure to discharge the CRT anode:

Figure 3-1. CRT Anode Discharging

## Rear Cover Removal

The rear cover is secured by eight screws. Two of these screws also secure rubber feet to the bottom of the monitor cover. After disconnecting the power cord and video cable, remove these eight screws as shown in Figure 3-2. Slide the cover away from the monitor, allowing the video cable to pass through the opening in the cover. Tape the screws to the inside of the rear cover and set it aside.

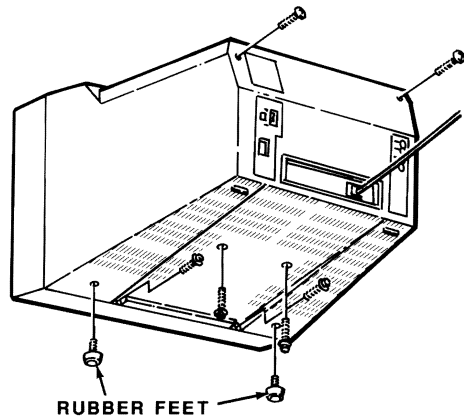


Figure 3-2. Rear Cover Removal

## Rear Chassis Panel Removal

Two panels are connected across the back of the monitor chassis. The upper panel adds support to the chassis. The lower panel holds the video cable ground clamp and strain relief. To remove the panels:

1. Refer to Figure 3-3 and remove the four hex screws that secure the upper panel to the chassis side panels. Remove the panel and replace the four screws into the side panels.

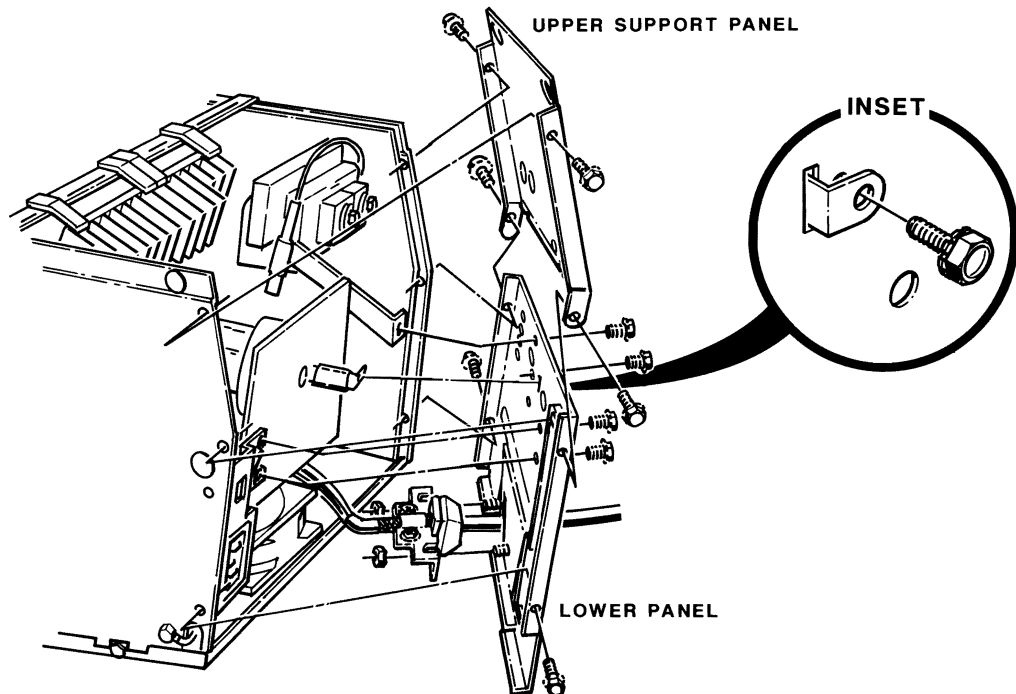


Figure 3-3. Rear Chassis Panel Removal

2. Refer to Figure 3-3 and remove the two hex screws from the bottom sides of the lower panel. Remove the screw that secures the flyback transformer bracket to the lower panel. (In some chassis, all of the high-voltage components are on the deflection board and this bracket may be different than the one shown. Adjust the procedure accordingly.) Refer to the inset of Figure 3-3 and remove the hex screw that secures the ground strap from the video board to the lower panel. Push the ground strap back through the slot in the lower panel and gently pull the lower panel away from the monitor chassis. The video cable is still held to this panel by its ground clamp.
3. Refer to Figure 3-3 and remove the two nuts that secure the video cable ground clamp to the lower panel. Slide the video cable strain relief down and out from the lower panel. It may be necessary to cut the decorative white sheet on the outside of the lower panel to allow the strain relief to slide down and away from the panel.

## Video Board Removal

1. Remove the rear chassis panels as described earlier.
2. Refer to Figure 3-4 and loosen the CRT socket clamp screw.
3. Gently wiggle the video board back and away from the CRT neck until the CRT is freed from the socket on the video board. Do not twist the video board while pulling it away from the CRT. To prevent damage to both the video board and the CRT, do not exert excessive force while removing the video board.

4. Disconnect the following cables entering the video board: 5R9, 5A9, 5A6, 5R6, 5S6, and 5A1.
5. Disconnect the following cables leaving the video board: 6S5 (to deflection board), 3R5 (to power supply board), and 8R5 (to dynamic focus board).
6. Disconnect the focus lead connector by twisting and pulling apart the plastic socket connector on the lead.
7. Remove the video board.

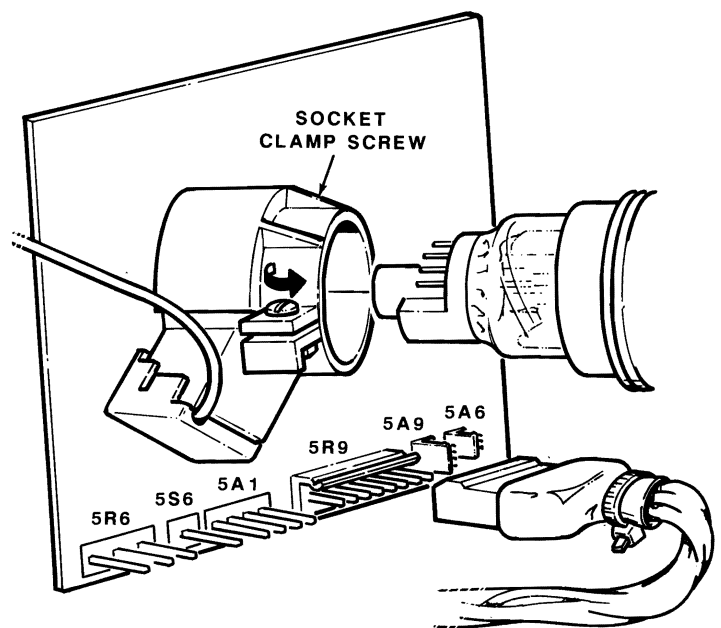


Figure 3-4. Video Board Removal



## Control Board Removal

The control board holds the external brightness and contrast controls. To remove the control board:

1. Refer to Figure 3-5 and slide the control board back and up from the tracks that hold it.
2. Disconnect connector 5A1 to the video board and remove the control board.

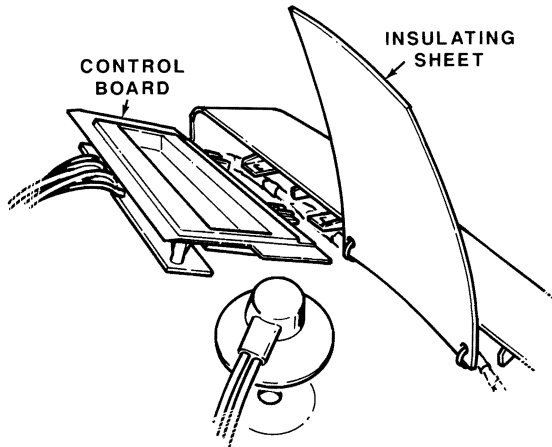


Figure 3-5. Control Board Removal

## PIN Board Removal

The PIN board is located at the top front portion of the monitor. It is held in place by two support rails that span the width of the chassis. To remove the PIN board:

1. Loosen the support rails. Refer to Figure 3-6 and remove the two hex screws holding each of the support rails in place.
2. Cut the cable ties indicated in Figure 3-6.
3. Disconnect the following cables entering the PIN board: 8R6, 8V6, and 8U6.
4. Disconnect the following cables leaving the PIN board: 4T8 (to dynamic focus board).
5. Lift the PIN board and support rails out of the monitor. The front support rail is held to the board by plastic standoffs. The rear support rail is screwed to the two heat sinks on the PIN board. Remove the rails as necessary.

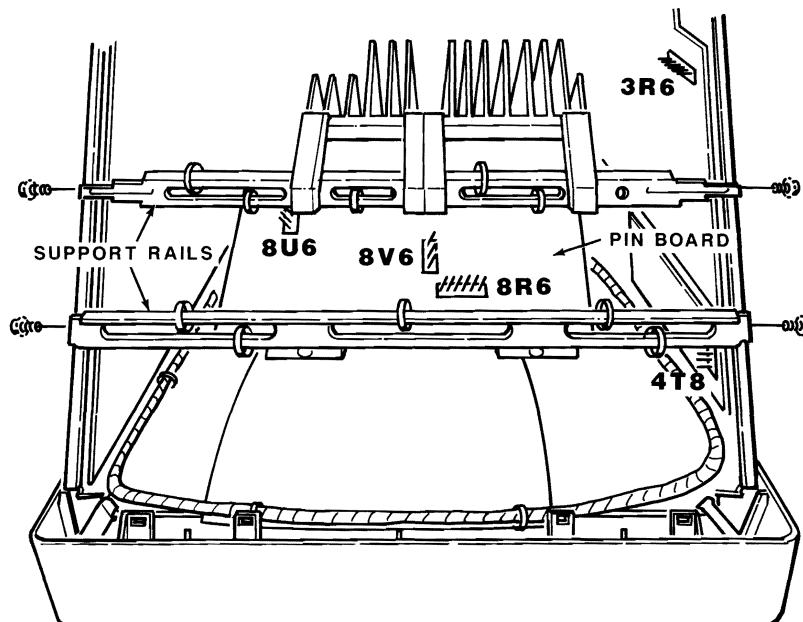


Figure 3-6. PIN Board Removal

## Fan and Bottom Panel Removal

A cooling fan is attached to the inside of the bottom panel of the monitor chassis. A portion of the high voltage assembly is also secured to this panel in some chassis. To remove the fan and bottom panel:

1. Carefully set the monitor face down on a soft surface. Be certain that there are no objects that can scratch the surface of the display glass. The glass is treated with a special non-glare OCLI coating that can be damaged by abrasives.
2. Loosen the bottom panel. Refer to Figure 3-7 and remove the four hex screws that secure the bottom panel to each of the side panels.
3. Remove the screw that holds part of the high voltage assembly to the bottom panel. In some units, the high voltage assembly is located entirely on the deflection board, so this step may be unnecessary. Pull the panel out to expose the fan.
4. Refer to Figure 3-7 and remove the three hex screws that secure the fan and air guide to the bottom panel. Remove the fan and disconnect the fan wires from the power supply board (connector 3S8).

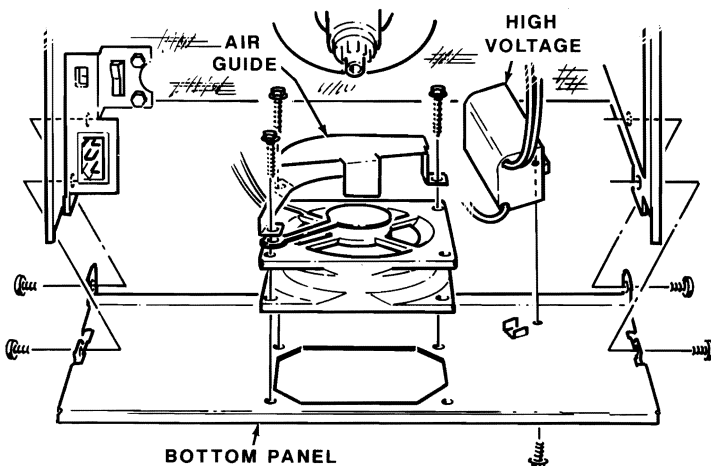


Figure 3-7. Fan and Bottom Panel Removal

## Support Bracket and Shield Removal

In addition to the bottom panel, a metal support bracket and wire mesh shield are connected to each of the side panels across the bottom of the chassis. To remove the support bracket and shield:

1. Remove the fan and bottom panel as described earlier.
2. Refer to Figure 3-8 and remove the six hex screws that hold the wire mesh shield in place. Lift the shield away from the support bracket and replace the screws.
3. Refer to Figure 3-8 and remove the two hex screws that secure the support bracket to the side panels. Remove the bracket and replace the screws. After this bracket is removed, the side panels (with the deflection, power supply, and dynamic focus boards attached) will lose most of their support.

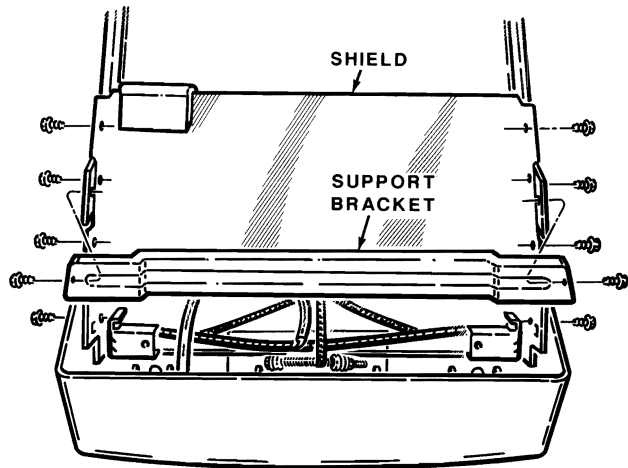


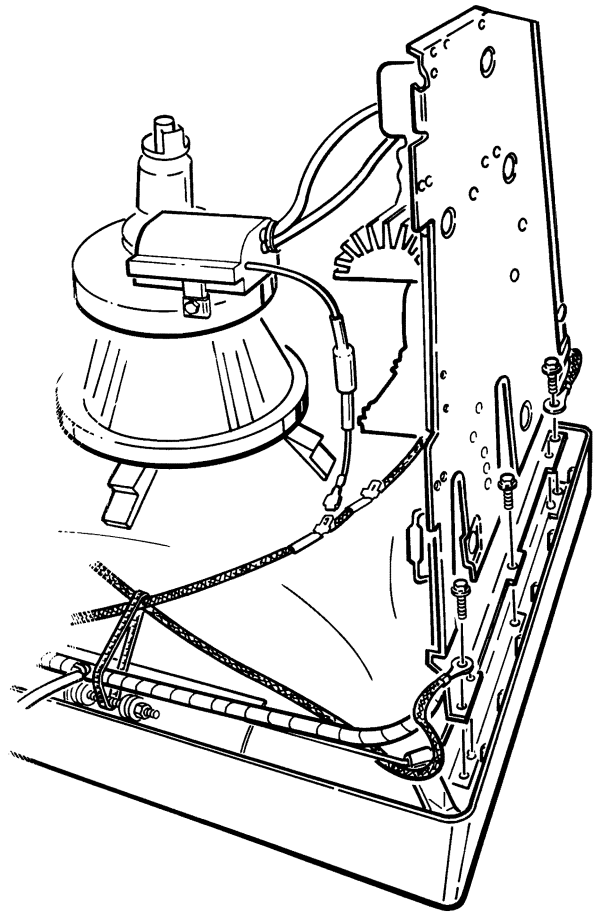
Figure 3-8. Support Bracket and Shield Removal

# Deflection Board Assembly Removal

The deflection board assembly consists of the side panel and the deflection board which is secured to the panel. To remove this assembly:

1. Remove the rear chassis panels as described earlier.
2. Remove the video board as described earlier. This step may be omitted for partial disassembly.
3. Remove the control board as described earlier. This step may be omitted for partial disassembly.
4. Remove the PIN board as described earlier. This step may be omitted for partial disassembly.
5. Remove the fan and bottom panel as described earlier.
6. Remove the support bracket and shield as described earlier.
7. Refer to Figure 3-9 and remove the three hex screws that secure the deflection board assembly to the bezel. Note the locations of the ground braid terminals.
8. Disconnect the yoke cable connectors (6R9, 6S9) from the deflection board. Two small

molded plastic dowels support the deflection board assembly. Lift the assembly up and away from the monitor. Replace the hex screws in the bezel.



**Figure 3-9. Deflection Board Assembly Removal**

## Deflection Board Removal

The deflection board is attached to the left metal side panel. To remove the deflection board from the side panel:

1. Remove the deflection board assembly as described earlier.
2. Refer to Figure 3-10 and remove the nine hex screws that secure the deflection board to the side panel. Lift the board away from the panel and replace the screws.

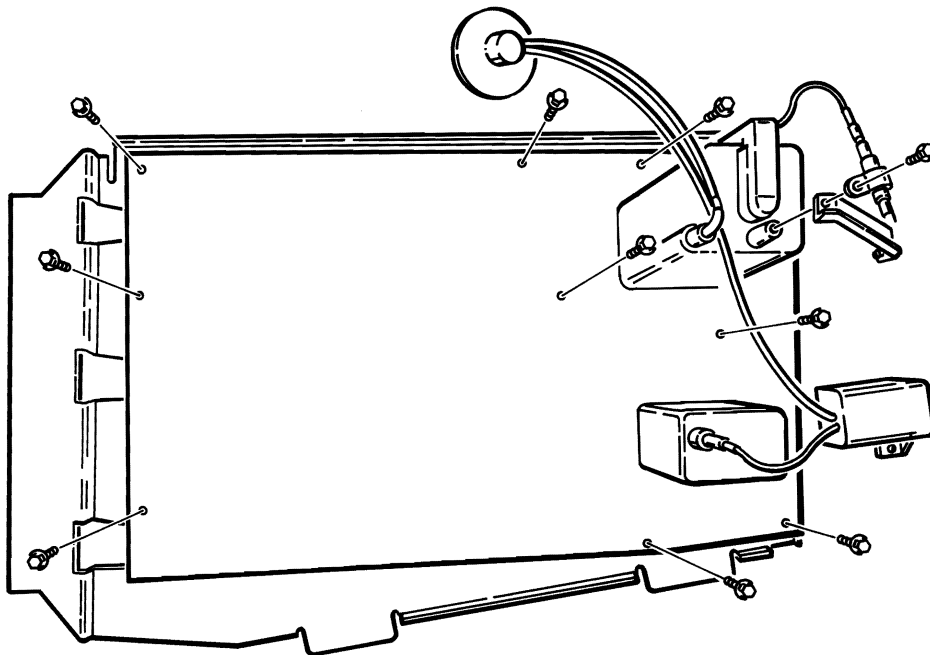


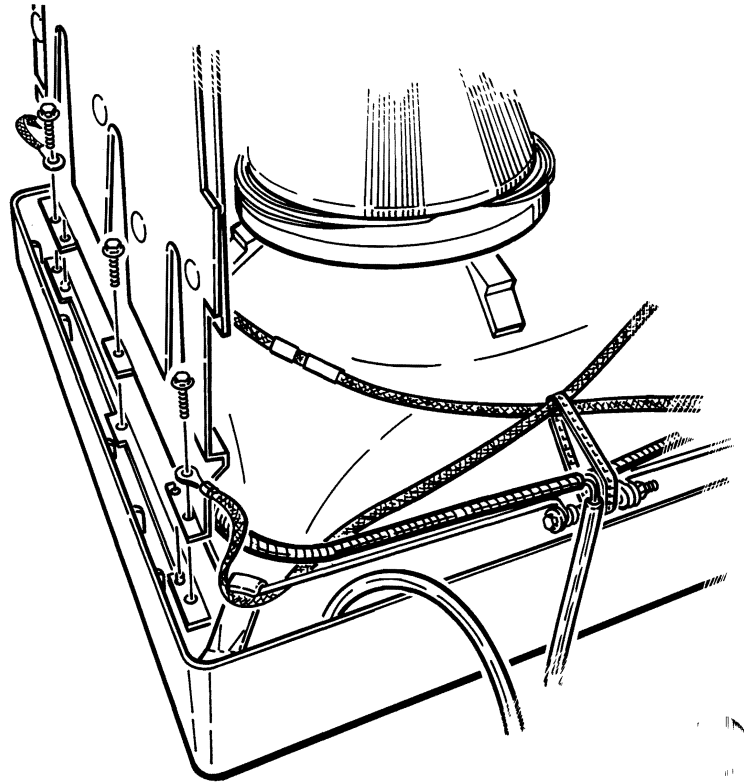
Figure 3-10. Deflection Board Removal

# Power Supply/Dynamic Focus Board Assembly Removal

The power supply/dynamic focus board assembly consists of the side panel and the power supply and dynamic focus boards which are secured to the panel. To remove this assembly:

1. Remove the rear chassis panels as described earlier.
2. Remove the video board as described earlier. This step may be omitted for partial disassembly.
3. Remove the control board as described earlier. This step may be omitted for partial disassembly.
4. Remove the PIN board as described earlier. This step may be omitted for partial disassembly.
5. Remove the fan and bottom panel as described earlier.
6. Remove the support bracket and shield as described earlier.
7. Refer to Figure 3-11 and remove the three hex screws that secure the power supply/dynamic focus board assembly to the bezel. Note the locations of the ground braid terminals.

8. Two small molded plastic dowels support the power supply/dynamic focus board assembly. Lift the assembly up and away from the monitor. Replace the hex screws in the bezel.



**Figure 3-11. Power Supply/Focus Board Assembly Removal**

# Power Supply and Dynamic Focus Board Removal

The power supply and dynamic focus boards are attached to the right metal side panel. To remove these boards from the side panel:

1. Remove the power supply/dynamic focus board assembly as described earlier.
2. Refer to Figure 3-12 and remove the appropriate hex screws for either the power supply board or the dynamic focus board. Lift the board away from the panel and replace the screws.

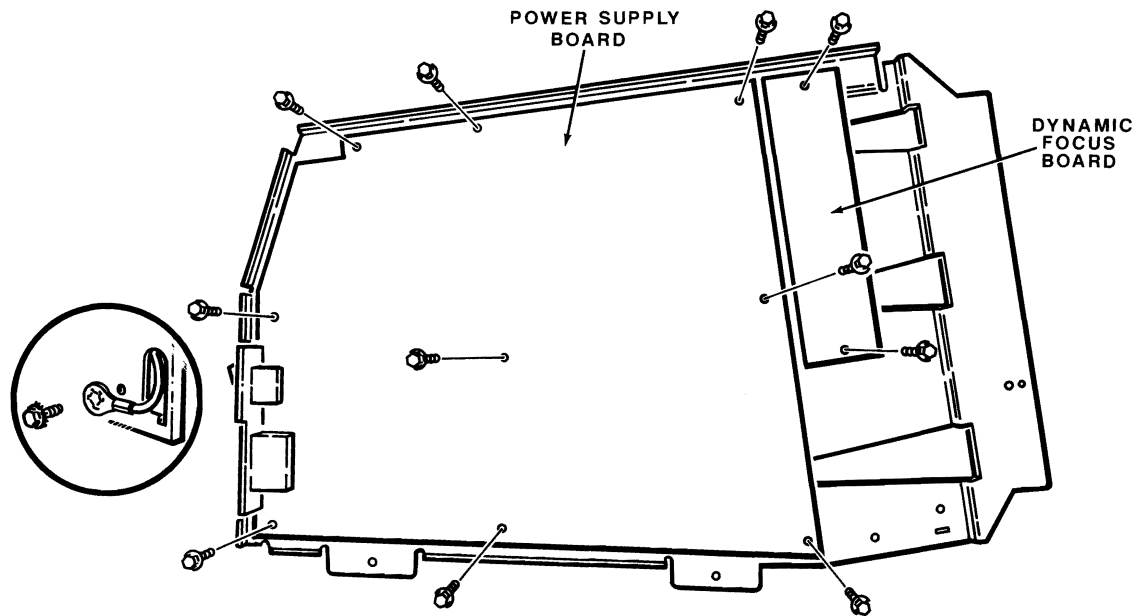


Figure 3-12. Power Supply and Dynamic Focus Board Removal

## CRT Lead Dress and Removal

The flat technology CRT is secured by four screws, clamps, and a tensioning ring. A degaussing coil is wrapped around the perimeter of the CRT. A grounding braid is also routed across the back of the CRT.

Refer to Figure 3-13 for the lead dress. To remove the CRT, remove the four hex screws with washers located at the corners of the bezel. Gently lift the CRT away from the bezel. Use Figure 3-13 as a guide when installing a new CRT.

**NOTE:** The CRT yoke is not replaceable and is considered part of the CRT.

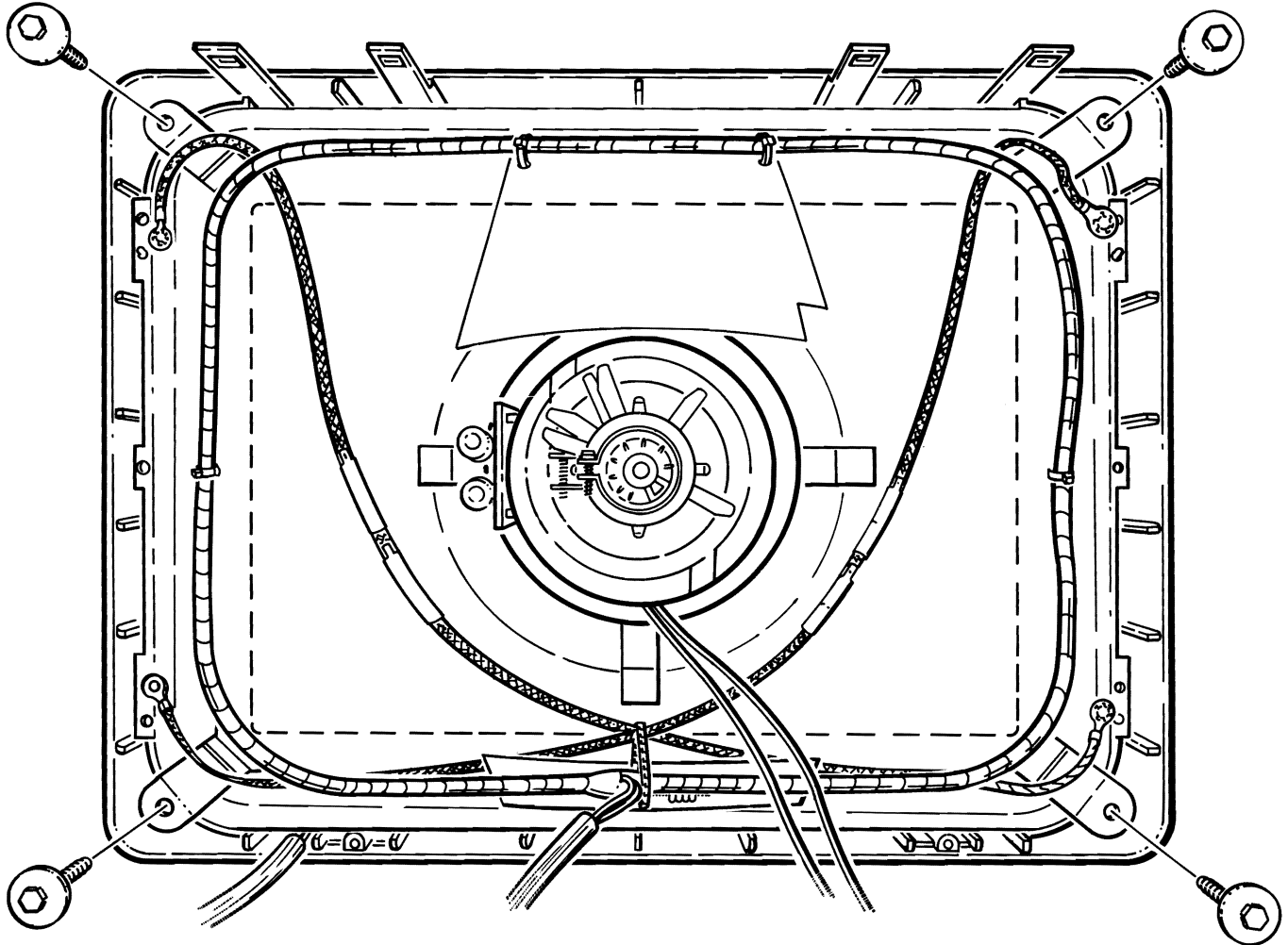


Figure 3-13. CRT Lead Dress and Removal

# Chapter 4

## Adjustments

This chapter contains instructions for performing the various monitor adjustments. Because these adjustments are performed while the monitor is on, observe proper precautions to avoid personal injury. Specific warnings are included where necessary.

Table 4-1 lists the various adjustment devices and their component numbers. They are arranged according to the circuit board or location where they can be found. Refer to Figures 4-1, 4-2, 4-3, and 4-4 to locate these adjustments on the video output board, the deflection board, and the PIN board, and the dynamic focus board respectively. Specific adjustment procedures follow these figures. If a specific adjustment procedure does not correct a problem, refer to chapters 5 and 6 for additional information.

**Table 4-1. Monitor Adjustment Devices**

DEVICE	DESCRIPTION
<b>External</b>	
R5401	Contrast (monitor top)
R5403	Brightness (monitor top)
R2148	Vertical centering (rear panel)
R2153	Vertical size (rear panel)
R3402	Horizontal size (rear panel)
R3418	Horizontal centering (rear panel)
<b>Video output board</b>	
R5139	Blue gain
R5154	Red gain
R5316	Red cutoff
R5317	Green cutoff
R5318	Blue cutoff
<b>Deflection board</b>	
R2107	Vertical linearity
R2117	Vertical hold
R2124	Vertical sub-size (480-line)

DEVICE	DESCRIPTION
<b>Deflection board (Cont'd.)</b>	
R2170	Vertical sub-size (400-line)
R2158	Vertical sub-size (350-line)
R3001	Horizontal centering
R3221	High-voltage (optional)
R3238	High-voltage shutdown (optional)
R3415	Horizontal hold
R3420	Horizontal phase
<b>PIN board</b>	
L7401	"W-M" phase
R7012	E-W trap
R7027	E-W level
R7039	E-W phase
R7106	Horizontal size
R7430	N-S trap
R7431	N-S parallelogram
R7433	South phase
R7434	South level
R7435	North phase
R7436	North level
R7454	North "W"
R7456	South "M"
R7460	IC701 trim (optional)
R7540	N-S crossover zero
<b>Dynamic focus board</b>	
R7703	Dynamic focus
<b>Control board</b>	
R5402	Contrast limit
R5404	Brightness limit
<b>Other</b>	
Focus	High-voltage resistor block
G2	High-voltage resistor block



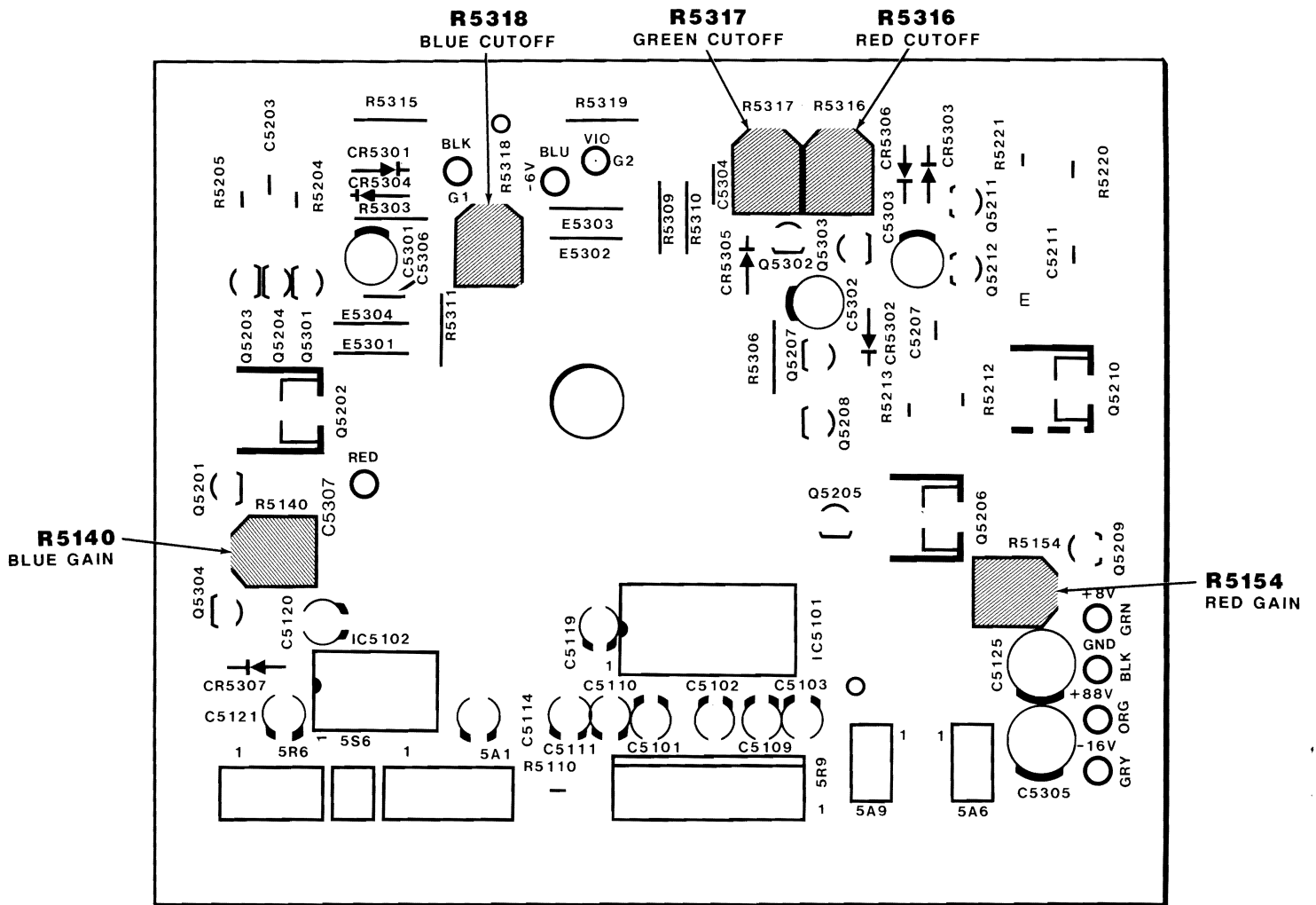


Figure 4-1. Video Board Adjustment Locations

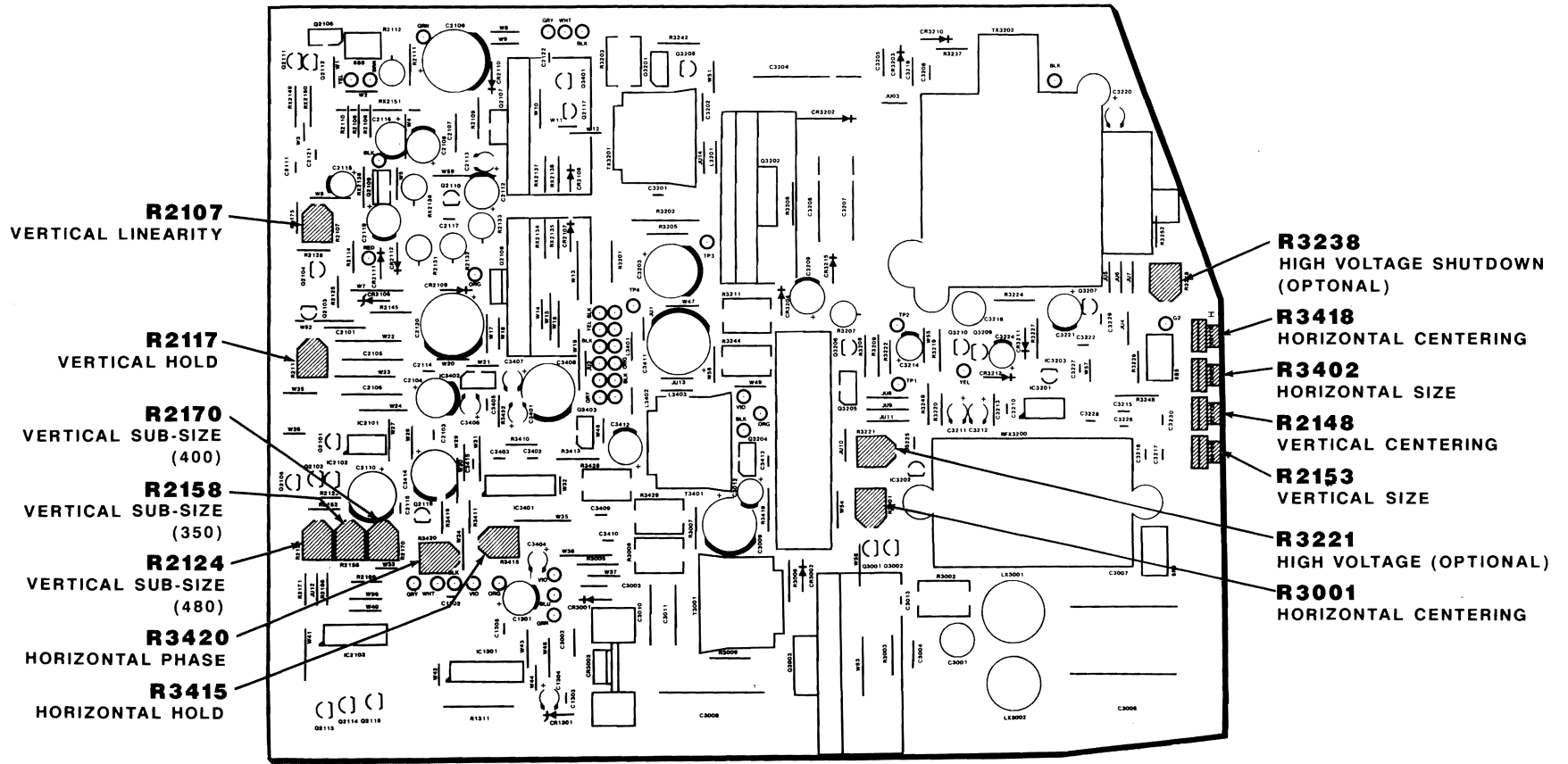


Figure 4-2. Deflection Board Adjustment Locations

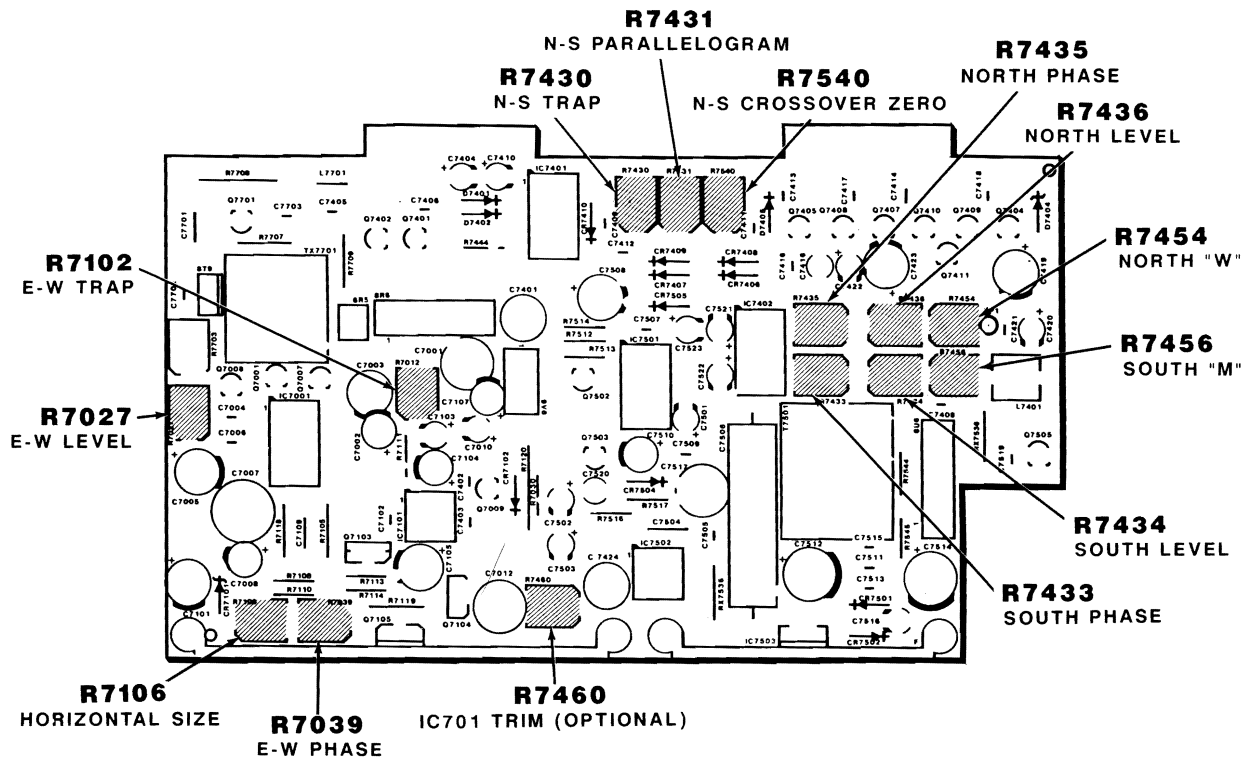


Figure 4-3. PIN Board Adjustment Locations

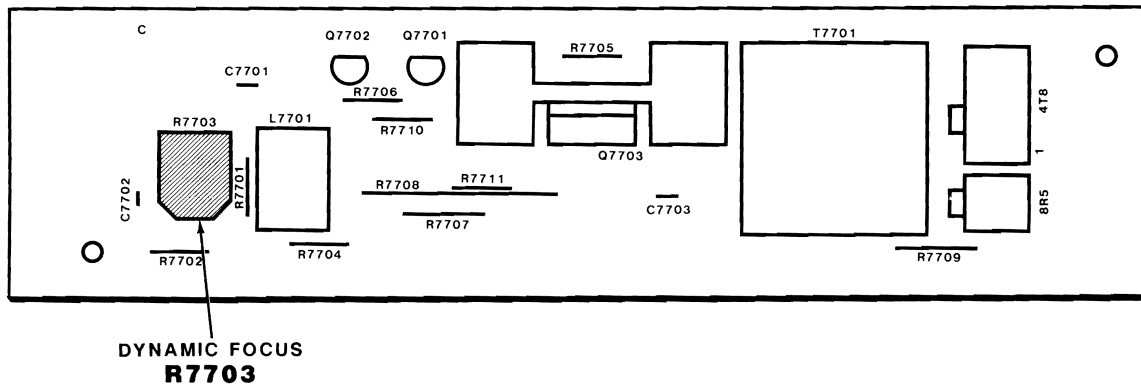


Figure 4-4. Dynamic Focus Board Adjustment Locations

# Deflection Board Adjustments

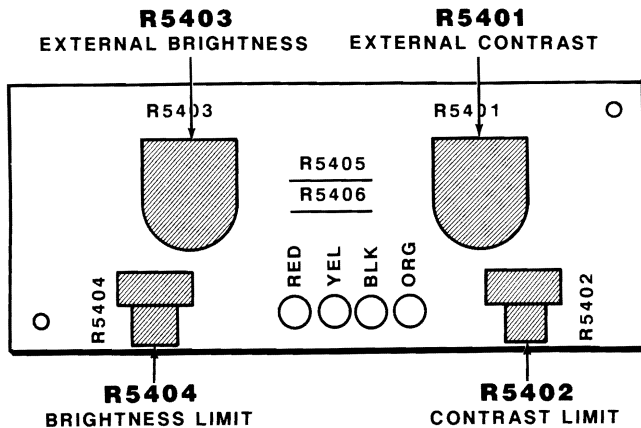


Figure 4-5. Control Board Adjustment Locations

## Preparation

Perform the following steps to prepare the monitor for adjustment.

1. Remove the cabinet back to access internal adjustments.
2. Turn the monitor on and allow it to warm up for approximately 30 minutes.
3. Prepare the computer to run disk-based diagnostics (refer to the "Inspection and Preparation" section of Chapter 6 for the procedure). They will be used to generate the test patterns required for specific adjustments. Be certain that the computer is functioning properly by first connecting it to a known good monitor.
4. Read each adjustment procedure completely before performing it.

The following sections contain procedures for performing the various deflection adjustments.

NOTE: Perform these adjustments only if you are certain that the pincushion (PIN) adjustments are satisfactory. Otherwise, proceed to the "Pincushion Adjustments" section and follow the steps indicated there. If the display appears symmetrical and undistorted, it is likely that the pincushion correction circuitry is adjusted properly.

## Horizontal Hold

The horizontal hold control (R3415) prevents the display from shifting horizontally and tearing apart in diagonal segments. To adjust the horizontal hold:

1. Adjust R3415 to eliminate horizontal tearing and restore horizontal hold.
2. Verify that the display is stable in all three modes by using software that forces the monitor to operate in each of the three modes.
3. Repeat the procedure until the display is stable in all three modes.

Alternatively, to adjust the horizontal hold:

1. Remove the horizontal sync signal from the deflection board.
2. Adjust R3415 to eliminate horizontal tearing and restore horizontal hold.
3. Re-apply the horizontal sync signal to the deflection board and check for a stable display.

NOTE: The horizontal phase control (R3420) interacts slightly with the horizontal hold control. If horizontal tearing or jittering cannot be completely eliminated by adjusting the horizontal hold control, try adjusting the horizontal phase control to completely stabilize the display.

## Horizontal DC Raster Centering

The horizontal DC raster centering control (R3001) sets the left-to-right centering of the raster within the bezel opening. To adjust the horizontal DC raster centering:

1. Turn the G2 control until the raster just appears.
2. Adjust R3001 to center the raster horizontally within the bezel opening.
3. Turn the G2 control until the raster just disappears.

## Horizontal Phase

The horizontal phase control (R3420) sets the left-to-right position of the display within the raster area. To adjust the horizontal phase:

1. Use the fill screen test to fill the display area with text.
2. Center the external horizontal centering control (R3418) located on the rear panel.
3. Adjust R3420 to center the display from left to right within the raster area.

## Horizontal Size

The horizontal size controls (R3402 and R7106) set the amount of horizontal (left-to-right) raster deflection. To adjust the horizontal size:

1. Use the fill screen test to fill the display area with text.
2. Center the external horizontal size control (R3402) located on the rear panel.
3. Adjust R7106 (located on the PIN board) for a display width of approximately 256 mm  $\pm$  2 mm (10.07 inches).

## Vertical Hold

The vertical hold control (R2117) prevents the display from rolling upwards or downwards. To adjust the vertical hold:

1. Adjust R2117 to stabilize the display by turning it first to one extreme and then backing off until the display just stabilizes. Repeat this procedure from the opposite extreme until the display just stabilizes. Set R2117 midway between the two settings that stabilize the display.
2. Verify that the display is stable in all three video modes by using software that forces the monitor to operate in each of the three modes.

## Vertical DC Raster Centering

The vertical DC raster centering control (R2148) sets the top-to-bottom centering of the raster within the bezel opening. To adjust the vertical DC raster centering:

1. Use appropriate software to fill the screen in the 480-line mode.
2. Adjust R2148 to center the displayed video vertically within the bezel opening. R2148 should be set within the middle portion of its range when this adjustment is completed.

## Vertical Size

The vertical size controls (R2124, R2169, and R2158) set the amount of vertical (top-to-bottom) raster deflection. So that the vertical size remains constant in all three video modes, there are three sub-size adjustments that must be set. To adjust the vertical size, center the external vertical size control and then proceed to the sub-size adjustments for each mode.

### To adjust the 480-line mode sub-size:

1. Use appropriate software to fill the screen in the 480-line mode.
2. Adjust sub-size control R2124 for a display height of approximately  $195 \text{ mm} \pm 2 \text{ mm}$  (7.67 inches).

### To adjust the 400-line mode sub-size:

1. Use appropriate software to fill the screen in the 400-line mode.
2. Adjust sub-size control R2170 for a display height of approximately  $195 \text{ mm} \pm 2 \text{ mm}$  (7.67 inches).

### To adjust the 350-line mode sub-size:

1. Use appropriate software to fill the screen in the 350-line mode.
2. Adjust sub-size control R2158 for a display height of approximately  $195 \text{ mm} \pm 2 \text{ mm}$  (7.67 inches).

## Vertical Linearity

The vertical linearity control (R2107) adjusts the vertical scanning for evenly spaced scanning lines on the display. To adjust the vertical linearity:

1. Display a crosshatch pattern. (Use appropriate software to generate this pattern in the 480-line mode.)
2. Adjust R2107 so that the horizontal lines of the crosshatch pattern are evenly spaced from the top to the bottom of the display. The resulting display will show minimal compression, crowding, or expansion of horizontal lines throughout the display.

## Focus

The focus control varies the focus voltage to sharpen the display detail. To adjust focus:

1. Display a dot test pattern (refer to the "Inspection and Preparation" section of Chapter 6 for the procedure). Alternatively, perform the fill screen test using the capital Z.
2. Set the external brightness and contrast controls to their detent positions.
3. Adjust the focus control (located on the high-voltage resistor block) for the best overall focus. Check the center, top center, bottom center, left center, and right center areas of the display for good focus.
4. Verify acceptable overall focus using the fill screen test with such characters as @ and #. If the focus is not fairly uniform throughout most of the screen, perform the dynamic focus adjustment.

**NOTE:** If the G2 control is adjusted after the focus control has been adjusted, it may be necessary to re-adjust the focus control.

## Dynamic Focus

The dynamic focus circuitry varies the focus voltage at the horizontal rate so that the voltage at the raster edges is increased and the voltage at the center is decreased. This results in a more uniform overall display focus. To adjust the dynamic focus control (R7703):

1. Display a dot test pattern (refer to the "Inspection and Preparation" section of Chapter 6 for the procedure). Alternatively, perform the fill screen test using the capital Z.
2. Set the external brightness and contrast controls to their detent positions.

3. Adjust R7703 for the best overall focus. Check the center, top center, bottom center, left center, and right center areas of the display for good focus.
4. Verify acceptable overall focus using the fill screen test with such characters as @ and #.
4. Adjust the south level control (R7434) to reduce any PIN distortion at the center of this line. That is, use this control to reduce any bowing in the middle portion of the line.
5. Adjust the north phase control (R7435) to obtain the straightest possible line. Re-adjust the north level control and the north phase control in turn until the straightest line with minimum PIN distortion results.

## Pincushion Adjustments

The following sections contain procedures for performing the various pincushion (PIN) correction adjustments. Because this monitor incorporates the new flat technology CRT, these adjustments are considerably more involved than those for a monitor having a conventional CRT.

**NOTE:** Read this procedure thoroughly before attempting to perform any PIN adjustments. The controls you will be adjusting are interactive; that is, changing one control may make it necessary to go back and change another control until the settings are optimized. For this reason, perform these adjustments in the order in which they are presented.

### North-South Pincushion

The north-south (N-S) pincushion adjustments control the symmetry of the top and bottom halves of the display. To adjust the N-S PIN:

1. Display a crosshatch pattern in the 480-line mode.
2. Locate the horizontal line nearest the top of the display.
3. Adjust the north level control (R7436) to reduce any PIN distortion at the center of this line. That is, use this control to reduce any bowing in the middle portion of the line.
6. Adjust the south phase control (R7433) to obtain the straightest possible line. Re-adjust the south level control and the south phase control in turn until the straightest line with minimum PIN distortion results.
7. Adjust the N-S trap control (R7430) to eliminate trapezoidal distortion in the display. Use the edges of the monitor bezel as references to obtain the most symmetrical display possible.
8. Adjust the N-S parallelogram control (R7431) to eliminate parallelogram distortion in the display. Use the edges of the monitor bezel as references to obtain the most symmetrical display possible.
9. Use appropriate software to fill the screen in the 480-line mode.
10. Adjust the N-S crossover zero control for minimum horizontal line separation across the center of the display. The resulting display should show fairly uniform horizontal line separation throughout the display.
11. Use both the crosshatch pattern and the fill screen test and verify that the N-S adjustments are correct. Repeat steps as needed to obtain the best possible display.

## East-West Pincushion

The east-west (E-W) pincushion adjustments control the symmetry of the left and right halves of the display. To adjust the E-W PIN:

1. Display a crosshatch pattern in the 480-line mode.
2. Adjust the E-W level control to reduce PIN distortion in the vertical lines. Use the edges of the monitor bezel as references to obtain the most symmetrical display possible.
3. Adjust the E-W trap control (R7012) to eliminate trapezoidal distortion in the display. Use the edges of the monitor bezel as references to obtain the most symmetrical display possible.
4. Locate the vertical lines nearest the left and right edges of the display.
5. Adjust the E-W phase control (R7039) to obtain the straightest possible vertical lines along the left and right sides of the display.

6. Use both the crosshatch pattern and the fill screen test and verify that the E-W adjustments are correct. Repeat steps as needed to obtain the best possible display.

## CRT Cutoff

The cutoff controls (R5316, R5317, and R5318) set the DC level at which the CRT is cut off during blanking and retrace times. The cutoff controls shift the entire waveform viewed at each of the three CRT guns up or down, thereby setting the level of the cutoff pulses (the rectangular pulses in the waveforms of Figure 4-6). Perform this adjustment in a dimly lit area. To adjust the cutoff controls:

1. Use the fill screen test to fill the display area with the capital Z.
2. Set the external contrast control to maximum.
3. Set the external brightness control to minimum.

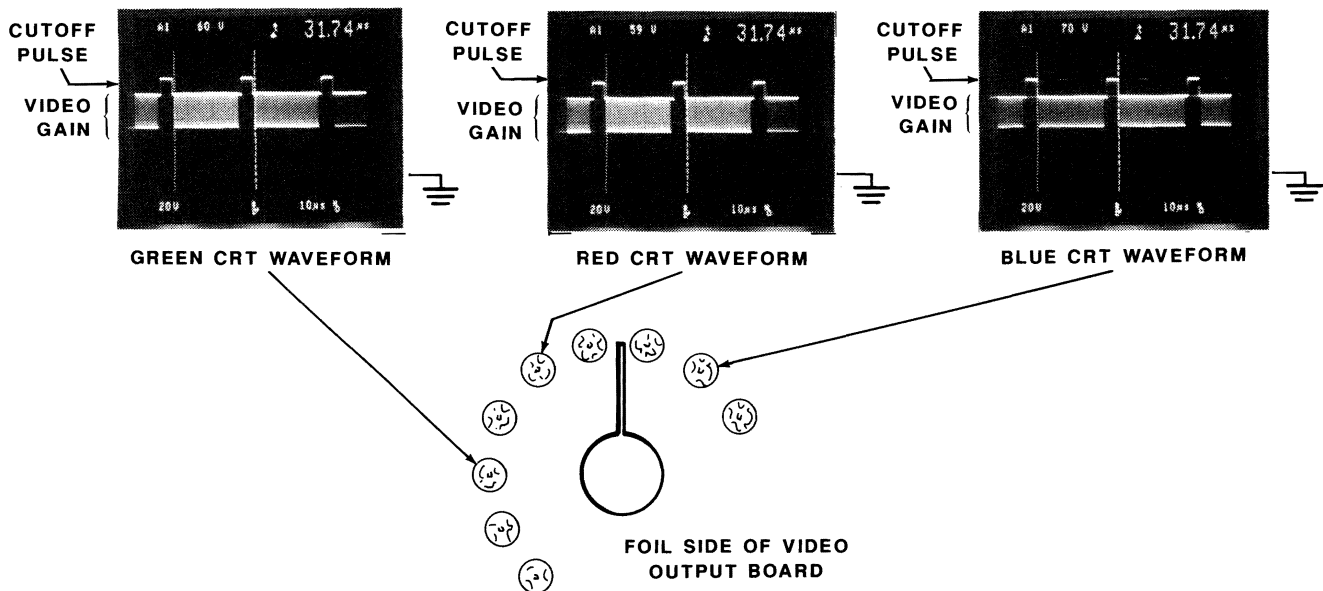


Figure 4-6. CRT Gun Waveforms



4. Set the red and blue gain controls to their mid-range positions.
  5. Adjust the G2 control until the raster just appears, then back off until it just disappears.
  6. Adjust the red cutoff control (R5316) until a red raster just becomes visible, then back off until it just disappears.
  7. Adjust the green cutoff control (R5317) until a green raster just appears, then back off until it just disappears.
  8. Adjust the blue cutoff control (R5318) until a blue raster just appears, then back off until it just disappears.
  9. Set the external brightness control to maximum and verify that the displayed raster is white. If the display does not appear white, adjust the cutoff controls slightly to eliminate any color cast.
  10. Set the external brightness control to its detent position and verify that the display background is black. If the background does not appear black, adjust the G2 control slightly to eliminate any background raster.
  11. Set the external brightness and contrast controls to their detent positions and compare the waveforms at the red, green, and blue CRT guns to those pictured in Figure 4-6. They should appear similar.
1. Use the fill screen test to fill the display area with the capital Z.
  2. Set the external contrast and brightness controls to maximum.
  3. Refer to Figure 4-6 and measure the waveform at the green gun of the CRT. It should be similar to the waveform photograph pictured.
  4. Refer to Figure 4-6 and measure the waveform at the red gun of the CRT. The peak-to-peak amplitude of the area labeled "video gain" in the red CRT gun waveform photograph should be equal to the peak-to-peak amplitude of the same area measured at the green gun (approximately 48 V peak-to-peak). Adjust R5154 until the amplitude of this area matches that of the green gun.
  5. Refer to Figure 4-6 and measure the waveform at the blue gun of the CRT. The peak-to-peak amplitude of the area labeled "video gain" in the blue CRT gun waveform photograph should be equal to the peak-to-peak amplitude of the same area measured at the green gun (approximately 48 V peak-to-peak). Adjust R5140 until the amplitude of this area matches that of the green gun.
  6. Set the external brightness and contrast controls to their detent positions, observe the display, and verify that the displayed characters appear white.

## Video Gain

The video gain controls (R5140 and R5154) set the amplitudes of the red and blue CRT drive voltages relative to the green drive voltage. (The green amplifier gain is fixed.) The gain controls shift the "video gain" portions of the CRT gun waveforms in Figure 4-6 up or down. When set properly, all three RGB drive voltages should be the same. To adjust the video gain.

## Final Checks

Before returning the monitor to service, perform the following final checks:

1. Perform the AC leakage test as described in Chapter 6.
2. Make sure that all circuit boards and modules are properly installed.

3. Make sure that all connectors are securely installed and that all cables are properly routed to avoid pinching or excessive heat.
4. Make sure that all mounting hardware, barriers, and screws are properly installed.
5. Check the display and verify that the monitor is adjusted and operating properly.
6. Leave the monitor turned on for at least one hour and check for intermittent or thermal problems.

## Chapter 5

# Circuit Descriptions

This chapter provides descriptions of the major circuits in the ZCM-1490 color video monitor. Use this material in conjunction with the troubleshooting and adjustment information provided elsewhere in this manual.

Refer to the appropriate schematics in Chapter 8 of when reviewing the component level circuit descriptions. Refer to the block diagram in Figure 5-1 when reviewing the overall operation of the monitor. Refer to the waveform photographs in Chapter 8 where

noted. Where appropriate, partial schematics are included within the circuit descriptions for clarity.

## Functional Overview

This section provides a brief explanation of the major functional blocks of the monitor. Each of the circuit boards of the monitor is discussed individually. Refer to the block diagram in Figure 5-1 while reading the explanation that follows.

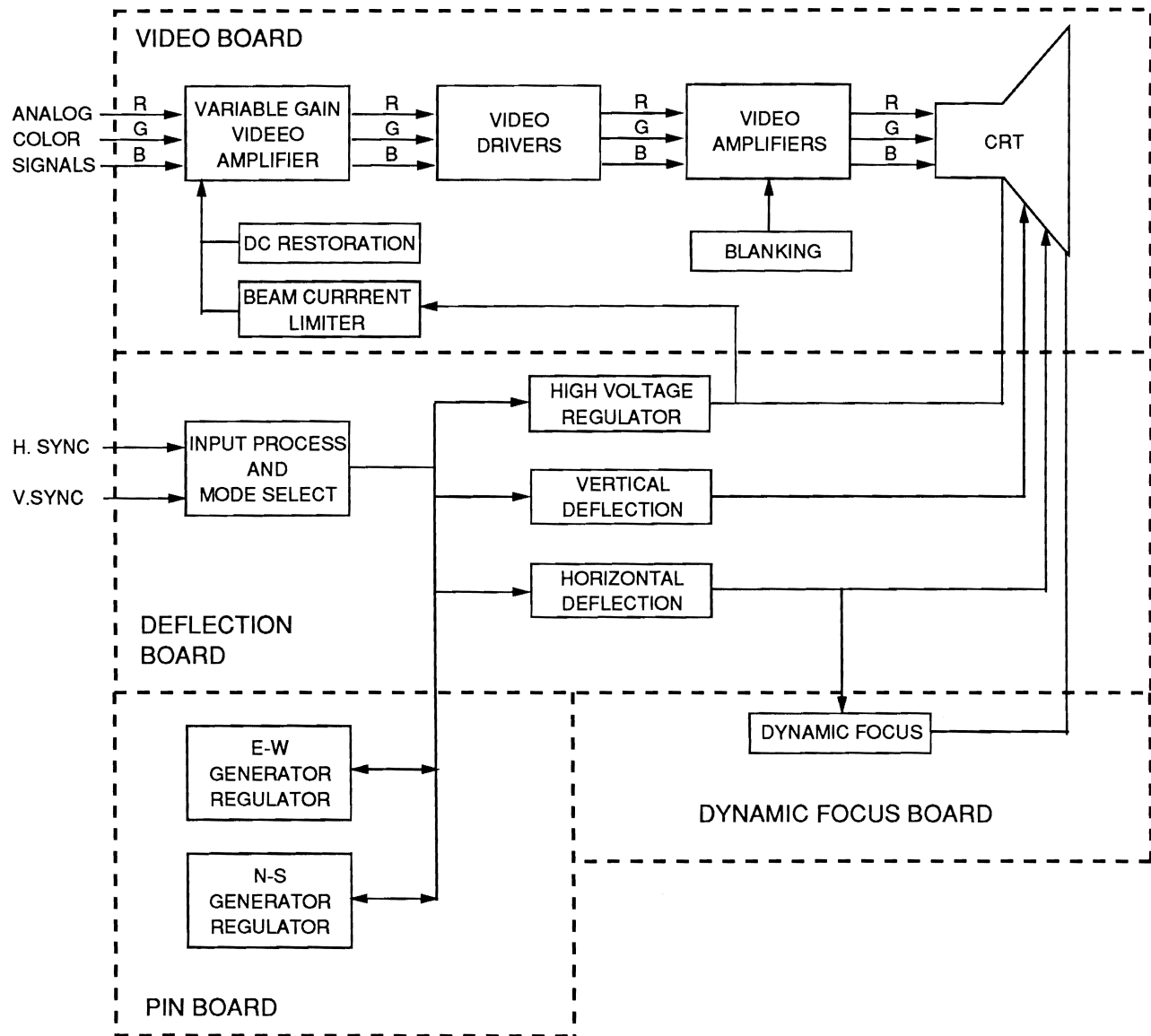


Figure 5-1. ZCM-1490 Block Diagram

The video output module contains RGB amplifiers, brightness and contrast control, automatic brightness limiter, and video blanking circuits. Analog signals containing color information are supplied to the monitor along with horizontal and vertical sync signals. The analog red, green, and blue video inputs are AC-coupled to a variable gain video amplifier. The DC component of the color signals is restored

here. The resulting R,G, and B color signals are applied to video driver and video output stages. The video output amplifiers activate the appropriate red, green, or blue guns of the CRT, allowing information to be displayed. Video blanking for horizontal and vertical retrace acts to shut off the CRT during retrace times.

The monitor deflection module contains the sync processing, high voltage, horizontal and vertical deflection circuitry, and associated feedback paths. Integrated circuits condition the incoming horizontal and vertical sync signals for use by the deflection circuitry. Horizontal deflection amplifiers provide the current required to move the electron beam in the CRT from left to right. Similarly, vertical deflection circuitry provides the current required to move the electron beam from top to bottom. The high voltage needed for the CRT anode is also generated here. Associated feedback-type circuitry includes the anode voltage regulator, pincushion correction, beam current limiting, and blanking pulses.

The FTM/PIN focus board generates the proper waveforms needed to produce a symmetrical display on the CRT. Because this monitor incorporates a flat technology CRT, a much more complex pincushion (PIN) correction circuit is required. Waveforms are generated to correct the display from east to west (E-W) and from north to south (N-S). These correction waveforms are then superimposed upon the horizontal and vertical scanning waveforms to form a symmetrical display.

In most CRTs, the shadow mask is curved to follow the contours of the screen and suspended by springs. This shadow mask may distort with changes in temperature, sacrificing some image quality even under ideal conditions. In the flat technology CRT, the shadow mask is stretched across a frame under extreme tension, resulting in a flat shadow mask that remains flat even with changes in temperature. In addition, the screen itself is perfectly flat. The result is higher resolution and a smaller overall tradeoff between contrast, brightness, and resolution.

## Video Input Processing

The red (R), green (G), and blue (B) analog color signals enter the video output module at connector 5R9. These signals are DC-terminated by 75 $\Omega$  resistors

R5101, R5102, and R5103. The color signals are then AC-coupled to the video inputs of IC5101 by capacitors C5101, C5102, and C5103.

IC5101 is a three-channel, variable gain video amplifier. A variable DC voltage applied to pin 2 of IC5101 controls the gain of the three channels. The external contrast control acts as a voltage divider to supply this variable voltage at pin 4 of connector 5A1. The integrator formed by R5112 and C5111 helps to smooth the action of the contrast control. The gains of the three channels will track to within about 3% over the range of the contrast control (+ 8 VDC at maximum contrast to 0 VDC at minimum contrast). The outputs of this gain stage are emitter followers. The characteristic low impedance output of the emitter follower allows for more efficient signal transfer to the following amplifier stages. The gain-controlled video signals appear at pins 12 (R), 15 (G), and 18 (B) of IC5101.

IC5101 also contains an automatic brightness limiter (ABL) circuit. A voltage sample proportional to the average CRT anode current from the deflection board is applied to pin 1 of IC5101. As the average anode current increases, the voltage at pin 1 decreases. The ABL circuit is designed so that as the average anode current exceeds 750  $\mu$ A, the gain of the video signal is decreased. The resulting negative feedback loop limits the maximum average anode current to 750  $\mu$ A. This circuit is also referred to as a beam current limiter.

## Video Amplifiers

After the analog video input signals are processed by IC5101, they are further amplified before being applied to the color guns of the CRT. This amplification occurs in three stages, each of which is discussed individually in the following sections. In addition, the DC component of the color signals is restored here. Cutoff, retrace suppression, and black level circuit descriptions are also included here.

Circuit descriptions for the three video amplifiers are written with reference to the green video amplifier circuits. The red and blue amplifiers function identically. Refer to the partial schematic of Figure 5-2 while reading these circuit descriptions.

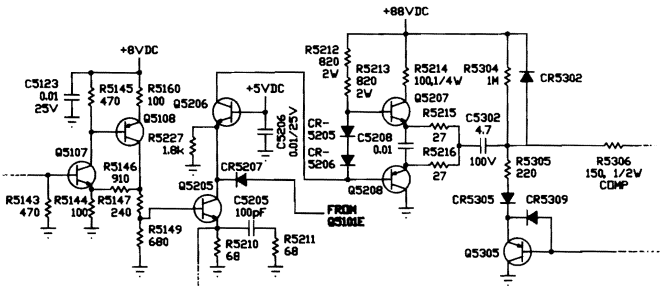


Figure 5-2. Video Amplifier Section (Green)

## Video Drivers

The gain-controlled green video signal leaving IC5101 at pin 15 is coupled to the resistor attenuator formed by R5117, R5134, and R5143. C5116 provides some high-frequency peaking for the video signal.

The video signal is then applied to a two-stage, direct-coupled, non-inverting amplifier formed by Q5107 and Q5108. The gain of the green channel is fixed by resistor R5147. In the red and blue channels, potentiometers set the gain (R5156 for red and R5139 for blue) relative to the green channel. The red and blue channel gains can be varied approximately 25% around the green gain.

## Cascode Output Amplifier

The video signal is applied to the cascode output amplifier formed by transistors Q5205 and Q5206.

The cascode arrangement allows high gain and wide bandwidth. The amplified video signal appears at the collector of Q5206 across load resistors R5212 and R5213. An emitter peaking network consisting of C5205, C5214, R5209, and R5211 provides frequency compensation for the cascode amplifier.

## DC Restoration

As noted earlier, the incoming analog color signals are AC-coupled to the inputs of IC5101. The DC-component of the video signal is then restored as follows. During the horizontal and vertical retrace interval, the voltage at the emitter of Q5205 is sampled by the RC network formed by R5209 and C5214. At this time, the video signal is at black level and the clamp pulse at pin 1 of the 5R6 connector is active-high. This sampled voltage is fed back to pin 14 of IC5101 and compared to a reference voltage developed at pin 13 of IC5101. This reference voltage is used by all three channels in the same manner.

A push-pull current source at the output of the comparator within IC5101 charges or discharges hold capacitor C5105 depending on the magnitude and polarity of the difference between the sampled voltage and the reference voltage. The voltage developed across the hold capacitor C5105 controls the DC bias of the gain-controlled video output at pin 15 of IC5101. During the active clamp pulse time, the DC restoration feedback loop is gated on and the DC bias is set such that the black level emitter voltage of Q5205 equals the reference voltage at pin 13 of IC5101. During the video time, the DC restoration feedback loop is gated off and the voltage across the hold capacitor supplies the required DC bias until the next clamp pulse arrives. In this manner, the AC-coupled video signal applied to the input of IC5101 is DC-restored and an accurate and stable bias is supplied to the cascode output amplifier.

## Class AB Output Stage

The amplified video signal at the collector of output transistor Q5206 is applied to a pair of emitter followers (Q5207 and Q5208). Diodes CR5205 and CR5206 force the complementary pair to operate in a class AB mode, thereby reducing crossover distortion as compared to class B operation. This stage isolates the cathode capacitance from the collector of output transistor Q5206 and provides a low-impedance drive for the cathode clamp. (Isolating the cathode capacitance is necessary to mitigate the effect of excess capacitive reactance. Because capacitive reactance is inversely proportional to frequency, it can reduce the load impedance seen by the output amplifier, thereby reducing the gain of the amplifier.) The output of this stage is AC-coupled to the CRT cathode (the green gun) by C5302.

## Cutoff

After the output is AC-coupled to the CRT cathode, the DC component is restored by the gated clamp circuit formed by transistors Q5304, Q5305, and their associated circuitry. A positive TTL-level composite blanking pulse is applied to IC5102, where it is buffered and appears at pin 3. This signal is applied to the base of Q5304. With a positive-going pulse at its base, Q5304 produces a negative-going pulse at its collector. This pulse appears at the base of Q5305 after passing through the green cutoff adjustment (R5317). The Q5305 emitter is coupled to the CRT cathode through CR5305 and R5305. Thus, the cathode is forced to the peak level of the gate pulse at the anode of CR5305 during blanking time. The cutoff control determines the DC operating point of the cathode by setting the clamping level.

## Retrace Line Prevention

In addition to the video blanking circuitry, a retrace suppressor circuit is included so that the retrace lines produced during flyback do not appear on the screen. A buffered composite blanking pulse from pin 11 of IC5102 is applied to the base of Q5101. The output of this emitter-follower stage is applied to diodes CR5203, CR5207, and CR5211. In the pres-

ence of a pulse, these diodes conduct, thereby steering current away from the cascode output amplifier transistors and shutting them off. This causes a positive blanking pulse to be superimposed onto the cathode video signal during retrace times, thereby preventing a retrace line from being displayed. In addition, this action provides a pedestal for the cutoff circuit clamp.

## Black Level

A black level control establishes the difference between black picture information and blanking pulses in the video signal. A buffered blanking pulse from pin 8 of IC5102 is coupled to the variable pedestal generator circuit formed by Q5102, Q5104, and associated circuitry. The output of this generator appears at the emitter of Q5104. During blanking time, a fixed voltage of 7.3 VDC appears at the emitter. During trace time, this voltage is variable, based on the DC voltage applied to the base of Q5102. The external brightness control is a voltage divider supplying this voltage during trace time. The range of the supplied voltage is 7.3 VDC to 5.3 VDC. The resulting pedestal voltage at the emitter of Q5104 is summed to the three video outputs of IC5101.

## Sync Input Processing

The horizontal and vertical sync input processing circuitry includes sync input buffering, mode (horizontal scan line) selection, and sync waveform conditioning circuits. In addition, horizontal and vertical size, phase, and hold controls are located here.

## Mode Selection

The ZCM-1490 can operate in one of three video modes. In mode 1 (350 scan lines), the monitor can produce an EGA-type display. In mode 2 (400 scan lines), the monitor can produce a CGA-type display (double-scanned). In mode 3 (480 scan lines), the monitor can produce a VGA-type display. In all three modes, the video source supplying the monitor must be a 31.49 kHz analog RGB signal.

The mode of operation is determined by the polarity of the incoming horizontal and vertical sync signals. Table 5-1 lists the required sync polarities for each of the three video modes.

**Table 5-1. Mode Selection**

	Mode 1 (350 line)	Mode 2 (400 line)	Mode 3 (480 line)
Horizontal sync polarity	(+)	(-)	(-)
Vertical sync polarity	(-)	(+)	(-)

Sync input PROM IC1301 produces mode select signals at pins 4 (mode 1), 3 (mode 2), and 5 (mode 3) based on the incoming sync signal polarities as outlined in Table 5-1.

Regardless of the polarity of the incoming sync signals, the polarity of the horizontal sync signal leaving IC1301 at pin 2 is always positive, while the polarity of the vertical sync signal leaving IC1301 at pin 1 is always negative. The vertical sync signal is applied to the base of transistor Q2116 and appears as a positive sync signal at the collector. The horizontal sync signal is applied to the sync processor, IC3401.

## Vertical Processing and Controls

The vertical sync signal at the collector of Q2116 is coupled to the noninverting input of IC2101 at pin 3 through the differentiator formed by CR2122, R2101, and C2103. IC2101 and Q2101 form an oscillator stage. C2101 and R2102 determine the oscillator time constant. IC2101 acts as a comparator with positive feedback, while Q2101 is an emitter follower whose voltage follows that of the output of comparator IC2101 at pin 1. As the output of the comparator changes state from low to high, Q2101 is activated and charges C2115 through CR2102 and R2102. At the same time, the threshold voltage at the noninverting comparator input (pin 3) rises as determined by R2117, R2116, and R2115. C2101 continues to charge until its voltage exceeds that of pin 3,

at which point the comparator output becomes low and the capacitor discharges. The vertical hold control (R2117) controls the threshold voltage at pin 3, thereby changing the free-running frequency of the oscillator.

The external vertical size control (R2153), along with vertical sub-size controls R2158 (mode 1), R2170 (mode 2), and R2124 (mode 3), establish the height of the display. IC2102, Q2102, and Q2105 form a precision current sink that discharges C2105 and C2106 at a linear rate. The sub-size controls determine the discharge current of the circuit, while IC2102 maintains a constant voltage. Thus, as the resistance of the sub-size control is changed, the emitter current of Q2102 changes, as does the collector current. The change in collector current changes the slope of the discharge for capacitors C2105 and C2106, thereby increasing or decreasing the amplitude of the ramp signal.

Transistors Q2103 and Q2104 form a PNP darlington emitter follower pair that acts as a buffer to transform the high-impedance signal at C2105 and C2106 to a lower impedance at R2107. The vertical linearity control (R2107) determines the amount of vertical ramp signal feedback to the junction of C2105 and C2106. This feedback improves the linearity of the sawtooth rise.

## Horizontal Controls

IC3401 and its associated circuitry conditions the horizontal sync signal for use by the horizontal deflection and high voltage circuits. The horizontal sync pulses are applied to pins 8 and 9. The processed output appears at pin 3. The customer horizontal phase control (R3418) and the internal horizontal phase control (R3420) interact with the phase detector circuitry to determine the position of the display within the raster area. The horizontal hold control (R3415) adjusts the horizontal oscillator frequency. The horizontal size control (R3402) interacts with the PIN board circuitry to set the horizontal display width.



# Horizontal Deflection

The horizontal deflection circuitry is responsible for generating the scanning current needed in the horizontal deflection coils to fill the width of the raster. Three main stages are involved here: the horizontal driver, horizontal output, and pincushion (PIN) correction circuits. Because the ZCM-1490 employs a flat technology CRT, the PIN circuitry is more elaborate than in previous monitors. The PIN circuitry is described in a separate section.

## Horizontal Driver

Transistor Q3403 is the horizontal deflection driver. This driver acts as a buffer or isolation stage to prevent the horizontal output circuit from changing the oscillator frequency. The horizontal oscillator output voltage is applied to the base of Q3403. The output of this stage, taken at the collector, is applied to the interstage transformer (TX3401). R3428 and C3409 dampen the primary of TX3401. The transformer steps down the B+ voltage supplied through R3429 to match the low-impedance drive of Q3003. C3009, R3007, and R3009 shape the resulting base drive waveform for Q3003.

## Horizontal Output

Transistor Q3003 is the horizontal output transistor. Refer to the following parts of Figure 5-3 while reading this circuit description. Figure 5-3a shows the output voltage waveform at R3009. The corresponding amplifier current in Figure 5-3b shows that Q3003 is cut off during retrace plus a part of the trace at the left side of the raster. Diode CR3003 conducts during this time, producing part of the trace at the left side of the raster and reducing the average amplifier current (thus increasing efficiency). Figure 5-3c illustrates this damper current. Combining Figures 5-3b and 5-3c yields the sawtooth current needed for a complete trace from left to right, as shown in Figure 5-3d.

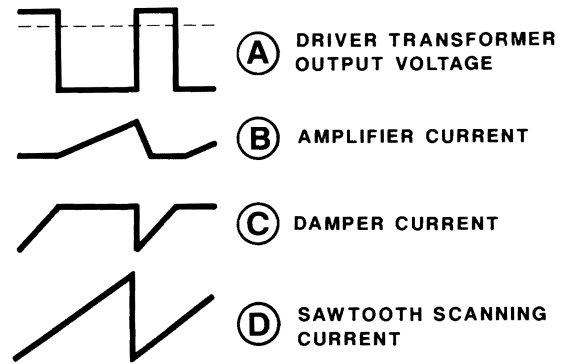


Figure 5-3. Horizontal Output Amplifier Waveforms

Q3003 and CR3003 are the essential parts required for horizontal deflection. Q3003 is the horizontal power amplifier while CR3003 is a damper diode used to increase efficiency. Immediately after flyback, CR3003 is forward-biased by the negative voltage stored in retrace capacitor C3008. CR3003 rectifies the stored energy of the yoke and the core of T3001, thereby recharging capacitors C3006 and C3007. Damping is needed because the oscillations produce white vertical bars at the left side of the raster.

In summary, the resulting current waveshape is related to horizontal scanning as follows:

1. Damped current produces the left side of a trace.
2. As the damped current diminishes and the output stage begins to conduct, the beam is at the center.
3. Current from the output amplifier produces the remainder of the trace.

Series linearity coil LX3002 provides a varying inductance with changing yoke current, resulting in improved linearity. R3003 and C3004 prevent ringing in the coil which might occur with fast changes in signal.

## Horizontal Centering

The horizontal centering control (R3001) electrically centers the display from left to right within the raster area. R3001, Q3001, and Q3002 form a voltage divider. Electrical centering is accomplished by supplying direct current through the horizontal deflection coil.

## Control Grid Voltage

The G1 control grid voltage is developed from the horizontal output applied to transformer T3001. The output is rectified by diode CR3002 and then regulated at approximately  $-40$  VDC by CR3004.

## Anode Voltage

The high voltage required by the anode is developed from the horizontal oscillator output. This signal is applied to the base of driver Q3201 and then to transformer TX3201. The signal from the secondary of TX3201 is in turn applied to anode voltage driver transistor Q3202, which feeds the flyback transformer (TX3202) to produce the required high voltage. The high-voltage output of TX3202 is rectified before being applied to the anode. The focus and G2 voltages are derived at the high-voltage resistor block. The focus control determines the voltage on the last grid of the CRT, thereby regulating the spot size of the beam in order to produce sharp scanning lines.

## Anode Voltage Regulator

The anode high voltage is dynamically regulated by IC3201, Q3205, Q3206, Q3203, Q3202, and their associated circuitry. The anode voltage is sensed through a voltage divider and applied to the non-inverting input of IC3201. A reference voltage is established at the inverting input of IC3201 by IC3202 and R3221 (or the associated resistors and jumpers). IC3201 is a difference amplifier which drives Q3205 based on the difference between the the reference

and feedback voltages at its input terminals. Q3205 drives regulating transistors Q3204 and in turn, Q3205. Q3206 provides additional feedback to insure a stable regulated output voltage from this stage. CR3205, CR3206, CR3216, and CR3217 are protection diodes that limit input transients to IC3201.

## High Voltage Shutdown

The high voltage shutdown circuitry disables the horizontal drive input to the anode voltage circuitry when the anode voltage exceeds a certain limit set by circuit parameters. When the shutdown circuit is activated, the collector of Q3207 is held at a DC voltage by emitter resistor R3228. This voltage, appropriately divided by R3232 and R3233, activates Q3208. The horizontal sync pulses at the collector of Q3208 are directed to ground when this transistor is switched on, thereby disabling the base drive to Q3201 and shutting down the high voltage circuitry.

Q3209 senses the CRT anode current at the secondary of the high voltage transformer. If excessive beam current is being drawn, the cathode of CR3207 is forced negative, thereby turning Q3207 on. R3253-R3256 control the high voltage shutdown point by adjusting the shutdown threshold voltage of IC5203. As the sensed voltage at R3230 becomes negative enough to turn Q3207 on, the high voltage shutdown occurs.

## Automatic Brightness Limiter

The automatic brightness limiter is a feedback circuit that limits the maximum CRT anode current. The current is sampled at the secondary of the high voltage transformer through transistor Q3210. This sample is passed on to connector 5S6 on the video module. R5111 and C5119 average this signal and apply it to pin 1 of IC5101. As the average anode current exceeds  $750 \mu\text{A}$ , the gain of the video amplifiers is decreased to limit the maximum anode current.

## Vertical Deflection

The vertical deflection circuitry is responsible for generating the scanning current needed in the vertical deflection coils to fill the raster from top to bottom. The vertical sawtooth waveform is sensed by R2127 and applied to IC2101 pin 6. A sample of the vertical output is also fed back to this IC. Diodes CR2114 and CR2115 limit the swing of the signal input applied to IC2101. The output of this IC is applied to driver transistor Q2106.

The output at the collector of Q2106 is applied to the input of the complementary-symmetry amplifier formed by Q2107 and Q2108. Note that Q2107 is a PNP-type transistor, while Q2108 is an NPN-type. The complementary-symmetry, or push-pull action of these two transistors occurs as follows. For a positive-going sawtooth at the base of Q2106, a negative-going drive is applied at the base of Q2107, increasing its collector current. The same negative-going drive applied at the base of Q2108 reduces the forward voltage at the base, resulting in less collector current for this NPN transistor.

Similarly, when a negative-going sawtooth is applied to the base of driver Q2106, a positive-going drive is applied at the base of Q2108, increasing its collector current. In a like manner, less collector current results in Q2107.

Diodes CR2107 and CR2108 set the crossover bias and determine the time that both Q2107 and Q2108 will be active during the middle portion of the sawtooth.

To quicken the vertical retrace action, a "boosted" voltage is generated for retrace. As the yoke voltage rises, Q2110 senses the rise in voltage at its base and activates. This in turn activates retrace switch transistor Q2109. During the scan time prior to

retrace, C2119 in the emitter circuit of Q2109 charges to about +72 V through RX2139, RX2138, and CR2112. When Q2109 is activated at the start of retrace, the stored voltage at C2119 is applied to the collector of Q2108. At this point, Q2108 is conducting and the voltage is transferred to the yoke. The "boosted" voltage causes retrace to occur much faster than it otherwise would.

Diode CR2109 couples +16 VDC to the collector of Q2108 during scan time; during retrace time, it is reverse-biased as the boosted voltage is applied. CR2113 protects the base-emitter junction of Q2109 against reverse-bias damage. CR2114 and CR2115 protect IC2101 from static discharge at the inputs.

Capacitor C2112 performs two functions. First, it increases the load impedance in the collector circuit of Q2106. Because the output circuit may produce crossover distortion with large signals, a large amount of feedback is incorporated to compensate for this. To accommodate this feedback, more gain is required. C2112 supplies positive feedback, increasing the load impedance presented to driver Q2106, and thereby increasing the gain. Second, C2112 maintains Q2108 in a conducting state at all times. This is necessary because large positive peaks in the signal can cut Q2108 off by placing the base and emitter at the power supply potential. The voltage stored across C2112 while the circuit is idling keeps Q2108 conducting at all times.

## Vertical Centering

The vertical centering control (R2148) electrically centers the display from top to bottom within the raster area. R2148, Q2111, and Q2112 form a voltage divider. Electrical centering is accomplished by supplying direct current through the vertical deflection coils.

# Blanking Pulses

The composite blanking pulse signal is generated from the vertical and horizontal flyback pulses. Transistors Q2117, Q3401, and associated circuitry produce these blanking pulses. Refer to Figure 5-4. The vertical pulse is AC-coupled to the blanking circuit by C2118. Zener diode CR2116 limits this pulse to 5.6 V. The pulse is applied to the base of Q2117, activating it and, in turn, bringing the base of Q3401 to ground. With Q3401 now off, +5 V appears at the collector for the duration of the vertical blanking interval.

Similarly, the -70 V horizontal flyback pulse is AC-coupled by C3413 to the base of Q3401. A negative pulse shuts off Q3401, resulting in a +5 V blanking pulse at the collector for the duration of the horizontal blanking interval.

Diode CR3404 conducts during the retrace portion of the horizontal flyback pulse to prevent reverse-bias damage to Q2117 and Q3401. During the trace portion of the horizontal flyback pulse, CR3404 conducts and holds the collector of Q3401 low. Thus, a composite blanking pulse appears at the collector of Q3401.

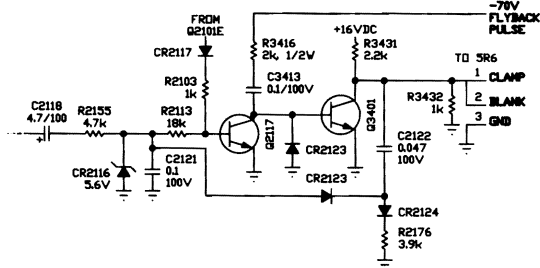


Figure 5-4. Blanking Pulse Circuit

# Pincushion Correction

As noted earlier, this monitor incorporates the new flat technology CRT. Because this is a perfectly flat display, a more complex pincushion (PIN) correction must be performed to produce a geometrically correct display. The PIN circuitry can be broken into four functional blocks: an east-west waveform generator, an east-west regulator, a north-south waveform gen-

erator, and a north-south output circuit. Each block is explained individually in the following sections.

# East-West Waveform Generator

The east-west (E-W) waveform generator produces the PIN correction waveform for the left and right sides of the display. The resulting waveform modulates the B+ voltage supplied to the horizontal deflection circuitry at the vertical scan rate. In this way, the left and right sides of the display can be corrected as the beam deflects vertically.

The E-W waveform generator produces three waveforms which are then combined to form the final E-W PIN correction waveform. A parabolic waveform is generated to correct parabolic distortion at the left and right sides of the raster. A ramp waveform at the vertical scan rate is added to the parabola to correct trapezoidal distortion at the left and right sides of the raster. A sine wave at the vertical scan rate is generated and added to the parabola to correct phase errors in this waveform. Refer to Figure 5-5.

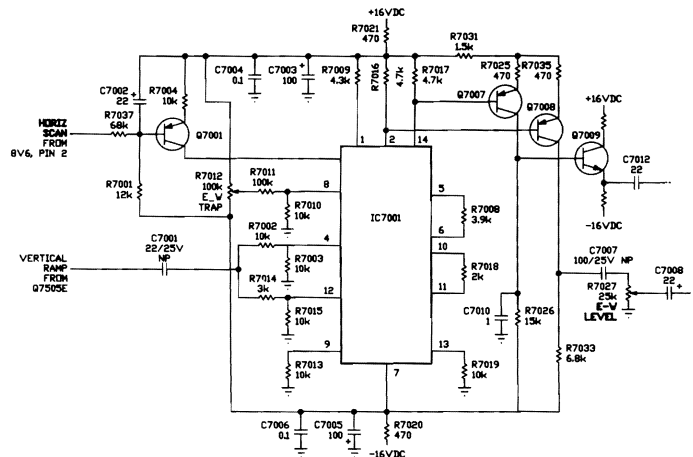


Figure 5-5. E-W Waveform Generator

A multiplier circuit (IC7001) is used to generate the parabolic waveform. The multiplier produces an output that is a product of its input terms (the X and Y input signals) and a constant (denoted by "K"). A vertical ramp at pin 5 of connector 8U6 is buffered by transistor Q7505. This ramp is coupled to the multiplier inputs of IC7001 by C7001, R7002, and R7014.

Pin 4 of IC7001 is the Y(+) multiplier input, pin 8 is the Y(-) multiplier input, pin 9 is the X(+) multiplier input, and pin 12 is the X(-) multiplier input. Each of these inputs is biased and balanced by a corresponding resistor: R7003 for pin 4, R7010 for pin 8, R7013 for pin 9, and R7015 for pin 12. When the inputs are balanced, a vertical ramp applied to both pins 4 and 12 will produce a parabola at the output of the multiplier.

A ramp waveform at the vertical scan rate is added to the parabola to correct trapezoidal distortion at the left and right sides of the raster. To add the ramp to the parabola, the bias of the (balanced) inputs of multiplier IC7001 is offset. When the bias is offset, a portion of one of the input signals is present at the output of the multiplier. In this manner, the vertical ramp is "added" to the parabolic waveform. The input bias is offset by R7011 and R7012, the E-W trap (trapezoid) control. R7012 adjusts the amount of offset to obtain the desired amplitude and polarity of the vertical ramp to be added to the parabolic waveform.

The outputs of multiplier IC7001 are applied to the differential amplifier formed by transistors Q7007 and Q7008. The output from pin 2(+) is applied to the base of Q7008. The output of Q7008 is coupled to the E-W level control (R7027) by C7007. R7027 controls the amplitude of the parabolic waveform. The signal from the E-W level control is coupled to the E-W regulator.

The multiplier output from pin 14(-) is applied to the base of Q7007. The output of Q7007 (a parabolic waveform) is integrated by C7010 to form a sine wave. This is the sine wave mentioned earlier that is added to the parabolic waveform to correct phase errors. The sine wave is buffered by Q7009 and applied to the E-W phase control (R7039). The signal from the E-W phase control is applied to the E-W regulator.

The E-W waveform generator must also produce the proper correction waveform regardless of changes in horizontal and vertical display sizes. A vertical size change is automatically compensated for because the vertical ramp amplitude determines the vertical display size. Thus, a larger ramp at the input of the multiplier circuit results in a correspondingly larger output. To compensate for a change in the horizontal

display size, the B+ voltage supplied to the horizontal deflection circuitry is sampled and used to adjust the correction waveform accordingly.

The B+ voltage at pin 2 of connector 8V6 is scaled and filtered by R7037, R7001, and C7002. Transistor Q7001 compares the resulting signal to a fixed voltage of about 12V (sensed by R7004). The output of this transistor is applied to the K (multiplication constant) input (pin 3) of IC7001. As the sampled B+ voltage changes at the base of Q7001, the current applied to the K input of IC7001 changes. Because the output of the multiplier circuit is KXY (a constant times the X and Y inputs), the K factor corrects the resulting parabolic waveform as the horizontal size changes. In this manner, changes in either the horizontal or vertical size are compensated for.

## East-West Regulator

The E-W regulator determines how much of the E-W correction waveform is imposed onto the horizontal scan voltage. It also supplies the current (with the correction waveform) to the horizontal deflection circuitry. Refer to Figure 5-6.

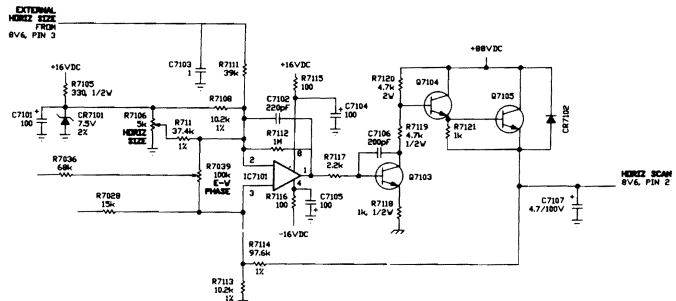


Figure 5-6. E-W Regulator

The output of the E-W level control (R7027) is coupled to the non-inverting input of IC7101 by C7008 and R7028. R7027 controls the amplitude of the parabolic waveform that is applied to IC7101.

The output of the E-W phase control (R7039) is applied to both the inverting and non-inverting inputs of IC7101. When this control is set to its midpoint, the sine wave formed by integrating the parabola signal at C7010 is applied equally to both inputs. Thus, no part of the sine wave appears at the output of

IC7101. As the E-W phase control is offset from its midpoint, a part of the sine wave signal appears at the output of IC7101.

A sample of the output voltage of the E-W regulator is also applied to IC7101 through the divider formed by R7113 and R7114. A reference voltage generated by CR7101 is divided by R7106 and applied as to IC7101. R7106 is the main horizontal size control. Altering the reference voltage supplied to IC7101 by this control alters the horizontal size. The external horizontal size control (R3402, located on the deflection board) also alters this reference voltage, but with a limited range. IC7101 combines these signals to produce an E-W PIN correction waveform at its output (pin 1).

The E-W correction waveform is inverted and buffered by transistor Q7103. Q7104 provides current gain for the E-W pass regulator transistor. The pass

regulator transistor (Q7105) passes the current to the horizontal deflection circuit and drops the voltage. In this manner, the E-W PIN correction waveform is superimposed onto the horizontal scan voltage.

## North-South Waveform Generator

The north-south (N-S) waveform generator produces the PIN correction waveform for the top and bottom of the display. The resulting waveform modulates the vertical ramp at the horizontal rate. The purpose is to increase the vertical deflection at the top center and bottom center of the display. In addition, as the electron beam approaches the center of the screen (from the top), the correction waveform must diminish, then reverse phase and increase again as the electron beam moves toward the bottom of the screen. Refer to Figure 5-7.

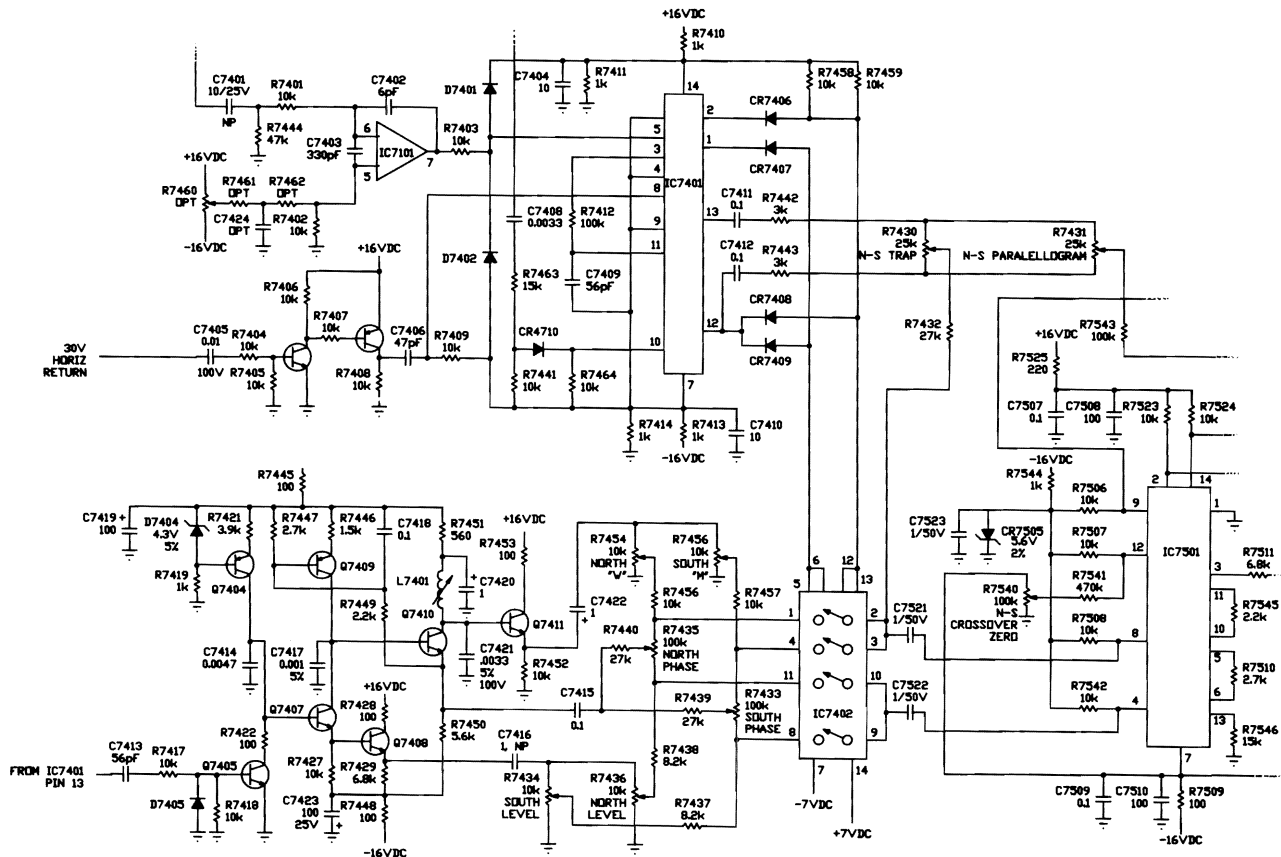


Figure 5-7. N-S Waveform Generator

The 30V horizontal retrace pulse at pin 1 of connector 8V6 is coupled to a signal-shaping circuit formed by transistors Q7402 and Q7401. The resulting signal at the collector of Q7401 is a pulse with a fast rising edge and a delayed, slow falling edge. This shaped pulse is differentiated by C7406 and R7409 and applied to the set input (pin 8) of IC7401, a dual D-type flip-flop. This half of IC7401 is configured as a one-shot multivibrator. (A one-shot multivibrator converts an input pulse of short duration to an output pulse of longer duration.) An RC network formed by R7412 and C7409 delays the clock input signal to pin 11 of IC7401 by approximately 4  $\mu$ S. This delay in effect sets the duration of the output pulse. Thus, when the shaped pulse from Q7401 is applied to the set input, output Q2 at pin 13 becomes logic high. The RC network samples this logic high output, delays it by about 4  $\mu$ S, and applies it to the clock input (pin 11). When the clock input goes high, the signal at the D input (pin 9) causes Q2 to go low. C7408, R7463, and R7441 differentiate the vertical retrace pulse. CR7410 and R7464 sense this and apply it to the reset input of flip-flop IC7401, thereby resetting the flip-flop at the start of each vertical frame. This prevents flip-flop "latchup" caused by static discharge.

The Q2 signal at pin 13 of IC7401 is coupled to transistor Q7405. This transistor, along with C7414, Q7404, and D7404, forms a horizontal ramp generator. C7414 is charged by the current source formed by Q7404, D7404, and associated components. A pulse at the base of Q7405 causes this transistor to conduct, thereby discharging C7414. The horizontal ramp is formed in this manner. This ramp is buffered by transistors Q7407 and Q7408 and coupled to the south level (R7434) and north level (R7436) controls.

A parabolic waveform is also generated to correct north and south phase. Transistor Q7407 is a modulated current sink for the parabola generator. This transistor, along with C7417 and Q7409, forms a parabola generator. C7417 is charged by the current source formed by Q7409 and associated components. The modulated signal at the base of Q7407 causes this transistor to conduct, thereby discharging C7417. To stabilize the DC bias point of C7417, the current source (Q7409) is DC-modulated by feed-

back from Q7410. The parabolic waveform is formed in this manner. This waveform is buffered by Q7410 and coupled to the south phase (R7433) and north phase (R7435) controls.

Q7410 also acts as a current sink for the resonant circuit formed by C7421 and L7401. A sinewave at twice the horizontal frequency is present at C7421. L7401 adjusts the phase of this sinewave. Q7411 buffers the sinewave for the North "W" (R7454) and South "M" (R7456) controls.

IC7402 is a CMOS switch activated by the appropriate signals from the Q outputs of IC7401. The switches within IC7402 are configured (by external connections) as single pole double throw switches. In this way, the proper set of controls (either north or south) is connected to the following stages based on which half of the raster is being scanned (either the top or bottom). Diodes CR7406 and CR7407 activate the CMOS switches based on the Q1 and not-Q1 signals from IC7401, pins 2 and 1 respectively. Diodes CR7408 and CR7409 open both sets of switches during horizontal retrace time based on the not-Q2 signal from IC7401, pin 12.

The processed horizontal rate signals, routed through IC7402 from previous stages, are applied to the carrier inputs of a balanced modulator-demodulator (IC7501). (A balanced modulator-demodulator forms an output voltage which is a product of an input signal and a carrier.) IC7501 and its associated circuitry modulate the horizontal rate signal (the carrier) with a vertical ramp (the input signal) such that as the beam approaches the center of the screen (from the top), the amplitude of the signal decreases to zero. As the beam crosses the center of the screen, the amplitude again begins to increase, but the phase is now reversed for scanning the bottom half of the screen. The vertical ramp is coupled to IC7501 through C7501 from buffer transistor Q7505. The north-south crossover zero control (R7450) adjusts the crossover point where the horizontal signal amplitude is reduced to zero and the phase reverses. Bias for IC7501 is supplied by Q7502 and Q7503 as a function of the horizontal scan voltage. The gain of this stage is set by R7510 and R7545.

## North-South Output

The N-S output circuit provides the current to modulate the vertical ramp at the horizontal rate. Refer to Figure 5-8. The output of IC7501 is coupled to operational amplifier IC7502. The positive polarity output (pin 6) is applied to the noninverting input of IC7502 and the negative polarity output (pin 12) is applied to the inverting input. The signal from the N-S parallelogram control (R7431) is also added to the noninverting input through R7543. IC7502 provides gain to drive op-amp IC7503. Power amplifier IC7503 in turn drives step-up transformer T7501.

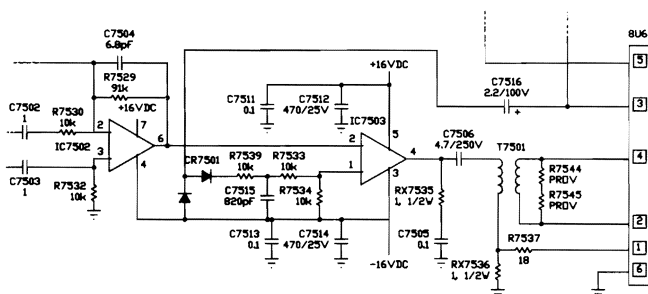


Figure 5-8. N-S Output

The secondary of T7501 is in effect in parallel with the vertical yoke and the N-S pincushion correction waveform is thus imposed onto the vertical output. Although the secondary of T7501 is in series with the vertical yoke, the output of the vertical scan is at AC ground compared to the horizontal rate signal, and the yoke coupling capacitor and resistor present a low impedance.] Thus, T7501 is in effect in parallel with the vertical yoke.

## Dynamic Focus

The dynamic focus circuitry varies the focus voltage at the horizontal rate so that the voltage at the raster edges is increased and the voltage at the center is decreased. The horizontal rate waveform is applied to the base of Q7701. R7703 controls the amplitude of the signal applied to the dynamic focus circuit. Q7701 and Q7703 amplify the incoming waveform. T7701 steps up the resulting waveform to generate the 500V p-p focus voltage.

## Degaussing Coil

Degaussing refers to demagnetizing the iron and steel parts of the picture tube, in particular the steel shadow mask and frame within the CRT. This is necessary because a steady magnetic field magnetizes these parts and affects the beam register on the color phosphors, resulting in poor purity.

A degaussing coil is wrapped around the CRT and controlled by a positive temperature coefficient thermistor in the power supply. When the monitor is first turned on, current flows through the thermistor and activates the degaussing coil. As the thermistor heats up, its resistance becomes very high and the degaussing coil is deactivated. The thermistor can require up to 30 minutes to cool and reset before the degaussing coil can be reactivated.



# Chapter 6

## Troubleshooting

This chapter provides information on troubleshooting the ZCM-1490 color video monitor. Enough information is included to assist in diagnosing most faults to the major component level.

General troubleshooting information is included in the beginning sections of this chapter. Read these sections before proceeding. They contain important safety guidelines, initial tests and diagnostics, and other important information.

Following this general information is a series of troubleshooting flowcharts. These charts are designed to assist in diagnosing faults to the major component level when used with the schematics and waveform photographs in Chapter 8. Always begin with the General Troubleshooting Chart. This chart will direct you to an adjustment or to a more detailed chart.

Waveform photographs and schematics are located in Chapter 8. Refer to these as directed when troubleshooting or performing adjustments. Read the "Troubleshooting Charts" section in this chapter and "Waveform Explanations" in Chapter 8 before using the waveform photographs.

Voltage and resistance measurement tables are included after the troubleshooting charts. Use these tables when specific circuits are suspected or when the monitor cannot be turned on for tests.

In the ZCM-1490, measurements on the deflection board cannot be made safely while the monitor is on. To gain access to this board, it must be removed from the monitor chassis. With the exception of a few

specific test points, this board must be serviced by first identifying the symptom and then using the resistance measurement tables to isolate the faulty components. Use the troubleshooting charts to begin by identifying possible problem areas.

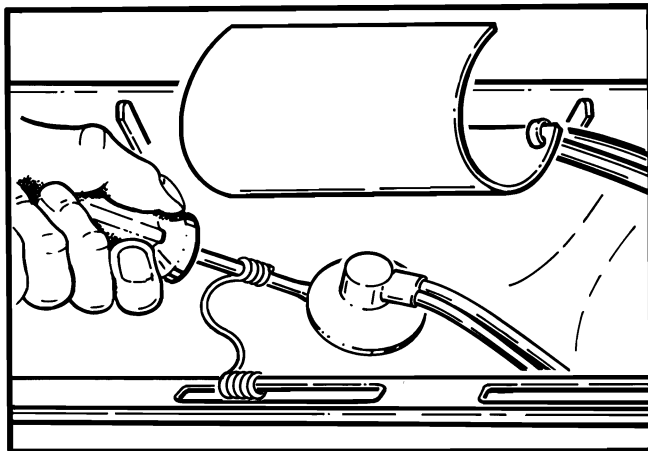
### Safety Guidelines

Read the following safety notes carefully before attempting to troubleshoot or service this monitor.

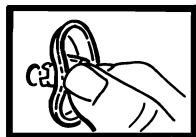
#### WARNING

The CRT anode retains a potentially lethal voltage even when the monitor is turned off. Perform repairs only after the CRT anode has been properly discharged. Refer to Figure 6-1 and the following procedure to discharge the CRT anode:

1. Connect a clip lead or heavy gauge wire to chassis ground.
2. Connect the other end of the lead to the stem of a flat blade screwdriver that has an insulated handle.
3. Insert the blade of the screwdriver under the rubber insulation that covers the anode lead on the CRT and make contact with the anode terminal. Depending on the amount of charge present on the anode, a distinct snap may be heard as the CRT discharges.



1. CAREFULLY SLIDE A GROUNDED FLAT SCREWDRIVER TIP UNDER THE LIP OF THE ANODE LEAD.



2. AFTER DISCHARGING THE VOLTAGE, DISCONNECT THE ANODE LEAD FROM THE CRT.

Figure 6-1. CRT Anode Discharging

### WARNING

The switch mode power supply contains circuits that generate dangerous high frequency, high amplitude, quasi-square wave signals that present a potentially lethal shock hazard. In the ZCM-1490, this circuitry is located on a separate, exposed circuit board located along the left side of the monitor when viewed from the back. Do not attempt to service the power supply.

### WARNING

To prevent both personal injury and equipment damage, always use an isolation transformer when troubleshooting this monitor.

### CAUTION

Under no circumstances should the original design be modified or altered without per-

mission from Zenith Electronics Corporation. All components should be replaced only with types identical to those in the original circuit, and their physical location, wiring, and lead dress must conform to the original layout upon completion of repairs.

## AC Leakage Test

Repair and reassembly of the monitor can inadvertently result in the loss of electrical isolation between the AC power wires and the exposed metal parts of the monitor. If this isolation is lost or significantly reduced, electrical shock can result.

Any AC voltage leak that exceeds 0.75 V rms (0.5 mA) constitutes a potential shock hazard and must be corrected. To prevent electrical shock after reassembly, perform an AC leakage test on all exposed metal parts of the monitor using the following procedure (do not use an isolation transformer during this test):

1. Construct an AC leakage voltmeter circuit as shown in Figure 6-2 using the following parts:
  - An AC voltmeter with an internal impedance of 5 K $\Omega$  or more. The overall range of the meter is not critical but the 0 to 0.75 V range must be easy to read accurately.
  - An AC-type 0.15  $\mu$ F capacitor.
  - A 1500  $\Omega$ , 10 watt resistor.
2. Connect one side of the test circuit to a good earth ground, such as a water pipe, and the other side to an exposed metal part of the monitor.
3. With the monitor turned on, measure the voltage leak between the earth ground and the monitor. Verify that any AC leakage is less than 0.75 V rms (0.5 mA).
4. Reverse the meter leads and repeat the measurement.

- Repeat steps 3 and 4 until all exposed metal parts are verified to have AC leakage levels less than 0.75 V rms (0.5 mA).

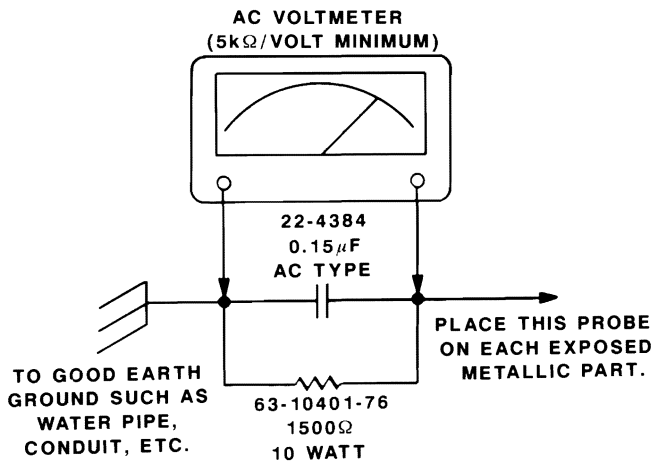


Figure 6-2. AC Leakage Voltmeter Circuit

## Suggested Tools and Equipment

The following tools and supplies are recommended for servicing the monitor:

- Flat-blade screwdrivers
- Philips screwdrivers
- Hex drivers
- Plastic alignment tools
- Diagonal cutters
- Wire strippers
- Long nose pliers
- Soldering iron, 25 to 40 watt
- Solder, 60/40
- Desoldering braid
- Plastic cable ties.

The following equipment is recommended for troubleshooting the monitor as described in this chapter:

- Z-100 or Z-200 Series PC-compatible computer or equivalent
- Disk-based diagnostics (CB-5063-28)

- Z-449 31.49 kHz analog video card or equivalent
- Oscilloscope — DC to 100 MHz, dual trace, triggered sweep (Tektronix Model 2235 or equivalent)
- Oscilloscope probe — low capacitance, 4 ns rise time (Heath Model PKW-105 or equivalent)
- Digital voltmeter — high-impedance input, 0 to 1000 V, 0 to 1 megohm (Heath Model SM-2215 or equivalent)
- High-voltage probe — 0 to 40 KV (Heath Model IM-5215 or equivalent)
- Isolation transformer.

## Inspection and Preparation

Before turning the monitor on, inspect the power cord, video cable, and all connectors for damaged insulation or loose prongs. Inspect the exterior of the monitor for signs of damage. If physical damage is evident, remove the cabinet back and inspect further before proceeding.

If these preliminary checks do not indicate a problem, proceed as follows:

1. Connect the video cable from the monitor to the computer.
2. Turn the computer and monitor on. Observe the display for faults and refer to the troubleshooting charts in this chapter only after reading the remaining procedures in this section.
3. Allow the monitor to warm up for approximately 30 minutes, unless a fault diagnosed in step 2 prevents this.
4. Perform the ROM-based color bar test and other tests as necessary. The instructions for performing these tests are included here for convenience.

## Color Bar Test

The ROM-based color bar test can be used to set the display brightness and contrast to comfortable levels. To display the color bars using a Zenith Data Systems PC-compatible computer:

1. Press the CTRL, ALT, and INS keys in sequence, hold them, and then release them.
2. After the Monitor prompt appears, press C and then press RETURN.
3. Color bars, in the form of a gray scale, should now be displayed.

Use this test in conjunction with the troubleshooting charts at the end of this chapter.

## Fill Screen Test

The ROM-based keyboard test can be used to set the brightness, contrast, focus, and dimensions of the display to comfortable levels. This test fills the screen with any character entered from the keyboard. To perform the fill screen test:

1. Press the CTRL, ALT, and INS keys in sequence, hold them, and then release them.
2. After the Monitor prompt appears, type TEST and then press RETURN.
3. Select the keyboard test.
4. Press any displayable key to fill the screen with that character. (The capital Z is a good character to display for assessing display characteristics.)

## Disk-Based Diagnostics

The disk-based diagnostics can be used to generate test patterns that may be helpful when performing

display adjustments. The diagnostics are menu-driven. A general procedure for using the diagnostics follows. For further information about the disk-based diagnostics, refer to the documentation supplied with the disk.

1. Boot the disk-based diagnostics.
2. Use the arrow keys to select the computer configuration you are using.
3. Select NO when prompted for the fast test.
4. The diagnostic menu will now be displayed. Use the arrow keys to choose the single test, and then use the arrow keys to choose the video diagnostic menu.
5. The video diagnostic menu will now be displayed. Use the arrow keys to choose the single test, and then use the arrow keys to choose the video patterns. Finally, use the arrow keys to select the coarse grid or the focus pattern as needed.

## Cleaning Procedure

### CAUTION

Unplug the monitor before cleaning. Be sure that the monitor is completely dry before plugging in the unit.

Clean the cabinet with a lint-free cloth, lightly dampened with a mild cleaning solution. Do not spray liquids directly on the monitor or use a wet, saturated cloth.

Clean the screen with a good quality, non-abrasive glass cleaner. The display glass of the ZCM-1490 is treated with an OCLI HEA coating to reduce glare. Fingerprints and smudges are more noticeable with this coating. Glass cleaners containing isopropyl alcohol are effective in removing these marks.

# Surface Mount Component Replacement

This monitor incorporates surface mount technology on many of the circuit boards. To replace a surface mount component:

1. Unsolder the defective component. Use a desoldering braid and a low-wattage soldering iron with a fine tip to remove the solder from the component tabs. Be careful not to form solder bridges with nearby surface mount components.
2. Remove the defective component. The surface mount components are held in place by a small drop of non-conductive cement. Either heat the cement or gently break the component away and remove it.
3. Position the new component. Use a drop of non-conductive cement to hold the component in place on the circuit board. Alternatively, rest the circuit board horizontally and position the new component.
4. Solder the new component. Use a low-wattage soldering iron with a fine tip and solder the new component in place. Be careful not to form solder bridges with nearby surface mount components.

## Troubleshooting Charts

This section contains a series of troubleshooting charts designed to assist in diagnosing faults to the major component level. Use these charts with the schematics and waveform photographs included in Chapter 8. The charts emphasize AC signal analysis and monitor adjustments. Refer to the next section in this chapter for DC voltage and resistance measurements.

Refer to the appropriate schematic as you work through the steps of a troubleshooting chart. While these charts are designed to assist in diagnosing faults, they cannot substitute for the information contained in the schematics.

As noted earlier, measurements on the deflection board cannot be made safely while the monitor is on. With the exception of a few specific test points, this board must be serviced by first identifying the symptom and then using the resistance measurement charts to isolate the suspect components. Use the troubleshooting charts to begin to identify possible problem areas.

Always begin with the General Troubleshooting Chart. This chart will then direct you to check a particular item, to perform an adjustment, or to consult a more detailed chart. The charts are:

- General troubleshooting chart
- Video board troubleshooting chart
- Deflection troubleshooting chart
- PIN Board Troubleshooting Chart
- Power Supply Troubleshooting Chart

The waveform photographs in Chapter 8 are numbered and labeled with a brief identifying note. When a block in a troubleshooting chart directs you to check a waveform, the number of that waveform photograph appears in a circle. The same waveform photograph number appears as a circled number on the schematics in Chapter 8.

Sometimes a particular block of a troubleshooting chart requires additional explanation. In this case, a number is placed in the lower left corner of the troubleshooting block. This number refers you to the notes on the charts. Always read these notes before performing a step.

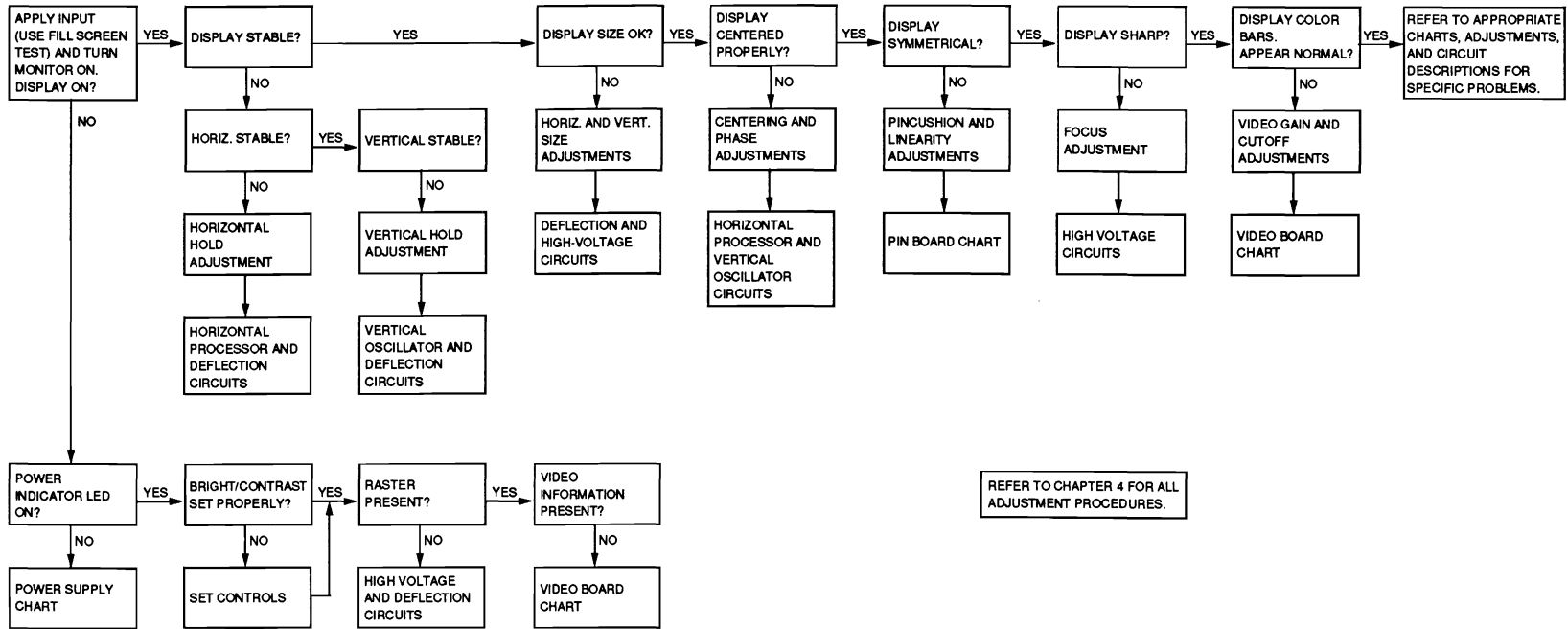


Figure 6-3. General Troubleshooting Chart

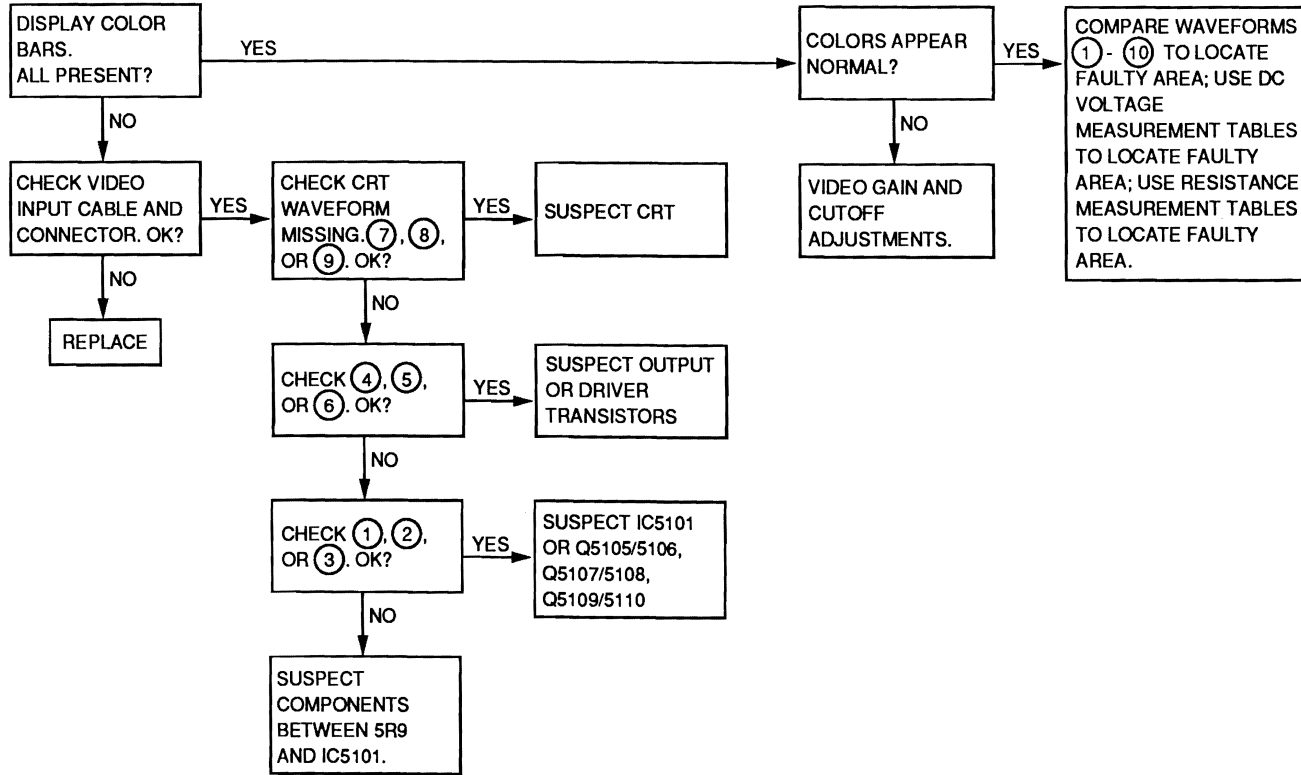
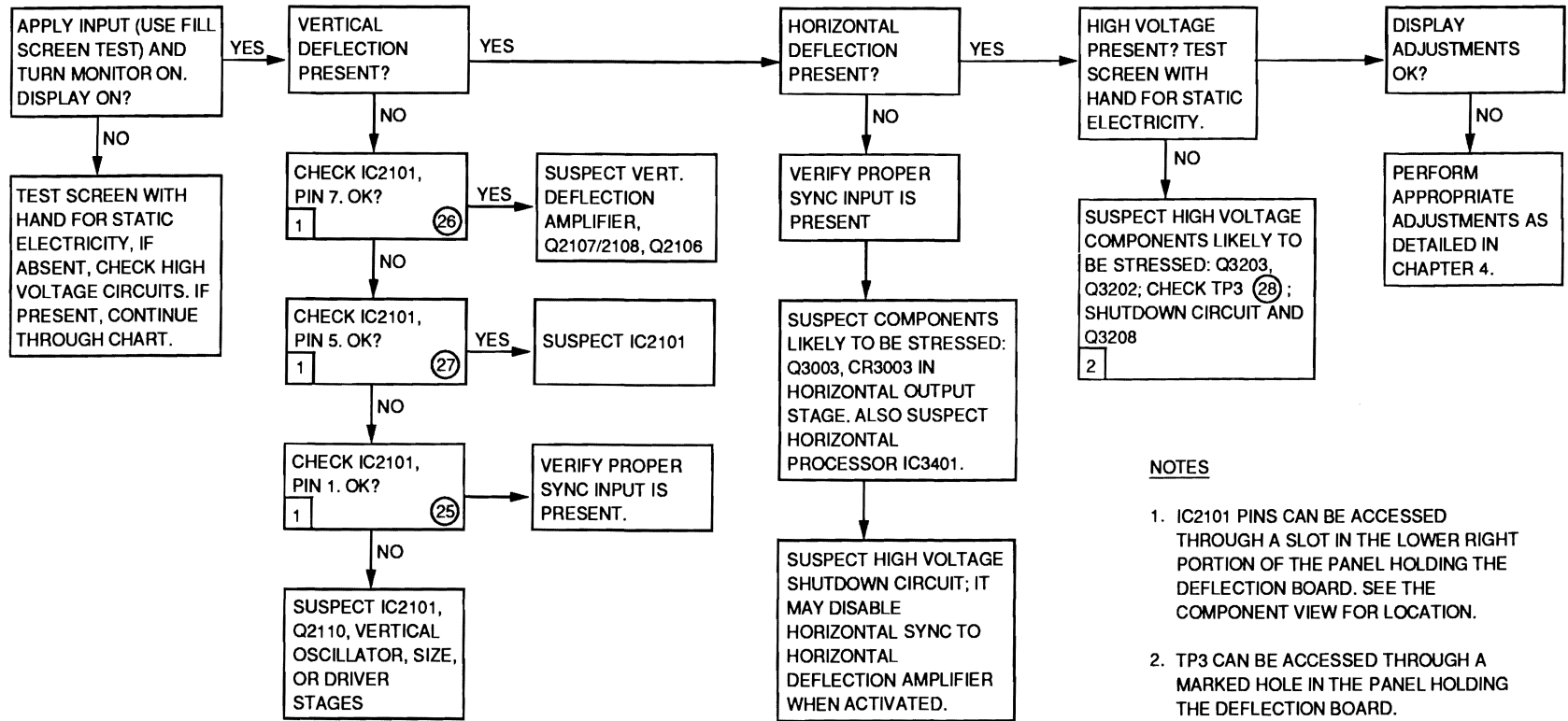


Figure 6-4. Video Board Troubleshooting Chart

THIS CHART CAN ONLY ASSIST IN DIAGNOSING FAULTY CIRCUIT AREAS BY SYMPTOM. WAVEFORM MEASUREMENTS CANNOT BE MADE SAFELY WHILE THE MONITOR IS ON. TO BE SERVICED, THIS BOARD MUST BE REMOVED FROM THE MONITOR. USE THE RESISTANCE MEASUREMENT TABLES TO IDENTIFY FAULTY COMPONENTS AFTER A FAULTY CIRCUIT AREA IS IDENTIFIED.



NOTES

1. IC2101 PINS CAN BE ACCESSED THROUGH A SLOT IN THE LOWER RIGHT PORTION OF THE PANEL HOLDING THE DEFLECTION BOARD. SEE THE COMPONENT VIEW FOR LOCATION.
2. TP3 CAN BE ACCESSED THROUGH A MARKED HOLE IN THE PANEL HOLDING THE DEFLECTION BOARD.

Figure 6-5. Deflection Board Troubleshooting Chart



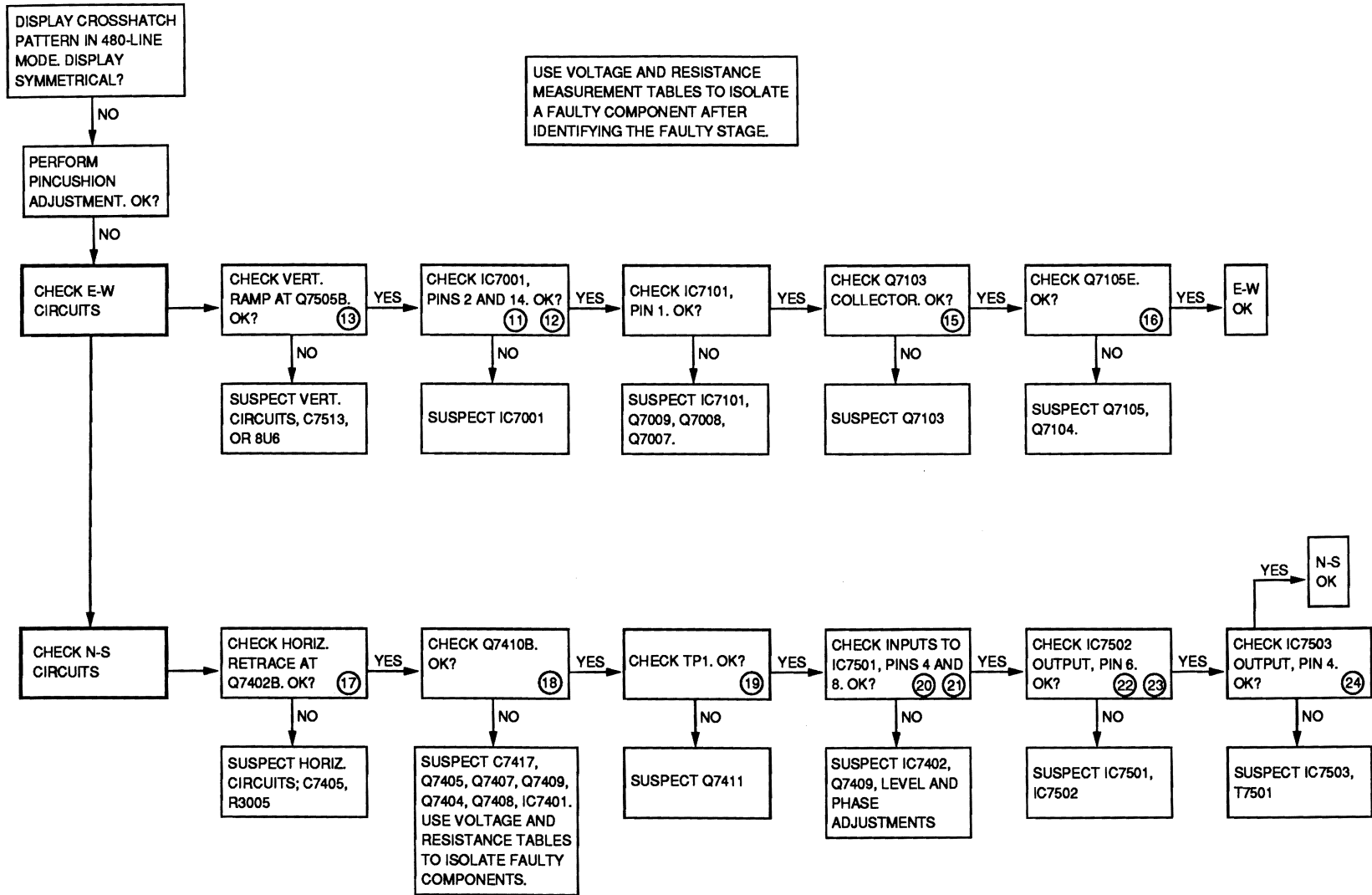


Figure 6-6. Pin Board Troubleshooting Chart

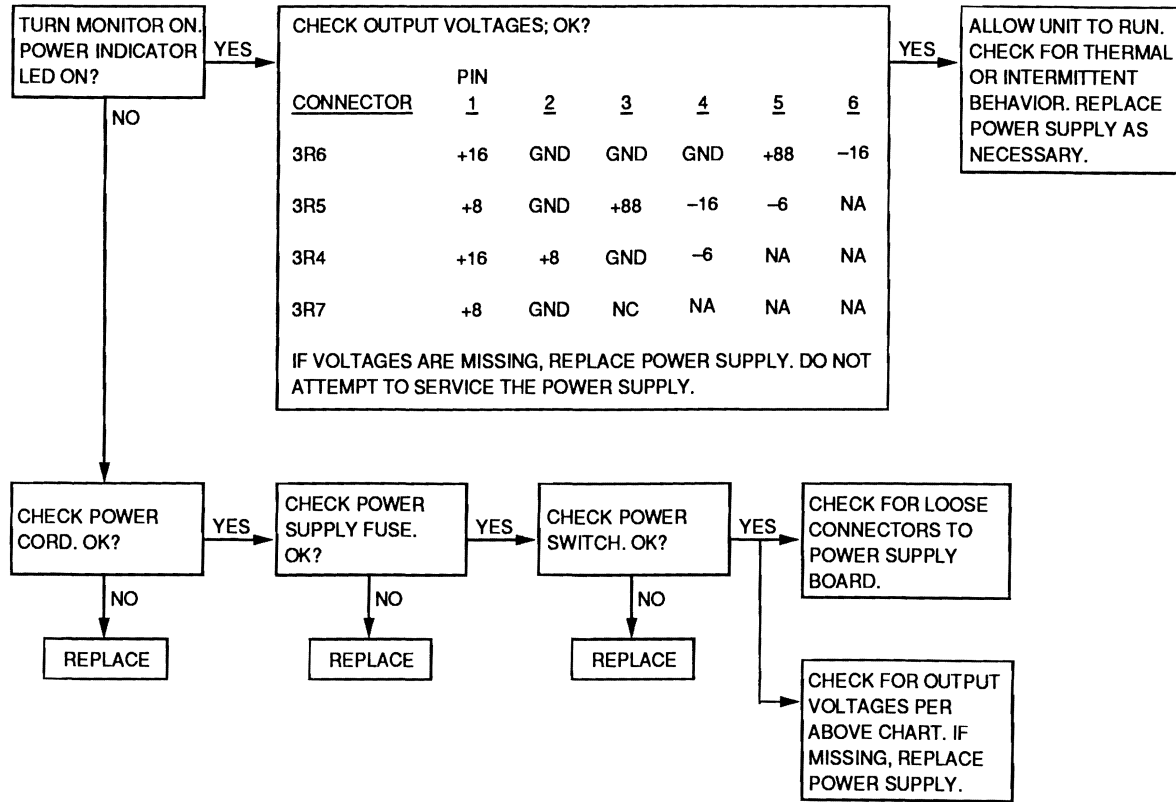


Figure 6-7. Power Supply Troubleshooting Chart

# Resistance Measurements

This section contains the measured resistance to chassis ground for a number of the active devices in the monitor. The measurements were made using a Heath by Fluke SM-77 digital volt-ohm meter. Verify these values with the monitor off and the power cord disconnected. Use these measurements to locate faulty components in the circuitry. A (+) symbol after the value indicates a charging action with an increasing meter reading; a (-) symbol after a value indicates a charging action with a decreasing meter reading.

**Table 6-1. PIN Board Transistor Resistance Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q7001	10.8kΩ	11.6kΩ	3.26MΩ
Q7007	2600Ω(+)	5.46kΩ	15.7kΩ
Q7008	2600Ω(+)	5.38kΩ	6kΩ(+)
Q7009	10kΩ(+)	15.7kΩ	200Ω(+)
Q7401	150kΩ(+)	20.3kΩ	10.1kΩ
Q7402	0Ω	10kΩ	10.3kΩ
Q7404	4.21kΩ	994Ω	3.35MΩ
Q7405	0Ω	1673Ω	3.31MΩ
Q7407	10.6kΩ	3.3MΩ	3.13MΩ
Q7408	7.42kΩ	10.6kΩ	200Ω(+)
Q7409	1825Ω	2230Ω	3.14MΩ
Q7410	2845Ω	3.14MΩ	880Ω
Q7411	10kΩ	850Ω(+)	200Ω(+)
Q7502	8.62kΩ	0Ω	1500Ω(+)
Q7503	8.62kΩ	11.9kΩ	3.35MΩ
Q7505	1445Ω	1023Ω	326Ω

**Table 6-2. PIN Board IC Resistance Measurements**

PIN	IC7001	IC7101	IC7401	IC7402	IC7501	IC7502
1	3.96kΩ	1MΩ	4MΩ	9.26kΩ	0Ω	36.5kΩ
2	5.37kΩ	6.7kΩ	4MΩ	3.4MΩ	10.5kΩ	3.5MΩ
3	3.24MΩ	8.3kΩ	3.9MΩ	3.4MΩ	3.3MΩ	10kΩ

**Table 6-2 (continued). PIN Board IC Resistance Measurements**

PIN	IC7001	IC7101	IC7401	IC7402	IC7501	IC7502
4	7kΩ	700Ω(-)	600Ω(+)	9.3kΩ	11.4kΩ	600Ω(-)
5	12.3MΩ	10.1kΩ	1.3MΩ	10.5kΩ	11.9MΩ	36.4kΩ
6	12.3MΩ	56Ω	600Ω(+)	10.5kΩ	11.9MΩ	3.6MΩ
7	800Ω(+)	1.34MΩ	600Ω(+)	600Ω(+)	600Ω(-)	100Ω(+)
8	9.29kΩ	200Ω(+)	10.6kΩ	11kΩ	11.4kΩ	
9	10kΩ	-	600Ω(+)	3.5MΩ	11.5kΩ	-
10		-	10.7kΩ	3.5MΩ		-
11		-	4MΩ	10.9kΩ		-
12	7kΩ	-	4MΩ	10.6kΩ	11.2kΩ	-
13	10.1kΩ	-	3.9MΩ	10.6kΩ	15.3kΩ	-
14	5.43kΩ	-	560Ω	550Ω	10.5kΩ	-

**Table 6-3. Video Board Transistor Resistance Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q5101(SM)	3.3kΩ	12.3kΩ	655Ω
Q5102(SM)	1280Ω	1722Ω	3.36kΩ
Q5104(SM)	1258Ω	3.36kΩ	655Ω
Q5105(SM)	95.3Ω	432Ω	1120Ω
Q5106(SM)	755Ω	1120Ω	480Ω
Q5107(SM)	94.8Ω	430Ω	1120Ω
Q5108(SM)	756Ω	1120Ω	484Ω
Q5109(SM)	96Ω	430Ω	1126Ω
Q5110(SM)	756Ω	1126Ω	478Ω
Q5201	67.4Ω	441Ω	
Q5202		953Ω	
Q5203	3.5MΩ(+)	5kΩ(-)	2900Ω(+)
Q5204	3.5MΩ(+)	0.1Ω	
Q5205	67.7Ω	442Ω	
Q5206		954Ω	
Q5207	2.2MΩ(+)	5kΩ(-)	2900Ω(+)
Q5208	3.5MΩ(+)	0.1Ω	
Q5209	67.6Ω	453Ω	
Q5210		954Ω	
Q5211	3.3MΩ(+)	5kΩ(-)	2900Ω(+)
Q5212	3.5MΩ(+)	0.1Ω	
Q5301	3.5MΩ	3.8kΩ	0.1Ω
Q5302	3.47MΩ	5kΩ(-)	0.1Ω
Q5303	3.45MΩ	5kΩ(-)	0.1Ω
Q5304	130Ω	3.12MΩ	7.67kΩ

**Table 6-4. Video Board IC Resistance Measurements**

PIN	IC5101	IC5102
1	11.7kΩ	848Ω
2	1312Ω	0.2Ω
3	10.3kΩ	3.1MΩ
4	4.36MΩ	835Ω
5	10.3kΩ	835Ω
6	4.35MΩ	I
7	639Ω	0.3Ω
8	10.2kΩ	1.46MΩ
9	4.35MΩ	849Ω
10	0.3Ω	0.2Ω
11	1068Ω	3MΩ(+)
12	1433Ω	849Ω
13	661Ω	0.2Ω
14	1058Ω	835Ω
15	1427Ω	
16	655Ω	
17	1068Ω	
18	1430Ω	
19	1698Ω	
20	0.2Ω	

**Table 6-5. Deflection Board Transistor Resistance Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q2101	13kΩ(-)	3.54MΩ	100Ω(±)
Q2102	3.29MΩ	5.11kΩ	120kΩ
Q2103	11kΩ(+)	121.7kΩ	0.8M(-)
Q2104	1000Ω(+)	11.1kΩ	15kΩ(-)
Q2105	1000Ω(±)	5.1kΩ	999Ω
Q2107	400Ω(+)	I	0.3Ω
Q2108	400Ω(+)	1.06MΩ(+)	4MΩ(+)
Q2110	179.2Ω	2213Ω	17MΩ(+)
Q2111	1000Ω(+)	1000Ω(±)	100Ω(±)
Q2112	1000Ω(+)	1090(+)	0.1Ω
Q2113	2100Ω(+)	0.3Ω	1.44MΩ(-)
Q2114	2100Ω(+)	0.3Ω	1.44MΩ(-)
Q2115	2100Ω(+)	0.5Ω	1.5MΩ(-)
Q2116	0.3Ω	630Ω(+)	5.1kΩ(+)
Q3001	1.59MΩ(+)	1000Ω(±)	100Ω(±)

**Table 6-5 (continued). Deflection Board Transistor Resistance Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q3002	1.8MΩ(+)	1000Ω(+)	2500Ω(-)
Q3003	0.1Ω	1.7Ω	1MΩ(+)
Q3202	0.3Ω	1.9Ω	4MΩ(+)
Q3203	1MΩ(+)	1MΩ(+)	1.15MΩ(+)
Q3205	1025Ω	1.02MΩ	0.5MΩ(+)
Q3206	6kΩ(+)	2.85MΩ	2.8MΩ(+)
Q3207	1600Ω(+)	59.1kΩ	15.55kΩ
Q3208	0.3Ω	2881Ω	2.6MΩ(+)
Q3209	4.2MΩ(+)	0.3Ω	I
Q3210	4.1MΩ(+)	0.3Ω	I
Q3403	0.2Ω	6.43kΩ	0.5MΩ(+)

**NOTE:** These measurements were taken with the deflection board removed and disconnected from the rest of the monitor.

**Table 6-6. Deflection Board IC Resistance Measurements**

PIN	IC1301	IC2101	IC2103	IC3201	IC3401
1	500Ω(+)	3.68MΩ	3.4MΩ	39.5kΩ(-)	1600Ω(-)
2	600Ω(+)	95kΩ(+)	55kΩ(+)	10.7kΩ(+)	550Ω(+)
3	700Ω(+)	14kΩ(+)	73kΩ(+)	0.322MΩ	4.65kΩ
4	600Ω(+)	200kΩ(-)	3.39MΩ	22kΩ(-)	10.8kΩ(+)
5	700Ω(+)	24.6kΩ(+)	19kΩ(+)	40kΩ(-)	61.6kΩ
6	I	23.8kΩ(+)	200kΩ(-)	1.02MΩ	13.12kΩ
7	I	2.22MΩ	200kΩ(-)	180Ω(±)	4.09kΩ
8	0.3Ω	100kΩ(±)	200kΩ(-)	I	6.3kΩ(+)
9	I	-	200kΩ(-)	-	6.3kΩ(+)
10	744Ω	-	70kΩ(-)	-	9.65kΩ
11	338Ω	-	3.38MΩ	-	0.3Ω
12	745Ω	-	19kΩ(+)	-	0.4Ω
13	336Ω	-	19kΩ(+)	-	109.4kΩ
14	0.3Ω	-	0.6Ω	-	4.49MΩ
15	0.3Ω	-	-	-	8.04kΩ
16	200Ω(±)	-	-	-	0.3Ω

**NOTE:** These measurements were taken with the deflection board removed and disconnected from the rest of the monitor.

**Table 6-7. Dynamic Focus Board Transistor Resistance Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q7701	2156Ω	8.01kΩ	11.78kΩ
Q7702	1995Ω	11.78kΩ	51.3kΩ
Q7703	1003Ω	1994Ω	51.3kΩ

**NOTE:** These measurements were taken with the PIN board removed and disconnected from the rest of the monitor.

**Table 6-8. PIN Board Transistor Voltage Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q7001	1.19V	0.61V	-10.6V
Q7007	8.73V	8.13V	0.87V
Q7008	8.41V	7.81V	-1.38V
Q7009	0.315V	0.93V	16.6V
Q7401	16.6V	16.29V	7.81V
Q7402	0.019V	-1.84V	13.6V
Q7411	12.5V	13.13V	16.7V
Q7502	0.58V	0.019V	-15.0V
Q7503	-0.64V	0.052V	-7.65V
Q7505	-0.5V	0.114V	15.08V

**Table 6-9. PIN Board IC Voltage Measurements**

PIN	IC7001	IC7501
1	5.45V	0.019V
2	7.86V	6.27V
3	-10.63V	-14.8V
4	0.03V	0V

**Table 6-9 (continued). PIN Board IC Voltage Measurements**

PIN	IC7001	IC7501
5	-1.37V	-7.02V
6	-1.33V	0V
7	-11.9V	-16.05V
8	0.041V	-5.65V
9	0.002V	-5.65V
10	-1.37V	-7.02V
11	-1.36V	-7.06V
12	0.003V	-5.69V
13	-10.67V	0V
14	8.18V	6.39V

**Table 6-10. Video Board Transistor Voltage Measurements**

DEVICE	EMITTER	BASE	COLLECTOR
Q5201	0.80V	1.55V	4.50V
Q5202	4.50V	4.94V	73.0V
Q5203	73.9V	74.4V	88.7V
Q5204	73.7V	0V	73.1V
Q5205	0.805V	1.52V	4.48V
Q5206	4.48V	4.94V	72.9V
Q5207	73.7V	74.2V	88.8V
Q5208	73.5V	72.8V	0.001V
Q5209	0.80V	1.53V	4.48V
Q5210	4.48V	4.94V	73.1V
Q5211	73.8V	74.4V	88.9V
Q5212	73.7V	0.01V	73.2V
Q5301	85.5V	85.5V	0.001V
Q5302	85.5V	85.6V	0.001V
Q5303	85.5V	85.6V	0.001V
Q5304	0.60V	0.814V	72.0V

# Chapter 7

## Parts List

This chapter contains the replacement parts lists for the ZCM-1490 color video monitor.

### CAUTION

Some components contain an X in their reference number. For safety reasons, these components must be replaced only with identical components.

**Table 7-1. Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors</b>		
C1301	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C1302	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C1303	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C1304	022-07859-05A	10 $\mu$ F, 20%, 16V, electrolytic
C2101	022-07702-24	0.1 $\mu$ F, 2%, 100V, polypropylene
C2103	022-07773	0.001 $\mu$ F, 5%, 100V, polyester
C2104	022-07860-12	470 $\mu$ F, 20%, 25V, electrolytic
C2105	022-07702-30	0.33 $\mu$ F, 2%, 100V, polypropylene
C2106	022-07702-30	0.33 $\mu$ F, 2%, 100V, polypropylene
C2107	022-07704-28	0.22 $\mu$ F, 10%, 100V, polypropylene
C2108	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C2109	022-07860-15	3300 $\mu$ F, 20%, 25V, electrolytic
C2110	022-07860-12	470 $\mu$ F, 20%, 25V, electrolytic

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C2111	022-07773-04	0.0022 $\mu$ F, 5%, 100V, polyester
C2112	022-07862-07A	33 $\mu$ F, 20%, 50V, electrolytic
C2113	022-07864A	0.47 $\mu$ F, 20%, 100V, electrolytic
C2114	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C2115	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C2116	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C2117	022-07786C	1000pF, 10%, 500V, ceramic disc
C2118	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C2119	022-07864-06	22 $\mu$ F, 20%, 100V, electrolytic
C2120	022-07860-15	3300 $\mu$ F, 20%, 25V, electrolytic
C2121	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C2122	022-07773-20	0.047 $\mu$ F, 5%, 100V, polyester
C3001	022-07405-06	22 $\mu$ F, 20%, 25V, NP electrolytic
C3002	022-05704	180pF, $\pm$ 10%, 3000V, ceramic disc
C3003	022-02670	0.0033 $\mu$ F, $\pm$ 10%, 500V, cer. disc
C3004	022-07244	0.0015 $\mu$ F, $\pm$ 5%, 500V, ceramic disc
C3006	022-07683-05	0.047 $\mu$ F, 5%, 200V, polypropylene
C3007	022-07683-05	0.047 $\mu$ F, 5%, 200V, polypropylene

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C3008	022-07672-10	0.011 $\mu$ F, 5%, 1600V, polypropylene
C3009	022-07860-13	1000 $\mu$ F, 20%, 25V, electrolytic
C3010	022-07876-20	0.47 $\mu$ F, 5%, 250V, polyester
C3011	022-07876-20	0.47 $\mu$ F, 5%, 250V, polyester
C3012	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C3013	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C3201	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C3202	022-07242	0.0018 $\mu$ F, $\pm$ 10%, 500V, ceramic disc
C3203	022-07860-13	1000 $\mu$ F, 20%, 25V, electrolytic
C3204	022-07672-30	0.0215 $\mu$ F, 5%, 1600V, polypropylene
C3205	022-05704	180pF, $\pm$ 10%, 3000V, ceramic disc
C3206	022-07786-10C	470pF, 10%, 500V, ceramic disc
C3207	022-07876-20	0.47 $\mu$ F, 5%, 250V, polyester
C3208	022-07876-20	0.47 $\mu$ F, 5%, 250V, polyester
C3209	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C3210	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C3211	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C3212	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C3214	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C3216	022-07773-15	0.018 $\mu$ F, 5%, 100V, polyester
C3217	022-07773-16	0.022 $\mu$ F, 5%, 100V, polyester

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C3218	022-07405-05	10 $\mu$ F, $\pm$ 20%, 35V, NP electrolytic
C3219	022-07242	0.0018 $\mu$ F, $\pm$ 10%, 500V, ceramic disc
C3220	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C3221	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C3222	022-07958-57	2400pF, 5%, 100V, ceramic chip
C3224	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C3225	022-07774-12	0.01 $\mu$ F, 10%, 100V, polyester
C3226	022-07621-27B	51pF, 5%, 50V, ceramic disc
C3227	022-07621-34B	100pF, 5%, 50V, ceramic disc
C3228	022-07621-27B	51pF, 5%, 50V, ceramic disc
C3229	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C3401	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C3402	022-07774-12	0.01 $\mu$ F, 10%, 100V, polyester
C3403	022-07958-57	2400pF, 5%, 100V, ceramic chip
C3404	022-07862-02A	2.2 $\mu$ F, 20%, 50V, electrolytic
C3405	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C3406	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C3407	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C3408	022-07860-13	1000 $\mu$ F, 20%, 25V, electrolytic
C3409	022-07786-16C	1800pF, 10%, 500V, ceramic disc
C3410	022-07773-26	0.15 $\mu$ F, 5%, 100V, polyester
C3411	022-07909	47 $\mu$ F, +50/-10%, 200V, electrolytic

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C3412	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C3413	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C3415	022-08003-02A	0.1 $\mu$ F, 5%, 50V, ceramic chip
C5101	022-07862-04A	4.7 $\mu$ F, 20%, 50V, electrolytic
C5102	022-07862-04A	4.7 $\mu$ F, 20%, 50V, electrolytic
C5103	022-07862-04A	4.7 $\mu$ F, 20%, 50V, electrolytic
C5104	022-08039-01A	6800pF, 20%, 25V, ceramic, tubular, leadless
C5105	022-08039-01A	6800pF, 20%, 25V, ceramic, tubular, leadless
C5106	022-08039-01A	6800pF, 20%, 25V, ceramic, tubular, leadless
C5108	022-07991A	2200pF, 10%, 16V, ceramic, tubular, leadless
C5109	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C5110	022-08016A	10 $\mu$ F, 20%, 16V, NP electrolytic
C5111	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic
C5112	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5114	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic
C5115	022-07985-23A	6pF, $\pm$ 0.5pF, 50V, ceramic, tubular, leadless
C5116	022-07985-23A	6pF, $\pm$ 0.5pF, 50V, ceramic, tubular, leadless
C5117	022-07985-23A	6pF, $\pm$ 0.5pF, 50V, ceramic, tubular, leadless
C5118	022-07984-15A	1000pF, 10%, 50V, ceramic, tubular, leadless
C5119	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C5120	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C5121	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C5122	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5124	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5125	022-07859-09A	100 $\mu$ F, 20%, 16V, electrolytic
C5201	022-08036-36A	100pF, 5%, 50V, ceramic, tubular, leadless
C5202	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5203	022-04948	1000pF, GMV, 500V, ceramic disc
C5204	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5205	022-08036-36A	100pF, 5%, 50V, ceramic, tubular, leadless
C5206	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5207	022-04948	1000pF, GMV, 500V, ceramic disc
C5208	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5209	022-08036-36A	100pF, 5%, 50V, ceramic, tubular, leadless
C5210	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5211	022-04948	1000pF, GMV, 500V, ceramic disc
C5212	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C5213	022-07984-03A	100pF, 10%, 50V, ceramic, tubular, leadless
C5214	022-07984-03A	100pF, 10%, 50V, ceramic, tubular, leadless
C5215	022-07984-03A	100pF, 10%, 50V, ceramic, tubular, leadless
C5301	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C5302	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic



**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C5303	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C5305	022-07961-11	10 $\mu$ F, 20%, 160V, electrolytic
C7001	022-07405-06	22 $\mu$ F, 10%, 25V, NP electrolytic
C7002	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic
C7003	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7004	022-07774-24	0.1 $\mu$ F, 10%, 100V, polyester
C7005	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7006	022-07774-24	0.1 $\mu$ F, 10%, 100V, polyester
C7007	022-07405-09	100 $\mu$ F, $\pm$ 20%, 25V, NP electrolytic
C7008	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic
C7010	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7012	022-07405-06	22 $\mu$ F, 10%, 25V, NP electrolytic
C7101	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7102	022-07613-04C	220pF, 10%, 50V, ceramic disc
C7103	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7104	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7105	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7106	022-05719	200pF, $\pm$ 5%, 500V, ceramic disc
C7107	022-07864-04A	4.7 $\mu$ F, 20%, 100V, electrolytic
C7401	022-07405-05	10 $\mu$ F, $\pm$ 20%, 25V, NP electrolytic
C7402	022-07621-06B	6pF, $\pm$ 0.25pF, 50V, ceramic disc
C7403	022-07613-06C	330pF, 10%, 50V, ceramic disc

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C7404	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C7405	022-07774-12	0.01 $\mu$ F, 10%, 100V, polyester
C7406	022-07621-26B	47pF, 5%, 50V, ceramic disc
C7408	022-07773-06	0.0033 $\mu$ F, 5%, 100V, polyester
C7409	022-07621-28B	56pF, 5%, 50V, ceramic disc
C7410	022-07860-05A	10 $\mu$ F, 20%, 25V, electrolytic
C7411	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7412	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7413	022-07621-42B	220pF, 5%, 50V, ceramic disc
C7414	022-07773-08	0.0047 $\mu$ F, 5%, 100V, polyester
C7415	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7416	022-07407-01	1 $\mu$ F, $\pm$ 20%, 50V, NP electrolytic
C7417	022-07958-48	1000pF, 5%, 100V, ceramic chip
C7418	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7419	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7420	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7421	022-07958-60	3300pF, 5%, 100V, ceramic chip
C7422	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7423	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7501	022-07860-06A	22 $\mu$ F, 20%, 25V, electrolytic
C7502	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7503	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7504	022-07743-10	6.8pF, 10%, 50V, ceramic, tubular

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Capacitors (continued)</b>		
C7505	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7506	022-08001-04	4.7 $\mu$ F, 10%, 250V, polyester
C7507	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7508	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7509	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7510	022-07860-09A	100 $\mu$ F, 20%, 25V, electrolytic
C7511	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7512	022-07860-12	470 $\mu$ F, 20%, 25V, electrolytic
C7513	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7514	022-07860-12	470 $\mu$ F, 20%, 25V, electrolytic
C7515	022-07613-11C	820pF, 10%, 50V, ceramic disc
C7516	022-07864-02A	2.2 $\mu$ F, 20%, 100V, electrolytic
C7517	022-08015-01A	22 $\mu$ F, 20%, 25V, NP electrolytic
C7518	022-07613	100pF, 10%, 50V, ceramic disc
C7519	022-08039-03A	10000pF, 20%, 25V, ceramic, tubular, leadless
C7520	022-07407-01	1 $\mu$ F, $\pm$ 20%, 50V, NP electrolytic
C7521	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7522	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7523	022-07862-01A	1 $\mu$ F, 20%, 50V, electrolytic
C7701	022-07773-28	0.22 $\mu$ F, 5%, 100V, polyester
C7702	022-07773-24	0.1 $\mu$ F, 5%, 100V, polyester
C7703	022-07773-28	0.22 $\mu$ F, 5%, 100V, polyester

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Diodes</b>		
CR1301	103-00301-05A	Zener, 5.1V, 1W
CR1302	103-00398A	Si, general, tubular, leadless
CR1303	103-00398A	Si, general, tubular, leadless
CR1304	103-00398A	Si, general, tubular, leadless
CR1305	103-00398A	Si, general, tubular, leadless
CR1306	103-00398A	Si, general, tubular, leadless
CR1307	103-00398A	Si, general, tubular, leadless
CR1308	103-00398A	Si, general, tubular, leadless
CR1309	103-00398A	Si, general, tubular, leadless
CR2101	103-00398A	Si, general, tubular, leadless
CR2102	103-00398A	Si, general, tubular, leadless
CR2103	103-00398A	Si, general, tubular, leadless
CR2104	103-00398A	Si, general, tubular, leadless
CR2105	103-00398A	Si, general, tubular, leadless
CR2106	103-00301-16A	Zener, 12V, 1W
CR2107	103-00142-01	Si, general
CR2108	103-00142-01	Si, general
CR2109	103-00344-02A	General
CR2110	103-00344-02A	General
CR2111	103-00344-02A	General
CR2112	103-00344-02A	General
CR2113	103-00398A	Si, general, tubular, leadless
CR2114	103-00398A	Si, general, tubular, leadless
CR2115	103-00398A	Si, general, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Diodes (continued)</b>		
CR2116	103-00399-11A	Zener, 5.6V, 0.5W, tubular leadless
CR2117	103-00398A	Si, general, tubular, leadless
CR2119	103-00398A	Si, general, tubular, leadless
CR2120	103-00398A	Si, general, tubular, leadless
CR2121	103-00398A	Si, general, tubular, leadless
CR2122	103-00398A	Si, general, tubular, leadless
CR2123	103-00398A	Si, general, tubular, leadless
CR2124	103-00398A	Si, general, tubular, leadless
CR3001	103-00344-06A	General
CR3002	103-00344-06A	General
CR3003	103-00431	Si, high frequency
	114-01325-03	Screw, 4-24 x 0.312, hex head
CR3004	103-00399-38A	Zener, 39V, 0.5W, tubular leadless
CR3201	103-00398A	Si, general, tubular, leadless
CR3203	103-00344-06A	General
CR3204	103-00254-01	Si, general
CR3205	103-00398A	Si, general, tubular, leadless
CR3206	103-00398A	Si, general, tubular, leadless
CR3207	103-00398A	Si, general, tubular, leadless
CR3208	103-00398A	Si, general, tubular, leadless
CR3209	103-00398A	Si, general, tubular, leadless
CR3210	103-00344-06A	General
CR3211	103-00254-01	Si, general
CR3212	103-00254-01	Si, general
CR3213	103-00398A	Si, general, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Diodes (continued)</b>		
CR3214	103-00398A	Si, general, tubular, leadless
CR3215	103-00344-02A	General
CR3216	103-00398A	Si, general, tubular, leadless
CR3217	103-00398A	Si, general, tubular, leadless
CR3401	103-00398A	Si, general, tubular, leadless
CR3404	103-00398A	Si, general, tubular, leadless
CR5101	103-00399-10A	Zener, 5.1V, 0.5W, tubular leadless
CR5102	103-00398A	Si, general, tubular, leadless
CR5104	103-00398A	Si, general, tubular, leadless
CR5105	103-00399-10A	Zener, 5.1V, 0.5W, tubular leadless
CR5201	103-00398A	Si, general, tubular, leadless
CR5202	103-00398A	Si, general, tubular, leadless
CR5203	103-00398A	Si, general, tubular, leadless
CR5204	103-00399-10A	Zener, 5.1V, 0.5W, tubular leadless
CR5205	103-00398A	Si, general, tubular, leadless
CR5206	103-00398A	Si, general, tubular, leadless
CR5207	103-00398A	Si, general, tubular, leadless
CR5209	103-00398A	Si, general, tubular, leadless
CR5210	103-00398A	Si, general, tubular, leadless
CR5211	103-00398A	Si, general, tubular, leadless
CR5301	103-00415-02A	Si, general
CR5302	103-00415-02A	Si, general
CR5303	103-00415-02A	Si, general

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Diodes (continued)</b>		
CR5304	103-00415-02A	Si, general
CR5305	103-00415-02A	Si, general
CR5306	103-00415-02A	Si, general
CR5307	103-00415-02A	Si, general
CR5308	103-00398A	Si, general, tubular, leadless
CR5309	103-00398A	Si, general, tubular, leadless
CR5310	103-00398A	Si, general, tubular, leadless
CR7101	103-00336-15A	Zener, 7.5V, 0.5W
CR7102	103-00254-01	Si, general
CR7406	103-00142-01	Si, general
CR7407	103-00142-01	Si, general
CR7408	103-00142-01	Si, general
CR7409	103-00142-01	Si, general
CR7410	103-00142-01	Si, general
CR7501	103-00142-01	Si, general
CR7502	103-00142-01	Si, general
CR7504	103-00308	Zener, 12V, 0.5W
CR7505	103-00279-11A	Zener, 5.6V, 0.5W
D7401	103-00142-01	Si, general
D7402	103-00142-01	Si, general
D7404	103-00279-08A	Zener, 4.3V, 0.5W
D7405	103-00142-01	Si, general
<b>Integrated Circuits</b>		
IC1301	A-15305-01	Programmable IC
IC2101	221-00240	Dual wideband op-amp
IC2102	221-00265	Adjustable shunt regulator
IC2103	221-00173	Quad switch
IC3201	221-00438	JFET input op-amp
IC3202	221-00265	Adjustable shunt regulator
IC3203	221-00265	Adjustable shunt regulator
IC3401	221-00440	Horizontal processor
IC3402	221-00166-04	Regulator, 12V, 500mA, linear
IC5101	221-00397	RGB video processor, ANALOG input

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Integrated Circuits (continued)</b>		
IC5102	221-00318-03	Quad, 2-input exclusive-OR gate
IC7001	221-C0309	Four-quadrant multiplier (contract assembly only)
IC7101	221-00240	Dual wideband op-amp
IC7401	221-00146	Dual D-type flip-flop
IC7402	221-00173	Quad switch
IC7501	221-C0309	Four-quadrant multiplier (contract assembly only)
IC7502	221-00438	JFET input op-amp
IC7503	221-00504	4 Amp linear driver
<b>Inductors</b>		
L3401	020-03831	Coil, RFC filter
L3402	020-03831	Coil, RFC filter
L7401	020-03849A	Coil, RFC, tunable
L7701	020-03831A	Coil, RFC
LX3001	020-04233	Coil, RFC, tunable, centering choke
	064-00519-02	Eyelet, rolled flange
LX3002	020-04279	Coil, linearity
<b>Transistors</b>		
Q2101	121-01040	NPN, Si
Q2102	121-00975A	NPN, Si
Q2103	121-00973A	PNP, Si
Q2104	121-00973A	PNP, Si
Q2105	121-00975A	NPN, Si
Q2106	121-01037-01	NPN, Si
Q2107	121-01188	PNP, Si, power, 2A
	114-01325-03	Screw, 4-24 x 0.312, hex head
Q2108	121-01187	NPN, Si, power, 2A
	114-01325-03	Screw, 4-24 x 0.312, hex head
Q2109	121-01188	PNP, Si, power, 2A
Q2110	121-01063A	NPN, Si
Q2111	121-01035A	NPN, Si
Q2112	121-01036A	PNP, Si

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Transistors (continued)</b>		
Q2113	121-00973A	PNP, Si
Q2114	121-00973A	PNP, Si
Q2115	121-00973A	PNP, Si
Q2116	121-00975A	NPN, Si
Q2117	121-00975A	NPN, Si
Q3001	121-01035A	NPN, Si
Q3002	121-01036A	PNP, Si
Q3003	121-01198	NPN, Si, horizontal output
	114-01325-03	Screw, 4-24 x 0.312, hex head
Q3201	121-01037-01	NPN, Si
Q3202	121-01199	NPN, Si
Q3203	121-01204	NPN, Si, power, 10A
	114-01115-04	Screw, 6-20 x 0.375, hex head
Q3204	121-01037-01	NPN, Si
Q3205	121-01037-01	NPN, Si
Q3206	121-00895A	NPN, Si
Q3207	121-00973A	PNP, Si
Q3208	121-00895A	NPN, Si
Q3209	121-01063A	NPN, Si
Q3210	121-00895A	NPN, Si
Q3401	121-01096A	NPN, Si
Q3403	121-01037-01	NPN, Si
Q5101	121-01130A	NPN, Si, chip
Q5102	121-01139A	NPN, Si
Q5104	121-01130A	NPN, Si, chip
Q5105	121-01139A	NPN, Si
Q5106	121-01127-01A	PNP, Si
Q5107	121-01139A	NPN, Si
Q5108	121-01127-01A	PNP, Si
Q5109	121-01139A	NPN, Si
Q5110	121-01127-01A	PNP, Si
Q5201	121-01096A	NPN, Si
Q5201E	149-00555-16	Core, ferrite bead
Q5202	121-01156-01	NPN, Si
Q5203	121-01170A	NPN, Si, 150V, 50mA
Q5204	121-01186A	PNP, Si, high voltage
Q5205	121-01096A	NPN, Si
Q5205E	149-00555-16	Core, ferrite bead

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Transistors (continued)</b>		
Q5206	121-01156-01	NPN, Si
Q5207	121-01170A	NPN, Si, 150V, 50mA
Q5208	121-01186A	PNP, Si, high voltage
Q5209	121-01096A	NPN, Si
Q5209E	149-00555-16	Core, ferrite bead
Q5210	121-01156-01	NPN, Si
Q5211	121-01170A	NPN, Si, 150V, 50mA
Q5212	121-01186A	PNP, Si, high voltage
Q5301	121-01059A	PNP, Si
Q5302	121-01059A	PNP, Si
Q5303	121-01059A	PNP, Si
Q5304	121-01063A	NPN, Si
Q7001	121-00973A	PNP, Si
Q7007	121-00973A	PNP, Si
Q7008	121-00973A	PNP, Si
Q7009	121-00895A	NPN, Si
Q7103	121-01037-01	NPN, Si
Q7104	121-01037-01	NPN, Si
Q7105	121-01072-01	NPN, Si
Q7401	121-00973A	PNP, Si
Q7402	121-00895A	NPN, Si
Q7404	121-00973A	PNP, Si
Q7405	121-00895A	NPN, Si
Q7407	121-00895A	NPN, Si
Q7408	121-00895A	NPN, Si
Q7409	121-00973A	PNP, Si
Q7410	121-00895A	NPN, Si
Q7411	121-00895A	NPN, Si
Q7502	121-00973A	PNP, Si
Q7503	121-00973A	PNP, Si
Q7505	121-00895A	NPN, Si
Q7701	121-01063A	NPN, Si
Q7702	121-01063A	NPN, Si
<b>Resistors</b>		
R1301	063-11020-58A	240Ω, 5%, 1/4W, film, tubular, leadless
R1302	063-11020-58A	240Ω, 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R1303	063-11020-66A	510Ω, 5%, 1/4W, film, tubular, leadless
R1304	063-11020-66A	510Ω, 5%, 1/4W, film, tubular, leadless
R1307	063-11020-65A	470Ω, 5%, 1/4W, film, tubular, leadless
R1308	063-11020-65A	470Ω, 5%, 1/4W, film, tubular, leadless
R1309	063-11020-65A	470Ω, 5%, 1/4W, film, tubular, leadless
R1310	063-11020-65A	470Ω, 5%, 1/4W, film, tubular, leadless
R1311	063-10836-48 086-00836	100Ω, 5%, 2W, film Terminal, male
R1312	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R1313	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R1314	063-11020A	0Ω, 5%, 1/4W, film, tubular, leadless
R1315	063-11020A	0Ω, 5%, 1/4W, film, tubular, leadless
R2101	063-11021-35A	390kΩ, 5%, 1/4W, film, tubular, leadless
R2102	063-11021-21A	100kΩ, 5%, 1/4W, film, tubular, leadless
R2103	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R2104	063-11020-23A	120kΩ, 5%, 1/4W, film, tubular, leadless
R2105	063-11020-99A	12kΩ, 5%, 1/4W, film, tubular, leadless
R2106	063-10936-46	2.67kΩ, 1%, 1/4W, film
R2107	063-10651-22	Control, rotary trimmer
R2108	063-10934-10	124Ω, 1%, 1/4W, film
R2109	063-10243-08	2.2Ω, 5%, 1/2W, film
R2110	063-10936-33	2.05kΩ, 1%, 1/4W, film
R2111	063-10243-62	390Ω, 5%, 1/2W, film
R2112	063-10422-24 086-00836 194-01987	1Ω, 10%, 2W, wirewound Terminal, male Spacer, ceramic tube
R2113	063-11021-03A	18kΩ, 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R2114	063-10236-05	24kΩ 5%, 1/4W, film
R2115	063-11021-21A	100kΩ, 5%, 1/4W, film, tubular, leadless
R2116	063-11020-93A	6.8kΩ, 5%, 1/4W, film, tubular, leadless
R2117	063-10651-11	Control, rotary, trimmer
R2118	063-11020-81A	2.2kΩ, 5%, 1/4W, film, tubular, leadless
R2119	063-11020-36A	30Ω, 5%, 1/4W, film, tubular, leadless
R2120	063-11020-61A	330Ω, 5%, 1/4W, film, tubular, leadless
R2121	063-11020-57A	220Ω, 5%, 1/4W, film, tubular, leadless
R2122	063-11020-90A	5.1kΩ, 5%, 1/4W, film, tubular, leadless
R2123	063-10938-69	41.2kΩ, 1%, 1/4W, film
R2124	063-11052-08	Control, rotary, trimmer, black
R2125	063-10934-99	732Ω, 1%, 1/4W, film
R2126	063-10934-86	562Ω, 1%, 1/4W, film
R2127	063-11021-06A	24kΩ, 5%, 1/4W, film, tubular, leadless
R2128	063-11021-53A	2.2MΩ, 5%, 1/4W, film, tubular, leadless
R2129	063-11020-77A	1.5kΩ, 5%, 1/4W, film, tubular, leadless
R2131	063-10836-70 086-00836 194-01987	820Ω, 5%, 2W, film Terminal, male Spacer, ceramic tube
R2132	063-10836-68 086-00836 194-01987	680Ω, 5%, 2W, film Terminal, male Spacer, ceramic tube
R2133	063-10836-70 086-00836 194-01987	820Ω, 5%, 2W, film Terminal, male Spacer, ceramic tube
R2140	063-11020-89A	4.7kΩ, 5%, 1/4W, film, tubular, leadless
R2141	063-11020-81A	2.2kΩ, 5%, 1/4W, film, tubular, leadless
R2142	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R2143	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2144	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2145	063-10243-48	100 $\Omega$ , 5%, 1/2W, film
R2146	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2147	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2148	063-10854-13	Control, rotary, trimmer
R2152	063-10940-27	180k $\Omega$ , 1%, 1/4W, film
R2153	063-11005	Control, rotary, trimmer
R2154	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2155	063-11020-89A	4.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2157	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2158	063-11052-08	Control, rotary, trimmer, black
R2159	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2160	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2161	063-11020-65A	470 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2162	063-11020-77A	1.5k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2163	063-11021-03A	18k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2164	063-11021-03A	18k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2165	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2166	063-11021-03A	18k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2167	063-11020-77A	1.5k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2168	063-11020-77A	1.5k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2169	063-10936-71	4.3k $\Omega$ , 1%, 1/4W, film
R2170	063-11052-08	Control, rotary, trimmer, black

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R2171	063-10938-26	17.8k $\Omega$ , 1%, 1/4W, film
R2172	063-11020-89A	4.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2173	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2174	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R2175	063-10235-72	1k $\Omega$ , 5%, 1/4W, film
R2176	063-11020-87A	3.9k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3001	063-10651-30	Control, rotary, trimmer
R3002	063-10840-51	130 $\Omega$ , 5%, 3W, film
	012-08568-03	Metal stamping bracket, resistor support
	194-01987	Spacer, ceramic tube
R3003	063-10243-62	390 $\Omega$ , 5%, 1/2W, film
R3005	063-10243	1 $\Omega$ , 5%, 1/2W, film
R3006	063-10243-24	10 $\Omega$ , 5%, 1/2W, film
R3007	063-10243-06	1.8 $\Omega$ , 5%, 1/2W, film
R3008	063-10442-56	22 $\Omega$ , 5%, 5W, wirewound
	012-08568-03	Metal stamping bracket, resistor support
	194-01987	Spacer, ceramic tube
R3009	063-10243-32	22 $\Omega$ , 5%, 1/2W, film
R3010	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3011	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3201	063-10243-82	2.7k $\Omega$ , 5%, 1/2W, film
R3202	063-10836-76	1.5k $\Omega$ , 5%, 2W, film
	086-00836	Terminal, male
R3203	063-10840-86	3.9k $\Omega$ , 5%, 3W, film
	012-08568-03	Metal stamping bracket, resistor support
	194-01987	Spacer, ceramic tube
R3204	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3205	063-10243-08	2.2 $\Omega$ , 5%, 1/2W, film
R3206	063-10243-32	22 $\Omega$ , 5%, 1/2W, film
R3207	063-10836-88	4.7k, 5%, 2W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R3208	063-10243-88	4.7kΩ, 5%, 1/2W, film
R3209	063-10243-72	1kΩ, 5%, 1/2W, film
R3210	063-11020-89A	4.7kΩ, 5%, 1/4W, film, tubular, leadless
R3211	063-10444-42	5.6Ω, 10%, 5W, wirewound
	012-08568-03	Metal stamping bracket, resistor support
	194-01987	Spacer, ceramic tube
R3212	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3214	063-11020-81A	2.2kΩ, 5%, 1/4W, film, tubular, leadless
R3215	063-11021-45A	1MΩ, 5%, 1/4W, film
R3216	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R3217	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R3218	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R3219	063-10243-66	560Ω, 5%, 1/2W, film
R3220	063-10938-23	16.5kΩ, 1%, 1/4W, film
R3222	063-10936-71	4.3kΩ, 1%, 1/4W, film
R3223	063-11021-21A	100kΩ, 5%, 1/4W, film, tubular, leadless
R3224	063-10828-84A	3.3kΩ, 5%, 1/2W, film
R3225	063-11020-83A	2.7kΩ, 5%, 1/4W, film, tubular, leadless
R3226	063-11021-15A	56kΩ, 5%, 1/4W, film, tubular, leadless
R3227	063-10243-72	1kΩ, 5%, 1/2W, film
R3228	063-11020-84A	3kΩ, 5%, 1/4W, film, tubular, leadless
R3229	063-11020-99A	12kΩ, 5%, 1/4W, film, tubular, leadless
R3230	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3231	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3232	063-11020-91A	5.6kΩ, 5%, 1/4W, film, tubular, leadless
R3233	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R3234	063-11021-15A	56kΩ, 5%, 1/4W, film, tubular, leadless
R3237	063-10938-42	24.3kΩ, 1%, 1/4W, film
R3238	063-10651-22	Control, rotary trimmer
R3239	063-10936-33	2.05kΩ, 1%, 1/4W, film
R3240	063-11021-15A	56kΩ, 5%, 1/4W, film, tubular, leadless
R3241	063-11020-83A	2.7kΩ, 5%, 1/4W, film, tubular, leadless
R3242	063-10243-84	3.3kΩ, 5%, 1/2W, film
R3243	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R3244	063-10840-48	100Ω, 5%, 3W, film
	012-08568-03	Metal stamping bracket, resistor support
	194-01987	Spacer, ceramic tube
R3245	063-11021-21A	100kΩ, 5%, 1/4W, film, tubular, leadless
R3246	063-11021-14A	51kΩ, 5%, 1/4W, film
R3248	063-07799	2.2kΩ, 10%, 1/2W, carbon composition
R3249	063-10243-48	100Ω, 5%, 1/2W, film
R3250	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3252	063-10936-53	3.01kΩ, 1%, 1/4W, film
R3253	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless
R3254	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless
R3255	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless
R3256	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless
R3257	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3258	063-11020-73A	1kΩ, 5%, 1/4W, film, tubular, leadless
R3401	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R3402	063-10854-07	Control, rotary trimmer
R3403	063-11021-11A	39kΩ, 5%, 1/4W, film, tubular, leadless



**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R3404	063-11020-91A	5.6k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3405	063-11020-91A	5.6k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3406	063-11021-13A	47k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3407	063-11020-75A	1.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3408	063-11021-29A	220k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3409	063-11021-21A	100k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3410	063-10937-13	9.76k $\Omega$ , 1%, 1/4W, film
R3411	063-10938-64	37.4k $\Omega$ , 1%, 1/4W, film
R3414	063-11021-17A	68k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3415	063-10651-11	Control, rotary, trimmer
R3416	063-10243-79	2k $\Omega$ , 5%, 1/2W, film
R3417	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3418	063-10854-10	Control, rotary, trimmer
R3419	063-10235-96	10k $\Omega$ , 5%, 1/4W, film
R3420	063-10651-13	Control, rotary, trimmer
R3421	063-11021-16A	62k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3422	063-10235-60	330 $\Omega$ , 5%, 1/4W, film
R3427	063-11020-79A	1.8k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3428	063-10840-82 012-08568-03 194-01987	2.7k $\Omega$ , 5%, 3W, film Metal stamping bracket, resistor support Spacer, ceramic tube
R3429	063-10840-51 012-08568-03 194-01987	130 $\Omega$ , 5%, 3W, film Metal stamping bracket, resistor support Spacer, ceramic tube
R3430	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3431	063-11020-81A	2.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R3432	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R5101	063-11020-46A	75 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R5102	063-11020-46A	75 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R5103	063-11020-46A	75 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R5104	063-10979-70A	10k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5105	063-10979-70A	10k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5106	063-10979-70A	10k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5107	063-10979-32A	220 $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5108	063-10979-32A	220 $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5109	063-10979-32A	220 $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5110	063-10836-56 194-01987	220 $\Omega$ , 5%, 2W, film Spacer, ceramic tube
R5111	063-10979-68A	8.2k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5112	063-10979-32A	220 $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5113	063-10979-83A	39k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5115	063-10979-47A	1k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5116	063-10979-47A	1k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5117	063-10979-47A	1k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5118	063-10979-47A	1k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5119	063-10979-78A	22k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5120	063-10979-80A	27k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5121	063-10979-59A	3.3k $\Omega$ , 5%, 1/8W, film, tubular, leadless
R5122	063-10979-89A	68k $\Omega$ , 5%, 1/8W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R5123	063-10979-28A	150Ω, 5%, 1/8W, film, tubular, leadless
R5124	063-11020-55A	180Ω, 5%, 1/4W, film, tubular, leadless
R5126	063-10979-57A	2.7kΩ, 5%, 1/8W, film, tubular, leadless
R5130	063-10979-50A	1.3kΩ, 5%, 1/8W, film, tubular, leadless
R5131	063-10979-57A	2.7kΩ, 5%, 1/8W, film, tubular, leadless
R5132	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5133	063-10979-59A	3.3kΩ, 5%, 1/8W, film, tubular, leadless
R5134	063-10979-59A	3.3kΩ, 5%, 1/8W, film, tubular, leadless
R5135	063-10979-59A	3.3kΩ, 5%, 1/8W, film, tubular, leadless
R5136	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5137	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5138	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5139	063-10979-46A	910Ω, 5%, 1/8W, film, tubular, leadless
R5140	063-10651-28	Control, rotary, trimmer
R5142	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5143	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5144	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5145	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5146	063-10979-46A	910Ω, 5%, 1/8W, film, tubular, leadless
R5147	063-10979-33A	240Ω, 5%, 1/8W, film, tubular, leadless
R5149	063-10979-43A	680Ω, 5%, 1/8W, film, tubular, leadless
R5150	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R5151	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5152	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5153	063-10979-46A	910Ω, 5%, 1/8W, film, tubular, leadless
R5154	063-10651-28	Control, rotary, trimmer
R5156	063-10979-39A	470Ω, 5%, 1/8W, film, tubular, leadless
R5157	063-10979-70A	10kΩ, 5%, 1/8W, film, tubular, leadless
R5158	063-10979-81A	30kΩ, 5%, 1/8W, film, tubular, leadless
R5159	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5160	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5161	063-10979-24A	100Ω, 5%, 1/8W, film, tubular, leadless
R5162	063-10979-81A	30kΩ, 5%, 1/8W, film, tubular, leadless
R5201	063-10979-47A	1kΩ, 5%, 1/8W, film, tubular, leadless
R5202	063-11020-45A	68Ω, 5%, 1/4W, film, tubular, leadless
R5203	063-10979-20A	68Ω, 5%, 1/8W, film, tubular, leadless
R5204	063-10836-70 086-00836 194-01987	820Ω, 5%, 3W, film Terminal, male Spacer, ceramic tube
R5205	063-10836-70 086-00836 194-01987	820Ω, 5%, 3W, film Terminal, male Spacer, ceramic tube
R5206	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R5207	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5208	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5209	063-10979-47A	1kΩ, 5%, 1/8W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R5210	063-11020-45A	68Ω, 5%, 1/4W, film, tubular, leadless
	086-00836	Terminal, male
R5211	063-10979-20A	68Ω, 5%, 1/8W, film, tubular, leadless
R5212	063-10836-70	820Ω, 5%, 3W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube
R5213	063-10836-70	820Ω, 5%, 3W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube
R5214	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R5215	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5216	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5217	063-10979-47A	1kΩ, 5%, 1/8W, film, tubular, leadless
R5218	063-11020-45A	68Ω, 5%, 1/4W, film, tubular, leadless
R5219	063-10979-20A	68Ω, 5%, 1/8W, film, tubular, leadless
R5220	063-10836-70	820Ω, 5%, 3W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube
R5221	063-10836-70	820Ω, 5%, 3W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube
R5222	063-11020-49A	100Ω, 5%, 1/4W, film, tubular, leadless
R5223	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5224	063-11020-35A	27Ω, 5%, 1/4W, film, tubular, leadless
R5225	063-10979-35A	300Ω, 5%, 1/8W, film, tubular, leadless
R5301	063-10980-16A	1.0MΩ, 5%, 1/8W, film, tubular, leadless
R5302	063-10979-32A	220Ω, 5%, 1/8W, film, tubular, leadless
R5303	063-07749	150Ω, 5%, 1/2W, carbon composition

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R5304	063-10980-16A	1.0MΩ, 5%, 1/8W, film, tubular, leadless
R5305	063-10979-32A	220Ω, 5%, 1/8W, film, tubular, leadless
R5306	063-07749	150Ω, 5%, 1/2W, carbon composition
R5307	063-10980-16A	1.0MΩ, 5%, 1/8W, film, tubular, leadless
R5308	063-10979-32A	220Ω, 5%, 1/8W, film, tubular, leadless
R5309	063-07749	150Ω, 5%, 1/2W, carbon composition
R5310	063-07799	2.2kΩ, 10%, 1/2W, carbon composition
R5311	063-07799	2.2kΩ, 10%, 1/2W, carbon composition
R5314	063-10979-27A	130Ω, 5%, 1/8W, film, tubular, leadless
R5315	063-10243-80	2.2kΩ, 5%, 1/2W, film
R5316	063-10651-30	Control, rotary, trimmer
R5317	063-10651-30	Control, rotary, trimmer
R5318	063-10651-30	Control, rotary, trimmer
R5319	063-10243-72	1kΩ, 5%, 1/2W, film
R5320	063-11020-01A	1Ω, 5%, 1/4W, film, tubular, leadless
R5401	063-10764-03	Control, rotary, single
R5402	063-10854-04	Control, rotary, trimmer
R5403	063-10764-03	Control, rotary, single
R5404	063-10854-12	Control, rotary, trimmer
R5405	063-10235-86	3.9kΩ, 5%, 1/4W, film
R5406	063-10235-86	3.9kΩ, 5%, 1/4W, film
R5407	063-10235-67	620Ω, 5%, 1/4W, film
R7001	063-11020-99A	12kΩ, 5%, 1/4W, film, tubular, leadless
R7002	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R7003	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R7004	063-11020-97A	10kΩ, 5%, 1/4W, film, tubular, leadless
R7008	063-11020-87A	3.9kΩ, 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7010	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7011	063-11021-21A	100k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7012	063-10857-17	Control, rotary, trimmer
R7013	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7014	063-11020-84A	3k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7015	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7016	063-11020-89A	4.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7017	063-11020-89A	4.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7018	063-11020-80A	2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7019	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7020	063-11020-65A	470 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7021	063-11020-65A	470 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7025	063-11020-65A	470 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7026	063-11021-01A	15k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7027	063-10857-14	Control, rotary, trimmer
R7028	063-11021-01A	15k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7030	063-10235-48	100 $\Omega$ , 5%, 1/4W, film
R7031	063-11020-77A	1.5k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7033	063-11020-93A	6.8k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7034	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7035	063-11020-65A	470 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7036	063-11021-17A	68k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7037	063-11021-17A	68k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7039	063-10857-17	Control, rotary, trimmer
R7105	063-10243-60	330 $\Omega$ , 5%, 1/2W, film
R7106	063-10857-11	Control, rotary, trimmer
R7108	063-10938-01	10.2k $\Omega$ , 1%, 1/4W, film
R7110	063-10938-48	27.4k $\Omega$ , 1%, 1/4W, film
R7111	063-10236-10	39k $\Omega$ , 5%, 1/4W, film
R7112	063-11021-45A	1M $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7113	063-10937-13	9.76k $\Omega$ , 1%, 1/4W, film
R7114	063-10940	100k $\Omega$ , 1%, 1/4W, film
R7115	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7116	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7117	063-11020-81A	2.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7118	063-10243-72	1k $\Omega$ , 5%, 1/2W, film
R7119	063-10243-88	4.7k $\Omega$ , 5%, 1/2W, film
R7120	063-10836-88	4.7k $\Omega$ , 5%, 2W, film
R7121	086-00836	Terminal, male
R7121	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7401	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7402	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7403	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7404	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7405	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7406	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7407	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7408	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7409	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7410	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7411	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7412	063-11021-21A	100k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7413	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7414	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7417	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7418	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7419	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7421	063-11020-87A	3.9k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7422	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7427	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7428	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7429	063-11020-93A	6.8k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7430	063-10857-14	Control, rotary, trimmer
R7431	063-10857-14	Control, rotary, trimmer
R7432	063-11021-07A	27k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7433	063-10857-17	Control, rotary, trimmer
R7434	063-10857-12	Control, rotary, trimmer
R7435	063-10857-17	Control, rotary, trimmer
R7436	063-10857-12	Control, rotary, trimmer
R7437	063-11020-95A	8.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7438	063-11020-95A	8.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7439	063-11021-07A	27k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7440	063-11021-07A	27k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7441	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7442	063-11020-84A	3k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7443	063-11020-84A	3k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7444	063-10236-12	47k $\Omega$ , 5%, 1/4W, film
R7445	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7446	063-11020-77A	1.5k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7447	063-11020-83A	2.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7448	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7449	063-11020-81A	2.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7450	063-11020-91A	5.6k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7451	063-11020-67A	560 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7452	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7453	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7454	063-10857-12	Control, rotary, trimmer
R7455	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7456	063-10857-12	Control, rotary, trimmer
R7457	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7458	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7459	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7463	063-11021-01A	15k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7464	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7465	063-10235-72	1k $\Omega$ , 5%, 1/4W, film
R7501	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7506	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7507	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7508	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7509	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7510	063-11020-83A	2.7k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7511	063-11020-93A	6.8k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7512	063-10533-35	2k $\Omega$ , 1%, 1/4W, film
R7513	063-10533-35	2k $\Omega$ , 1%, 1/4W, film
R7514	063-10533-18	6190 $\Omega$ , 1%, 1/4W, film
R7515	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7516	063-10938-96	68.1k $\Omega$ , 1%, 1/4W, film
R7517	063-10938-07	11.8k $\Omega$ , 1%, 1/4W, film
R7518	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7523	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7524	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7525	063-11020-57A	220 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7529	063-11021-20A	91k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7530	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7532	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7533	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7534	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7537	063-11020-31A	18 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7538	063-11020-49A	100 $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7539	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Resistors (continued)</b>		
R7540	063-10857-17	Control, rotary, trimmer
R7541	063-11021-37A	470k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7542	063-11020-97A	10k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7543	063-11021-21A	100k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7544	063-11020-73A	1k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7545	063-11020-81A	2.2k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7546	063-11021-01A	15k $\Omega$ , 5%, 1/4W, film, tubular, leadless
R7701	063-10235-88	4.7k $\Omega$ , 5%, 1/4W, film
R7702	063-10235-94	8.2k $\Omega$ , 5%, 1/4W, film
R7703	063-10651-18	Control, rotary, trimmer
R7704	063-10236-30	270k $\Omega$ , 5%, 1/4W, film
R7705	063-10235-80	2.2k $\Omega$ , 5%, 1/4W, film
R7706	063-10236-13	51k $\Omega$ , 5%, 1/4W, film
R7707	063-10243-96	10k $\Omega$ , 5%, 1/2W, film
R7708	063-10442-96	1k $\Omega$ , 5%, 5W, wirewound
R7709	063-07785	1k $\Omega$ , 10%, 1/2W, carbon composition
R7710	063-10235-96	10k $\Omega$ , 5%, 1/4W, film
R7711	063-10235-72	1k $\Omega$ , 5%, 1/4W, film
RX2134	063-10565	1 $\Omega$ , 5%, 1/2W, film
RX2135	063-10565	1 $\Omega$ , 5%, 1/2W, film
RX2136	063-10565	1 $\Omega$ , 5%, 1/2W, film
RX2137	063-10565	1 $\Omega$ , 5%, 1/2W, film
RX2138	063-10565-08	2.2 $\Omega$ , 5%, 1/2W, film
RX2139	063-10836-60	330 $\Omega$ , 5%, 2W, film
	086-00836	Terminal, male
	194-01987	Spacer, ceramic tube
RX2149	063-10565-36	33 $\Omega$ , 5%, 1/2W, film
RX2150	063-10565-36	33 $\Omega$ , 5%, 1/2W, film
RX2151	063-10840-51	130 $\Omega$ , 5%, 3W, film
	086-00836	Terminal, male
RX7535	063-10565	1 $\Omega$ , 5%, 1/2W, film
RX7536	063-10565	1 $\Omega$ , 5%, 1/2W, film

**Table 7-1 (continued). Designated Components Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
<b>Transformers</b>		
T3001	095-04040	Transformer, hybrid scan choke with secondary
T3401	095-03904-01	Transformer, driver
T7501	095-04048	Transformer, pincushion
T7701	095-04049-01	Transformer, dynamic focus
TX3201	095-03753	Transformer, horizontal driver

**Table 7-2. Miscellaneous Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
N/A	009-00688	Module, Video Output
N/A	009-00695-01	Module, PIN/Focus
N/A	009-00712-01	Module, Deflection
N/A	009-00740	Module, Dynamic Focus
N/A	011-00355	Power cord, 3-conductor, shielded
N/A	012-09446	Transistor locator, molded plastic
N/A	012-09520-01	Metal bracket, CRT mounting
N/A	012-09521-02	Metal bracket, right side
N/A	012-09522-02	Metal bracket, left side
N/A	014-11812-03	Cabinet front, molded plastic
N/A	014-11813-01	Cabinet rear, molded plastic
N/A	020-04240-32	Coil, degausser
N/A	022-07523-01B	Capacitor, 0.01 $\mu$ F, $\pm$ 20%, 2000V, ceramic disc
N/A	022-07859-13	Capacitor, 1000 $\mu$ F, 20%, 16V, electrolytic
N/A	030-01284	Name plate
N/A	046-10445-01	Knob, thumbwheel, rotary
N/A	050-01645-03	5R9/5A9 connector and cable assembly

**Table 7-2 (continued). Miscellaneous Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
N/A	050-01654-01	5S6 connector and cable assembly
N/A	050-01656-01	5R6 connector and cable assembly
N/A	050-01657-01	6S5 connector and cable assembly
N/A	050-01659-02	8V6 connector and cable assembly
N/A	050-01662-02	5A6 connector and cable assembly
N/A	050-01674	5A1 connector and cable assembly
N/A	050-01675-01	8R5 connector and cable assembly
N/A	050-01758	8U6 connector and cable assembly
N/A	050-01769	3R6 connector and cable assembly
N/A	050-01770	8R6 connector and cable assembly
N/A	050-01772	3R5 connector and cable assembly
N/A	050-01783	4T8 connector and cable assembly
N/A	054-00250-05	Nut, machine, 6-32 $\times$ 0.312AF $\times$ 0.109THK, ZD hex
N/A	054-00347	Nut, machine, 6-32 $\times$ 0.312AF $\times$ 0.109THK, ZF hex with washer
N/A	054-00347-01	Nut, machine, 6-32 $\times$ 0.312AF $\times$ 0.114THK, ZD hex with washer
N/A	054-00348-01	Nut, machine, 8-32 $\times$ 0.344AF $\times$ 0.130THK, ZD hex with washer
N/A	054-00349	Nut, machine, 10-32 $\times$ 0.375AF $\times$ 0.125 THK ZN hex with washer
N/A	054-00952-01	Nut, machine, 4-40 $\times$ 0.250AF $\times$ 0.093THK BX hex
N/A	054-00952-04	Nut, machine, 4-40 $\times$ 0.250AF $\times$ 0.093THK ZD hex

**Table 7-2 (continued). Miscellaneous Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
N/A	063-11020-85A	Resistor, 3.3kΩ, 5%, 1/4W, film, tubular, leadless
N/A	074-00291	Screen, ventilating
N/A	082-00275-18	Strap, ground, insulated
N/A	082-00371-01	Strap, CRT retaining
N/A	095-04072-01	Transformer, high voltage
N/A	101-07941	Label, X-ray safety notice
N/A	101-08051	Label, shock hazard
N/A	101-08068	Label, warning or caution, electric shock
N/A	101-08102	Label, UL information
N/A	103-00385-05	Diode, visible LED, rectangular, green
N/A	112-01093-03	Screw, thread forming, 4-40 × 0.250, type C, ZD pan head, phillips
N/A	112-01160-02	Screw, thread forming, 8-18 × 0.437, type B, black oxide, pan head, phillips, cabinet rear top
N/A	112-01689-03	Screw, machine, 4-40 × 0.625 ZD, pan head, phillips
N/A	112-01697-07	Screw, machine, 4-40 × 0.375 ZN, pan head, phillips
N/A	112-01724-01	Screw, machine, 6-32 × 1.250 ZD, pan head, phillips
N/A	112-01865	Screw, thread forming, 6-20 × 0.437, type B, cadmium pan head, phillips, two bumpers to foot brackets
N/A	112-02280-01	Screw, thread forming, 8-18 × 0.375, type B, black oxide, flat head, phillips, four insulators to support crossbrace rear
N/A	112-02556	Screw, machine, 6-32 × 0.500 ZD, pan head, phillips
N/A	114-00549-01	Screw, machine, 10-32 × 2.125 ZD × 0.312AF, hex head with washer

**Table 7-2 (continued). Miscellaneous Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
N/A	114-00894-02	Screw, thread forming, 8-18 × 0.5 TP B, ZD 0.250 AF, hex washer head, insulators to heatsink FTM module
N/A	114-00984-03	Screw, thread forming, 6-20 × 0.625 type B, 0.250 AF, hex washer head
N/A	114-01100-01	Screw, thread forming, 8-18 × 0.750 type B, 1/4AF, hex head with washer, two cabinet rear to cabinet front bottom
N/A	114-01108	Screw, thread cut, 620 × 0.375 type BT, ZN 1/4AF, hex washer head, 9 to side bracket, 2 to rear bracket, 2 foot support bracket to side
N/A	114-01108-01	Screw, thread cut, 6-20 × 0.375 type BT, ZD 250AF, hex washer head, deflection module to side brackets
N/A	114-01190-01	Screw, thread forming, 8-18 × 0.625 type AB, ZD 0.250AF, hex washer head
N/A	114-01261	Screw, thread forming, 8-18 × 0.500 type AB, ZD 250AF, hex head with washer
N/A	114-01274	Screw, thread forming, 8-18 × 0.625 type AB, bronze 1/4AF, hex head with washer
N/A	114-01325-03	Screw, thread forming, 4-24 × 0.312 type B, ZD 0.187AF, hex washer head
N/A	114-01379-03	Screw, thread forming, 8-10 × 0.500 hi-riser, ZD 0.250AF, hex washer head
N/A	114-01393-01	Screw, thread cut, 8-10 × 0.625 hi-riser, 0.250AF, hex washer head, frame to front



**Table 7-2 (continued). Miscellaneous Parts List**

REFERENCE NUMBER	ZENITH PART NUMBER	DESCRIPTION
N/A	114-01399	Screw, thread forming, 6-20 × 1.25 type B, bronze, hex washer head, fan and deflector to fan mounting bracket
N/A	114-01403	Screw, machine, 4-40 × 0.250 BX, 0.187AF, hex washer head
N/A	114-01463-01	Screw, thread cut, 10-8 × 1.000 hi-riser, 1/4AF, hex head with washer, CRT bosses
N/A	114-01470-02	Screw, machine, 8-32 × 0.500, 0.250AF, ZD hex head, phillips, I/O cable clamp
N/A	114-01483-01	Screw, thread forming, 6-32 × 0.310 type B, ZN 0.250AF, hex head with washer, contact spring to power supply bracket
N/A	114-01483-03	Screw, thread forming, 6-32 × 0.310 type B, ZD 0.250AF, hex head with washer, contact spring to power supply bracket
N/A	141-00227-03	Fan, 12 VDC
N/A	152-00343-01	Wedge, rubber, CRT retainer

**Table 7-3 Heath Parts List**

HEATH PART NUMBER	DESCRIPTION
234-954	CRT and yoke assembly
234-955	Power supply
234-956	Video output module
234-957	PIN/focus module
234-958	Deflection module
234-959	Dynamic focus module
234-971	Fan, 12 VDC
234-972	Cabinet, front and nameplate
234-973	Cabinet, rear
234-974	LED and cable assembly
234-975	Carton assembly, ZCM-1490

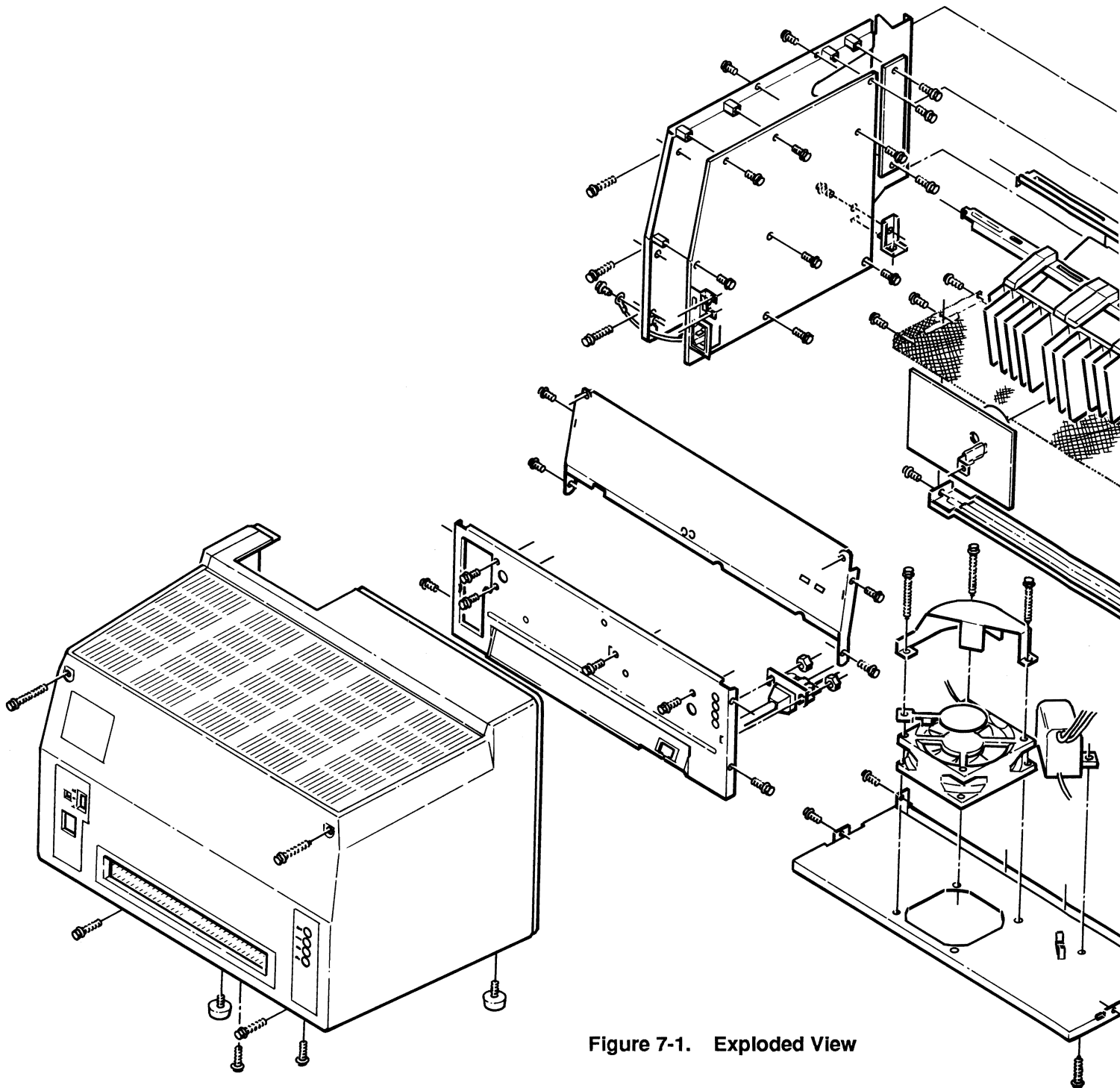
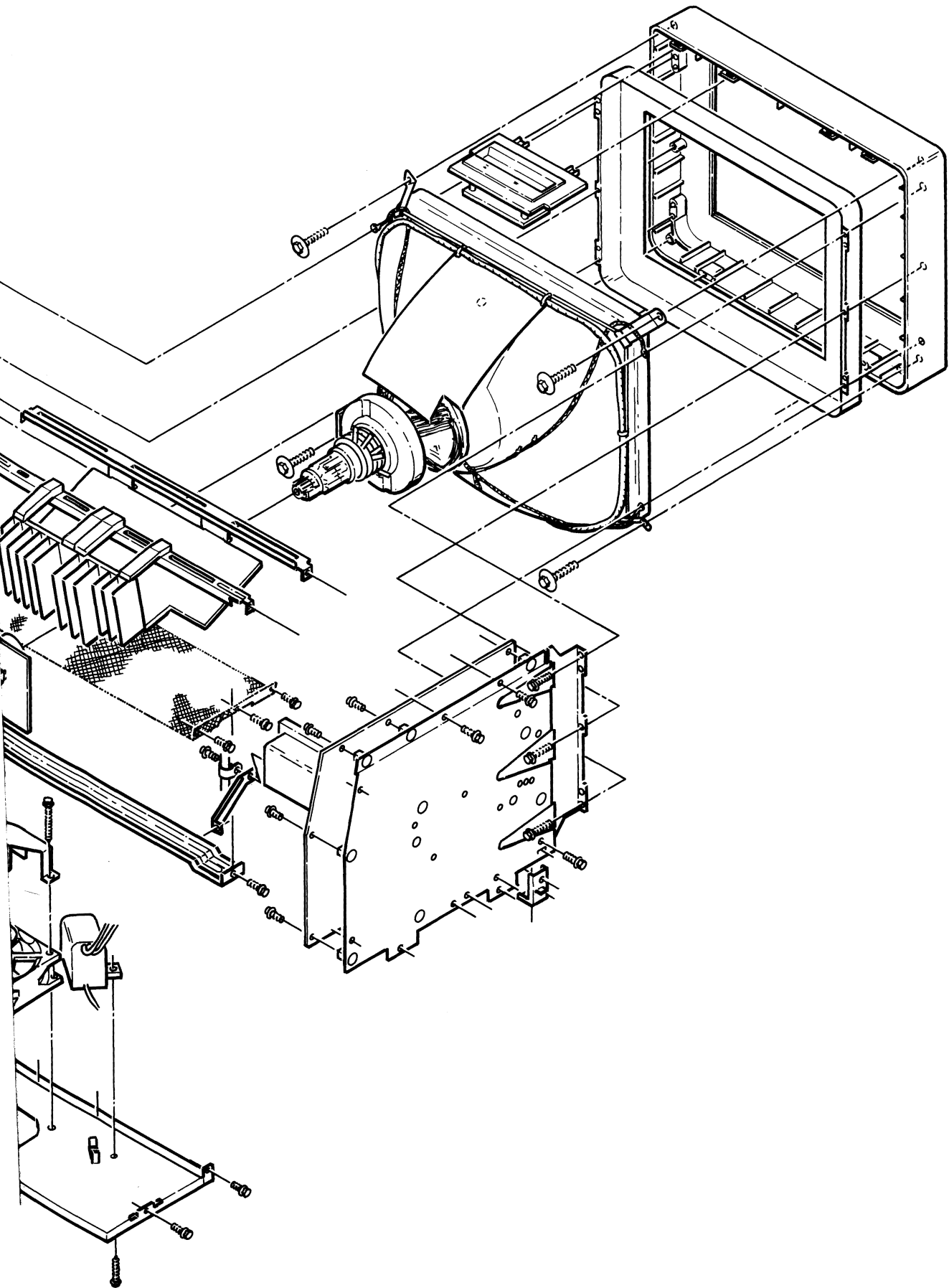


Figure 7-1. Exploded View



# Chapter 8

## Schematics and Waveforms

This chapter contains schematics, waveforms, and component views for the ZCM-1490 color video monitor. Where appropriate, test points are designated on the schematics and component views by a circled number that refers to a corresponding waveform photograph.

### Waveform Explanation

This chapter contains all waveform photographs referred to throughout the manual. Figure 8-1 and the notes that follow it explain the waveform display window and oscilloscope settings. All waveforms were taken with the external brightness and contrast controls set to their detent position. The fill screen test with the capital Z was displayed.

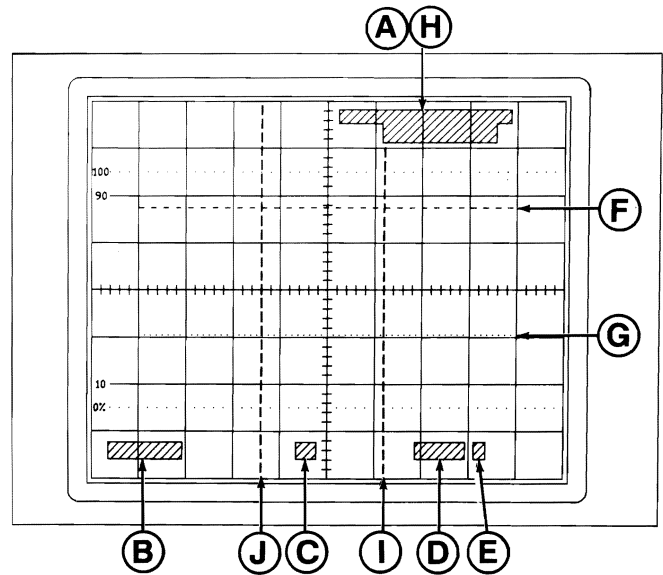
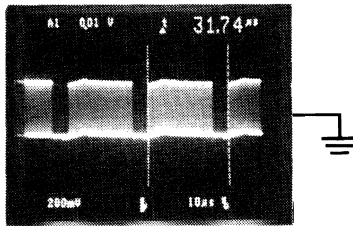


Figure 8-1. Oscilloscope Display Information

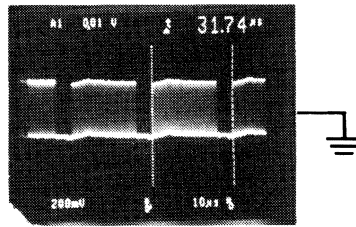
Each waveform photograph is numbered and labeled with a brief identifying note. The waveforms were taken using a Tektronix Model 2445 150 MHz oscilloscope. Your waveforms may be slightly different due to differences in test equipment, monitors, etc. These waveform photographs should serve as a guide for troubleshooting and servicing.

- (A) The delta voltage established between the variable reference cursor (dotted line G) and the variable data cursor (dotted line F). This value, when displayed, indicates the peak-to-peak voltage of the waveform.
- (B) The channel 1 scale factor (volts/division).
- (C) 20 MHz bandwidth limitation indicator.
- (D) Sweep time base (seconds/division).

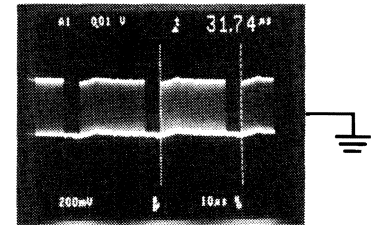
- (E) Holdoff indicator (holdoff refers to the amount of time between the end of the sweep and the time that a triggering signal can initiate the next sweep).
- (F) Data cursor that can be varied on the vertical axis to provide a reference for the delta voltage.
- (G) Data cursor that can be varied on the vertical axis to provide a reference for the delta voltage.
- (H) The delta time established between the variable reference cursor (dotted line J) and the variable data cursor (dotted line I). This value, when displayed, indicates the period of the waveform.
- (I) Data cursor that can be varied on the horizontal axis to provide a reference for the delta time.
- (J) Data cursor that can be varied on the horizontal axis to provide a reference for the delta time.



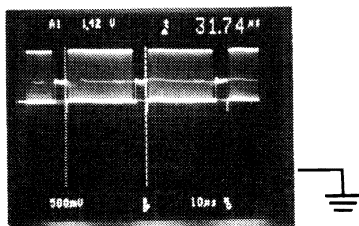
**1. IC5101, PIN 3**



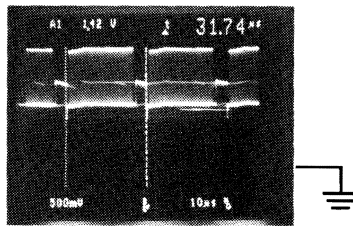
**2. IC5101, PIN 5**



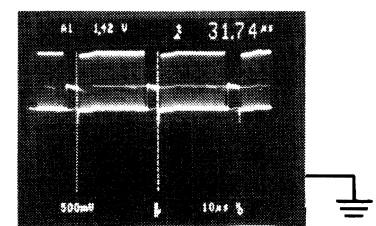
**3. IC5101, PIN 8**



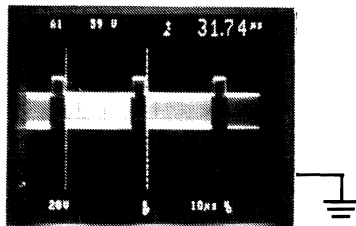
**4. Q5201 BASE**



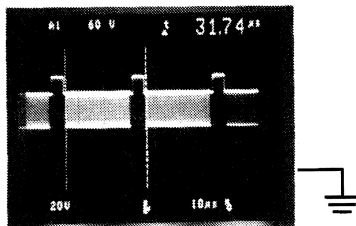
**5. Q5205 BASE**



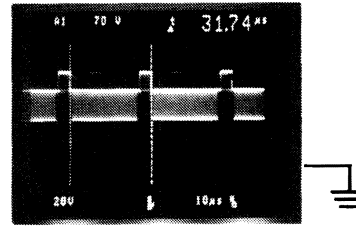
**6. Q5209 BASE**



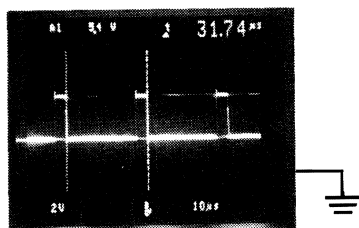
**7. CRT RED**



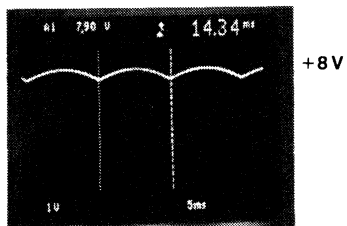
**8. CRT GREEN**



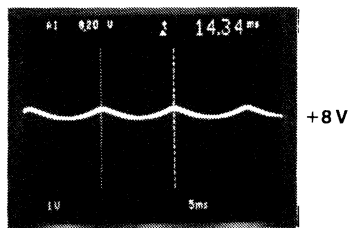
**9. CRT BLUE**



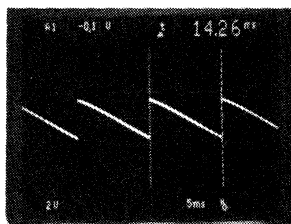
**10. Q5101 EMITTER**



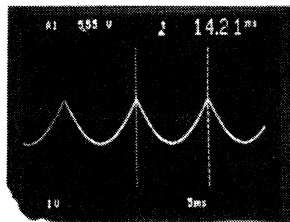
**11. IC7001, PIN 2**



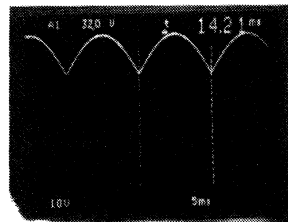
**12. IC7001, PIN 14**



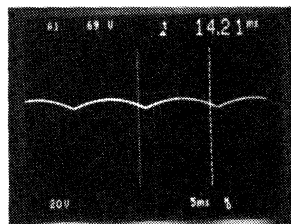
**13. 8U6, PIN 5 (Q7505 BASE)**



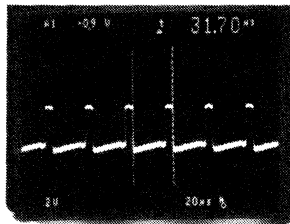
**14. IC7101, PIN 1**



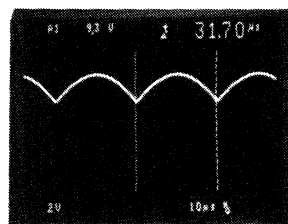
**15. Q7103 COLLECTOR**



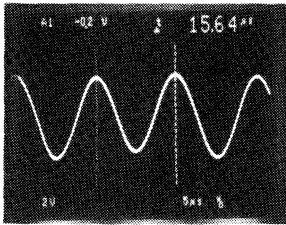
**16. Q7105 EMITTER**



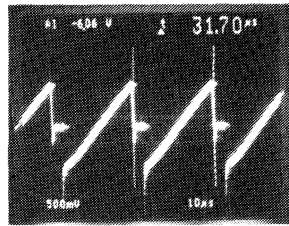
**17. Q7402 BASE**



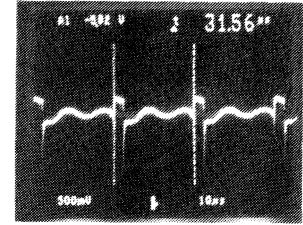
**18. Q7410 BASE**



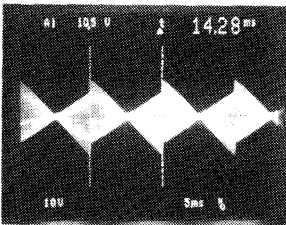
**19. TP1, PIN BOARD**



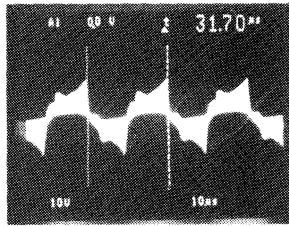
**20. IC7501, PIN 4**



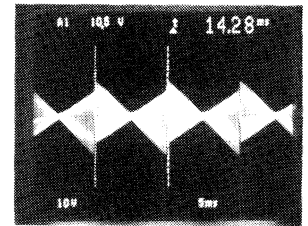
**21. IC7501, PIN 8**



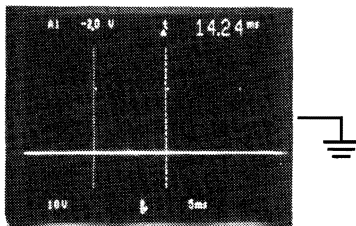
**22. IC7502, PIN 6 (ENVELOPE)**



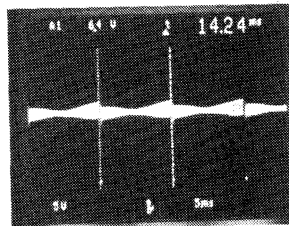
**23. IC7502, PIN 6 (CARRIER)**



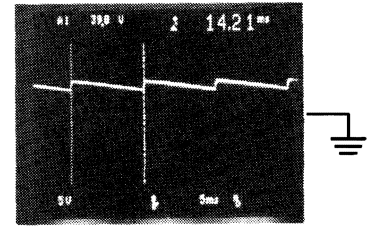
**24. IC7503, PIN 4 (ENVELOPE)**



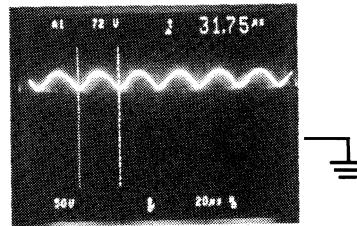
**25. IC2101, PIN 1**



**26. IC2101, PIN 7**



**27. IC2101, PIN 5**



**28. TP3, DEFLECTION BOARD**

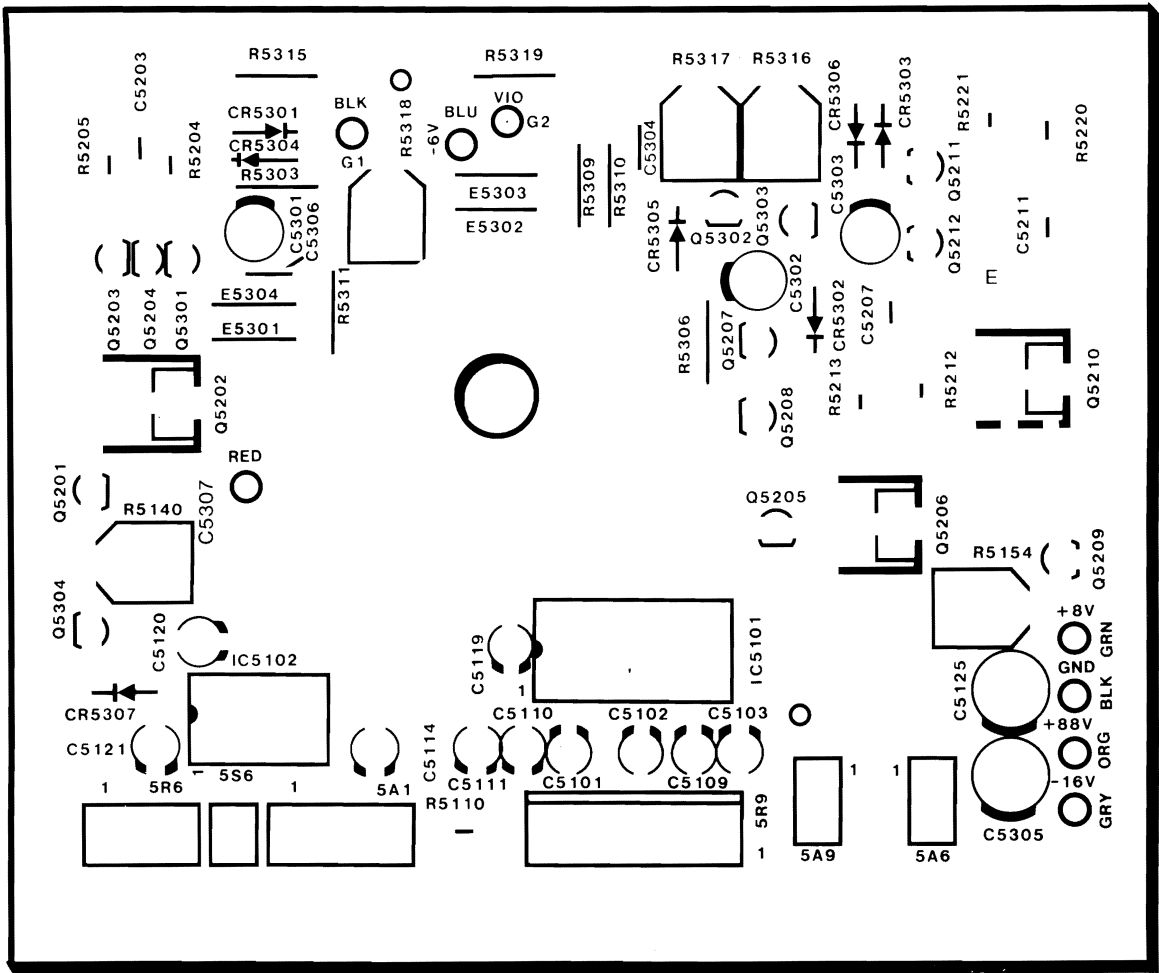


Figure 8-2. Video Board Component View (Component Side)





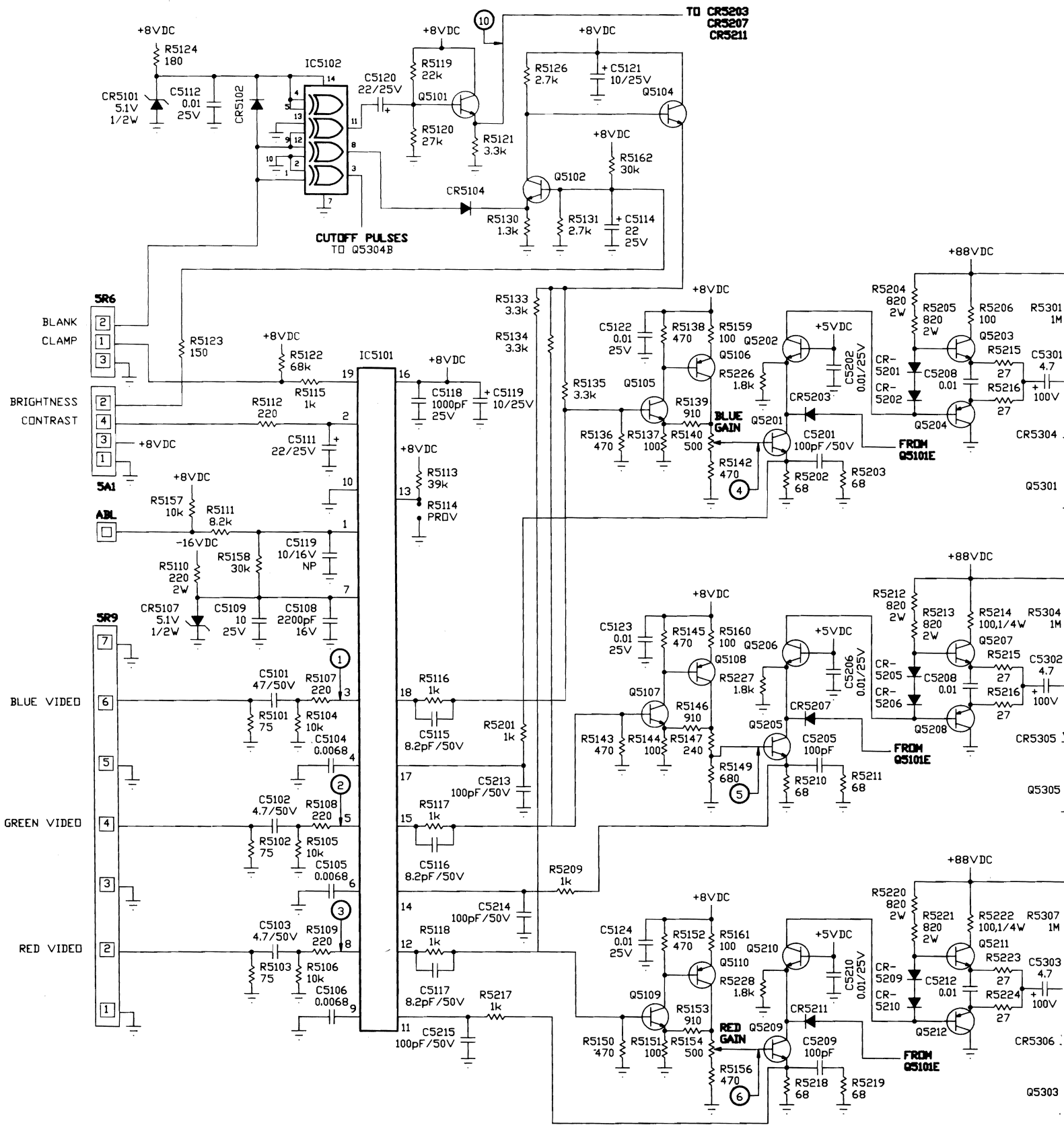
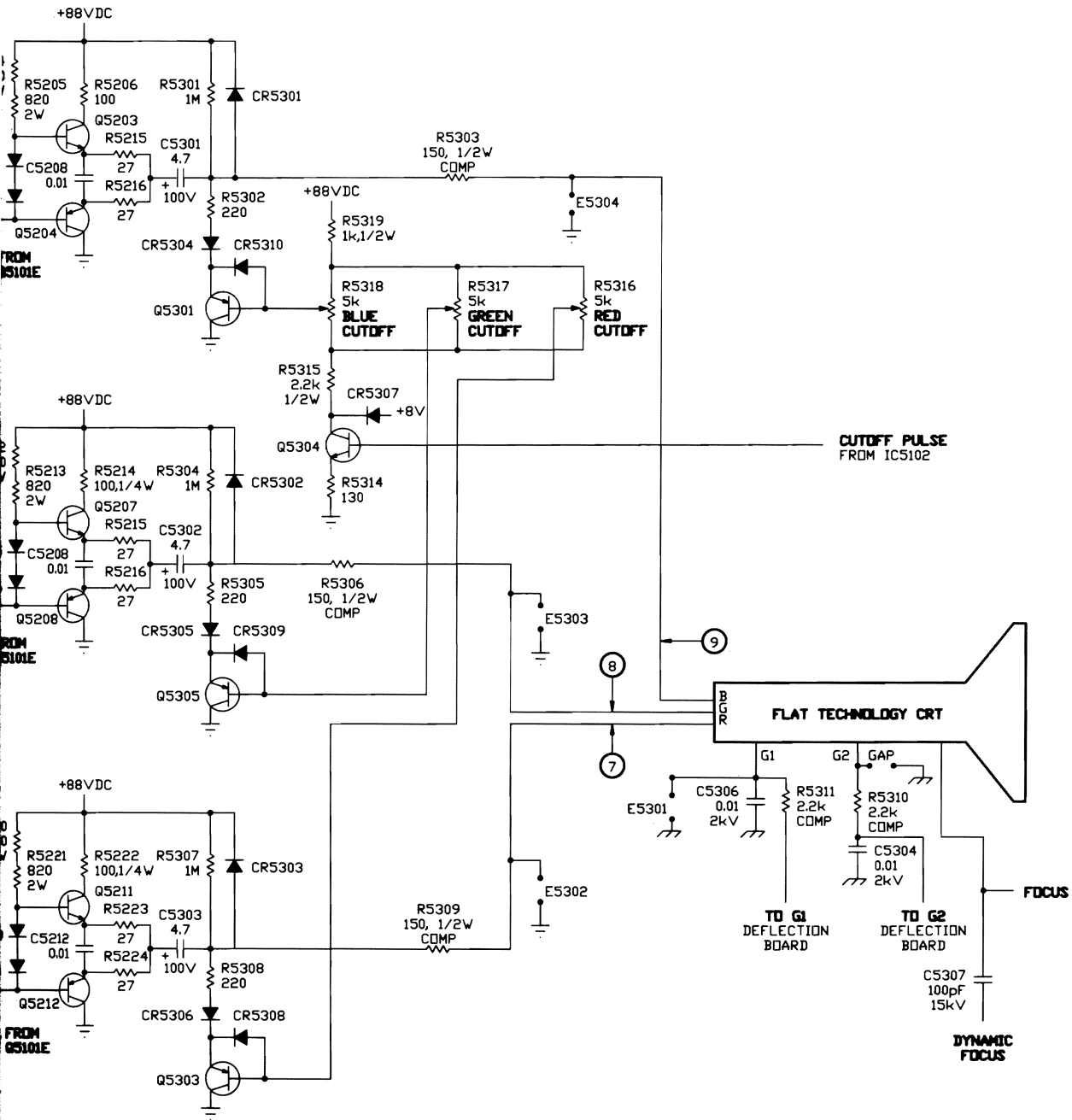
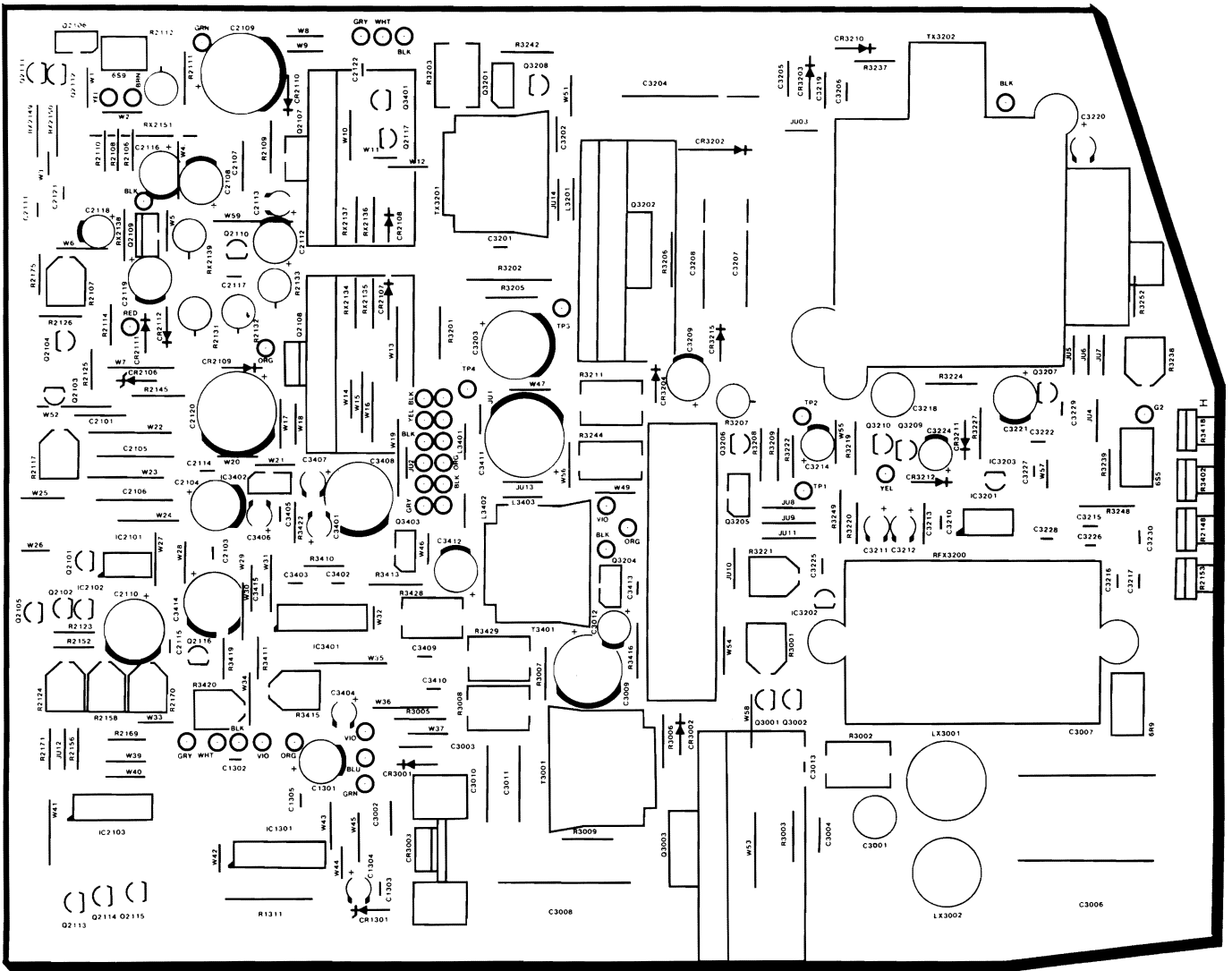


Figure 8-4. Video Board Schema

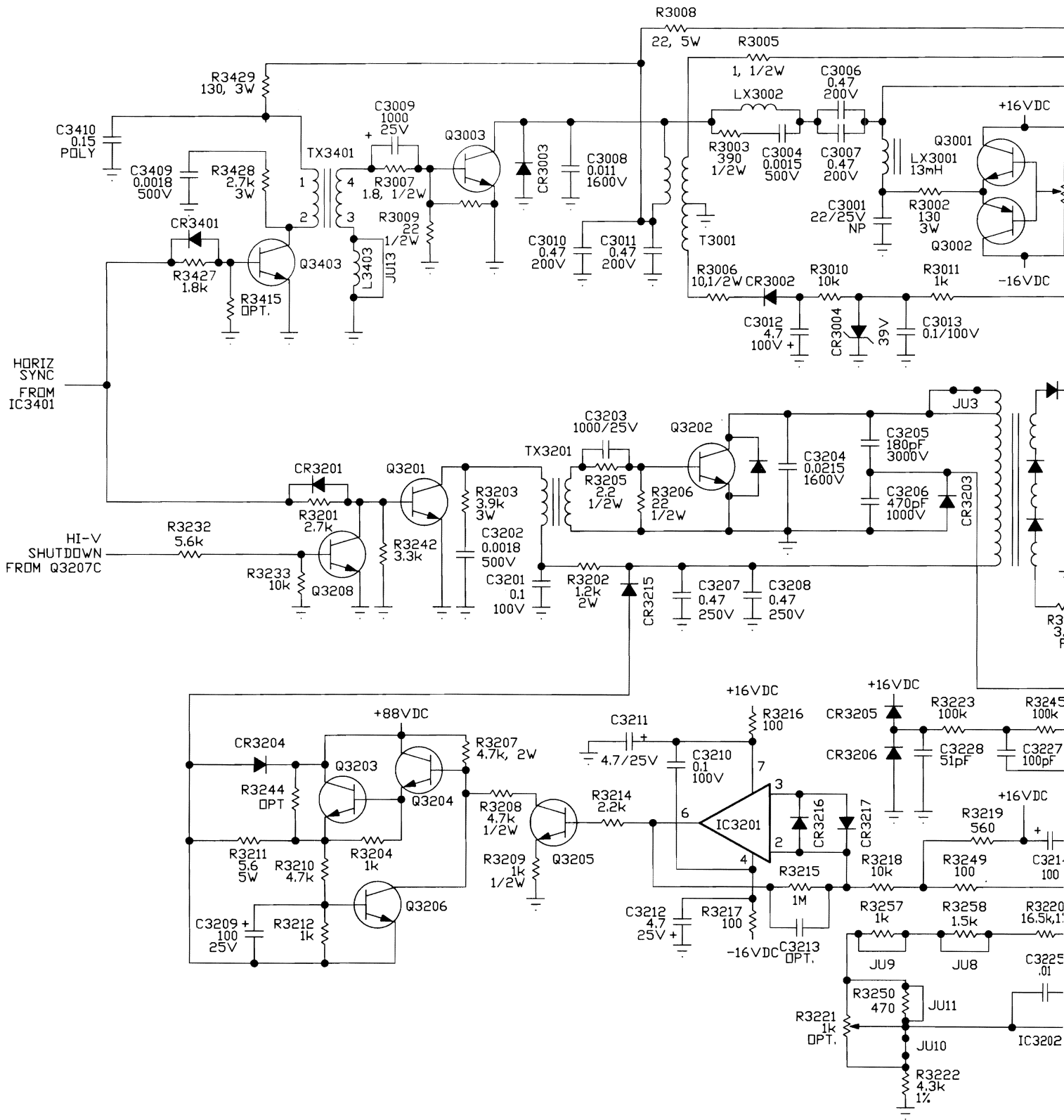


Video Board Schematic



**Figure 8-5. Deflection Board Component View (Component Side)**

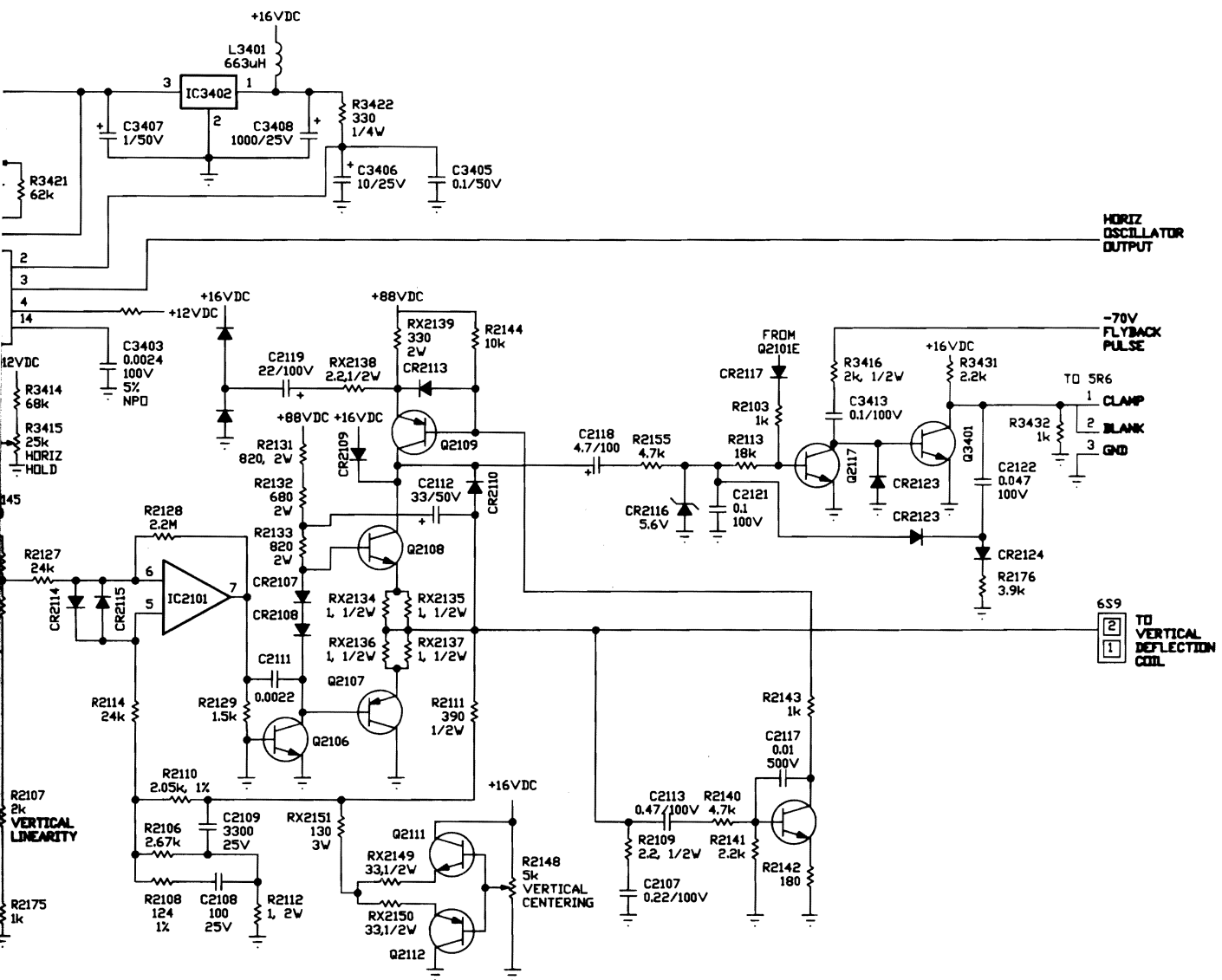












ction/Mode Selection Schematic





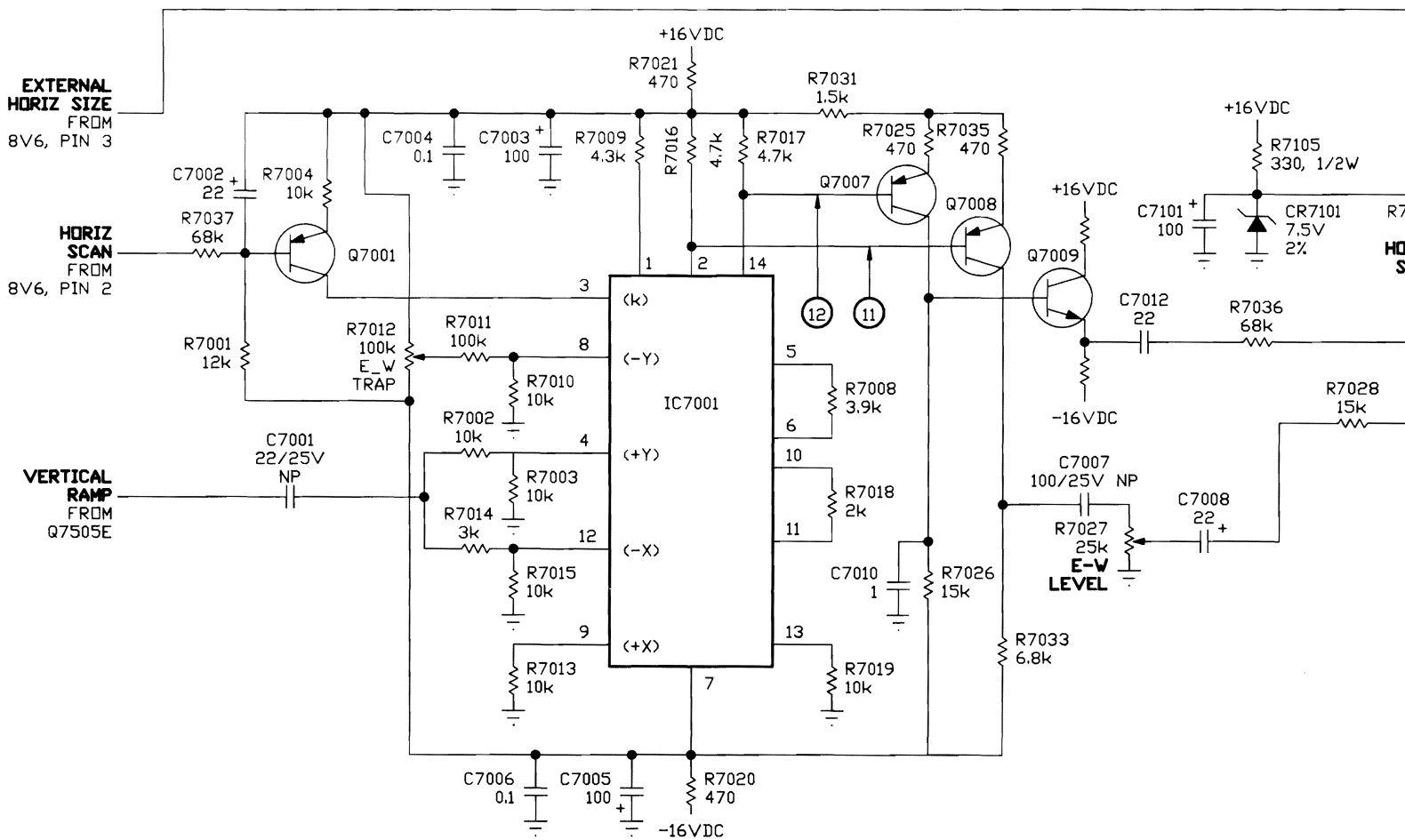
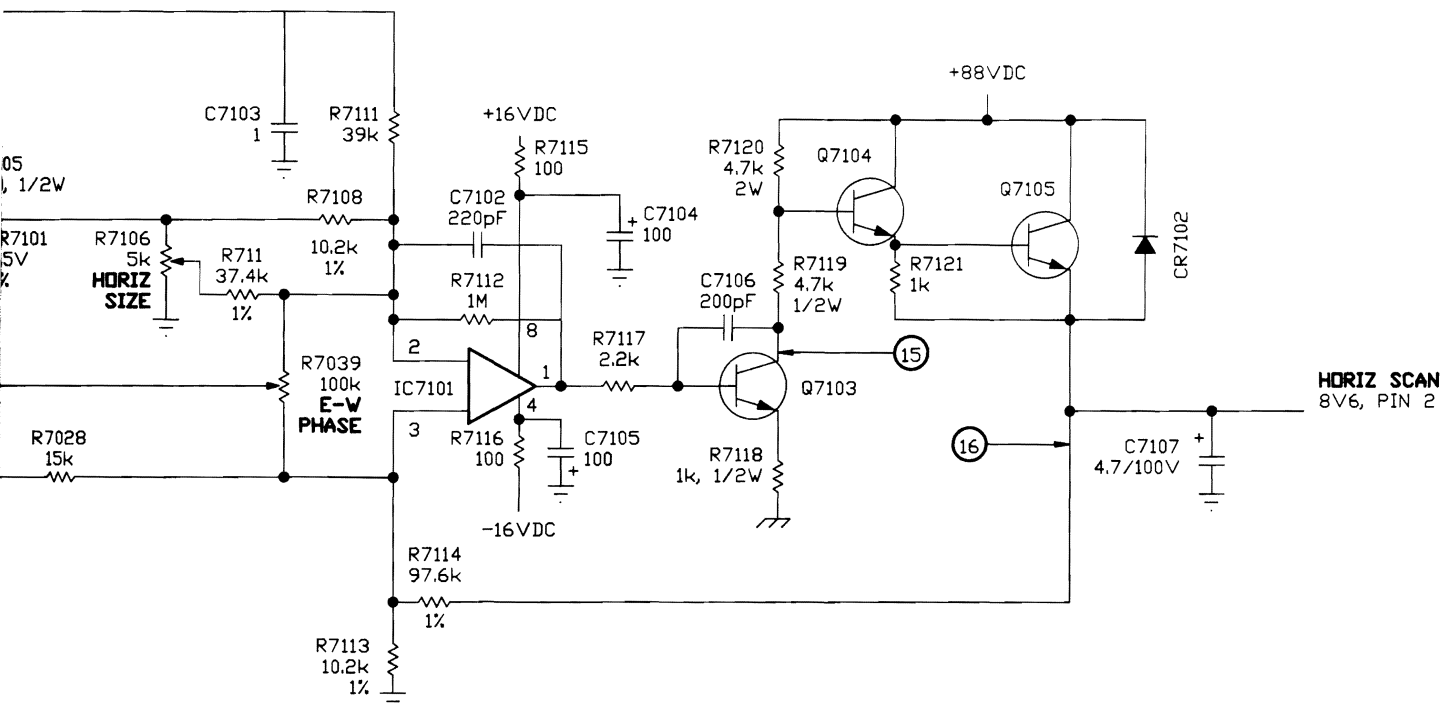


Figure 8-11. E-W Generator/Regulator



or/Regulator Schematic

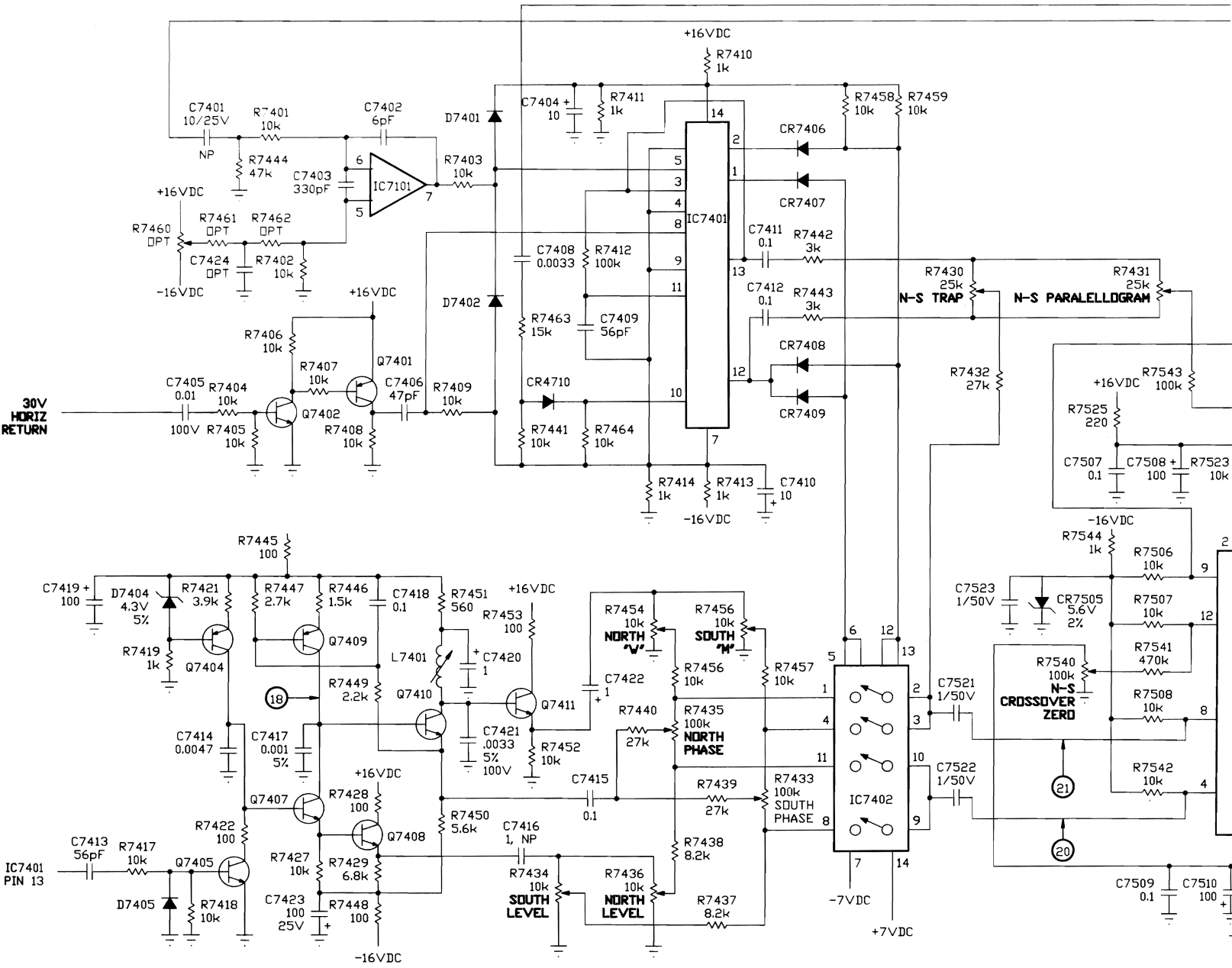
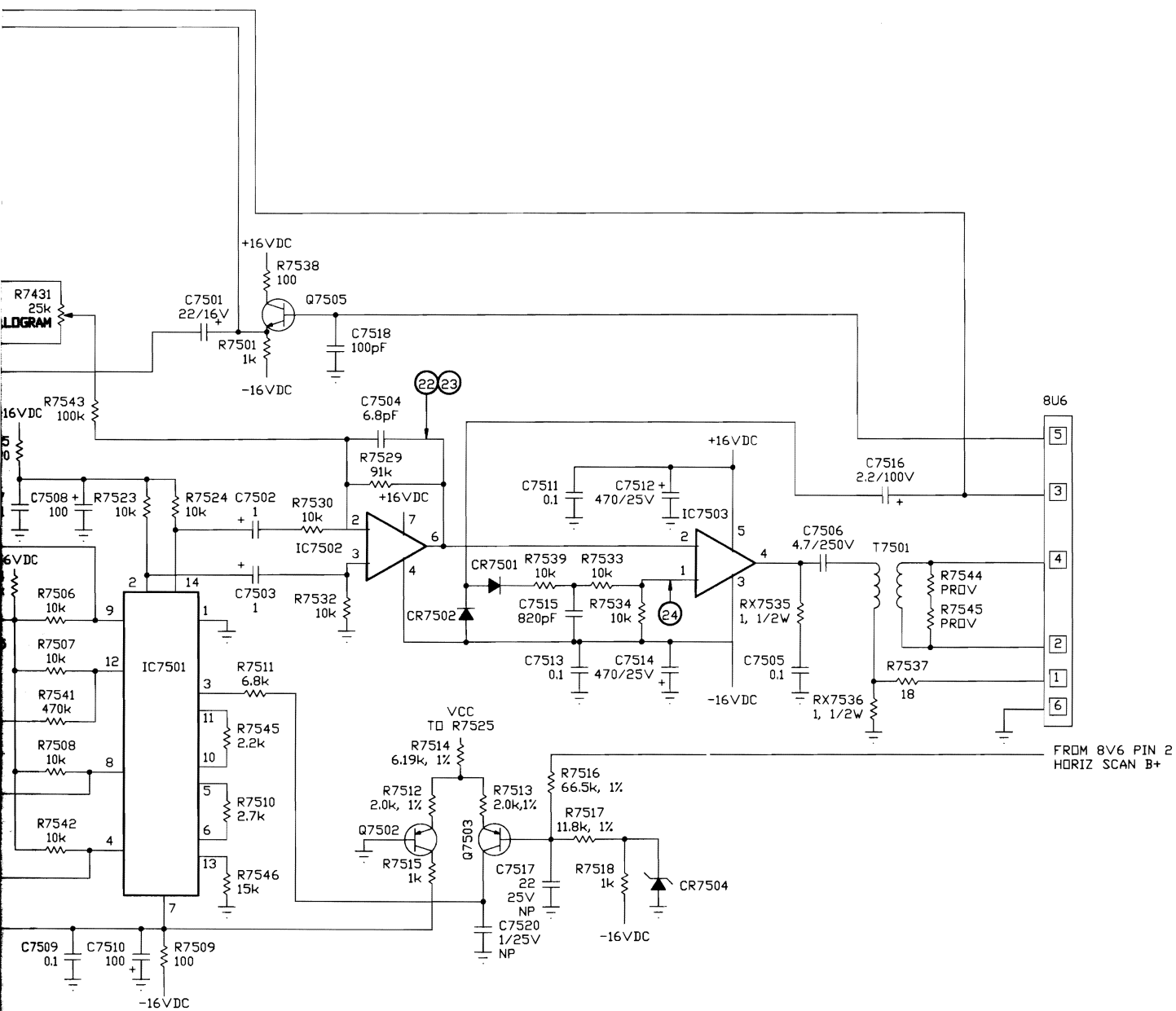


Figure 8-12. N-S Generator/Output Schematic



Output Schematic

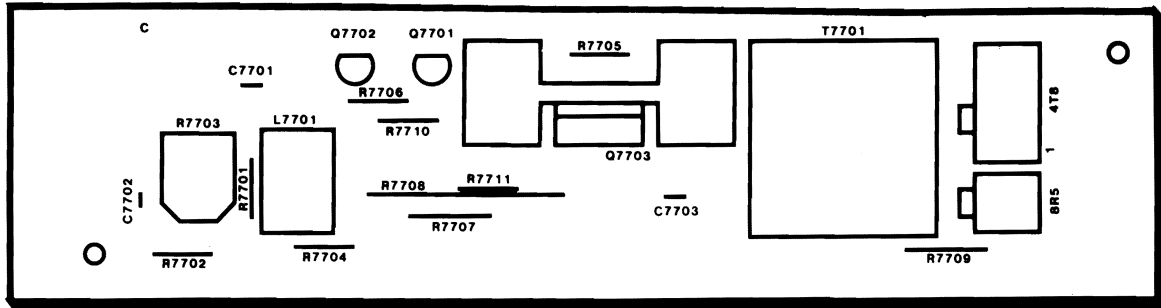


Figure 8-13. Dynamic Focus Board Component View

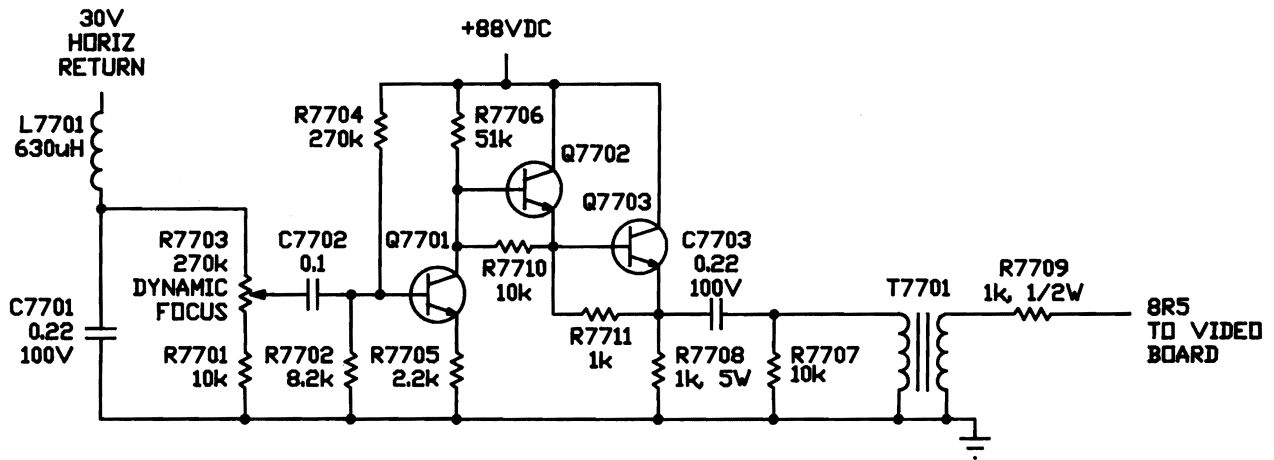


Figure 8-14. Dynamic Focus Schematic

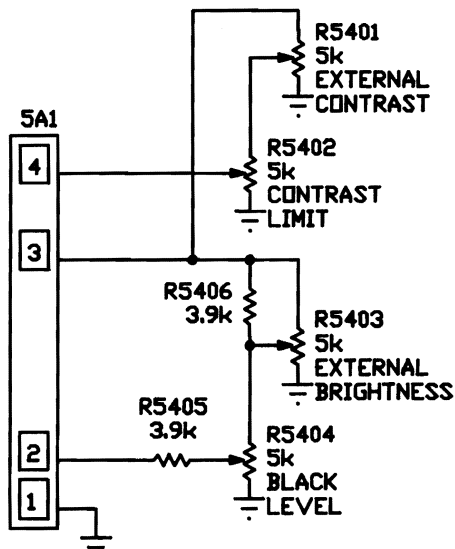


Figure 8-15. Control Board Schematic



# SERVICE MODULE

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# Color Video/Floppy Controller Card

**Z-100 PC Series Computers**

**Part Number 181-5312**

---

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

## Record of Field Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Zenith Data Systems Corporation  
St. Joseph, Michigan 49085

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# Introduction

The Color Video/Floppy Controller Card combines the capabilities of the Z-309-A Video Card and the Floppy Disk Controller Card. This single card provides all of the functions and operations previously supplied by each separate card. Video circuitry and floppy disk controller circuitry may be viewed as two discrete circuits responsible for controlling and processing data for the entire card.

The video section of the card provides an interface between the computer and various display output devices, including a monochrome and a color monitor. The monochrome output connects to an RCA phono jack, and the RGBI output connects to a 9-pin, D-type connector. Both connectors are located directly on the card and project through the rear of the computer cabinet. An optional light pen also may be interfaced to the computer through this card. The light pen connects to a 6-pin connector strip located on the card.

The floppy disk controller section of the card is capable of supporting two separate internal disk drives, and provides communication to peripherals through a single DTE serial channel.

# Chapter 1

## Specifications

### Video

Video RAM .....	16K × 8
Color Selection .....	Foreground, background, and border
Mode Selection .....	Text mode, all points-addressable graphics
ROM Font .....	256 character
Bandwidth .....	7 or 14 MHz, mode-dependent
Output .....	Monochrome and/or color (RGBI)
Sync .....	External vertical, horizontal, and/or composite with selectable polarity
Cursor Type .....	Block, line, blinking, etc.
Light Pen Interface .....	Provided with selectable polarity

### Serial I/O

Communication Channel .....	Single DTE
Communication Element .....	Western Digital 8250 Asynchronous Communica- tions Element (ACE)
Baud rates .....	50 to 19200
Word Length .....	5, 6, 7, or 8 bit
Parity .....	Odd, even, or no parity
Start Bits .....	One
Stop Bits .....	One or two
CPU Port Addressing .....	COM1 (03F8H-03FFH) COM2 (02D0-02DF)
Software Programming .....	Full- or half-duplex

### Floppy Disk Controller

Capacity .....	Two internal 5.25-inch double-sided double-den- sity disks
Floppy Controller .....	NEC $\mu$ PD765
CPU Port Addressing .....	03F0H-03F7H
Heads .....	Two
Encoding Format .....	40 track, 8 or 9 sectors/track, 512 bytes/sector, double density, Modified Frequency Modula- tion (MFM)
Motor Start Time .....	500 ms
Head Load Time .....	35 ms
Head Settle Time .....	25 ms
Stepping Time .....	6 ms track to track

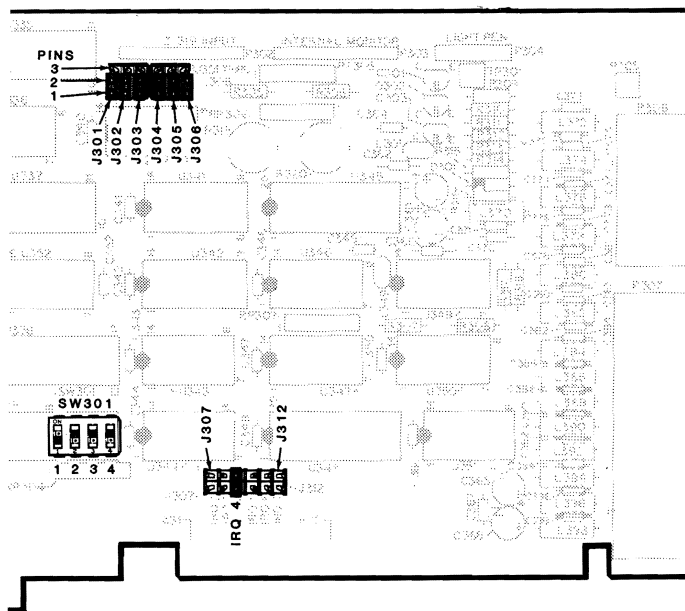
# Chapter 2

## Installation

**CAUTION:** This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

### Configuration

Make configuration selections by positioning jumpers and switches on the Color Video/Floppy Controller Card (Figure 2.1) as specified in Tables 2.1, 2.2, and 2.3.



**Figure 2.1. Switch and Jumper Locations**



## Installation

---

**Table 2.1. Interrupt Vector Selection**

JUMPER	INTERRUPT VECTOR
J307	Interrupt 2
J308	Interrupt 3 (COM2)
J309	Interrupt 4 (COM1) <sup>1</sup>
J310	Interrupt 5
J311	Interrupt 6
J312	Interrupt 7

1. Initial jumper position.

Notes: Normally J308 COM2 (IRQ3) or J309 COM1 (IRQ4) is jumpered.

Only one jumper is to be installed for J307 through J312.

---

**Table 2.2. Monitor Synchronization and Light Pen Configuration**

JUMPER	DESCRIPTION	JUMPER PINS
J301	Light pen polarity	
	positive edge	2-3
	negative edge	1-2 <sup>1</sup>
J302	Ext. monitor vertical sync	
	composite sync	2-3
	pure vertical sync	1-2 <sup>1</sup>
J303	Ext. monitor vertical sync polarity	
	positive	1-2 <sup>1</sup>
	negative	2-3
J304	Int. monitor vertical sync polarity	
	positive	1-2 <sup>1</sup>
	negative	2-3
J305	Ext. monitor horizontal sync polarity	
	positive	1-2 <sup>1</sup>
	negative	2-3
J306	Int. monitor horizontal sync polarity	
	positive	1-2 <sup>1</sup>
	negative	2-3

1. Initial jumper position.

NOTE: Video Sync signals interface with external connector P306 and internal monitor connector P303.

---

**Table 2.3. DIP Switch Options**

SWITCH <sup>1</sup>	DESCRIPTION	POSITION
SW301, pin 1	Character code select custom standard <sup>2</sup>	ON OFF
SW301, pin 2	Serial port select COM1 (IRQ4) <sup>2</sup> COM2 (IRQ3)	ON OFF
SW301, pin 3	Serial port enable enabled <sup>2</sup> disabled	ON OFF
SW301, pin 4	Video enable enabled <sup>2</sup> disabled	ON OFF

1. These pin designations refer to the printing on the card. The pin designations on SW301 may differ depending on installation orientation of the switch.

2. Initial switch position.

## Installation Steps

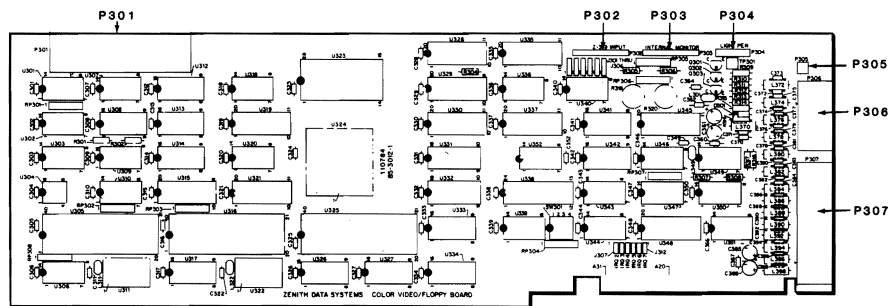
**NOTE:** Do not attempt to replace the two individual cards (Video and Floppy Controller) with this 181-5312 Video/Floppy Controller card.

1. Using the current Z-150 computer, refer to the procedures in the *Z-150 Base Unit Service Module* and remove the video card and floppy controller card.
2. Make sure that the Color Video/Floppy Controller Card is properly configured for monitor synchronization and interrupt vector selection.
3. Plug the card into one of the long vacant slots on the backplane board; make sure to install the bracket retaining screw.
4. Connect the floppy disk drive cable to P301 on the Color Video/Floppy Controller Card.

## Installation

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5. If the computer has a Z-319 high-resolution graphics card installed, connect its cable to P302 on the Color Video/Floppy Controller Card.
6. Connect the internal monitor cable (Z-160 only) to P303 (see Figure 2.2).
7. Install the disk drive cover assembly (Z-160 only).
8. Connect external device cables to P305 (Composite Video), P306 (RGBI Video), and P307 (Serial Port) at the rear of the computer as required.



**Figure 2.2. Card Connectors**

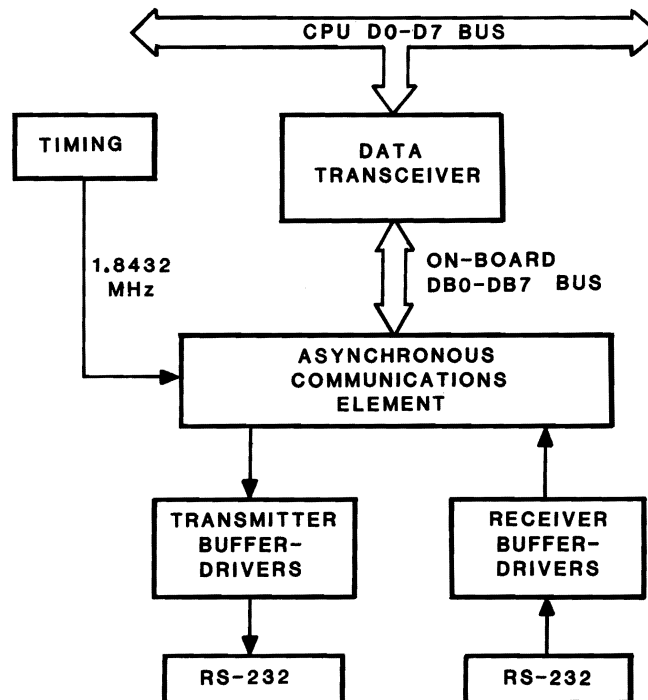
# Chapter 3

## Circuit Description

**NOTE:** The symbols on the schematics (Figures 5.2 through 5.5) represent logic flow rather than any specific device's design.

### Serial I/O Interface

Data transmission to and from the Data Terminal Equipment (DTE) is interfaced to the CPU D0 through D7 data bus through an Asynchronous Communications Element (ACE), and a data transceiver (see Figure 3.1). The ACE accepts parallel data at the onboard DB0 through DB7 bus inputs and converts the data to serial format for transmission. The ACE also accepts serial data from the DTE and converts the data to parallel format for application to the onboard DB0 through DB7 bus.



**Figure 3.1. Serial I/O Block Diagram**

## Circuit Description

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### Detailed Circuit Description

- **ACE Bus Interface** — Data transceiver U348 transfers data from the CPU D0 through D7 bus to the onboard DB0 through DB7 bus when the data direction (XCVRD) signal from pin 15 of PAL Address Decoder (U338) is in a high state. When the XCVRD signal is low, data from the onboard DB0 through DB7 bus is transferred to the CPU D0 through D7 data bus.
- **Chip Selection** — When the chip select signal (CS8250\*) from pin 18 of U338 is true, 8 different internal registers of the ACE (U316) can be accessed. Bits A0, A1, and A2 of the main address bus are used to select a particular register within the ACE. Data can then be written into or read from that register. The IOWDLY\* signal from pin 8 of U309 enables the selected register to be written to, and the IORDLY\* signal from pin 6 of U309 enables the selected register to be read.
- **Interrupt Conditions** — The ACE (U316) provides four levels of interrupt conditions. The Receiver Line Status is of the highest priority, followed by the Received Data Ready, Transmitter Holding Register Empty, and MODEM status conditions. The interrupt signal is issued at pin 30 (INTRPT) of U316 and is buffered by three-state driver U339, which is enabled through a software controlled low signal at pin 31 of the ACE (U316). Jumpers J307 through J312 allow the user to determine which interrupt vector from IRQ2 to IRQ7 to use. Only one jumper at a time should be connected. The standard configuration for COM1 is to use IRQ4 (J309) and COM2 to use IRQ3 (J308).
- **Data Transmission and Reception** — Received signals are buffered and converted to TTL levels by U347 and U350. The input lines to U347 are pulled up by resistor pack RP307. If a signal is not present on one of the input lines, RP307 makes sure that a high exists on that line. Transmitted signals are buffered and inverted by U351. The I/O signals are filtered by L-C networks to dampen RFI emissions.
- **Timing** — U322 is a 1.8432 MHz oscillator which clocks the ACE's internal circuitry and baud rate generator. The clock signals are applied to pin 16 (XTAL1) of the ACE (U316).

## Floppy Disk Controller

The Floppy Disk Controller (FDC) allows data to be read from and written to one of two mini-floppy drives internal to the machine (see Figure 3.2). The FDC interfaces with the CPU D0 through D7 bus for data transfer, Direct Memory Access (DMA) operations, and interrupt requests. Data can be transferred using DMA capabilities or by generating interrupts for each data byte.

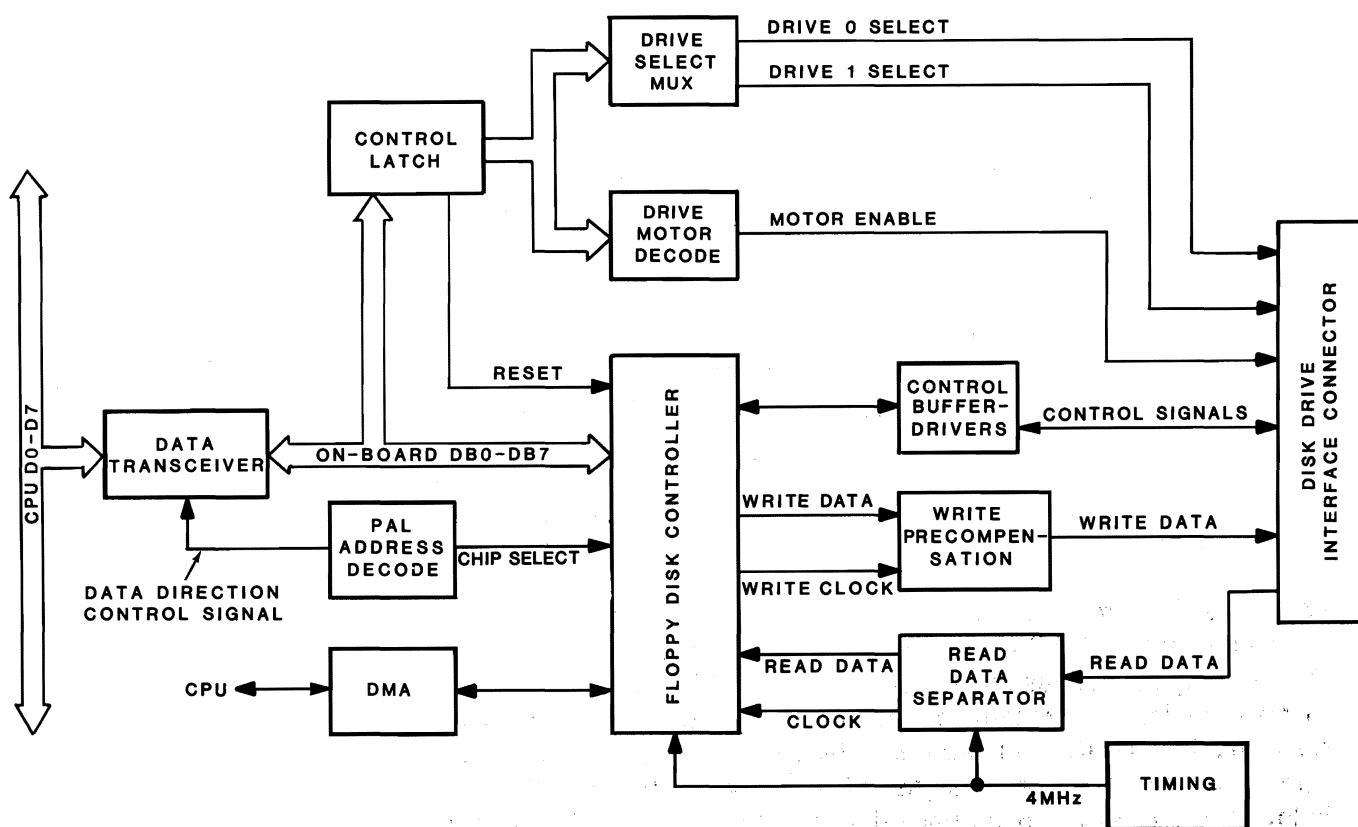


Figure 3.2. Floppy Disk Controller Block Diagram

## Circuit Description

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### Detailed Circuit Description

- **Hard Reset** — The signal on bit DB2 of the onboard DB0 through DB7 data bus is set low by the CPU at power up. The low signal is latched by pin 6 of U321 and inverted by pin 12 of U302. The resulting high at pin 1 of U305 holds the floppy controller (U305) in a “reset” condition until a software controlled command changes the status of bit DB2.
- **Chip Selection** — The signal on bit A1 of the main address bus is buffered by pin 6 of U339 and then ORed with the signal from pin 17 of PAL address decoder U338 to provide the chip select (CS\*) signal to floppy controller U305.
- **Register Selection** — The signal on bit A0 of the main address bus is buffered by pin 11 of U339 and acts as an input to pin 5 of U305. The status of bit A0 enables the internal data register (A0 = 1) or internal status register (A0 = 0) of U305 to transfer its contents to the on-board DB0 through DB7 data bus.
- **Direct Memory Access (DMA)** — The floppy controller originates a request for a direct memory access to the DMA processor on the CPU card. The direct memory access request (DRQ2) signal from pin 14 of U305 is delayed by flip-flop U313. Pin 13 of U317 provides 2 MHz clock signals to the delay flip-flop. The delayed DRQ2 signal is buffered and driven by pin 10 of U308 to the DMA processor on the CPU card.

When the CPU recognizes the DMA request (DRQ2) signal, an acknowledge signal (DACK2\*) is provided to floppy controller U305. The DACK2\* signal enables the internal registers of floppy controller U305 to be read from or written to. The DACK2\* signal also clears the delay flip-flop U313. PAL address decoder U338 then outputs the transceiver direction control signal XCVRD. When the XCVRD signal is low, transceiver U348 is enabled to transfer data from the onboard DB0 through DB7 bus to the CPU D0 through D7 bus.

## Circuit Description

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When transceiver U348 Pin 1 is in a high state, the direction of data transfer is from the CPU D0 through D7 bus to the onboard DB0 through DB7 data bus. When the data transfer is complete, floppy controller U305 issues an interrupt request (IRQ6) at pin 18 of U305, causing the DMA operation to stop. The IRQ6 signal is buffered and driven onto the computer backplane bus by pin 14 of U308.

- **Disk Drive Selection** — Disk drive selection is made through the decoded outputs of U312. Two separate internal disk drives can be selected to interface with the floppy controller. The CPU places data onto the onboard DB0 through DB7 bus through data transceiver U348. The status of data bits DB0 and DB1 are latched by pins 2 and 5 of flip-flop U321 and provide the select A and select B inputs to U312. The status of bits DB4 and DB5 are latched and then ORed by pin 3 of U320 to provide the data input to pin 1 of U312. Similarly, the status of data bits DB6 and DB7 are latched and then NORed by pin 13 of U301 to provide the data input to pin 15 of U312. The decoded disk drive select signal (DS0\*, DS1\*, DS2\*, or DS3\*) is transmitted to the disk drive through pin 10, 12, 14, or 6 of P301, respectively. The outputs at pin 3 of U320 and pin 13 of U301 supply the MOTOR\* signal to pin 16 of P301.
- **Beginning of Track** — The INDEX\* signal from the selected disk drive is interfaced to the floppy controller through pin 8 of connector P301, pulled up by pin 5 of resistor pack RP301, and inverted by pin 8 of U302. The resulting IDX signal at pin 17 of U305 indicates the beginning of a track on the disk.
- **Read/Write Head Selection** — A high head select (HD) output signal from pin 27 of U305 is inverted by pin 6 of U307 providing the SIDE1\* signal to pin 32 of connector P301. When the signal at pin 6 of U307 is high, SIDE0 is selected.
- **Disk Sector Seek — Read/Write Modes** — The floppy controller initiates either a seek or read/write mode. In the seek mode, the head within the floppy disk drive can be moved to a different portion of the magnetic disk. The read/write mode allows data to be read from a sector on a disk or to be written to a sector on a disk.



## Circuit Description

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When pin 39 of U305 is high, the SEEK signal is active and forces the output at pin 1 of U306 low, indicating to the floppy controller that it is seeking on a two-sided disk. The head within the drive can be moved in either of 2 directions. The SEEK signal enables pin 3 of NAND gate U306 which buffers and inverts the head direction control signal (DIR) from pin 38 of U305. The status of the DIR\* signal determines which direction the head will be moved and is interfaced to the disk drive through pin 18 of connector P301.

In the read/write mode pin 39 of U305 is low, driving pins 3 and 6 of U306 high which disable the head stepping and direction control signals. The head within the disk drive therefore remains on that track allowing data to be either written to or read from that track.

- **Head Stepping** — A stepping pulse is used to move the head within the floppy drive to a different track. The SEEK signal enables pin 6 of NAND gate U306 which buffers and inverts the stepping pulse signal (STP) from pin 37 of U305. The STP\* signal is interfaced to the disk drive through pin 20 of connector P301. After the head is stepped to a different track and encounters track 0, the TRACK0\* signal becomes active-low and forces pin 4 of U301 high, indicating to the floppy controller that track 0 has been found.
- **Write Data** — Write data is converted from parallel to serial form by the Floppy Disk Controller (FDC), buffered, and synchronized with the Write Gate\* signal by external logic.

The Write Enable (WE) signal from pin 25 of floppy controller U305 is buffered and inverted by pin 3 of three-state buffer U308. The resulting WRITE GATE\* signal is interfaced to the disk drive through pin 24 of connector P301, and enables the drive to accept data.

Data is written onto the disk at a rate determined by the WCK clock frequency. The ripple carry output signal at pin 15 of U317 is paralleled with pin 9 of OR gate U320 and pin 3 of flip-flop U315. The flip-flop delays the signal and provides inputs to pin 10 of OR gate U320 and pin 4 of flip-flop U315. The output at pin 8 of U320 is used to provide the WCK clock signals which govern the Write Data transmission rate. A high signal at pin 5 of U315 enables pin 3 of U310 to transfer Write Data.

## Circuit Description

- **Write Precompensation** — The Write Data (WDA) output from pin 30 of U305 is applied to the write precompensation circuitry consisting of flip-flop U315, the three NAND gates of U310, and multiplexer U314. The PS0 and PS1 inputs to U314 are used to determine early, late, and nominal precompensation status. See the following Precompensation Chart.

	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

When the status is nominal, the WDA is output at pin 9 of U314, fed back to flip-flop U315, and then output as the WRTDATA signal. Pin 4 of U307 buffers and inverts the WRTDATA signal providing the WRTDATA\* signal which is interfaced to the disk drive through pin 22 of connector P301.

- **Write Protection** — During the write cycle, pin 39 of U305 is in a low state, enabling pin 11 of NOR gate U306. If the disk being used has a write protect tab on it, a low signal will result at pin 12 of NOR gate U306. The output at pin 11 of U306 therefore goes high indicating to the floppy controller that the disk in use cannot be written to.

During the write cycle, the low signal at pin 39 of U305 disables pins 3 and 6 of NAND gates U306 so that the direction (DIR) and stepping pulse (STEP) signals cannot affect the read/write head in the disk drive.

- **Read Data** — During the read cycle, data is interfaced to the Color Video/ Floppy Controller Card through pin 30 of connector P301. The serial signals are applied to data separation chip U304 which separates the serial clock signals from data signals as they are received from a floppy drive. U304 is active on the leading edge of a pulse and has a reference clock input of approximately 4 MHz derived from pin

## Circuit Description

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14 of flip-flop U317. Pins 5 and 6 of U304 are used to select the internal division ratio of the reference clock. With both inputs tied low, the division ratio is one. The Separated Clock (SCLK) signal therefore provides the Read Data Window (RDW) input at pin 22 of floppy controller U305 with 4 MHz timing signals. The Separated Data (SEPD) from U304 is buffered and inverted by pin 4 of U303, and then input to pin 23 of U305. The FDC converts serial data reception into parallel form for application to the onboard DB0 through DB7 data bus.

While the read cycle is active, the direction (DIR) and stepping (STEP) signals are disabled so that the read/write head is not affected, and Pin 11 of U306 is forced low indicating to the floppy controller that the disk being used is of a two-sided media.

- Timing — U311 is an 8.00 MHz oscillator which provides timing signals to flip-flop U315 and binary counter U317. The counter provides divided frequency outputs to floppy controller U305, the delay flip-flop U313, and the write precompensation flip-flop U315.

## CRT Controller

U325 is a Cathode-Ray Tube (CRT) controller IC. Data on the CPU D0 through D7 bus is interfaced to the CRT controller through a data transceiver U348. The CRT controller utilizes signals on the bus to derive control signals and video RAM addresses.

The following paragraphs define the functions and interrelationships of the signals appearing on the pins of the 6845. The signals fall into three categories: signals which interface the controller with the microprocessor and system busses; signals which interface the controller with the video memory bank and character generator logic; and signals which directly relate to controller/monitor interfacing.

## Microprocessor Interface Signals

Table 3.1 defines the signals used to provide communication and data transfer between the video portion of the card and the rest of the system.

## Circuit Description

**Table 3.1. Video Logic-to-System Logic Interface Signals**

SIGNAL	FUNCTION
A0 to A19	The 20 system address lines used to access memory locations.
D0 to D7	Bidirectional data lines which transfer information between the CPU and the internal registers of the 6845.
CS*	Chip Select signal typically generated by system address decoding logic. CS* must be low to read information from, or write information to, one of the 6845 internal registers.
RS	6845 register select signal. Rather than sacrifice five of the 40 available pins to 6845 register-addressing, one of the registers is used as an address register to access the other 18 registers. When the RS signal is low, the address register is accessed and then can be loaded with the address of the internal register to be accessed next. When RS is high, the addressed register may be accessed.
R/W*	The read/write signal. It determines whether data is to be written into or read from an internal register. R/W* is low for a write operation, high for a read operation.
E	The enabling (synchronizing clock) signal required by the 6845 which enables the internal I/O buffers and clocks data into and out of the internal registers via the data buffers. In this computer, the E input connects to the gate array.
CLK	Synchronizes the 6845's control signals. It is derived from the system clock to become the character rate clock in text mode. Although this signal is more closely related to the character generator and video interface, it is included here because it is the primary timing unit to the 6845.
RESET*	Initializes the 6845. When this pin goes low, the internal counters are cleared and the 6845 outputs go low, effectively stopping the video display operation. As the RESET* signal does not affect the program-accessible counters within the 6845, display may continue when RESET* goes high.
Vcc (+5 V) and Vss (Ground)	Standard TTL power levels which enable proper operation of the ICs.

## Circuit Description

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### Screen Memory and Character Generator Signals

There are two sets of signals provided by the 6845 to implement screen memory and character generator logic interface. MA0 through MA13 are screen memory address outputs, and RA0 through RA4 are the raster address signals to character generator logic. The 14 screen memory address lines allow the 6845 to address the 16K of video memory. The raster address lines are outputs from the 6845's scan line counter required by the character generator logic to determine which scan line of a character row is in progress.

### CRT Monitor Signals

HSYNC and VSYNC are standard horizontal and vertical synchronization signals required by the CRT monitor for display stabilization. DISPEN is the display enable signal which goes high whenever the video signal to the CRT is to be active. DISPEN is low during horizontal and vertical retrace, and also could be called the video blanking signal. CURSOR is the cursor enable signal which allows a steady stream of dots to be produced on the CRT screen as a cursor symbol.

LPEN is the light pen strobe input signal which may be used to interface a light pen. A high on the LPEN line signals the 6845 to save the contents of the screen memory address in one of the internal register sets so the microprocessor can subsequently determine the position on the monitor screen at which the light pen was detected.

### CRT Controller Registers

The 19 internal registers of the 6845 CRT controller can be software-programmed to define display and control parameters of a raster-scanned monitor. One of these registers, the address register, is used only as a pointer to the addresses of the other 18 registers. The address register is write-only and is loaded from the CPU, using an I/O OUT instruction to the I/O port at 3D4. This register is loaded with the five least-significant bits from the I/O port.

## Circuit Description

The other 18 registers are selected by the pointer information in the address register, then the CPU directs the information at address 3D5 to be loaded into the selected register. Transfers of address and parameter information to and from the registers is via data lines D0 through D7.

## Programming the Registers

Table 3.2 defines individual registers in terms of values contained in them and the results obtained with these values. All values are expressed in hexadecimal.

**Table 3.2. CRT Controller Register Functions**

REG. ADDR.	REG. NO.	REG. TYPE	UNITS	REG. STAT.	VALUES		
					40 × 25 TEXT	80 × 25 TEXT	GRAPHICS MODE
0	R0	Horiz. Total	Char.	Write	38	71	38
1	R1	Horiz. Dispd.	Char.	Write	28	50	28
2	R2	Horiz. Sync. Position	Char.	Write	2D	5A	2D
3	R3	Horiz. Sync.	Char.	Write	0A	0A	0A
4	R4	Vert. Total	Row	Write	1F	1F	7F
5	R5	Vert. Total Adjust	Scan Line	Write	06	06	06
6	R6	Vert. Dispd.	Row	Write	19	19	64
7	R7	Vert. Sync. Position	Row	Write	1C	1C	70
8	R8	Interface Mode	—	Write	02	02	02
9	R9	Max. Scan Line Addr.	Scan Line	Write	07	07	01
A	R10	Cursor Start	Scan Line	Write	06	06	06
B	R11	Cursor End	Scan Line	Write	07	07	07
C	R12	Start Addr.	High	Write	00	00	00
D	R13	Start Addr.	Low	Write	00	00	00
E	R14	Cursor Addr.	High	Read/Write	XX	XX	XX
F	R15	Cursor Addr.	Low	Read/Write	XX	XX	XX
10	R16	Light Pen	High	Read	XX	XX	XX
11	R17	Light Pen	Low	Read	XX	XX	XX

XX is a hexadecimal number from 00 to FF.

## Circuit Description

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The first group of registers, R0 through R3, establishes the horizontal format and timing parameters. Registers R4 through R9 determine vertical format and timing parameters. The remaining registers, R10 through R17, deal with cursor characteristics, screen memory addressing, and the light pen interface. Typically, registers R0 through R11 are loaded when the system is turned on and should not need to be accessed thereafter. The other six registers, R12 through R17, need to be accessed on an ongoing basis during display operations. R12 and R13 establish the 14-bit starting (top-of-page) address of screen memory. The contents of these registers may be manipulated to perform scrolling of the screen contents. R14 and R15 establish the 14-bit cursor address which establishes the cursor symbol position on the screen. R16 and R17 are used only if a light pen is interfaced.

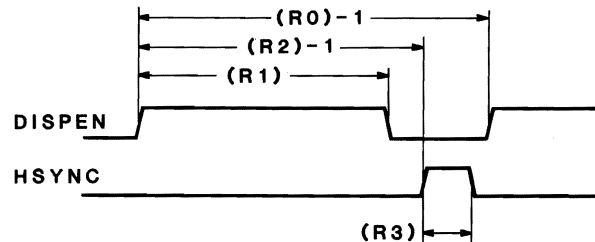
- Horizontal Timing and Format Registers — The contents of register R0 determines the total time allotted for one scan line in terms of character clock (CLK) cycles (total of displayed and undisplayed characters minus 1) per horizontal line, thus determining the horizontal sync (HSYNC) frequency.

R1 is the character row register. It is loaded with the total number of characters minus 1 in character clock (CLK) units.

The horizontal sync register, R2, establishes the point at which the HSYNC signal makes its negative-to-positive transition, specified in terms of CLKs. The reference point for the beginning of the HSYNC pulse is the left-most character position displayed on the scan line.

R3, the HSYNC width register, uses only the four least-significant bits of data to establish the duration of the HSYNC pulse in the range of 1 to 16 character clocks. This allows the HSYNC pulse duration to be adjusted to the requirements of the CRT monitor in use.

Figure 3.3 shows the interrelationship between the four horizontal timing and format registers (R0 through R3) in terms of CLK.



**Figure 3.3. Horizontal Timing and Format**

- **Vertical Timing and Format Registers** — Registers R4 through R9 are normally loaded at system startup and normally are not changed thereafter. The point of reference for these registers is the top-most character position displayed on the monitor screen.

The vertical total register, R4, and the vertical sync adjust register determine the total number of scan line times in a frame, including vertical retrace, establishing the overall frame rate or VSYNC frequency.

R4 is a 7-bit register loaded with the total number of character rows. Since a character row can consist of up to 32 scan lines, it may be difficult to establish a refresh frequency close to the line frequency. Register R5, a 5-bit VSYNC adjust register, then may be used to fine-tune the VSYNC frequency. R5 is loaded with a value representing scan line times.

The character-rows-displayed register, R6, is a 7-bit register which allows the selection of the number of rows of characters to be displayed, up to 128. What is specified for this register does not determine the positions of the VSYNC pulse, but the point at which display enable (DISPEN) will be reset for vertical retrace.

R7, the vertical sync (VSYNC) position register, determines the point at which the VSYNC signal makes its negative-to-positive transition to initiate vertical retrace. VSYNC position is determined by the character row time, measured from the first character row on the monitor



## Circuit Description

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screen. The VSYNC pulse always has a duration of 16 scan lines. Since the scan line frequency will vary from one application to another, and since the VSYNC pulse duration cannot be changed, external circuitry may be needed to achieve a pulse that is compatible with the CRT monitor being used.

The interlace mode register, R8, determines whether interlaced or non-interlaced scan is used.

The value in register R9 determines the number of scan lines per character row. This 5-bit register may be programmed for a character row of up to 32 scan lines. The value used will dictate the maximum count output by the raster address signals (RA0 through RA4) to the character generator logic. Load R9 with the desired scan line count minus 1.

The cursor formatting registers are comprised of the cursor start and cursor stop registers, R10 and R11, respectively. The five least-significant bits of each register determine the scan lines within a character row where the cursor symbol is to be activated. The scan line specified in R10 is the first scan in which the CURSOR signal is to be set and it will remain set until the scan line specified in R11 has been completed. Accordingly, if the cursor symbol is to occupy a single scan line, the same value must be loaded into both registers. If different values are loaded, a block-type cursor will be formed. In interlaced sync and video mode, both registers must be loaded with either odd or even values. Bits 5 and 6 determine whether or not the cursor is to blink, and if so, at either  $\frac{1}{16}$ <sup>th</sup> or  $\frac{1}{32}$ <sup>th</sup> of the field rate.

- **Primary Operating Registers** — The remaining six registers, R12 through R17, are considered the primary operating registers since, in the course of display programming, the contents will be changed on an ongoing basis rather than being loaded one-shot at system start-up. The six registers are arranged as three 14-bit register pairs (bits 6 and 7 of the most-significant byte are not used).

R12 and R13 comprise the top-of-page register which specifies the screen memory address containing the first character from the top-left corner to be displayed. At the end of each vertical retrace, the first

screen memory address generated will be the one contained in these registers. Since the 6845 addresses memory linearly, rather than on a row/column basis, scrolling can be performed on either a character-by-character or row-by-row basis.

The cursor position registers, R14 and R15, generate a cursor signal when the 6845 generates a screen memory address on MA0 through MA13 that matches the contents of this register pair, and when the scan line counter (RA0 through RA4) outputs fall within the limits established by registers R10 and R11. It may be necessary to delay the cursor signal with external logic circuitry to achieve display at the desired position. Cursor movement on the screen is accomplished by loading new values into R14 and R15. These registers are the 6845s only read/write registers so they also can be used to keep track of the cursor position, rather than copying this information from another memory location.

R16 and R17 are the light pen register pair, which will be loaded with the screen memory address corresponding to the screen position at which the LPEN signal was detected. Since there are several critical timing parameters involved with this signal, be sure to carefully study the documentation supplied with this option.

## **Raster Scan Signals**

The raster scan outputs, RA0 through RA4, provide the interface between the 6845 and the character generator logic. These outputs may represent scan line counts of from 0 to 31, or up to 32 scan lines per character row. Register R9, the scan lines/row register, determines the maximum count from the scan output registers before reset occurs. Scan line counts are incremented at the HSYNC rate, but also are dependent on the interlace format selected.

## Circuit Description

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### Video I/O Devices

Table 3.3 defines the I/O devices contained on the video interface.

**Table 3.3. Video I/O Port Assignments**

PORT ADDRESS	REGISTER
3D0	6845
3D1	6845
3D8	Mode Control
3D9	Color Select
3DA	Status/Mode I/O
3DB	Light Pen Latch CLEAR
3DC	Light Pen Latch PRESET

To address a given port, the address lines are programmed as defined in Table 3.4.

**Table 3.4. Video I/O Port Selection**

PORT ADDRESS	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
3D0	1	1	1	1	0	1	0	X	X	0
3D1	1	1	1	1	0	1	0	X	X	1
3D8	1	1	1	1	0	1	1	0	0	0
3D9	1	1	1	1	0	1	1	0	0	1
3DA	1	1	1	1	0	1	1	0	1	0
3DB	1	1	1	1	0	1	1	0	1	1
3DC	1	1	1	1	0	1	1	1	0	0

X = Don't care

The 6845 CRT controller occupies two I/O port addresses. The RS (register select) line is connected to the least-significant bit, A0. When A0 is reset, the address register is accessed to load it with the register address of the desired parameter, which would then be accessed by setting A0 (RS). A typical register access operation then would consist of two consecutive device write cycles, or a write cycle followed by a read cycle, and these cycles would be directed to consecutive memory or I/O locations.

- **Color Select Register** — The color select register, located at address 3D9, is a 6-bit output-only device (it cannot be read) which can be written to using the I/O OUT command. Only the six least-significant bits of the instruction are used, as shown in Table 3.5.

**Table 3.5. Color Select Register Logic**

Bit 0	B (blue) border color select (text mode) or 640 × 200 graphics dot color
Bit 1	G (green) border color select (text mode) or 640 × 200 graphics dot color
Bit 2	R (red) border color select (text mode) or 640 × 200 graphics dot color
Bit 3	I (intensity) intensifies border color (text mode) or 640 × 200 graphics dot color
Bit 4	Selects alternate background color palette for medium resolution graphics mode color
Bit 5	320 × 200, graphics color palette selection

Bits 6 and 7 are not used.

In text mode and 320 × 200 graphics mode, bits 0, 1, 2, and 3 determine the screen border color. In 640 × 200 graphics submode, these bits select the screen foreground color.

Bit 4, when set, selects an alternate, intensified palette of background colors in 320 × 200 graphics mode.

## Circuit Description

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Bit 5 is only used in the  $320 \times 200$  graphics submode to select the active palette of screen display colors. If bit 5 is a logical 1, color is determined by the logic of Table 3.6.

**Table 3.6. Color Palette Number 1 Selection**

C1	C0	COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Cyan
1	0	Magenta
1	1	White

If bit 5 is a logical 0, color is determined by the logic of Table 3.7.

**Table 3.7. Color Palette Number 2 Selection**

C1	C0	COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Green
1	0	Red
1	1	Brown

## Circuit Description

- **Mode Select Registers** — The mode select registers are also write-only registers. One is a 6-bit register at port address 3D8; the other is an 8-bit register at 3DA. Both can be written to using I/O OUT commands. The output register at 3D8 functions according to the logic of Table 3.8.

**Table 3.8. Mode Select Port 3D8 Logic**

MODE	BITS					
	0	1	2	3	4	5
40 × 25 ALPHA B & W	0	0	1	1	0	1
40 × 25 ALPHA COLOR	0	0	0	1	0	1
80 × 25 ALPHA B & W	1	0	1	1	0	1
80 × 25 ALPHA COLOR	1	0	0	1	0	1
320 × 200 B & W GRAPHICS	0	1	1	1	0	X
320 × 200 COLOR GRAPHICS	0	1	0	1	0	X
640 × 200 B & W GRAPHICS	0	1	1	1	1	X

**Bits**

- 0 — 80 × 25 ALPHA SELECT
- 1 — SELECT 320 × 200 GRAPHICS
- 2 — SELECT B & W MODE
- 3 — ENABLE VIDEO
- 4 — 640 × 200 B & W
- 5 — ENABLE BLINK ATTRIBUTE

X — Does Not Care

## Circuit Description

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The register at 3DA functions according to the logic of Table 3.9.

**Table 3.9. Mode Select Port 3DA Logic**

Bit 0	A logical 1 overrides the VIDEO ENABLE signal from 3D8; will eliminate monitor display flicker when in text mode.
Bit 1	Character font selection. Least-significant bit (LSB).
Bit 2	A logical 1 enables underline in text mode when Attribute bit 6 is a logical 1.
Bit 3	Not defined.
Bit 4	A logical 1 selects Z-319 video.
Bit 5	A logical 1 enables fast hardware scrolling in the 80 × 25 submode only.
Bits 6 and 7	Used to select one of four pages of display text from the 16K video RAM in text mode, according to the following logic:

<u>BIT 7</u>	<u>BIT 6</u>	<u>SCREEN PAGE SELECT</u>
0	0	First page
0	1	Second page
1	0	Third page
1	1	Fourth page

- **Status Register** — The status register, an 8-bit read-only buffer, resides at input port address 3DA. Table 3.10 summarizes the logical operation of this register.

**Table 3.10. Status Select Logic**

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Bit 0	A logical 1 indicates that a horizontal or vertical retrace is in progress. This bit can be used to update the video memory during screen refresh intervals.
Bit 1	A logical 1 in this bit position indicates that a positive-going light pen signal has set the light pen trigger. This trigger is reset at powerup and also may be cleared by issuing an I/O OUT command to port address 3DB. The reset is address-activated; no specific data need be output.
Bit 2	A logical 0 indicates that the light pen switch is on. The switch signal is not latched or debounced.
Bit 3	A logical 1 indicates that a vertical retrace is in progress.
Bit 4	LSB of the character font number.
Bit 5	MSB of the character font number.
Bits 6 and 7 are not used.	

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## Programming Sequence

In general, observe the following sequence when selecting operating parameters for the video interface:

1. Determine desired mode of operation, text mode, or all-points-addressable graphics.
2. Reset video enable bit. Also reset video override bit 0 in port address 3DA if not already reset.
3. Program the CRT controller to desired mode.
4. Determine desired submode(s), then program mode and color select registers.
5. Set video enable bit. Also set the video override bit, if desired.



## Circuit Description

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### Detailed Circuit Description

- **Data Bus Interface** — CPU data is interfaced to the video controller circuitry through data transceiver U348. The decoded data direction (XCVRD) signal from pin 15 of PAL address decoder U338 determines the direction of data transfer between the CPU D0 through D7 data bus and the onboard DB0 through DB7 data bus. When the XCVRD signal is low, data is transferred from the onboard DB0 through DB7 data bus to the CPU D0 through D7 data bus. When the signal is high, data is transferred from the CPU D0 through D7 data bus to the onboard DB0 through DB7 data bus.
- **Chip Selection** — PAL address decoder U338 provides the active-low chip select signal to pin 25 of the CRT controller (U325). Line A0 of the main address bus is used to provide the Register Select (RS) signal to pin 24 of U325. When RS is low, the address register is selected, and when RS is high, the data register is selected.
- **I/O Signals** — The CRT controller (U325) provides video memory addressing, timing, vertical sync (VS), horizontal sync (HS), cursor (CRSR), and display enable (DISPEN) status signals to the gate array (U324). The BCLK output from pin 30 of the gate array provides the CRT controller with synchronization clock signals that control the internal functions of the CRT controller.

Data on the MA1 through MA10 address lines of the CRT controller, and the T0, T1, VA11, and VA12 signals from the gate array are multiplexed with data on the A0 through A13 bits of the main address bus to derive video RAM address bytes.

Data on row address bits RA0, RA1, and RA2, address the character generator ROM and provide input signals to the gate array. The RA1 and RA2 signals are NANDed by pin 8 of U318 providing the negated (RA1 "AND" RA2) signal to the gate array.

- Timing — The ECLK output from pin 32 of the gate array provides the enable (E) input of the CRT controller with signals that enable the I/O buffer/drivers. The ECLK signals are used to clock data to and from the CRT controller. The status of the R/W\* signal provided by pin 31 of the gate array determines which operation will be performed.

## Video RAM Address Multiplexers

The signals on the MA1 through MA10 control lines of the CRT controller (U325), and the T0, T1, VA11, and VA12 signals from the gate array are multiplexed with the signals present on the A0 through A13 bits of the main address bus, to derive video RAM address bytes.

### Detailed Circuit Description

Each multiplexed output of U326, U327, U333, and U334 supply two bits of data to the VMA0 through VMA7 address bus when the refresh (NRFSH) signal at pin 18 of U335 is low. Each resulting address byte is used for row and column memory location definition within each RAM, U331 and U332.

## Video RAM

U331 and U332 form 16K attribute and character code storage banks. In the alphanumeric mode of operation, there is 8K of RAM available for attribute code storage and 8K of RAM available for character code storage. In the graphics mode of operation, there is 16K of pure data available within the video RAMs. The buffer address starts at B8000.

## Circuit Description

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In the alphanumeric mode, the video RAMs alternately output two bytes of data. One byte is used to address the character generator ROM, which supplies the character data byte to the gate array. The second byte is used as the attribute data byte and is read by the gate array directly.

In the graphics mode, each data byte output from video RAM is read directly by the gate array. Video RAM can be read from or written to depending on the status of the Memory Read (MRD) and Memory Write (MWR) signals from the CPU.

### Detailed Circuit Description

- **Memory Addressing** — Address bytes derived from the video RAM address multiplexers are applied to the VMA0 through VMA7 address bus. The address bytes are latched internally by the RAMs when the Row Address Select (RAS\*) signal from pin 20 of the gate array becomes active-low. The byte of data is retained by the RAM as the row address byte.

A few nanoseconds later, a second six-bit multiplexed address byte (VMA1 through VMA6) is latched by the RAMs when the Column Address Select (CAS\*) signal from pin 3 of U353 becomes active. Fourteen bits of data are required to complete the cycle of addressing one memory location within the RAM banks. The addressed memory location contains the data byte required to produce either the character or attribute data byte.

- **Read Cycle: Attribute/Character Bytes** — In the alphanumeric mode, the video RAMs output data bytes during each read cycle. One byte is used to address the character generator ROM when the ROMG\* signal is active. The second byte is used as the attribute data byte which is read by the gate array when the Write Enable signal at pin 11 of U318 is high, and the RAMG\* signal from pin 5 of the gate array becomes active-low. The RAMG\* signal enables three-state buffer U330 to transfer data from the VRAM0 through VRAM7 bus to the GA0 through GA7 bus during the read cycle.

## Circuit Description

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In the graphics mode, both bytes provided by the RAMs are read directly by the gate array as pure data required to define whether a pixel is on or off.

- **Write Cycle** — Data is written into the RAMs when the active memory write (MWR) signal from pin 2 of U340 drives pin 11 of U318 low, providing the Write Enable (WE\*) signal to the RAMs. Pin 11 of U318 also enables three-state buffer U329 so that data on the GA0 through GA7 bus can be transferred to the VRAM0 through VRAM7 bus during the write cycle.
- **Refresh** — Data contained within the memory locations of the RAMs (U331 and U332), must periodically be refreshed so that data is not lost.

During the refresh cycle, pin 16 of the gate array provides refresh (NRFSH) pulses to pin 4 of U318, and to the video RAM address multiplexers. When the NRFSH signal is low, pin 6 of NAND gate U318 is driven high allowing U336, a binary counter to supply three-state buffer U337 with a byte of data.

When a valid memory location is addressed, one of 256 possible rows within the video RAM is enabled to be refreshed. The Row Address Strobe (RAS\*) signal from pin 20 of the gate array is driven active-low to refresh the row of data determined by the addressed memory location.

## Circuit Description

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### Character ROM

Data output of the RAMs is used to provide the character generator ROM with a valid 8-bit address. The address selects a particular memory location in ROM that contains data required to generate a character on the display.

### Detailed Circuit Description

- **Character Addressing** — Data placed on the VRAM0 through VRAM7 bus by the video RAMs is latched by octal buffer U319 when the ROMG\* signal from pin 6 of the gate array is active-low. The latched data byte provides the character generator ROM with a valid 8-bit address value.
- **Read Cycle** — When the ROM receives a valid address from video RAM, the value represented is used to select a desired character from the font. The data byte output from the ROM is latched onto the GA0 through GA7 data bus by flip-flop U328 during the time when the ROMG\* signal from pin 6 of the gate array goes high. The gate array reads the data on the GA0 through GA7 bus and then processes the data internally.

### Gate Array Functional Description

The video controller gate array is an active device responsible for manipulating and processing data to derive desired output signals. Gate array technology provides an extremely flexible basis for many different internal circuit configurations. Video synchronization and control, as well as multiplexing, decoding, and timing are all functions accomplished by the gate array. Refer to Table 3.11 for gate array pinout and signal names. Refer to Figure 3.4 for Gate Array Block Diagram.

Circuit Description

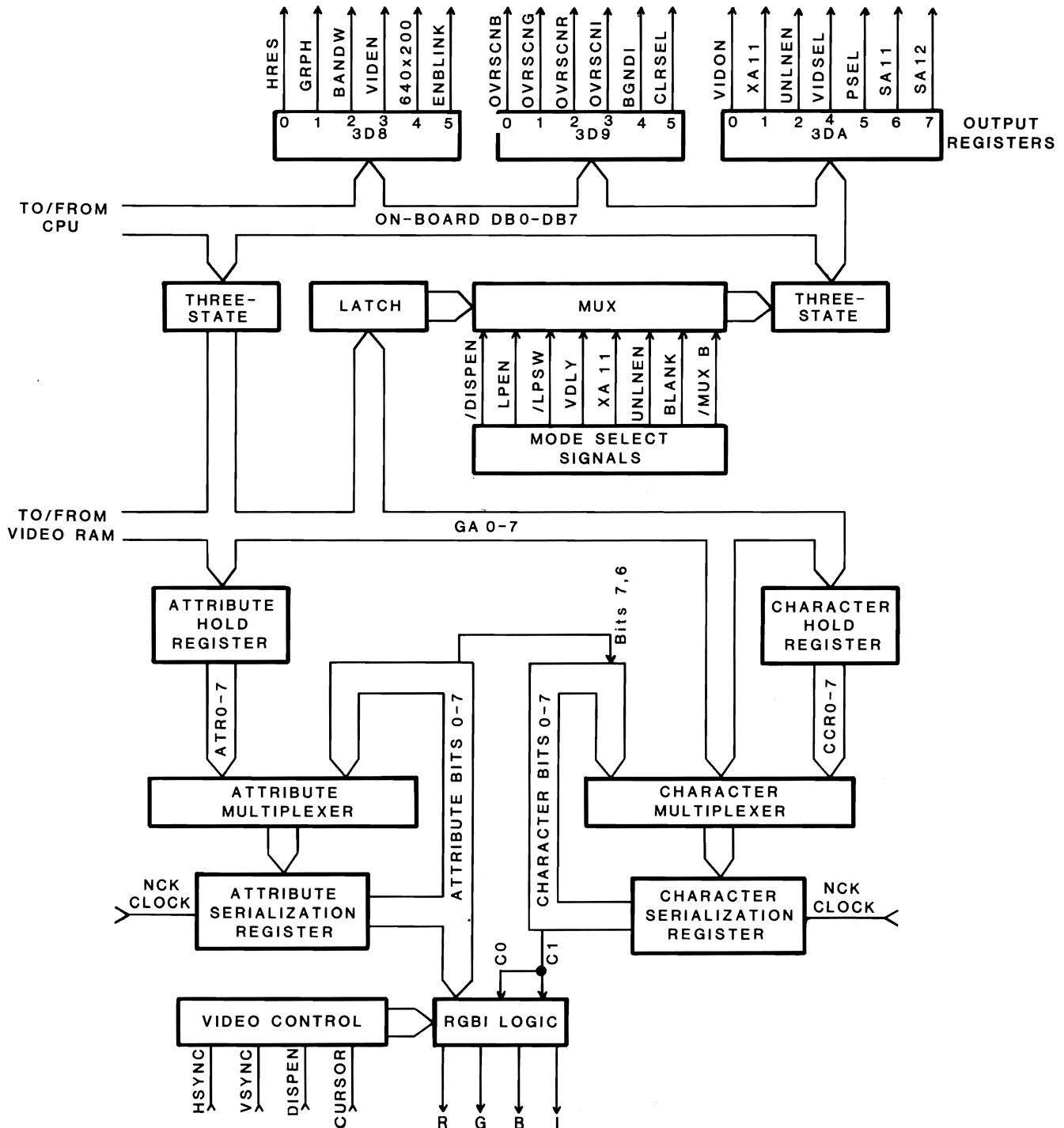


Figure 3.4. Gate Array Block Diagram

## Circuit Description

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**Table 3.11. Gate Array I/O Signal Description and Pinouts**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1, 18, 35, 52	GND	Ground.
2	LPIN	Light Pen input.
3	VRAM*	Video RAM decode.
4	LPSW	Light Pen Switch.
5	RAMG*	Enables U330 on RAM read cycle.
6	ROMG*	Enables U328 on ROM read cycle.
7 – 14	GA0 – GA7	8-bit onboard data bus.
15	CSGA*	Chip Select for gate array.
16	NRF5H	Enables RAM refresh cycle.
17, 34, 51, 68	+ 5 VDC	Gate array power source.
19	CAS*	Column Address Strobe, high during refresh cycle.
20	RAS*	Row Address Strobe, active signal that refreshes RAM.
21	RA1,2*	NANDed Row Address bits 1 and 2 from CRTC.
22	LPEN	Strobe input to CRTC.
23	MA11	Memory Address bit 11 from CRTC.
24	MA12	Memory Address bit 12 from CRTC.
25	RA0	Row Address bit 0 from CRTC.
26	VA11	Video RAM address multiplexer input.
27	VA12	Video RAM address multiplexer input.
28	VSYNC	Vertical sync input from CRTC.
29	HSYNC	Horizontal sync input from CRTC.

**Table 3.11. Gate Array I/O Signal Description and Pinouts**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
30	BCLK	Control/timing signals to CRTC.
31	RDNW	Enables READ when high, WRITE when low.
32	ECLK	Enables CRTC I/O drivers, and used to clock data in and out of CRTC.
33	NRDY	Activates "I/O CHIP READY" signal.
36	RASD*	Select 0 (S0) input to video RAM address multiplexers.
37	CPU	Select 0 (S0) input to video RAM address multiplexers, enables memory WRITE operation.
38	T0	Video RAM address multiplexer input.
39	T1	Video RAM address multiplexer input.
40, 41, 42	R1, G1, B1	RGB serial data.
43	I1	"INTENSITY" bit.
44	V1	Vertical sync output from gate array.
45	H1	Horizontal sync from gate array.
46	NIOW	I/O WRITE enable.
47	MRD*	Memory READ enable.
48	NIOR	I/O READ enable.
49	RESET*	Resets CRTC and U336.
50	OSC	Clock input to gate array.
53	VSEL	Video select output.



## Circuit Description

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**Table 3.11 (continued). Gate Array I/O Signal Description and Pinouts**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
54	XA11	Addresses bit A11 of the character ROM.
55	DISPEN	Display enable input from CRTC.
56	PCRSR	Cursor position input from CRTC.
57, 58, 59	A0, A1, A2	Bits A0, A1, and A2 of the main address bus.
60–67	DB0-DB7	8-bit onboard data bus.

## Video Port Configuration

Data on the CPU D0 through D7 bus is used in conjunction with data on the GA0 through GA7 bus to configure the video I/O ports 3D8, 3D9, and 3DA to establish mode selection and status transfer between the Color Video/Floppy Controller Card and the existing system. Bus selection is determined by an internal three-state device.

The video I/O ports act as mode select registers to configure the video interface for the desired operation. They determine medium or high resolution mode, monochrome or color operation, and enable or disable the video interface and character blink. Port 3D9 determines color palette in use, and screen border color. It also selects intensified background colors.

## Character and Attribute Data Byte Format

A two byte character/attribute format is used in text mode to define a display character position. This alphanumeric display architecture is utilized with both monochrome and color display operation. The character data byte defines the actual character to be displayed. The attribute data byte is then utilized to describe the appearance of the displayed character.

In the monochrome mode of operation, the attribute data byte can produce reverse video, blinking, and highlighting enhancement of the defined character. In the color mode of operation, sixteen foreground and eight background colors are available to enhance the displayed character. One of sixteen border colors may also be selected for screen border definition.

## Character and Attribute Data Registers

Character and attribute data bytes are read by the gate array over the GAO through GA7 data bus. The character data byte is internally latched, and then multiplexed with internal control signals. The byte output of the multiplexer is loaded into the character serialization register.

The attribute data byte is internally latched, and multiplexed with internal control signals. The byte output of the attribute multiplexer is loaded into the attribute serialization register.

## Data Serialization

- **Alphanumeric (40 × 25) Mode** — In the alphanumeric 40 × 25 mode, the multiplexed data contained within the character serialization register is serially shifted as single bits (C0) to the RGBI logic circuits. Each bit is used to define two adjacent pixels of the screen. The attribute data byte is used to describe the appearance of the displayed character.
- **Alphanumeric (80 × 25) Mode** — In the alphanumeric 80 × 25 mode, the multiplexed data contained within the character serialization register is serially shifted as single bits (C0) to the RGBI logic circuits. Each bit is used to define one pixel of the screen. The attribute data byte is used to describe the appearance of the displayed character.

## Circuit Description

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- **Color/Graphics Medium Resolution Mode** — In the medium resolution graphics mode of operation, up to 200 rows of 320 pixels each may be defined. The character and attribute data registers are linked together into one long shift register. The NCK signals shift the data bits as 2-bit (C0 and C1) pairs to the internal RGBI circuits. The C0 and C1 bit pairs are used to select 4 of 16 predetermined colors from either of two software selected color palettes. Refer to Table 3.12.

**Table 3.12. Software Selectable Color Palettes**

		<u>PALETTE 1</u>	<u>PALETTE 2</u>
		Cyan	Green
		Magenta	Red
		Light Gray	Brown
<u>C1</u>	<u>C0</u>	<u>CODE SELECT FOR DISPLAY POSITION</u>	
0	0	Dot takes on color of 1 of 16 preselected background colors.	
0	1	Select 1st color of preselected color palette 1 or 2 (see above).	
1	0	Select 2nd color of preselected color palette 1 or 2 (see above).	
1	1	Select 3rd color of preselected color palette 1 or 2 (see above).	

- **Color/Graphics High Resolution Mode** — In the high resolution mode, 200 rows of 640 pixels each may be defined. Due to memory limitations however, only a monochrome display may be generated in the high resolution mode. The character and attribute data registers are linked together into one long shift register. The NCK signals shift each bit (C0) of data from the character serialization register to the RGBI logic circuits. A logic 1 gives you a pixel of foreground color determined by the color select register 3D9; bits 0, 1, 2, and 3. A logic 0 blanks the pixel.
- **RGBI Logic Circuits** — In the alphanumeric mode of operation, the entire attribute data byte is used to describe the displayed character.

## Circuit Description

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The serial data stream from the character serialization register, as well as the video synchronization and control signals derived from the CRT controller determine the RGBI logic levels.

In the graphics modes of operation, all data is sent to the RGBI logic as a serial stream. In the medium resolution mode, bits C0 and C1 are used to define one pixel and in the high resolution mode only bit C0 is used to define whether a pixel is on or off.

Horizontal and vertical sync, display enable (DISPEN), and cursor (CURSOR) signals are derived from the CRT controller (U325). The signals are applied to internal synchronization and video control logic circuits of the gate array. The output of the logic circuits provide horizontal and vertical sync, display delay (DSPDLY), cursor delay (CRSDLY), cursor blink (CRSBLNK), and character blink (CHARBLNK) signals to the internal RGBI logic of the gate array.

## Video Output

The RGBI data from the gate array is multiplexed with optional external RGBI input signals. The output signals are buffered and driven to the internal and external monitor connectors, and to the video driver transistors.

Horizontal and vertical synchronization signals from the gate array are multiplexed with optional external horizontal and vertical signals, and are driven to the internal and external monitor connectors and driver transistors. The output of the driver transistors provide composite video signals.

Jumpers J302 through J306 are used to determine polarity of horizontal (H) and vertical (V) signals applied to both the internal and external monitor connectors. The jumpers also allow for selection of a composite signal at pins 2 and 3 of J302.

## Circuit Description

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### Detailed Circuit Description

- **RGBI Signals** — Pins 40, 41, 42, and 43 of the gate array provide RGBI data to multiplexer U342. Optional RGBI input is interfaced to multiplexer U342 through connector P302. Multiplexer U342 outputs the RDOT, GDOT, BDOT, and IDOT signals when the Video Select (VSEL) signal from pin 53 of the gate array becomes active-high.

The R, G, B, and I DOT signals are buffered and driven by U345 to the internal monitor connector P303, and through RFI filters to the external monitor connector P306. Resistor Pack RP306 converts the DOT signals to an analog level which biases driver transistor Q301. Different combinations of active DOT signals provide different intensities of bias voltage at the base of Q301, thereby producing video stepping voltages at the emitter of Q301.

If there are no active DOT signal outputs from multiplexer U342, the output at pin 8 of OR gate U346 goes low, effectively cutting off transistor Q301 so that the video signal is blanked.

- **Horizontal and Vertical Sync** — Pins 45 and 44 of the gate array provide the horizontal sync (H1) and vertical sync (V1) signals, respectively, to multiplexer U341. Optional external horizontal sync (H2) and vertical sync (V2) signals are interfaced to multiplexer U341 through connector P302. The horizontal (H) and vertical (V) signals are output from multiplexer U341 when the Video Select (VSEL) signal from pin 53 of the gate array is active-high.
- **Composite Sync** — The horizontal (H) and vertical (V) signals are ORed by pin 11 of U346 and inverted by pin 12 of U349 to produce the composite horizontal/vertical signal. The composite signal is used for synchronization between horizontal and vertical retrace and video output signals. When either horizontal or vertical retrace occurs, the composite sync signal is added to the composite video signal.

## Circuit Description

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When horizontal and vertical retrace are inactive, the composite RGBI video signal from the emitter of Q301, is applied to the base of Q302 and to the base of Q303. The output at the emitter of Q302 provides the composite video signal to internal monitor connector P303, and the output at the emitter of Q303 provides the composite video signal to external monitor connector P305.

The RFI filters are configured as pi-type capacitive input filters. The value of the inductor is 2.2 microhenries, and the value of each capacitor is 56 picofarads.

Capacitors C362, C363, and C364, in conjunction with inductor L301, provide filtering and decoupling of the 5 VDC supply before use by the video output transistors.

The light pen input signal is interfaced to the gate array through connector P304. Jumper J301 is used to establish light pen polarity and pin 10 of U344 provides pin 4 of the gate array with the light pen switch (LPSW) signal.

- **Contrast and Black Level Adjustments** — Potentiometer R319 allows for adjustment of the dark-to-light screen area ratio (contrast) and R320 allows for adjustment of the black level for different monitors. R320 should be adjusted to obtain a reading of 1 volt peak-to-peak at the base of Q301 (TP301).

## Circuit Description

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# PAL Equations

Refer to Table 3.13 for U338 Programmable Array Logic (PAL) equations.

**Table 3.13. PAL Logic Equations**

SIGNAL NAME	LOGIC EQUATION
CS765	$A9764 * A8 * A5 * /A3 * /AEN$
CSFDOR	$A9764 * A8 * A5 * /A3 * /AEN * IOW$
CS8250	$A9764 * A8 * A5 * A3 * COMEN * COM1 * /AEN$ $+ A9764 * /A8 * A5 * A3 * COMEN * /COM1 * /AEN$
CSGA	$A9764 * A8 * /A5 * A3 * VIDEN * /AEN$
CS6845	$A9764 * A8 * /A5 * /A3 * VIDEN * /AEN$
SELOUT	$(A9764 * A8 * A5 * /A3) + (A9764 * A8 * A5 * A3$ $* COMEN * COM1 + A9764 * /A8 * A5 * A3 *$ $COMEN * /COM1) + (A9764 * A8 * /A5 * VIDEN)$
XCVRD	$(SELIN * /AEN * IOR) + (VRAM * MRD) + (DACK * IOR)$

Refer to Table 3.14 for explanation of the logic designators used in the PAL language structure.

**Table 3.14. Logic Designators**

LOGIC FUNCTION	SYMBOL	EXAMPLE
AND	*	$A8 * A5$ (A8 "AND" A5)
	A9764	$A9 * A7 * A6 * A4$
OR	+	$A8 + A5$ (A8 "OR" A5)
NEGATED	/	$/A8$ ("NOT" A8)

Refer to Table 3.15 for description and pinout of PAL I/O signals.

**Table 3.15. PAL I/O Signal Description and Pinout**

<u>INPUT SIGNALS</u>		
PIN #	SIGNAL NAME	DEFINITION
1	/IOR	Bus I/O Read.
2	/MRD	Bus Memory Read.
3	/VRAM	Video RAM address decode.
4	/SELIN	SELOUT feedback.
5	/IOW	Bus I/O Write.
6	/A9764	Bus address /(A9 & A7 & A6 & A4).
7	A8	Bus address bit A8.
8	A5	Bus address bit A5.
9	A3	Bus address bit A3.
10	AEN	Bus DMA Address Enable.
11	/VIDEN	Enable Video (switch 4).
12	/COMEN	Enable COM port (switch 3).
13	/COM1	Enable COM port 1 (switch 2).
14	/DACK	Enable DACK2.
<u>OUTPUT SIGNALS</u>		
15	/XCVRD	Transceiver Direction control.
16	/CSFDOR	Chip Select, Floppy Output Register.
17	/CS765	Chip Select, $\mu$ PD765.
18	/CS8250	Chip Select, 8250 ACE.
19	/CSGA	Chip Select, Gate Array.
20	/CS6845	Chip Select, 6845 CRTC.
22	/SELOUT	Partial "OR" of selects.

## Backplane Signal Names

Refer to Table 3.16 for definition of the I/O bus signal names and edge connector pinout for the Color Video/Floppy Controller Card.



## Circuit Description

---

**Table 3.16. Backplane I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
A2–A9	D7–D0	Data bit 7 through Data bit 0.
A10	I/O CHRDY	I/O Channel Ready. Used by slower I/O devices to ensure data is not lost during read and write operations. May be held low (not ready) up to 10 clock cycles (210 ns).
A11	AEN	Address Enable. Assigns control of read and write operations to DMA controller.
A12–A31	A19–A0	Address bit 19 through address bit 0.
B1	GND	Ground.
B2	RESET	When high, resets, or initializes system logic devices.
B3	+ 5 VDC	+ 5 VDC bus.
B4	IRQ2	Interrupt Request 2. Not used but available for assignment to a user- selected device.
B6	DRQ2	DMA Request 2. Assigned to floppy disk controller.
B7	– 12 VDC	– 12 VDC bus.
B9	+ 12 VDC	+ 12 VDC bus.
B10	GND	Ground.
B11	MEMW*	Memory Write. When low, causes data on data bus to be stored in memory.
B12	MEMR*	Memory Read. When low, causes memory to drive data onto the data bus.
B13	IOW*	I/O Write. When low, instructs an I/O device to read data on the data bus.

## Circuit Description

**Table 3.16 (continued). Backplane I/O Bus Signal Names**

PIN	SIGNAL	DEFINITION
B14	IOR*	I/O Read. When low, instructs an I/O device to drive its data onto the data bus.
B19	DACK0*	DMA Acknowledge 0. Assigned for timer number 1. Initiates memory refresh cycle.
B20	CLK	4.77 MHz system clock.
B21	IRQ7*	Interrupt Request 7. Assigned to parallel interface.
B22	IRQ6*	Interrupt Request 6. Assigned to floppy disk controller.
B23	IRQ5*	Interrupt Request 5. Assigned to Winchester drive controller.
B24	IRQ4*	Interrupt Request 4. Assigned to serial port #1 (fixed).
B25	IRQ3*	Interrupt Request 3. Assigned to serial port #2 (configurable).
B26	DACK2*	DMA Acknowledge 2. Assigned to floppy disk controller.
B27	T/C	Terminal Count. Goes high when terminal count for any DMA channel is reached.
B29	+5 VDC	+5 VDC bus.
B30	OSC	A 14.31818 MHz oscillator provides the basic timing for the system.
B31	GND	Ground.

## Chapter 4

# Troubleshooting

**CAUTION:** This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

## General

Use of the information in this chapter assumes that one or more malfunctions have been traced to the Color Video/Floppy Controller Card, and the power on, menu selected, or disk-based diagnostics, or LEDs **have not** isolated the problem. The information provided here will supplement the procedures provided by the built-in debugging routines of system ROM. Refer to the "ROM Diagnostics" chapter in the *Base Unit Service Module* for details on the use of these routines.

An abundance of useful information is included in this chapter which will aid the service technician in troubleshooting problems at nearly any level of difficulty. If problems are encountered that do not warrant the degree of detail presented here, proceed to the general troubleshooting guide at the end of this chapter.

Refer to Chapter 3 for Programmable Array Logic (PAL) equations and I/O bus signal identification.

**NOTE:** If replacement of the gate array IC is required, a special IC extractor must be used. The extractor part number is HE-490-230.

## Serial Input/Output

Power-up diagnostics do not check serial I/O signals. If trouble is experienced with the serial port, several things must be checked before assuming component or card failure. Most suspected problems with serial I/O signals are not hardware related, but originate from incorrect software or incorrect protocol for serial communications.

The I/O portion of the Disk-Based Diagnostics Program (a purchase option), may be used to locate a problem. Refer to Chapter 4, "I/O Port Diagnostics" of the Disk-Based Diagnostics manual for more information. If the diagnostic tests indicate no problem, proceed with the following 5 steps in the order indicated.

1. Check for the correct serial cable. The I/O port is a DTE output device and cannot accommodate the HCA-10, 11, or 12 cable as indicated in ZDS literature for this computer. A "null modem" cable must be used which is supplied under the HCA-50, 51, and 52 catalog numbers.
2. If the correct cable is being used, run the CONFIGUR utility (supplied with MS-DOS) and reconfigure the output port to accommodate the protocol required by the serial device.

**NOTE:** MS-DOS normally routes the printer through the parallel port. If a customer is attempting to use a serial printer, CONFIGUR **must** be run before the printer will operate correctly.

3. If you are still experiencing problems with a serial device, try using the device with another computer that is known to work. Try both the hardware and customer's software. This should establish whether or not the fault lies with the device, computer, or software.
4. If none of the preceding checks have resulted in positive identification of the problem, replace the Color Video/Floppy Controller Card and rerun the checks. This should isolate the problem to the card. If the card is at fault, use Table 4.1 for checking the individual components.

**Table 4.1. Serial I/O Component Failures**

SYMPTOM	SUSPECTED PARTS	THINGS TO CHECK
No Output	U338, pin 18 U309, pin 8 U351, pins 6, 8, 11 U322, L322, C322	Active-low ACE chip select. I/O write control signal. Output signals. Check for base frequency of 1.8432 MHz.
Data Bus Fault	U348 U338, pin 15	Check for proper signal gating. Pin 15 determines data direction transfer.
No Output COM1, COM2	U347, U350, U351  U316, pin 31  U339, pin 8 J307–J312	Check signal flow through drivers and receivers. Software controlled interrupt enable. COM 1 interrupt signal. Check for proper IRQ selection. COM 1 uses IRQ4 (J309), COM 2 uses IRQ3 (J308).
Wrong baud rate COM1, COM 2	U322, L322, C322  U316	Check for base frequency of 1.8432 MHz. Replace ACE

## Floppy Disk Controller

Floppy disk systems can exhibit a number of symptoms that can be traced to poor or bad disks, dirty or misaligned disk drive heads, or improper user operation. As a result of any of these problems, several different error messages can be generated by either the computer firmware (ROM) or operating system software. You should be familiar with normal disk operation in computers before attempting to service this section of the floppy disk controller card.

The following quick checks should isolate the problem to the card, disk drive, or other parts of the computer system.

1. On normal power up, check the CPU diagnostic lights (LEDs) for proper sequencing.
  - With autoboot switched off (see CPU card switch settings), the DSK light on the CPU card should be the last light to go out (except for the RDY light, which will remain lit until a disk has been successfully booted).
  - With autoboot switched on (floppy disk boot), the DSK light will remain on until a disk is inserted. Otherwise, an error message will be generated, which reads:

```
+++ DISK ERROR: DRIVE NOT READY! +++
```

This is a normal error message and indicates that a bootable disk has not been placed in the disk drive. Timing of the timeout is controlled by the ROMs on the CPU card. Therefore, if you get this error message immediately after resetting the computer by pressing the CTRL, ALT, and DEL keys at the same time, you should check the ROM on the CPU card.

Other conditions that can cause this error message include disk improperly placed in the drive and drive door (latch) not closed.

2. On normal powerup, the message:

```
+++ DISK ERROR: Seek failure! +++
```

can result from the disk drives not being plugged into the controller card or not receiving the correct power supply voltages. After having the computer off for at least five seconds, turn it back on and watch the drive access indicators. If they momentarily come on, then the drive is probably receiving the correct power supply voltages and signals from the floppy disk controller. Make the next check.

3. On normal power up, the messages:

```
+++ DISK ERROR: Invalid address mark detected! +++  
+++ DISK ERROR: Sector not found! +++  
+++ DISK ERROR: Seek failure! +++  
+++ DISK ERROR: CRC error! +++
```

or no error message at all (but the system is attempting to boot a disk) can indicate a bad or unformatted disk, wrong format (CP/M instead of MS-DOS), or wrong operating system (Z-DOS instead of MS-DOS). The "sector not found" error message also may indicate a data disk (non-bootable disk).

In any of these cases, reset the computer (you will probably have to turn it off, wait five seconds, and then turn it back on), and attempt to boot the system with a *known* good disk. Do not use distribution disks for this purpose; use a backup.

4. The message:

```
System disk
```

indicates that the disk has the correct format, but not an operating system.

5. If you are servicing the computer with the drives out, make sure that all parts are free to move normally. Do not lay the drive flat on top of the power supply. The magnetic flux fields can interfere with normal disk movement and cause the "seek failure" error message, even with a good disk. Also, the magnetic flux fields can erase enough information to cause intermittent conditions with a good disk.

## Troubleshooting

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6. If the DSK LED on the CPU card does not go out and the disk access LED(s) on the front of the drive(s) glow, check to make sure that the drive cable is plugged in properly. If it is reversed, the LED(s) on the front of the drive(s) will glow and the CPU DSK LED will not go out. Hardware unit numbers 0 and 1 should be plugged into P301.
7. Running the Disk READ tests from the Monitor ROM should give the same results for each drive plugged into P301. If data cannot be read from a known good disk, it is probable that the Read Window timing is incorrect. The read data is processed by a data separation chip which may malfunction internally. Note that the separated data output of the data separator is buffered by an active inverter which may also fail.
8. If the read operation is found to function properly when using a known good disk, but is reading erroneous data after a write operation, it is possible that the Write Precompensation circuitry is malfunctioning. Refer to Table 4.2.
9. If the diagnostic disk is available and can be booted, refer to the Disk-Based Diagnostics Manual, Chapter 6, "Floppy Disk Diagnostics," and run the tests. Be aware, however that these tests are designed to check drive reliability and will not aid you in locating problems in the controller, especially if you used it to boot the diagnostic disk.
10. If none of the preceding checks have resulted in any positive identification of the problem, replace the Color Video/Floppy Controller Card and rerun the checks. This should isolate the problem to the card. If the card is at fault, use Table 4.2 to check individual components.



**Table 4.2. Floppy Disk Controller Component Failures**

SYMPTOM	SUSPECTED PARTS	THINGS TO CHECK
No controller indication	U348 U305	Bus interface. FDC IC.
Drive motors will not turn on	U302, U307 U320, U321 U321 Power supply	Signal buffers. Logic gates. Signal decoder.
Driver motors come on but do not stay on	U301, U320, U321	Check pulse width after last access. It should last 2–3 seconds.
Erroneous data from good disk	U303 U304 U305, U308, U313	Read data buffer/inverter. Data separation chip. Read errors entering memory. Incorrect DMA signals causing incorrect processing of data. Check DMA processor on CPU card.
Bad card addressing or selection	U338	PAL address decoder. Refer to PAL equations in Chapter 3 for I/O signals.
Read sector errors	U302	Check for proper IDX signal.
Precomposition	U305, U310, U314, U315 U306, U311, U317	Check for correct precomp. signals (early, late). Check clock frequencies.
Erroneous data	U304, U314, U315	Check for correct signal pulses.
Will not write	U305, U308	Check write gate enable signal.

## Troubleshooting

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# Troubleshooting Table

**NOTE:** Use of the Disk-Based Diagnostics package, if available, is recommended for troubleshooting.

Table 4.3 lists some problems that may be encountered and some possible causes.

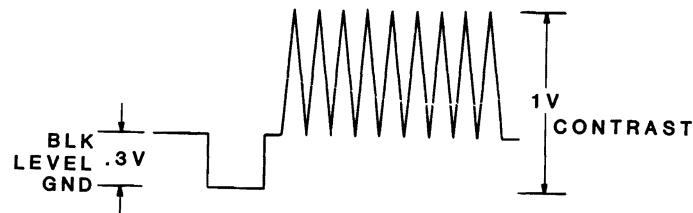
**Table 4.3. General Troubleshooting Guide**

PROBLEM	POSSIBLE CAUSE
No video dots.	Q301, Q302, Q303, RP306, U345, U346, U342, U324
Horizontal sync problems. Starting characters are off the left of screen, or first line does not start on the left side of the screen.	J305, J306, U341, U324, U325
Vertical sync problems. Rolling or starting point off the top of the screen.	J302, J303, J304, J313, U340, U341, U349, U324, U325
No monochrome (composite) vertical or horizontal sync.	J302, J303, J305, U341, U346, U349, U324, U325
No horizontal or vertical sync.	U341, U324, U325
No horizontal sync.	J305, U324, U325, U340, U349
Mismatched colors with missing intensity.	RP306, U342, U345, U324, U330, U331, U332, U326, U327, U334, U333
Background colors incorrect.	U324–U327, U330–U334
No RAM data output.	U325, U326, U327, U330–U334
Cursor not blinking.	U325
Wrong font or white screen.	SW301, pin 1, U319, U323–U328, U331–U334
No dots in graphics mode or wrong dot data.	U324–U327, U330–U334
Random characters and attributes.	U319, U323–U328, U330–U334

## Video Output Adjustments

The following paragraphs detail the procedure for setting the video output black level and contrast.

Connect the oscilloscope vertical input to the monochrome video output connector, P305. Connect oscilloscope external sync input to pin 5 of P303, HS. Obtain a stable waveform resembling Figure 4.1.



**Figure 4.1. Video Output Adjustment Waveform**

Adjust black level control, R319, for a pulse height of .3 volt. Then adjust the contrast control, R320, for a peak waveform height of 1 volt. The adjustments may be slightly interactive, so repeat these two operations as necessary to obtain the specified results.

# Chapter 5

## Parts List

### Introduction

**CAUTION:** This card contains Electrostatic-Sensitive Devices (ESD). Exercise extreme care when handling these devices to prevent damage.

This portion of the service module contains a component view of the Color Video/Floppy Controller Card (part number 181-5312) and related parts list. Refer to Figure 5.1 for location of parts and components.

**NOTE:** The symbols on the schematics (Figures 5.2 through 5.5) represent logic flow rather than any specific device's design.

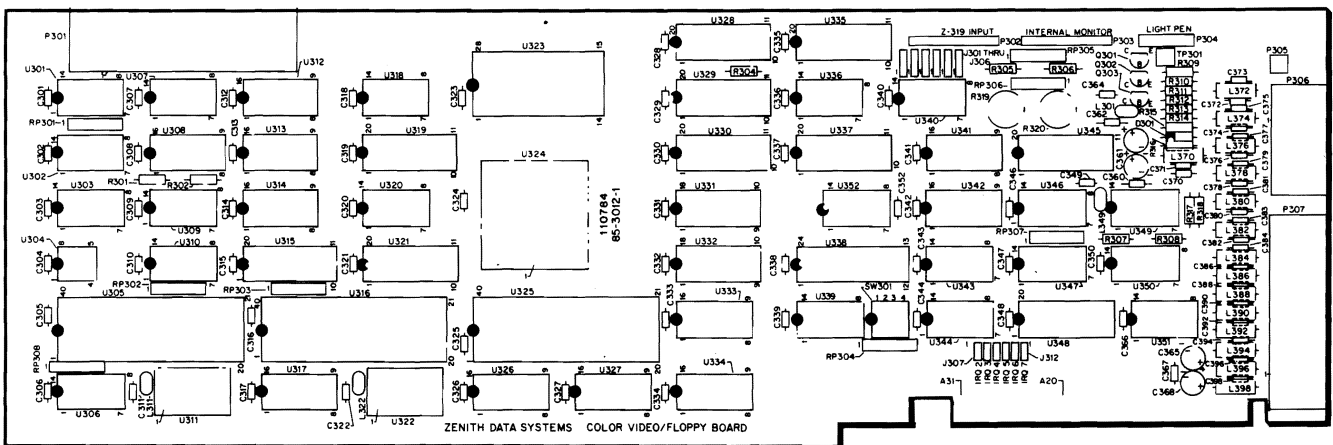


Figure 5.1. Component View



## Parts List

<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>	<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
<b>Diodes</b>			<b>Resistors</b>		
D301	HE-56-655		R301	HE-6-222-12	2200 ohm
			R302	HE-6-222-12	2200 ohm
<b>Jumpers</b>			R303	HE-9-131	330 ohm
J301	HE-432-1102	3M MOLEX	R304	HE-6-330-12	33 ohm
J302	HE-432-1102	3M MOLEX	R305	HE-6-2551-12	255 ohm
J303	HE-432-1102	3M MOLEX	R306	HE-471-12	47 ohm
J304	(not used)		R307	(not used)	
J305	HE-432-1102	3M MOLEX	R308	(not used)	
J306	(not used)		R309	(not used)	
J307 through J312	HE-432-1130	6M MOLEX (2 required*)	R310	HE-6-102-12	1000 ohm
<b>Inductors</b>			R311	(not used)	
L301	HE-235-299	RF choke 35 $\mu$ H	R312	(not used)	
L311	HE-235-299	RF choke 35 $\mu$ H	R313	HE-6-101-12	100 ohm
L322	HE-235-299	RF choke 35 $\mu$ H	R314	HE-6-470-12	47 ohm
L349	HE-235-299	RF choke 35 $\mu$ H	R315	HE-6-270-12	27 ohm
L374	HE-45-636	RF choke 3.2 $\mu$ H	R316	HE-6-122-12	1200 ohm
<b>Connectors</b>			R317	HE-6-102-12	1000 ohm
P301	HE-432-1302	34M AMP	R318	HE-6-102-12	1000 ohm
P302	HE-432-1233	10M MOLEX	R319	HE-10-1204	1000 ohm linear control
P303	(not used)		R320	HE-10-1204	1000 ohm linear control
P304	HE-432-1368	6M MOLEX	R321	HE-6-330-12	33 ohm
P305	HE-434-389	Socket phono	RP301	HE-9-120	150 ohm resistor pack
P306	HE-432-1358	9F AMP	RP302	HE-9-124	4700 ohm resistor pack
P307	HE-432-1478	25 WNCST Filtered	RP303	HE-9-124	4700 ohm resistor pack
<b>Transistors</b>			RP304	HE-9-124	4700 ohm resistor pack
Q301	HE-417-875	NPN	RP305	HE-9-99	1000 ohm resistor pack
Q302	(not used)		RP306	HE-9-156	Resistor ladder
Q303	HE-417-875	NPN	RP307	HE-9-106	10000 ohm resistor pack
			L374	HE-6-470-12	47 ohm
			L376	HE-6-470-12	47 ohm
			L378	HE-6-470-12	47 ohm
			L380	HE-6-470-12	47 ohm
* Each part provides one pin for all two-pin connectors J307 through J312.			<b>Switches</b>		
			SW301	HE-60-664	DIP SPST

## Parts List

<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>	<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
<b>Integrated Circuits</b>					
U301	HE-443-779	Quad 2-input NOR gate, 74LS02	U321	HE 443-805	Flip-flop octal three-state, 74LS273
	HE-434-298	14-pin socket		HE-434-311	20-pin socket
U302	HE-443-755	Hex inverter, 74LS04	U322	HE-150-165	Crystal 1.8432 MHz
	HE-434-298	14-pin socket	U323	HE-444-230-2	Prom 8K × 8
U303	HE-443-755	Hex inverter, 74LS04		HE-434-368	24-pin socket
	HE-434-298	14-pin socket	U324	HE-444-316	Video gate array
U304	HE-443-1218	Floppy disk data separator, 9216	U325	HE-434-380	68-pin PLCC socket
	HE-434-830	8-pin socket		HE-443-906	CRT controller, 6845
U305	HE-443-944	Floppy disk controller, μPD765	U326	HE-434-253	40-pin socket
	HE-434-253	40-pin socket		HE-443-1271	Dual 4-to-1 multiplexer, 74AS253
U306	HE-443-1232	Nand buffer, 74ALS38	U327	HE-434-299	16-pin socket
	HE-434-298	14-pin socket		HE-443-1271	Dual 4-to-1 multiplexer, 74AS253
U307	HE-443-1234	Hex inverting buffer, 74ALS1005	U328	HE-434-299	16-pin socket
	HE-434-299	16-pin socket		HE-443-1031	Flip-flop octal D, 74ALS574
U308	HE-434-1167	Quad RS422 line driver, 3487	U329	HE-434-311	20-pin socket
	HE-434-299	16-pin socket		HE-443-791	Buffer/driver, three-state, 74LS244
U309	HE-443-730	Flip-flop dual D, 74LS74	U330	HE-434-311	20-pin socket
	HE-434-298	14-pin socket		HE-443-1031	Flip-flop octal D, 74ALS574
U310	HE-443-728	Quad 2-input NAND gate, 74LS00	U331	HE-434-311	20-pin socket
	HE-434-298	14-pin socket		HE-443-1219	DRAM 16K × 4, 4416
U311	HE-150-138	Oscillator circuit	U332	HE-434-310	18-pin socket
U312	HE-443-902	Decoder, 74156		HE-443-1219	DRAM 16K × 4, 4416
	HE-434-299	16-pin socket	U333	HE-434-310	18-pin socket
U313	HE-443-752	Flip-flop quad D, 74LS175		HE-443-1271	Dual 4-to-1 multiplexer, 74AS253
	HE-434-299	16-pin socket	U334	HE-434-299	16-pin socket
U314	HE-443-955	Multiplexer, 74LS153		HE-443-1271	Dual 4-to-1 multiplexer, 74AS253
	HE 434-299	16-pin socket	U335	HE-434-299	16-pin socket
U315	HE 443-805	Flip-flop octal three-state, 74LS273		HE-443-754	Octal buffer, three-state, 74LS240
	HE-434-311	20-pin socket		HE-434-311	20-pin socket
U316	HE-443-874	UART, 8250	U336	HE-443-973	Binary counter, 74LS393
	HE-434-253	40-pin socket		HE-434-299	16-pin socket
U317	HE-443-757	4-bit counter	U337	HE-443-791	Buffer/driver, three-state, 74LS244
	HE-434-299	16-pin socket		HE-434-311	20-pin socket
U318	HE-443-728	Quad 2-input NAND gate, 74LS00	U338	HE-444-317	PAL, video address decoder
	HE-434-298	14-pin socket		HE-434-368	24-pin socket
U319	HE-443-1110	8-bit latch, 74LS377	U339	HE-443-811	Quad buffer, three-state, 74LS125
	HE-434-311	20-pin socket		HE-434-298	14-pin socket
U320	HE-443-875	Quad 2-input OR gate, 74LS32	U340	HE-443-872	Hex inverter, 74LS14
	HE-443-298	14-pin latch		HE-434-298	14-pin socket

## Parts List

<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>	<u>CIRCUIT REFERENCE DESIGNATOR</u>	<u>ZDS PART NO.</u>	<u>DESCRIPTION</u>
<b>Integrated Circuits (continued)</b>					
U341	HE-443-799 HE-434-299	Quad 2-input multiplexer 16-pin socket	U348	HE-443-885 HE-434-368	Transceiver 20-pin socket
U342	HE-443-799 HE-434-299	Quad 2-input multiplexer 16-pin socket	U349	HE-443-1234 HE-434-299	Hex inverting buffer 16-pin socket
U343	HE-443-732 HE-434-298	8-input NAND gate 14-pin socket	U350	HE-443-795 HE-434-298	Receiver RS232 14-pin socket
U344	HE-443-1196 HE-434-298	Hex driver 14-pin socket	U351	HE-443-794 HE-434-298	EIA driver 14-pin socket
U345	HE-443-791 HE-434-311	Buffer/driver, three-state 20-pin socket	U352	HE-443-798 HE-434-298	Dual 4-input NAND gate 14-pin socket
U346	HE-443-875 HE-434-298	Quad 2-input OR gate 14-pin latch	U353	HE-443-1072 HE-434-298	Quad positive OR gate 14-pin socket
U347	HE-443-795 HE-434-298	Receiver RS232 14-pin socket			



D

C

B

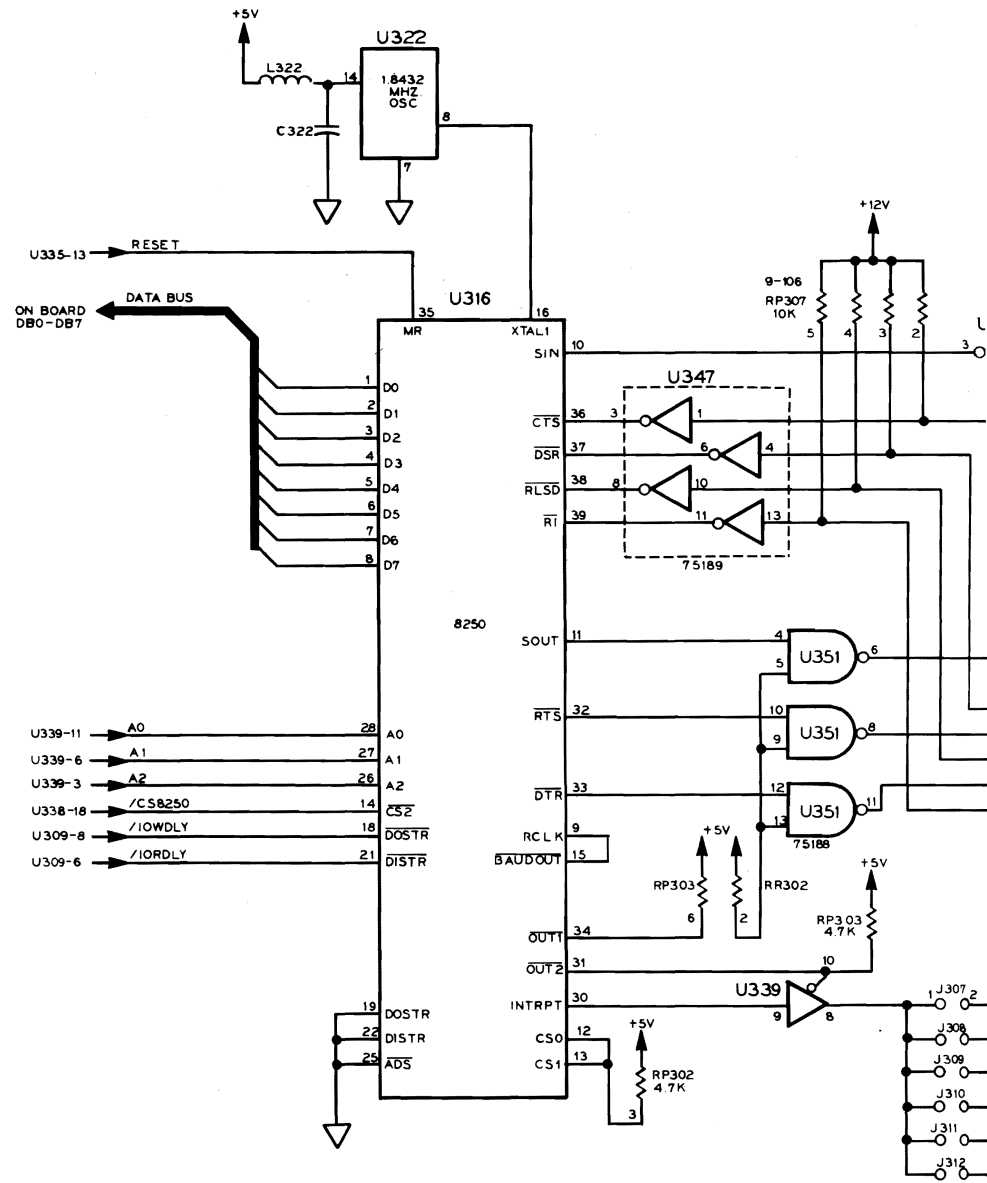
A

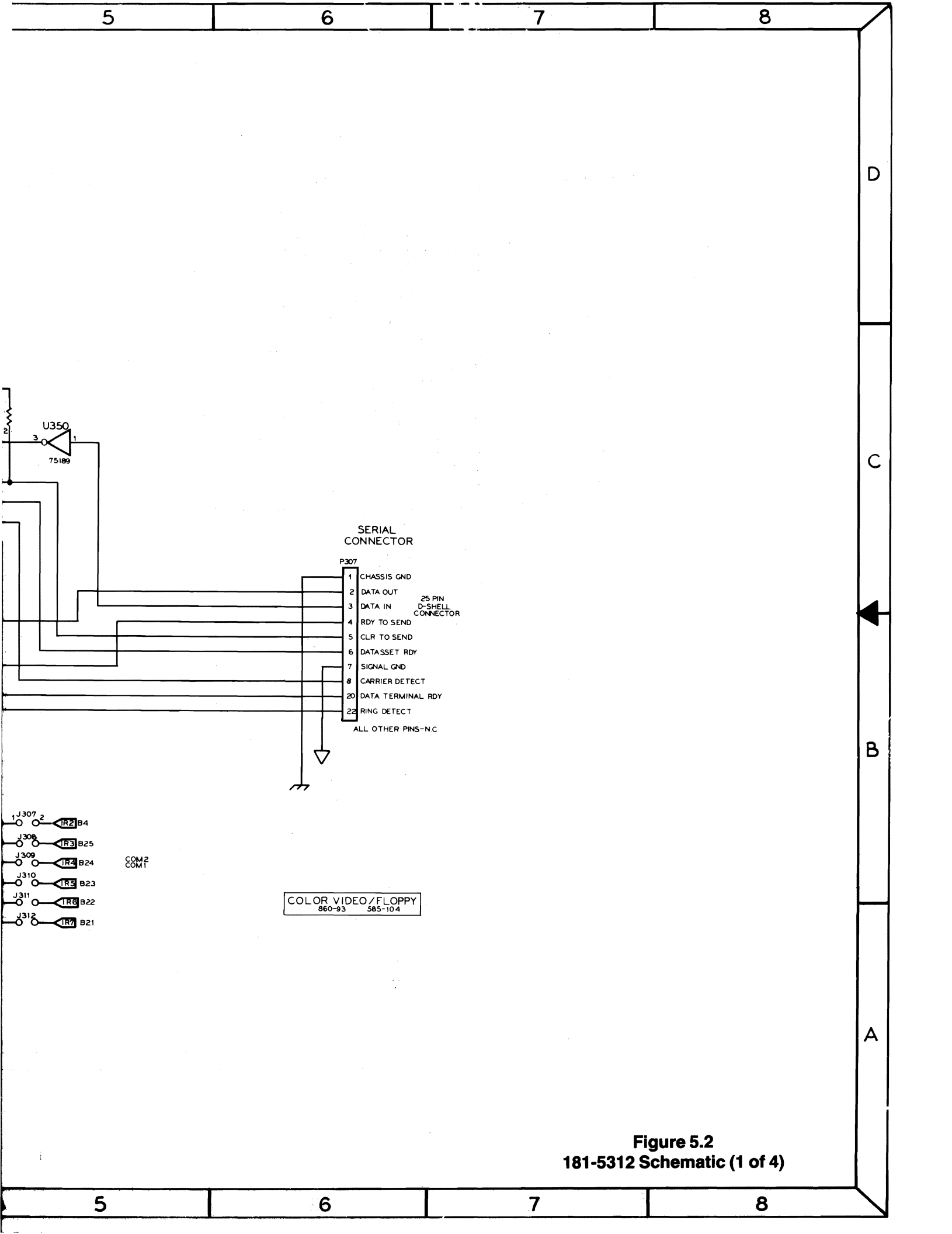
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3

4





**Figure 5.2**  
**181-5312 Schematic (1 of 4)**

1

2

3

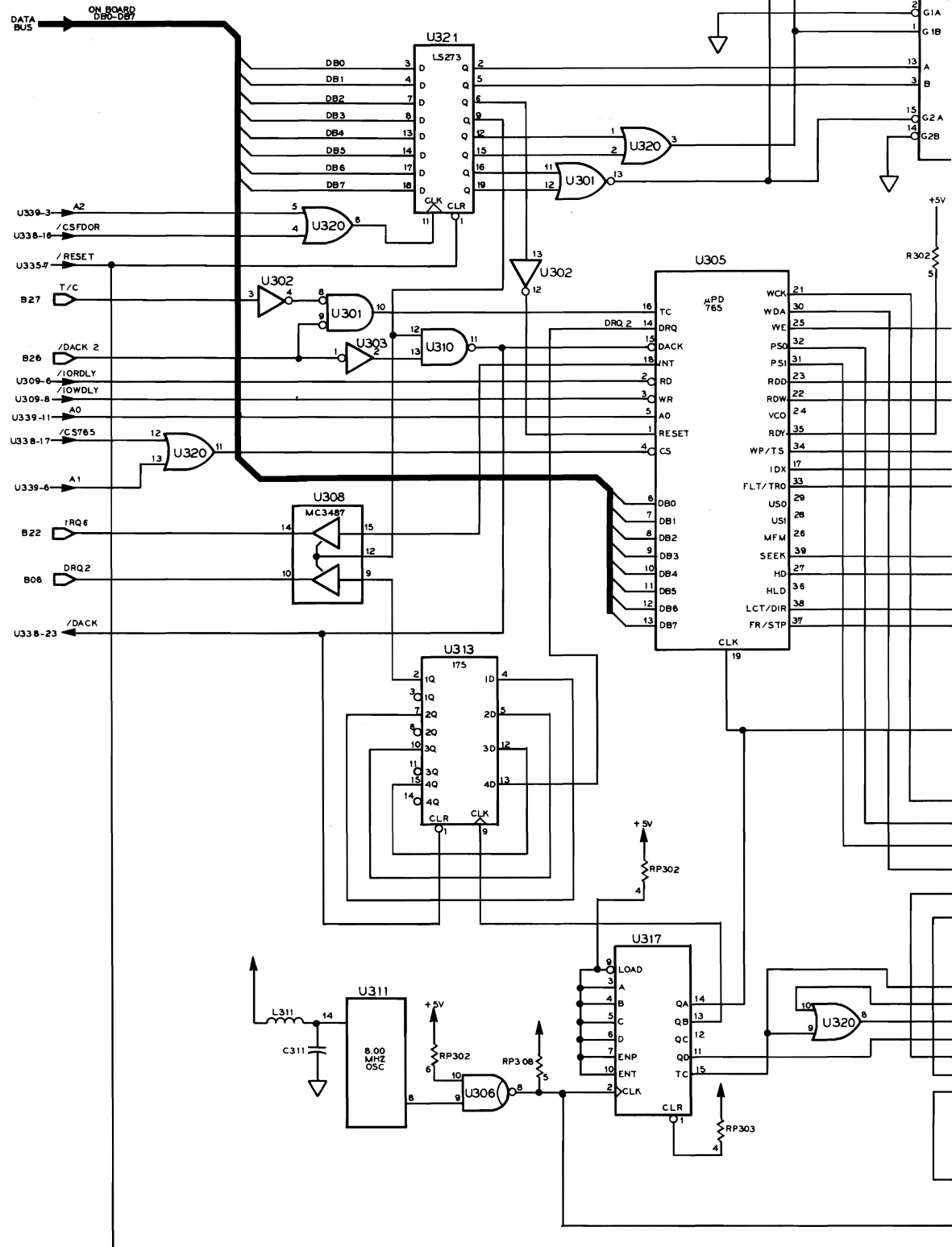
4

D

C

B

A

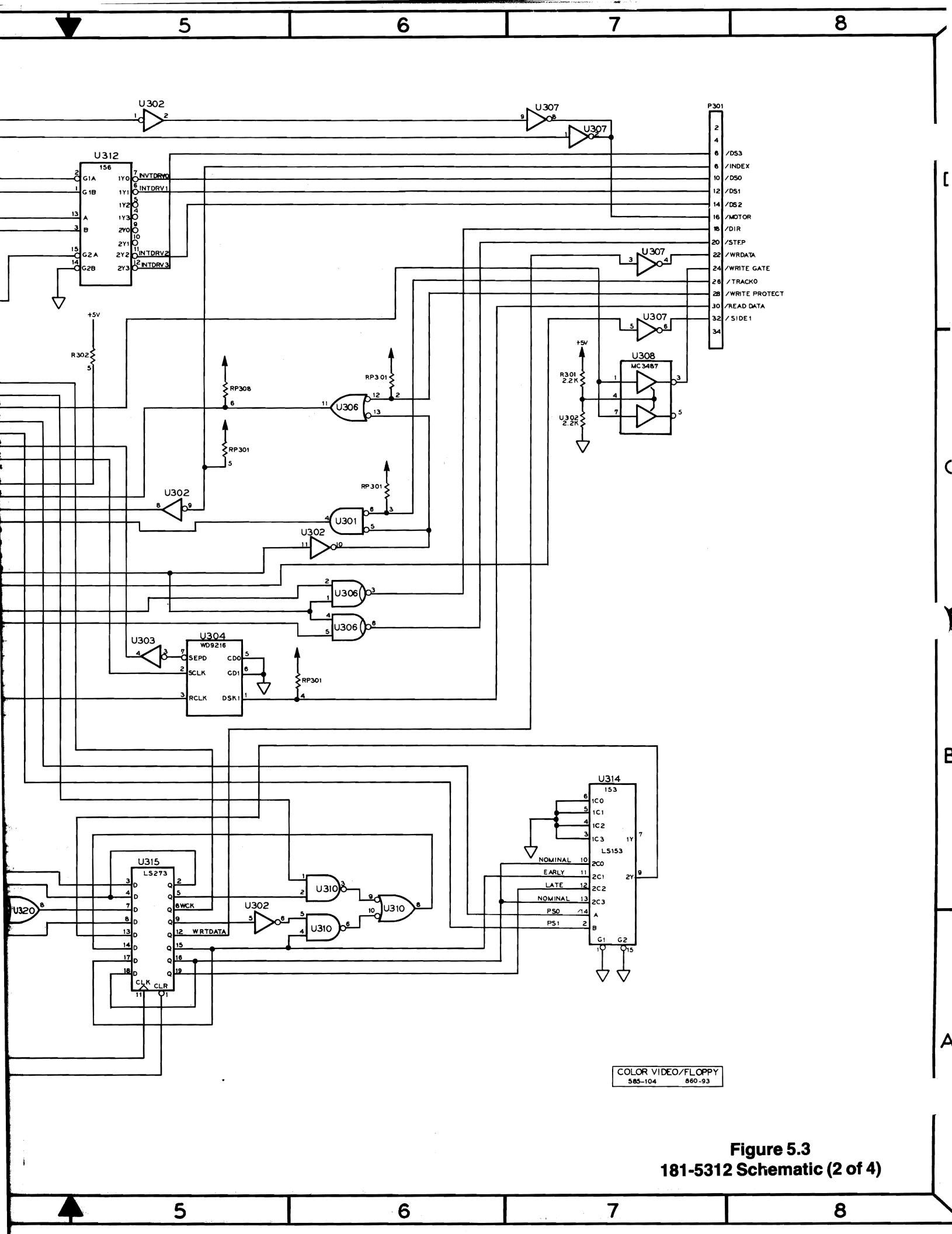


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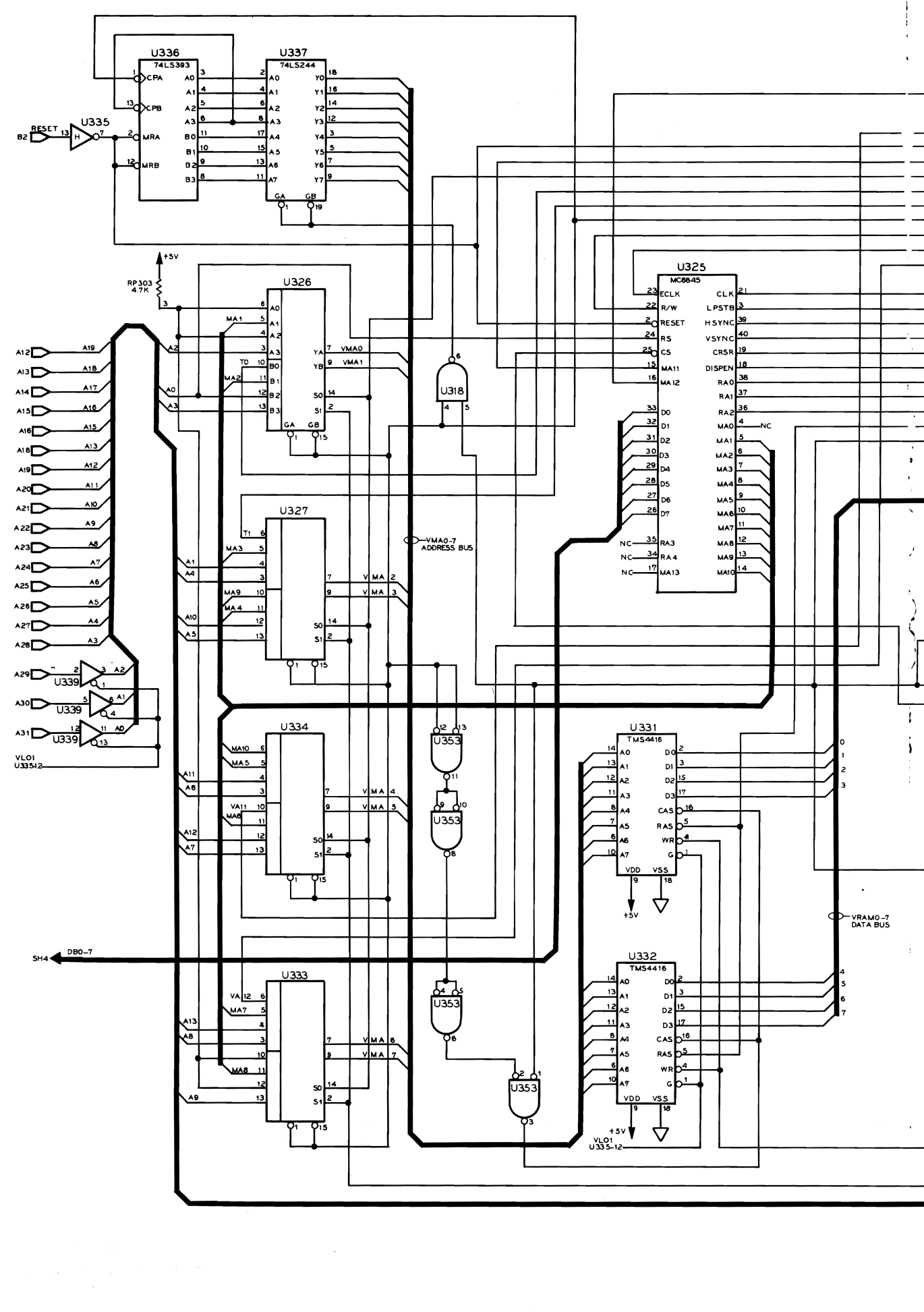
3

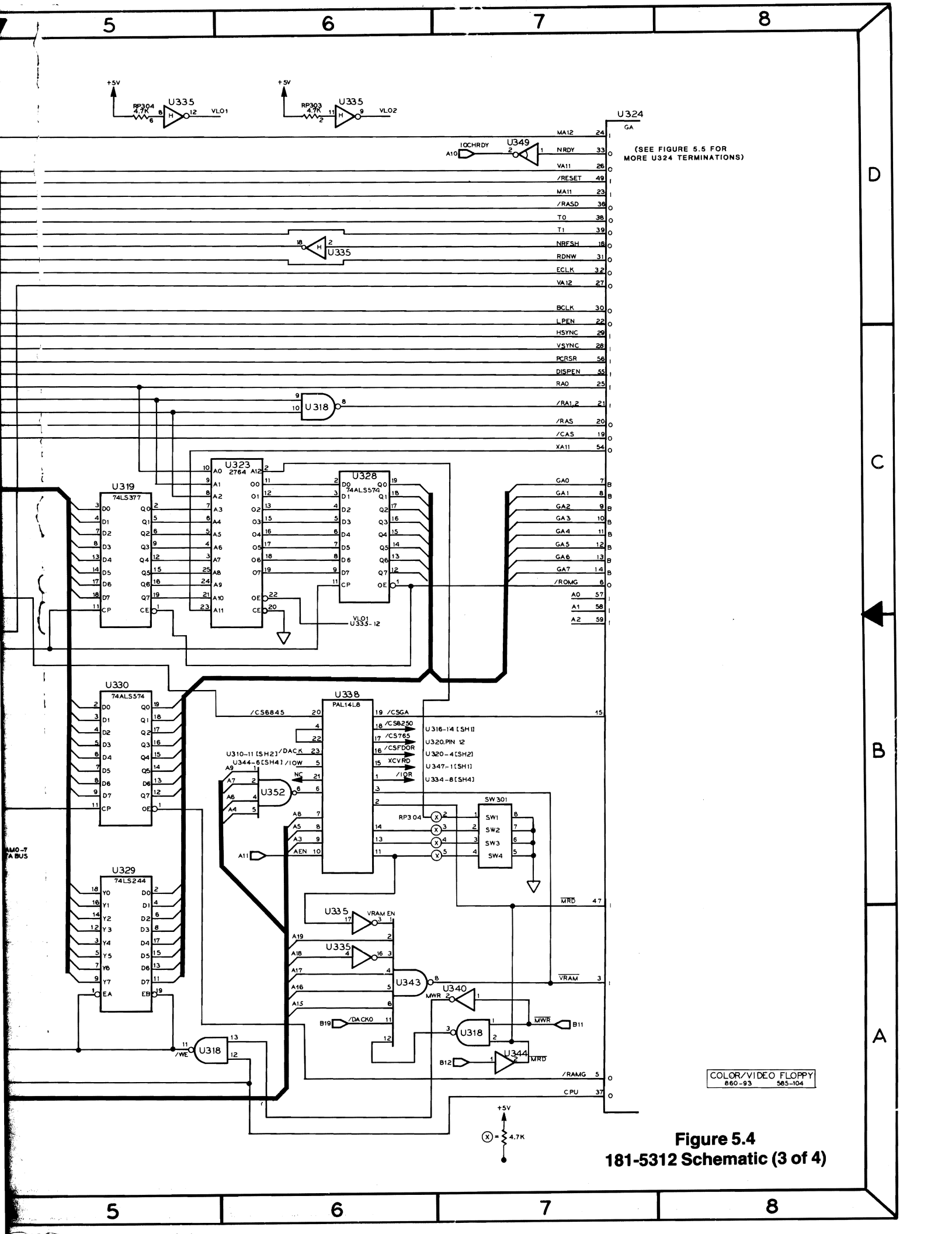
4



COLOR VIDEO/FLOPPY  
585-104 860-93

Figure 5.3  
181-5312 Schematic (2 of 4)





(SEE FIGURE 5.5 FOR MORE U324 TERMINATIONS)

COLOR/VIDEO FLOPPY  
860-93 565-104

Figure 5.4  
181-5312 Schematic (3 of 4)

1

2

3

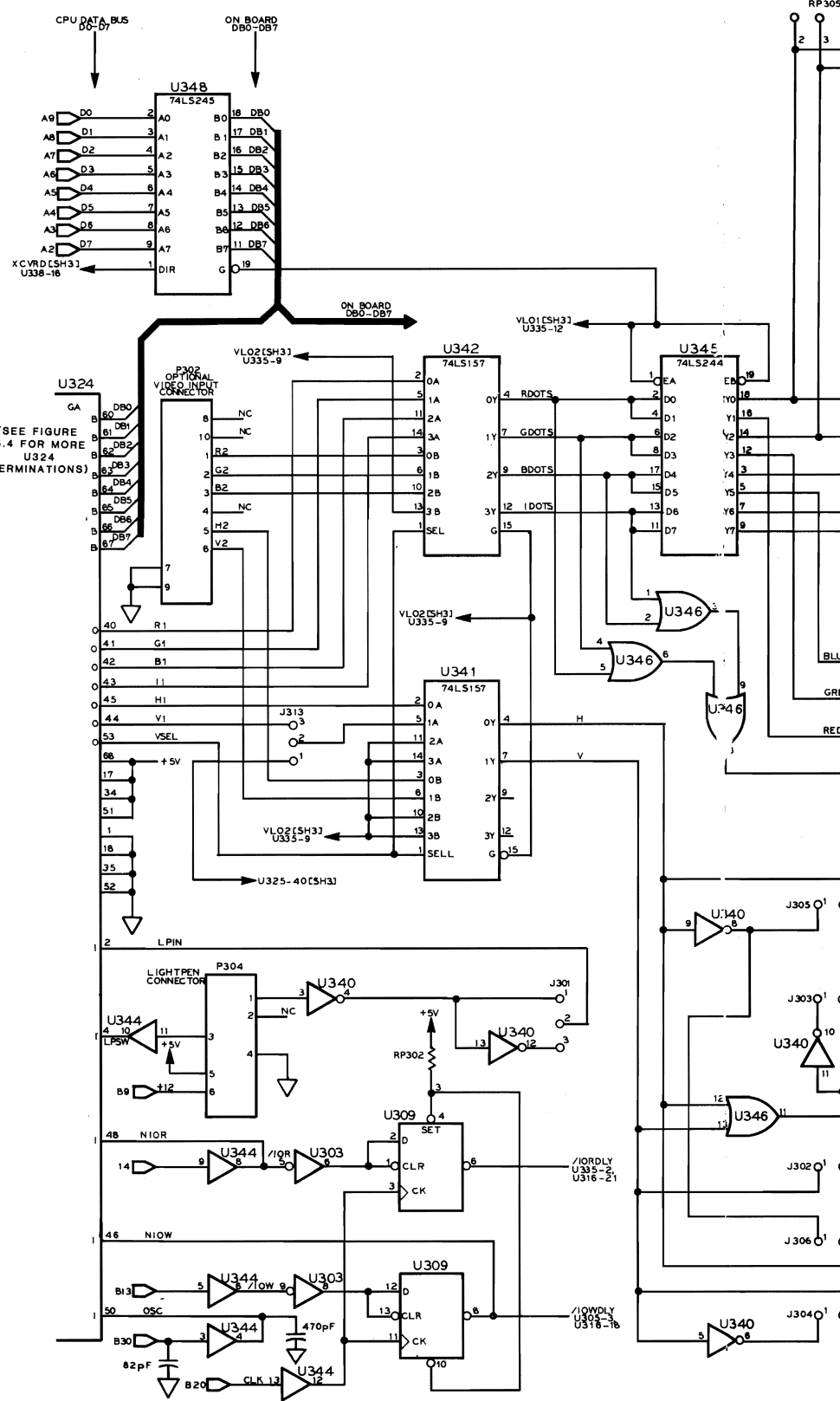
4

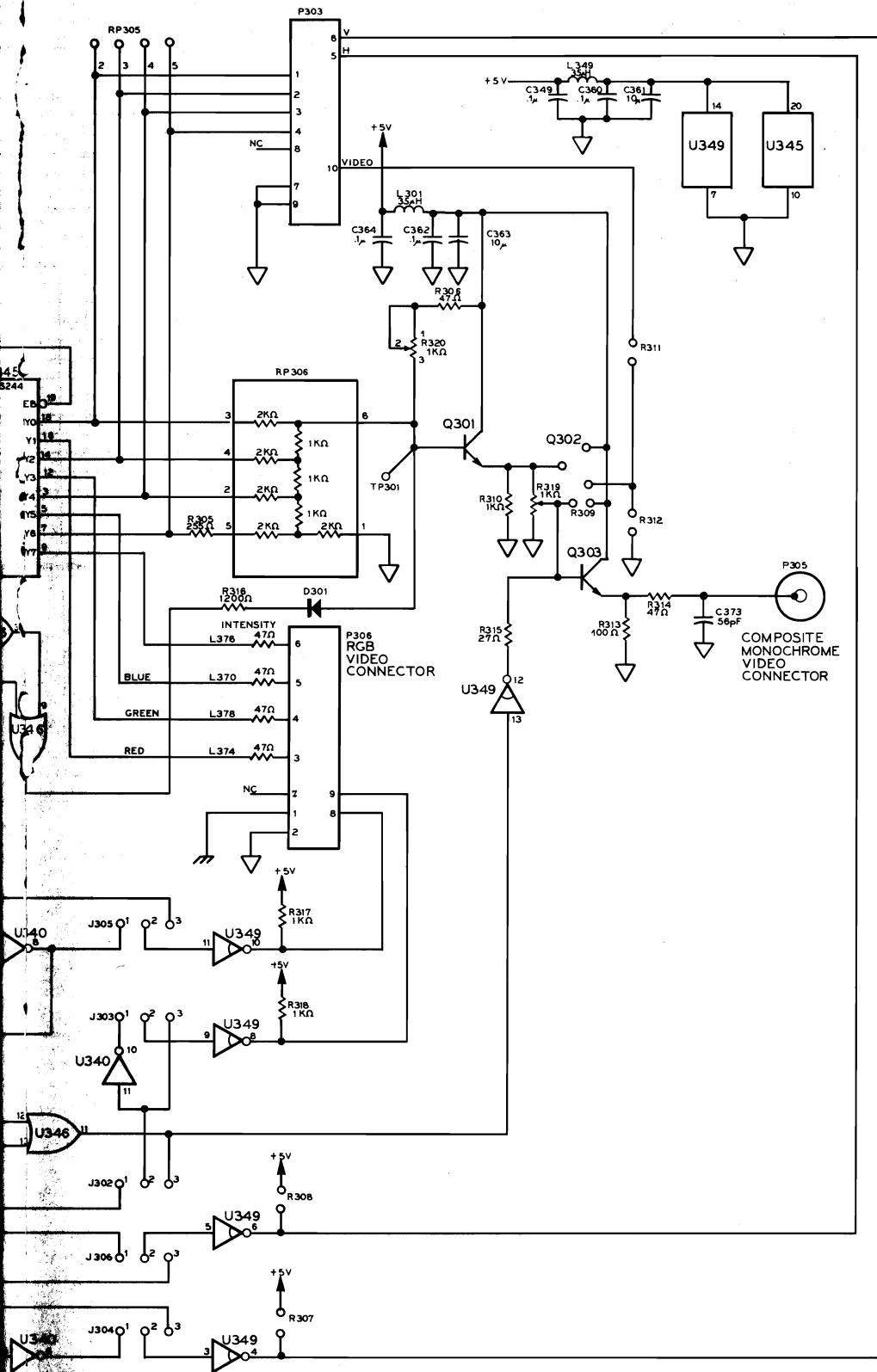
D

C

B

A





COLOR VIDEO/FLOPPY  
860-83 565-104

Figure 5.5  
181-5312 Schematic (4 of 4)



# SERVICE MODULE

---

# Shugart Drive

**Z-207-7**

---

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

## Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	- PURPOSE OF SERVICE BULLETIN	INITIALS

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St. Joseph, Michigan 49085

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# Introduction

This module contains the factory configuration and Shugart Service Manual. The service manual is included for testing and alignment purposes only. **DO NOT** attempt repair or order parts from the Shugart Service Manual.

## Parts Supplied

The following parts are supplied with the Z-207-7:

- Various manuals;
- A 5¼" half-height, 48 TPI, Shugart Drive;
- 2 foam strips;
- 4 mounting support brackets;
- 4 Phillips flathead screws;
- 4 Phillips panhead screws.

# Configuration

## Introduction

This chapter provides the factory configuration settings for single, dual, and multiple disk drives. For access to the disk drive(s), refer to disassembly procedures in the appropriate service manual or the Z-100 PC Base Units Service Modules.

## Single Disk Drive Configuration

Refer to Figure 2.1.

- Configure drive A by installing the jumper referred to in Inset #2 at location 1.
- **DO NOT** move the jumper located at pin DC.

## Configuration

---

# Dual Disk Drive Configuration

Refer to Figure 2.1.

## Drive A

- Configure drive A by installing the jumper referred to in Inset #2 at location 1.
- Remove and discard resistor pack referred to in Inset #2.
- **DO NOT** move the jumper located at pin DC.

## Drive B

- Configure drive B by installing the jumper referred to in Inset #1 at location 2.
- **DO NOT** remove resistor pack.

# Multiple Disk Drive Configuration

Refer to Figure 2.1.

- Configure drive A by installing the jumper referred to in Inset #2 at location 1.
- Remove and discard resistor pack referred to in Inset #2.
- **DO NOT** move jumpers located at pin DC.
- Configure drive B by installing the jumper referred to in Inset #1 at location 2.
- Remove and discard resistor pack referred to in Inset #2.
- Configure drive C by installing the jumper referred to in Inset #1 at location 3.
- Remove and discard resistor pack referred to in Inset #2.
- Configure drive D by installing the jumper referred to in Inset #1 at location 4.

**NOTE: DO NOT** remove resistor pack from drive C if you are using only three drives.

Configuration

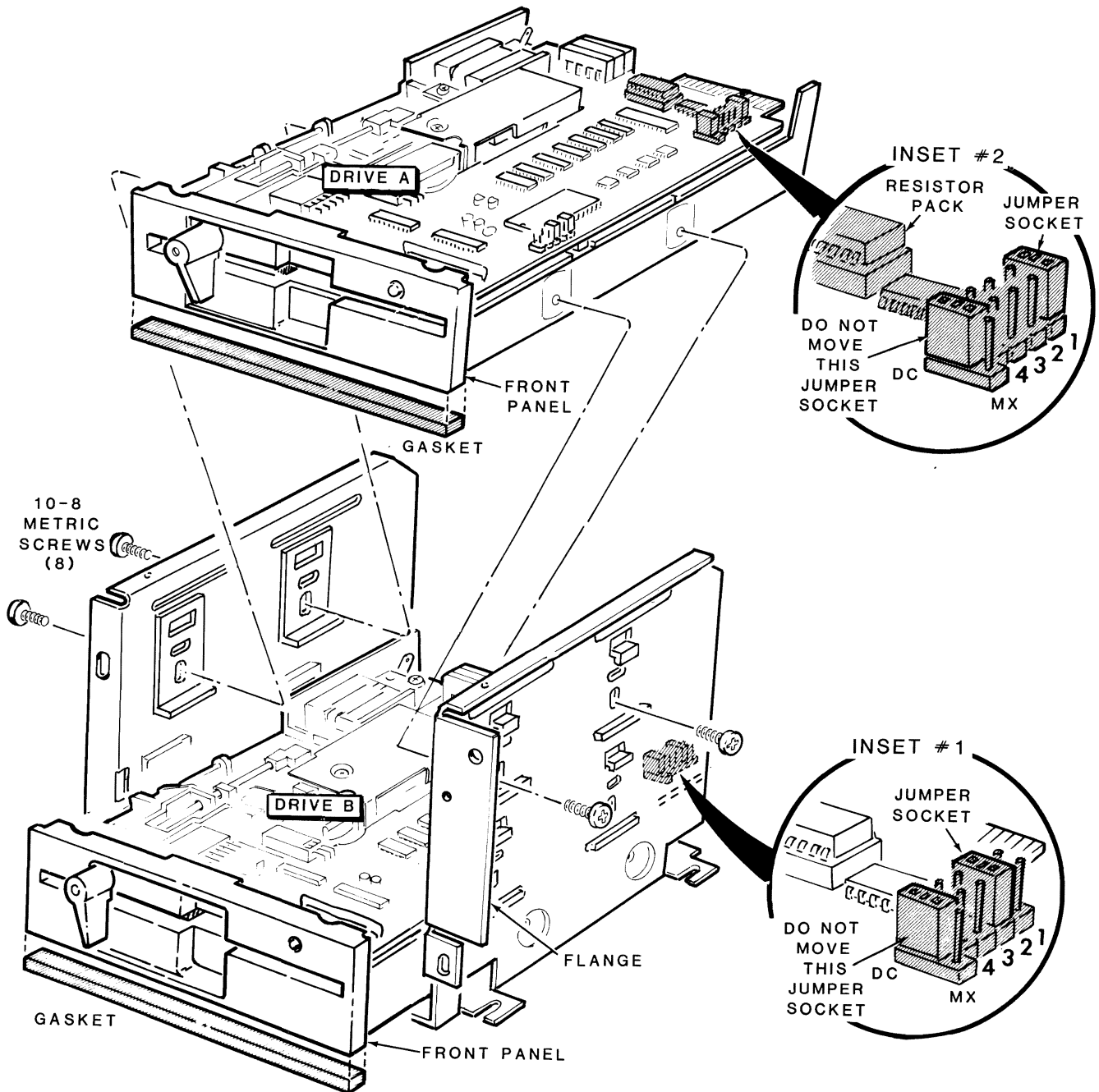


Figure 2.1. Configuration (Shown for the Z-150)

# Shugart Service Manual

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Sunnyvale, California 94086



**SA455/465  
Minifloppy™  
Drive**

**P/N 39239-0**

**Service Manual  
May 1983**

***Shugart***

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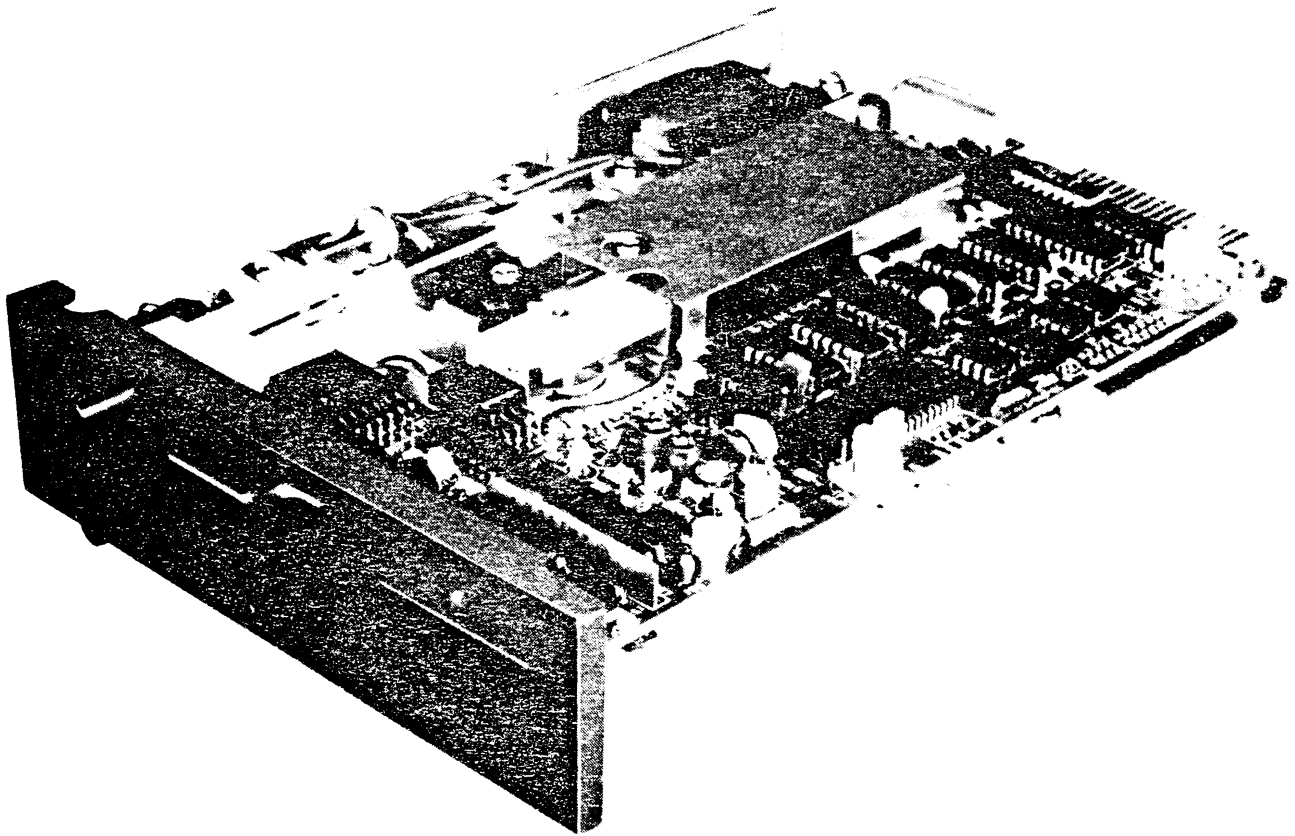
# ABBREVIATIONS/MNEMONICS

<b>AM</b>	Address Mark	<b>NRZ</b>	Non Return to Zero
<b>bpi</b>	Bits Per Inch	<b>PCB</b>	Printed Circuit Board
<b>CRC</b>	Cyclic Redundancy Check	<b>PM</b>	Preventive Maintenance
<b>fci</b>	Flux Changes Per Inch	<b>POH</b>	Power On Hours
<b>FM</b>	Frequency Modulation	<b>PSI</b>	Product Selection Index
<b>GND</b>	Ground	<b>TP</b>	Test Point
<b>ID</b>	Index	<b>tpi</b>	Tracks Per Inch
<b>I/O</b>	Input/Output	<b>TRK</b>	Track
<b>MFM</b>	Modified FM	<b>WG OFF</b>	Write Gate Off
<b>MTBF</b>	Mean Time Between Failures	<b>1F</b>	Single Density
<b>MTTR</b>	Mean Time to Repair	<b>2F</b>	Double Density

## ABOUT THIS MANUAL

While every effort has been made to ensure that the information provided herein is correct, please notify us in the event of an error or inconsistency. Direct any comments on the form at the back of this manual to:

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Technical Publications, MS 3-14  
475 Oakmead Parkway  
Sunnyvale, CA 94086  
(408) 733-0100



39238-01-A

**FIGURE 1-1. SA455/465 DOUBLE-SIDED MINIFLOPPY™ DRIVE**

# SECTION I INTRODUCTION

## 1.1 GENERAL DESCRIPTION

The SA455/465 Minifloppy Disk Drives are enhanced double-headed, half-height versions of the Shugart SA400 minifloppy drives. The SA455/465 provides up to four times the on-line storage capacity, faster access time, and improved reliability and maintainability.

SA455/465 drives read and write in single and double density on standard 5.25 inch diskettes on both sides of the diskettes. The new drives are half the height of the Shugart SA400 and are plug compatible.

The compact SA455/465 offers a reliable, low cost, high performance alternative to OEM data storage applications where tape cassette units would have been previously considered.

SA455/465 drives have these standard features: compact size - 1.62 inches high × 5.75 inches wide × 7.96 inches deep, and a weight of 3.3 pounds; low heat dissipation; dc drive motor with precision servo speed control and integral tachometer; band positioner; same proprietary glass bonded ferrite/ceramic read/write head as used in Shugart's large floppy drives; internal write protect circuitry; activity light, and solid die cast chassis.

Typical applications for the SA455/465 are word processing systems, entry level micro-processor systems, intelligent calculators, program storage, hobby computer systems, and other applications where low cost random access data storage is a requirement.

This manual provides depot level maintenance information necessary to maintain, trouble-shoot, and repair the SA455/465. A separate OEM manual (P/N 39238) is available which describes installation, interface, and power requirements useful for the applications of the drive.

### Key Features

- a. 0.5 Mbytes (SA455) or 1.0 Mbyte (SA465) storage capacity (unformatted)
- b. Low power (12.5 watts)
- c. 125/250 kbits/second transfer rate
- d. DC drive motor (eliminates ac requirements)

## 1.2 SPECIFICATION SUMMARY

### 1.2.1 Performance Specifications

Capacity (in bytes)	SA455 (40 Track)		SA465 (80 Track)	
	Single Density (FM)	Double Density (MFM)	Single Density (FM)	Double Density (MFM)
Unformatted				
Per Disk	250,000	500,000	500,000	1,000,000
Per Surface	125,000	250,000	250,000	500,000
Per Track	3,125	6,250	3,125	6,250



	<b>SA455 (40 Track)</b>		<b>SA465 (80 Track)</b>	
	Single Density	Double Density	Single Density	Double Density
Formatted (16 Records/Track)				
Per Disk	163,840	327,680	327,680	655,360
Per Track	2,048	4,096	2,048	4,096
Per Sector	128	256	128	256
Formatted (10 Records/Track)				
Per Disk	204,800	409,600	409,600	819,200
Per Track	2560	5120	2560	5120
Per Sector	256	512	256	512
Transfer Rate	125 kbits/sec	250 kbits/sec	125 kbits/sec	250 kbits/sec
Latency (avg.)	100 ms	100 ms	100 ms	100 ms
Access Time				
Track to Track	6 ms	6 ms	3 ms	3 ms
Average	93 ms	93 ms	94 ms	94 ms
Settling Time	15 ms	15 ms	15 ms	15 ms

### 1.2.2 Functional Specifications

Motor Start Time	500 ms	500 ms	500 ms	500 ms
Rotational Speed	300 rpm	300 rpm	300 rpm	300 rpm
Recording Density	2938 bpi	5876 bpi	2961 bpi	5922 bpi
Flux Density	5876 fci	5876 fci	5922 fci	5922 fci
Track Density	48 tpi	48 tpi	96 tpi	96 tpi
Media Requirements				
Soft sectored	SA154	SA154	SA164	SA164
16 sectors hard sectored	SA155	SA155	SA165	SA165
10 sectors hard sectored	SA157	SA157	SA167	SA167
Industry standard flexible diskette				
Oxide on 0.003 in. (0.08 mm) Mylar				
5.25 in. (133.4 mm) square jacket				

### 1.2.3 Physical Specifications

<b>Environmental Limits</b>	<b>Operating</b>	<b>Shipping</b>	<b>Storage</b>
Ambient Temperature	50° to 115°F (10.0° to 46.1°C)	-40° to 144°F (-40° to 62.2°C)	-8° to 117°F (-22.2° to 47.2°C)
Relative Humidity	20 to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	78°F (25.6°C)	No Condensation	No Condensation
Shock	0.5G 10 ms	15G 10 ms	35G 10 ms
Vibration	0.5G 5-600 Hz	3G 5-600 Hz	3G 5-600 Hz

#### DC Voltage Requirements

+12 V ± 10% @ 1.2 A (max), 0.6 A (typ), 100 mV ripple  
+ 5 V ± 5% @ 0.9 A (max), 0.6 A (typ), 50 mV ripple

#### Mechanical Dimensions (exclusive of front panel)

Width = 5.75 inches (146.1 mm)

Height = 1.62 inches (41.1 mm)

Depth = 7.96 inches (202 mm)

Weight = 3.3 lbs (1.5 kg)

Power Dissipation = 9.6 Watts (34.0 BTU) continuous typical  
3.6 Watts (13.5 BTU) standby

#### NOTE

Standby: Drive motor off, drive select off, and stepper at reduced current.

## 1.2.4 Reliability Specifications

MTBF: 10,000 POH under typical usage.  
PM: Not required.  
MTTR: 30 minutes.

### Error Rates:

Soft Read Errors: 1 per  $10^9$  bits read.  
Hard Read Errors: 1 per  $10^{12}$  bits read.  
Seek Errors: 1 per  $10^6$  seeks.

### Media Life:

Passes per Track:  $3.0 \times 10^6$   
Insertions: 30,000 +

## 1.3 FUNCTIONAL CHARACTERISTICS

The SA455/465 consists of read/write and control electronics, drive mechanism, read/write head, and precision track positioning mechanism. These components perform the following functions:

- a. Interpret and generate control signals.
- b. Move read/write heads to the desired track.
- c. Read and write data.

The interface signals and their relationship to the internal functions are shown in figure 1-2.

### 1.3.1 Read/Write and Control Electronics

The electronics package contains:

- a. Index detector circuits
- b. Head position actuator driver
- c. Read/write amplifier and transition detector
- d. Write protect detector
- e. Drive select circuit
- f. Drive motor control

### 1.3.2 Drive Mechanism

The dc drive motor under servo speed control (using an integral tachometer) rotates the spindle at 300 rpm through a direct drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange.

### 1.3.3 Positioning Mechanics

The read/write head assembly is accurately positioned through the use of a band positioner which is attached to the head carriage assembly. Precise track location is accomplished as this positioner is rotated in discrete increments by a stepping motor.

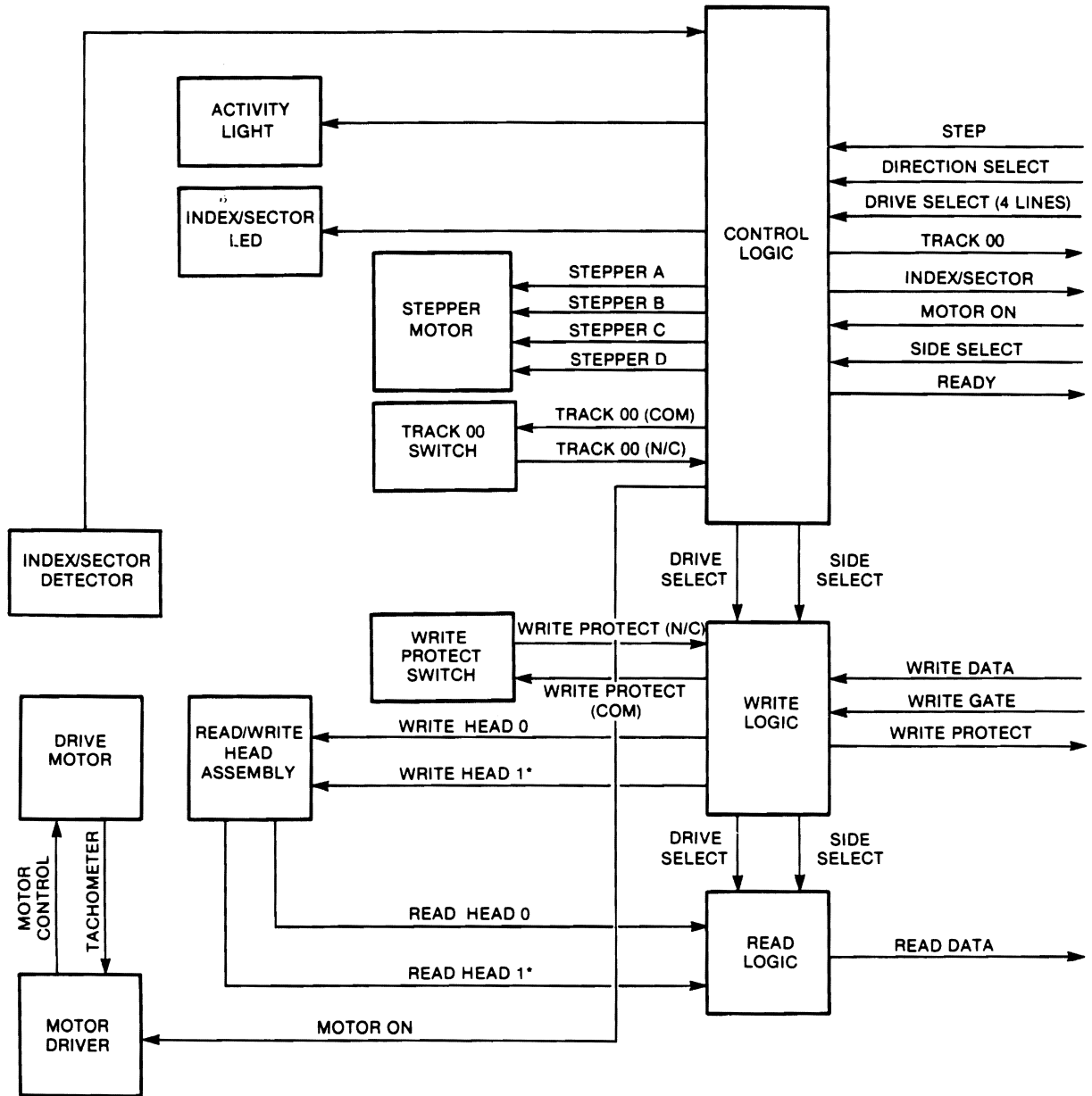
### 1.3.4 Read/Write Heads

The proprietary heads are a single element ceramic read/write head with tunnel erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal-to-noise ratio and diskette interchangeability is ensured.

The read/write heads are mounted on a carriage which is located on precision carriage ways. The diskette is held in a plane perpendicular to the read/write heads by a platen located on the base casting. This precise registration assures perfect compliance with the read/write heads. The read/write heads are in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette with minimum head/diskette wear.

### 1.3.5 Recording Formats

The formats of the data recorded on the diskette are totally a function of the host system. These formats can be designed around the user's application to take maximum advantage of the total available bits that can be written on any one track.



\*SA465 ONLY.

39238-02-A

FIGURE 1-2. SA455/465 FUNCTIONAL DIAGRAM

## **1.4 FUNCTIONAL OPERATIONS**

### **1.4.1 Power Sequencing**

Applying dc power to the SA455/465 can be done in any sequence. However, during power up, the WRITE GATE line must be held inactive or at a high level. This will prevent possible "glitching" of the media. After application of dc power, a 100 ms delay should be introduced before any operation is performed. After powering on, initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, a Step Out operation should be performed until the TRACK 00 line becomes active (Recalibrate).

### **1.4.2 Drive Selection**

Drive selection occurs when the proper DRIVE SELECT line is activated. Only the drive with this line jumpered will respond to input lines or gate output lines.

### **1.4.3 Motor On**

In order for the host system to read or write data, the dc drive motor must be turned on. This is accomplished by activating the line -MOTOR ON. A 500 ms delay must be introduced after activating this line to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the MOTOR ON line. The control electronics keep the motor active for 3 seconds, after MOTOR ON is deactivated. This allows reselecting during copy operations and will ensure maximum motor and media life.

### **1.4.4 Track Accessing**

Seeking the read/write heads from one track to another is accomplished by:

- a. Activating the DRIVE SELECT line.
- b. Selecting desired direction using the DIRECTION SELECT line.
- c. WRITE GATE being inactive.
- d. Pulsing the STEP line.

Multiple track accessing is accomplished by repeated pulsing of the STEP line (with direction valid) until the desired track has been reached. Each pulse on the STEP line will cause the read/write heads to move one track either in or out depending on the DIRECTION SELECT line. Head movement is initiated on the trailing edge of the step pulse.

### **1.4.5 Step Out**

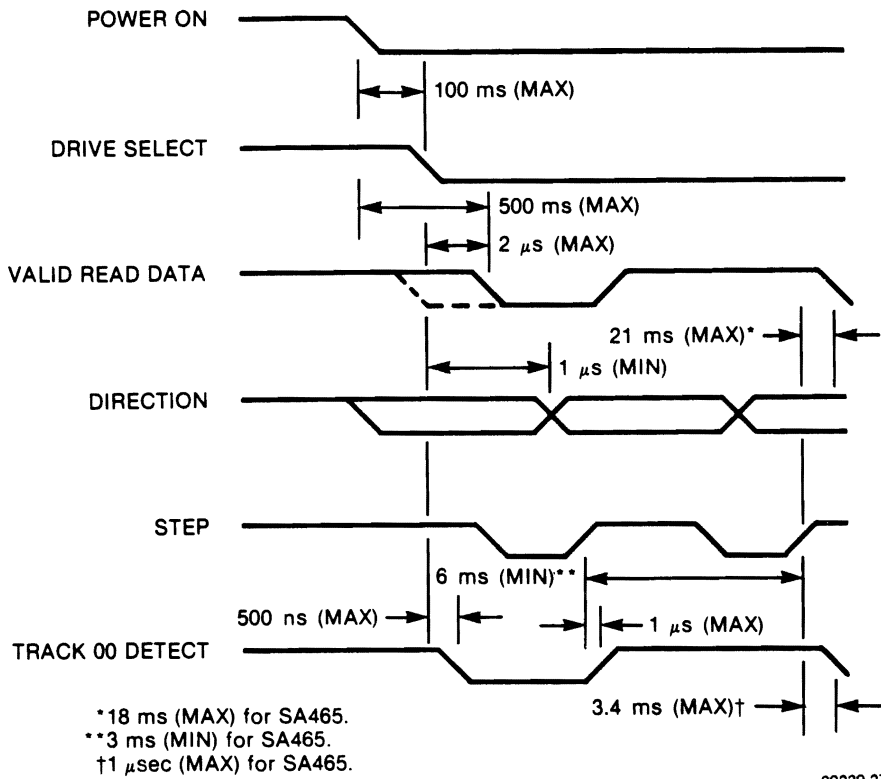
With the DIRECTION SELECT line at a plus logic level (2.4 to 5.25 V), a pulse on the STEP line will cause the read/write heads to move one track away from the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in figures 1-3 and 1-4.

### **1.4.6 Step In**

With the DIRECTION SELECT line at minus logic level (0 to 0.4 V), a pulse on the STEP line will cause the read/write heads to move one track closer to the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in figures 1-3 and 1-4.

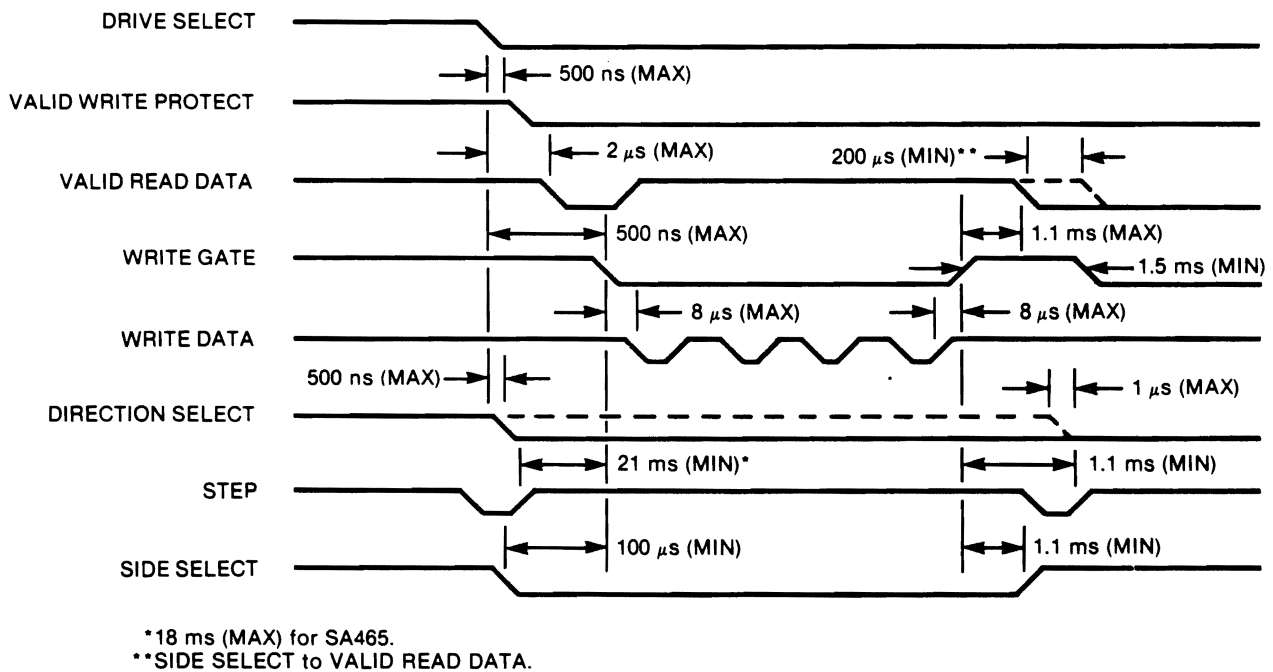
### **1.4.7 Side Selection**

Head selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the diskette. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100  $\mu$ s delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Figure 1-5 shows the use of SIDE SELECT prior to a read operation.



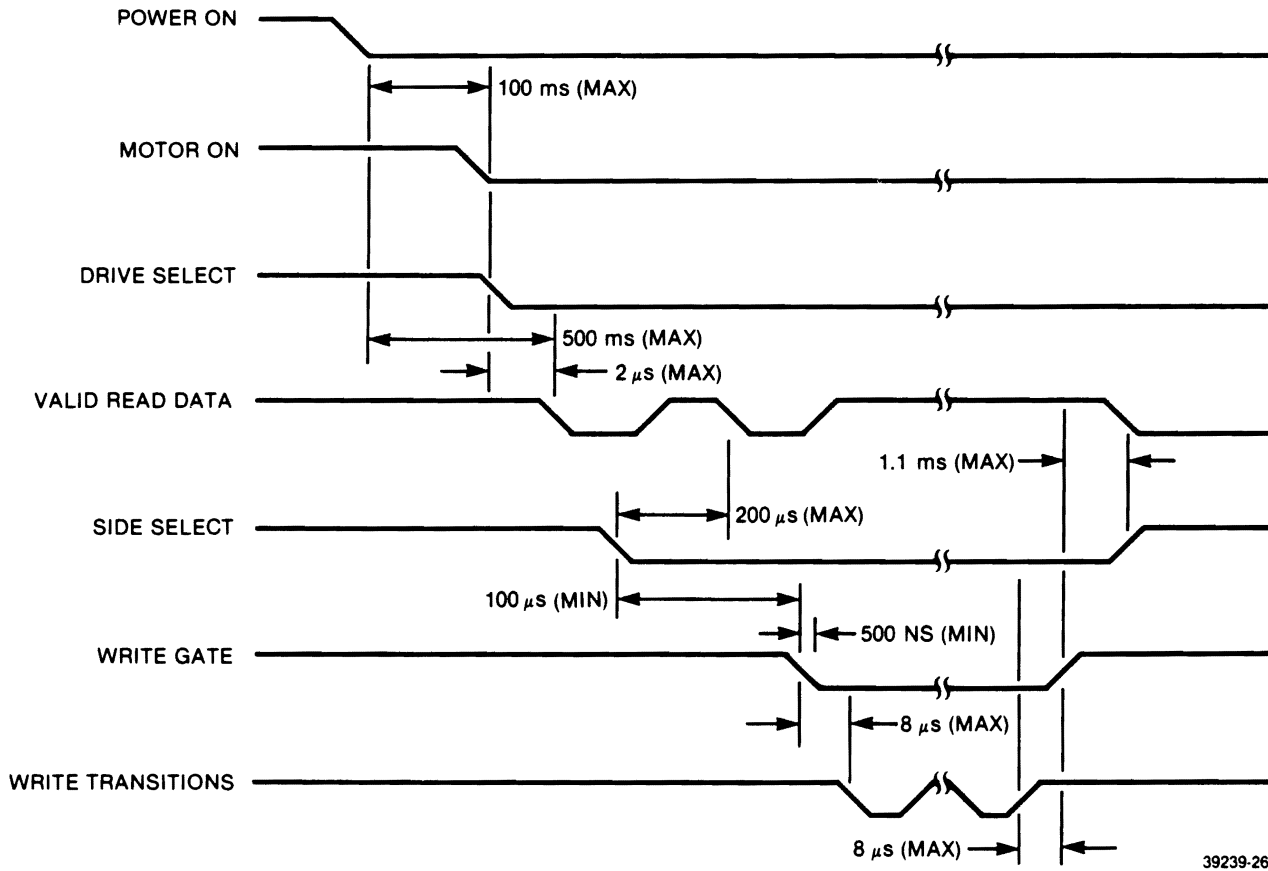
39239-27

FIGURE 1-3. STEP TO READ



39239-28

FIGURE 1-4. WRITE TO STEP



**FIGURE 1-5. READ TO WRITE (FM)**

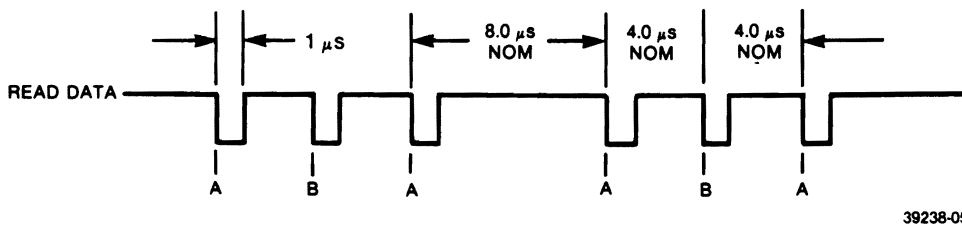
### 1.4.8 Read Operation

Reading data from the SA455/465 is accomplished by:

- Activating the DRIVE SELECT line.
- Selecting the head.
- WRITE GATE being inactive.

The timing relationships required to initiate a read sequence are shown in figure 1-5. These timing specifications are required in order to guarantee that the position of the read/write heads has stabilized prior to reading.

The timing of Read Data (FM) is shown in figure 1-6.

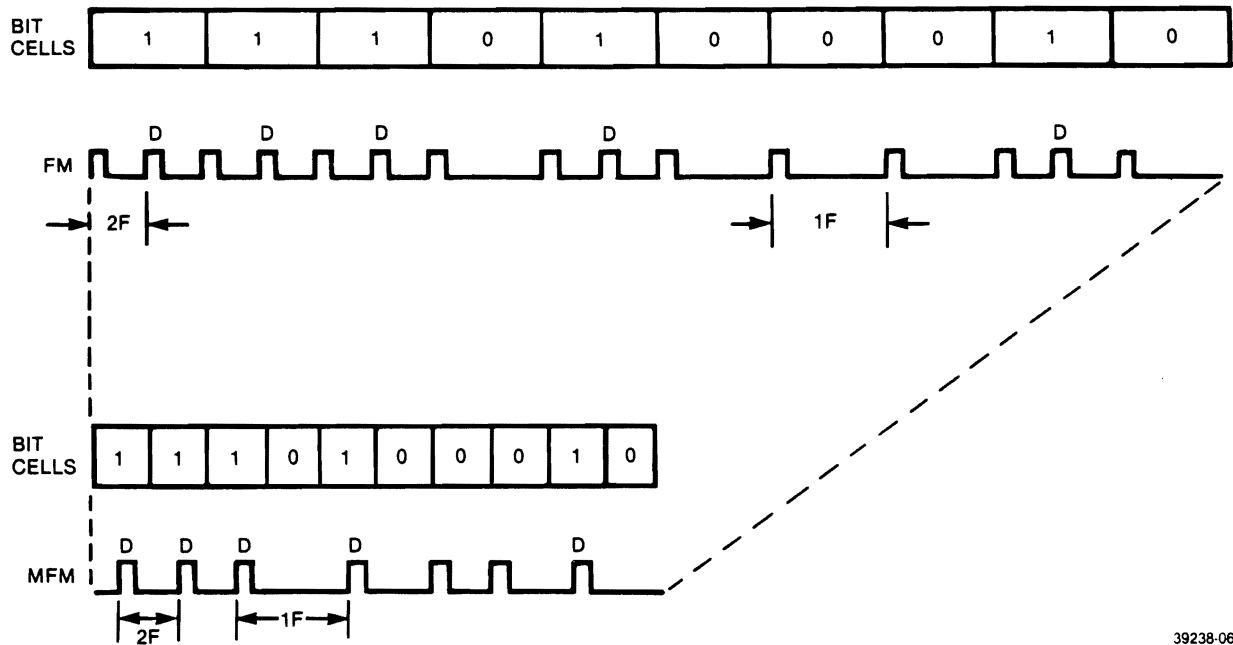


A = LEADING EDGE OF BIT MAY BE  $\pm 800$  ns FROM ITS NOMINAL POSITION  
 B = LEADING EDGE OF BIT MAY BE  $\pm 400$  ns FROM ITS NOMINAL POSITION

**FIGURE 1-6. READ DATA TIMNG (FM)**

The encoding scheme of the recorded data can be either FM or MFM. FM encoding rules specify a clock bit at the start of every bit cell and a data bit at the center of the bit cell if this cell contains a one data bit, (see figure 1-7). MFM encoding rules allow clock bits to be omitted from some bit cells with the following prerequisites:

- a. The clock bit is omitted from the current bit cell if either the preceding bit cell or the current bit cell contains a one data bit. See figure 1-7.
- b. In the above mentioned encoding schemes, clock bits are written at the start of their respective bits cells and data bits at the centers of their bit cells.



39238-06

FIGURE 1-7. FM AND MFM CODE COMPARISONS

#### 1.4.9 Write Operation

Writing data to the SA455/465 is accomplished by:

- a. Activating the DRIVE SELECT line.
- b. Selecting the head.
- c. Activating the WRITE GATE line.
- d. Pulsing the WRITE DATA line with the data to be written.

The timing relationships required to initiate a Write Data sequence are shown in figure 1-5. These timing specifications are required in order to guarantee that the position of the read/write heads has stabilized prior to writing.

The timing specifications for the write data pulses are shown in figure 1-8. Write data encoding can be FM or MFM. The write data should be precompensated 250 ns starting at track 22 (SA455) or track 40 (SA465) to counter the effects of bit shift. The direction of compensation required for any given bit in the data stream depends on the pattern it forms with nearby bits.

#### 1.4.10 Sequence of Events

The timing diagrams shown in figures 1-3, 1-4, 1-5, and 1-9 show the necessary sequence of events with associated timing restrictions for proper operation.

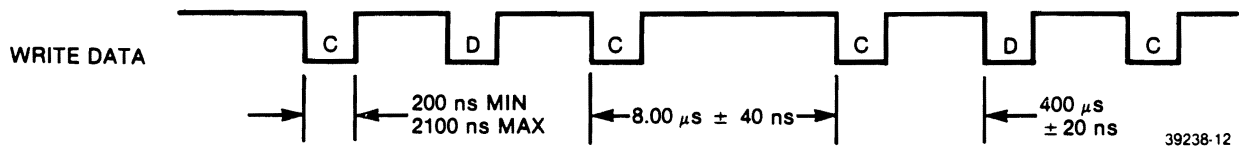


FIGURE 1-8. WRITE DATA TIMING (FM)

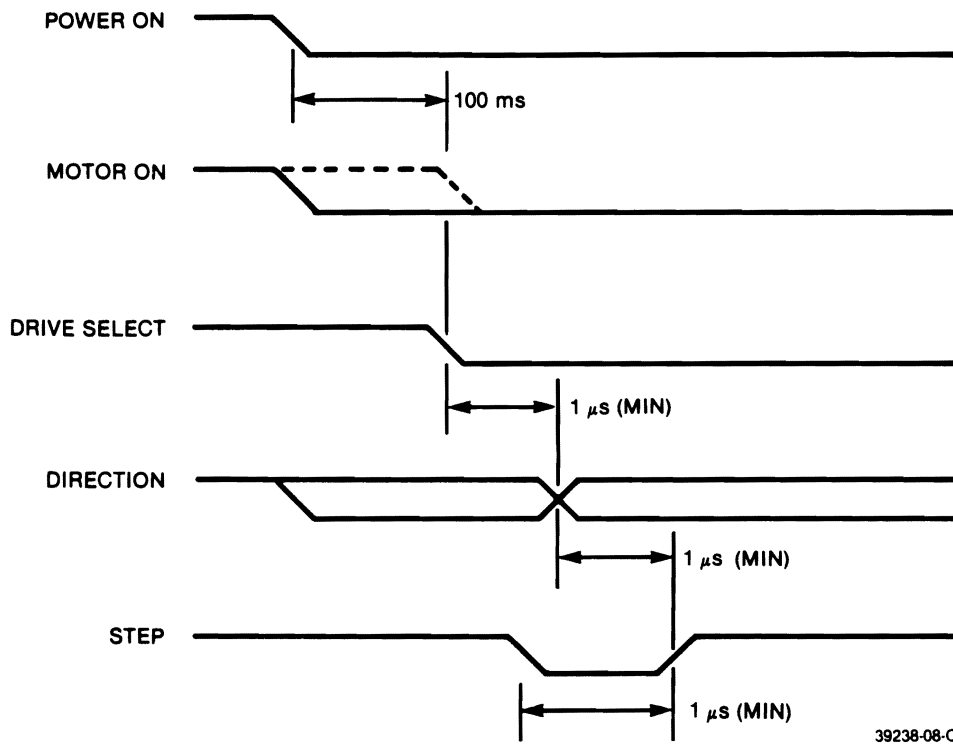


FIGURE 1-9. POWER ON TO STEP



## SECTION II ELECTRICAL INTERFACE

### 2.1 INTRODUCTION

The interface of the SA455/465 can be divided into two categories:

- a. Signal Lines
- b. Power Lines

The following sections provide the electrical definition for each line. See figure 2-1 for all interface connections.

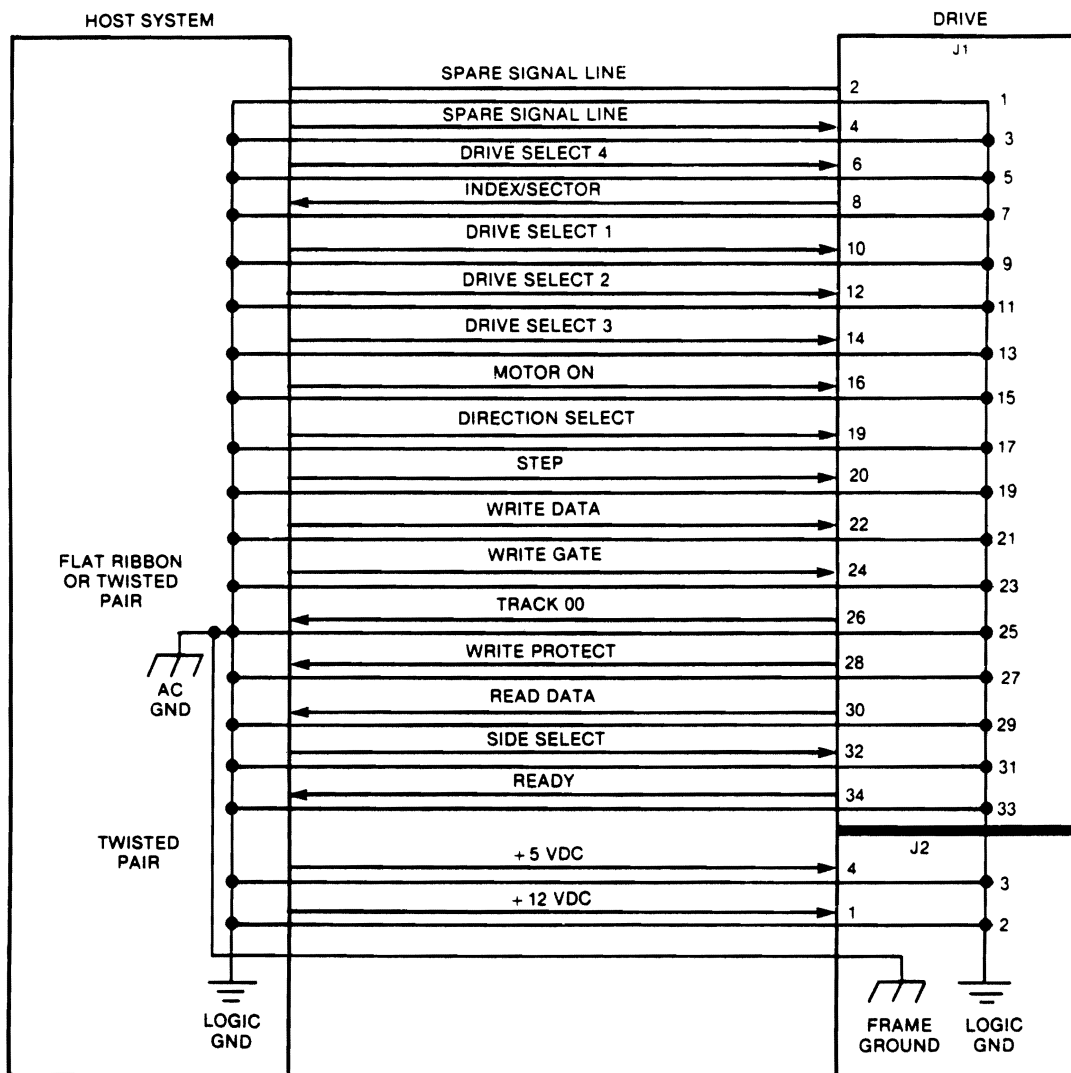


FIGURE 2-1. INTERFACE CONNECTIONS

39238-09-A

## 2.2 SIGNAL INTERFACE

The signal interface consists of two categories:

- a. Control Lines
- b. Data Transfer Lines

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

### 2.2.1 Input Lines

The input signals are of three types: those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing, and those signals which are not multiplexed and affect all the drives in a daisy chain system.

The input signals to be multiplexed are:

- a. DIRECTION SELECT
- b. STEP
- c. WRITE DATA
- d. WRITE GATE
- e. SIDE SELECT

The input signals which are intended to do the multiplexing are:

- a. DRIVE SELECT 1
- b. DRIVE SELECT 2
- c. DRIVE SELECT 3
- d. DRIVE SELECT 4

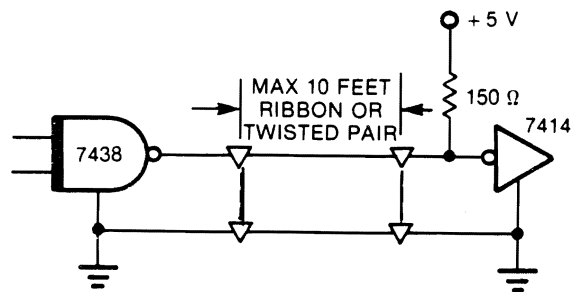
MOTOR ON is not multiplexed.

The input lines have the following electrical specifications. See figure 2-2 for the recommended circuit.

True = Logical zero =  $V_{in} \pm 0.0$  to  $+0.4$  V @  $I_{in} = 40$  mA (max)

False = Logical one =  $V_{in} + 2.5$  to  $+5.25$  V @  $I_{in} = 250$   $\mu$ A (open)

Input impedance = 150 ohms



39238-10

**FIGURE 2-2. INTERFACE SIGNAL DRIVER/RECEIVER**

### 2.2.2 Input Line Terminations

The SA455/465 has been provided with the capability of terminating the ten input lines listed below.

- |                   |                     |
|-------------------|---------------------|
| 1. DRIVE SELECT 1 | 6. DIRECTION SELECT |
| 2. DRIVE SELECT 2 | 7. STEP             |
| 3. DRIVE SELECT 3 | 8. WRITE DATA       |
| 4. DRIVE SELECT 4 | 9. WRITE GATE       |
| 5. MOTOR ON       | 10. SIDE SELECT     |

These lines are terminated through a 150 ohm resistor pack. In a single drive system, this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used. However, the user must provide the terminations beyond the last drive and each of the five lines must be terminated to +5 V dc through a 150 ohm, 1/4-watt resistor.

### 2.2.3 Drive Select 1 – 4

The SA455/465, as shipped from the factory, is configured to operate in a single drive system. The SA455/465 can be easily modified by the user to operate with other drives in a multiplexed multiple-drive system.

In a multiple drive system, the four input lines (DRIVE SELECT 1 through DRIVE SELECT 4) are provided so that the using system may select which drive on the interface is to be used. In this mode of operation, only the drive with its DRIVE SELECT line active will respond to the input lines and gate the output lines.

### 2.2.4 Motor On

This input, when activated to a logical zero level, will turn on the drive motor allowing reading or writing on the drive. A 500 ms delay after activating this line must be allowed before reading or writing. This line should be deactivated, for maximum motor life, if no commands have been issued to the drives within 2 seconds (10 revolutions of the media) after completion of a previous command.

### 2.2.5 Direction Select

This interface line defines the direction of motion the read/write heads will take when the STEP line is pulsed. An open circuit or logical one defines the direction as out. If a pulse is applied to the STEP line, the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as in. If a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

### 2.2.6 Step

This interface line is a control signal which causes the read/write heads to move in the direction of motion defined by the DIRECTION SELECT line. This signal must be a logical low going pulse with a minimum pulse width of 1  $\mu$ s and then logically high for 5 ms minimum between adjacent pulses. Each subsequent pulse must be delayed by 6 ms (SA455) minimum or 3 ms (SA465) minimum from the preceding pulse.

The access motion is initiated on each logical zero to logical one transition, or at the trailing edge of the signal pulse. Any change in the DIRECTION SELECT line must be made at least 1  $\mu$ s before the trailing edge of the STEP pulse. The DIRECTION SELECT logic level must be maintained 1  $\mu$ s after the trailing edge of STEP pulse. See figure 2-3 for these timings.

### 2.2.7 Write Gate

The active state of this signal, or logical zero, enables write data to be written on the diskette. The inactive state or logical one, enables the read data logic and stepper logic. See figure 2-4 for timings.

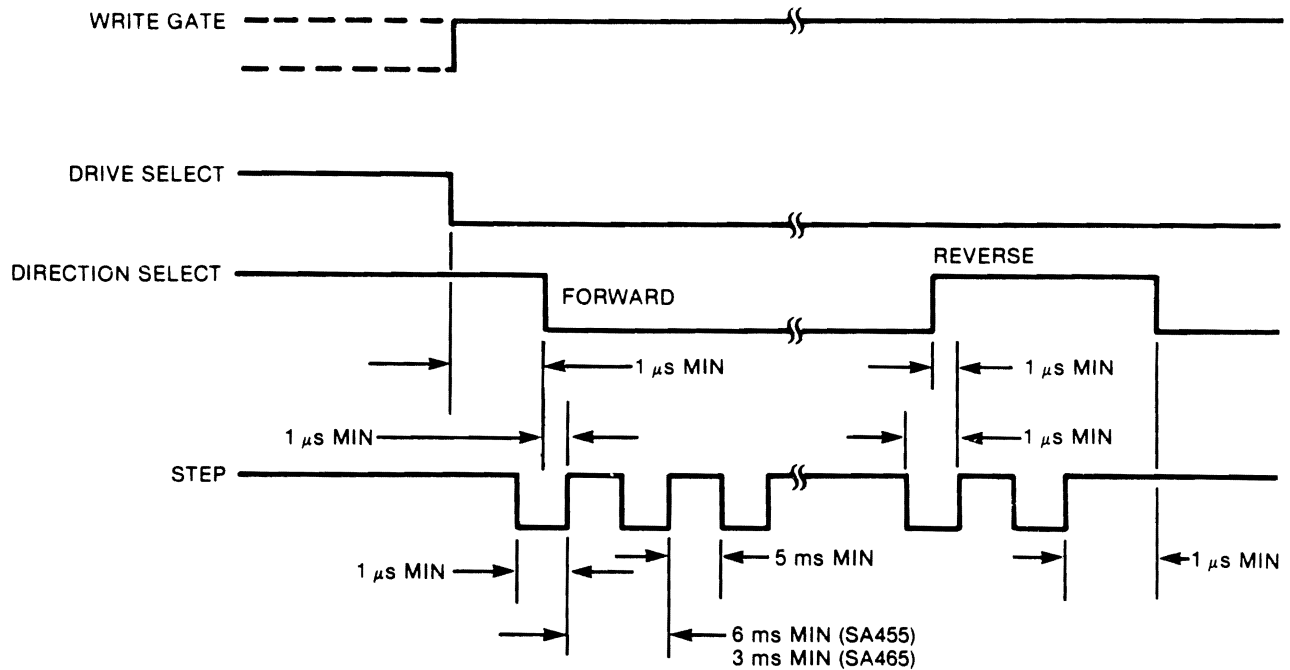


FIGURE 2-3. STEP TIMING

39238-11-A

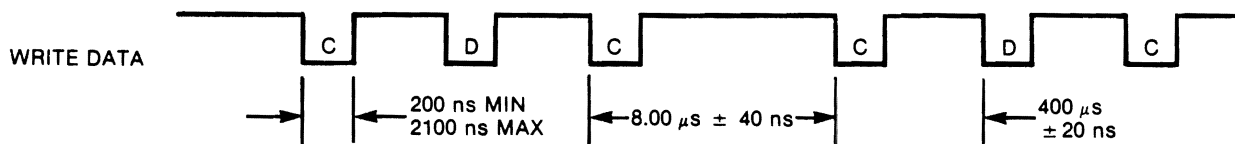


FIGURE 2-4. WRITE DATA TIMING

39238-12

### 2.2.8 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one to a logical zero level, will cause the current through the read/write heads to be reversed thereby writing a data bit. This line is enabled by WRITE GATE being active. Write data must be inactive during a read operation. A write data clamp is provided on the PCB at the interface which holds the WRITE DATA line at a logical zero whenever WRITE GATE is inactive. See figure 2-4 for timings.

### 2.2.9 Side Select

This signal defines which side of a two-sided diskette is to be written on or read from. A logical one selects the side 0 head. When switching from one side to the other, a 100 μs delay is required before a read or write operation can be initiated.

### 2.2.10 Output Lines

The output control lines have the following electrical specifications.

True = Logical zero = +0.0 to +0.4 V @ I<sub>out</sub> = 40 mA (max)

False = Logical one = +5 to +2.5 V (open collector) @ I<sub>out</sub> = 250 μA (max)

### 2.2.11 Track 00

The active or logical zero state of this interface signal indicates when the read/write heads are positioned at track zero (the outermost track) and the access circuitry is driving current through phase A of the stepper motor. This signal is at a logical one level, or inactive state, when the read/write heads are not at track zero. When the read/write heads are at track zero and an additional step out pulse is issued to the drive, a mechanical stop will keep the read/write heads at track zero. However, the TRACK 00 signal will go inactive. This is because the stepper motor will go to phase C and not phase A. One more step out pulse will put the stepper motor back into phase A and the TRACK 00 signal will go active again.

### 2.2.12 Index/Sector

This interface signal is provided by the drive each time an index or sector hole is sensed at the Index/Sector photo detector. Normally, this signal is at a logical one level and makes the transition to the logical zero level each time a hole is sensed.

When using SA154/164 media (soft sector), there will be one pulse on this interface signal per revolution of the diskette (200 ms). This pulse indicates the physical beginning of a track. See figure 2-5 for the timing.

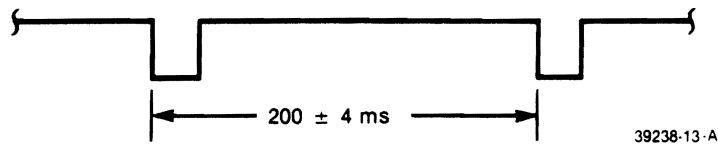


FIGURE 2-5. INDEX TIMING (SA154/164 MEDIA)

When using SA155/165 or SA157/167 media (hard sector), there will be 17 or 11 pulses on this interface line per revolution (200 ms). To indicate the beginning of a track, once per revolution there is one index transition between 16 or 10 equally spaced sector transitions. The timing for these signals is shown in figures 2-6 and 2-7.

When using the Index/Sector signal, look for an edge or transition rather than a level for determining the status. With no diskette inserted, this signal remains active or at a logical zero level which is an erroneous status.

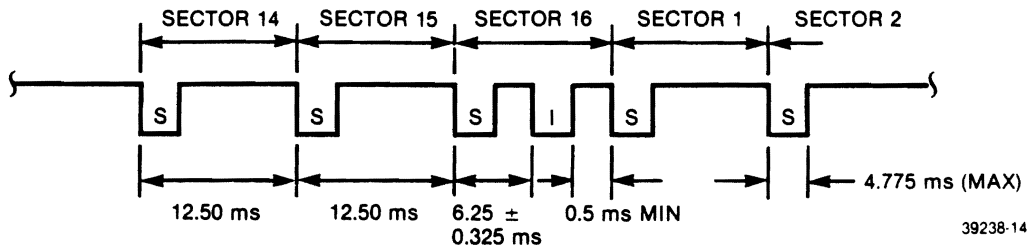


FIGURE 2-6. INDEX/SECTOR TIMING (SA155/165 MEDIA)

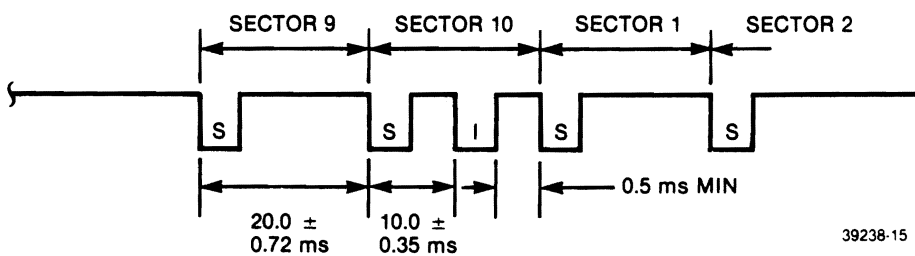


FIGURE 2-7. INDEX/SECTOR TIMING (SA157/167 MEDIA)

### 2.2.13 Read Data

This interface line provides the raw data (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figure 1-5 for the timing and bit shift tolerance within normal media variations.

### 2.2.14 Write Protect

This interface signal is provided by the drive to give the user an indication when a write protected diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

### 2.2.15 Ready

READY informs the controller that a diskette is properly inserted and that the drive motor is up to speed. 500 ms is required for starting the motor and an additional 200 ms is required for one revolution at the rated speed. Thus, READY is available 700 ms after power is applied to the motor. The SA455/465 generates READY by sensing index pulses and measuring their frequency of occurrence. When the index pulses are 200 ms apart, READY becomes active.

## 2.3 POWER INTERFACE

The SA455/465 requires only dc power for operation. DC power to the drive is provided via P2/J2. The two dc voltages, their specifications, and their P2/J2 pin designators are outlined in table 2-1. The specifications outlined on current requirements are for one drive. For multiple drive systems, the current requirements are a multiple of the maximum current times the number of drives in the system.

TABLE 2-1. DC POWER REQUIREMENTS

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+ 12 VDC	± 1.2 VDC	1.2 A MAX 0.6 A TYP	50 mV MAX ALLOWABLE
2	+ 12 RETURN			
3	+ 5 RETURN			
4	+ 5 VDC	± 0.25 VDC	0.9 A MAX 0.6 A TYP	50 mV MAX ALLOWABLE

39238-17-A

### 2.4 FRAME GROUND

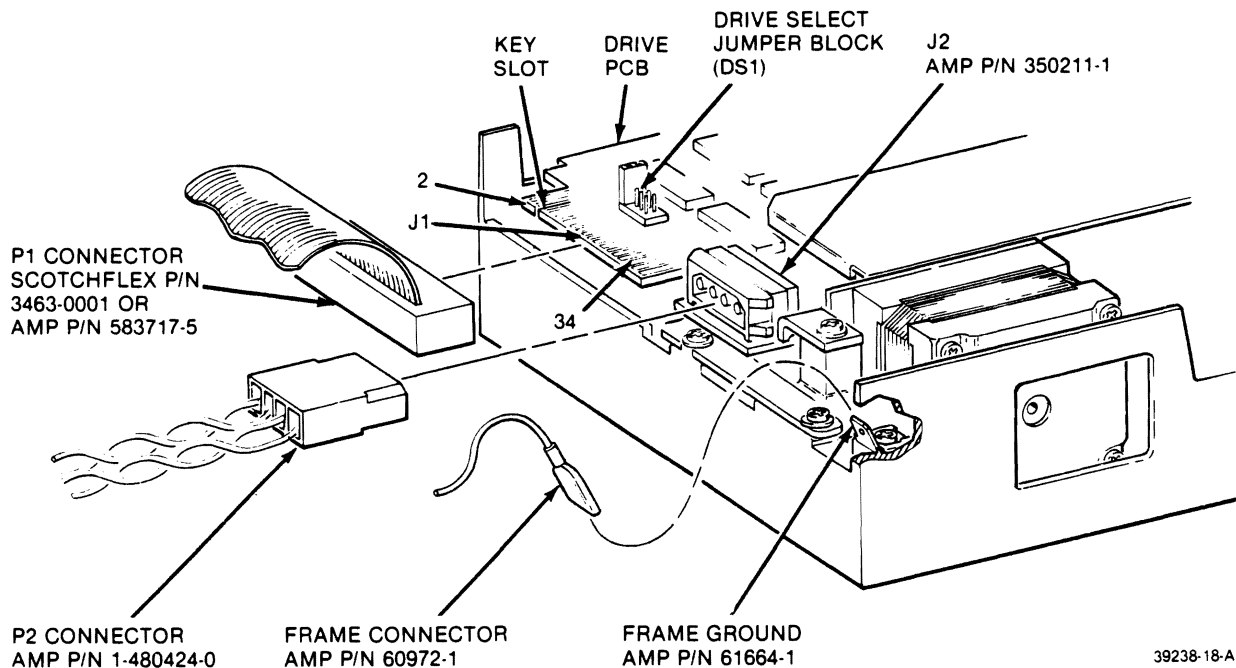
It is important that the drive be frame grounded to the host system ac ground or frame ground. Failure to do so may result in drive noise susceptibility.

## SECTION III PHYSICAL INTERFACE

### 3.1 INTRODUCTION

The electrical interface between the SA455/465 and the host system is via two connectors. The first connector, J1, provides the signal interface. The second connector, J2, provides the dc power.

This section describes the physical connectors used on the drive and recommended connectors to be used with them. See figure 3-1 for connector locations.



**FIGURE 3-1. INTERFACE CONNECTORS PHYSICAL LOCATIONS**

#### 3.1.1 J1/P1 Connector

Connection to J1 is through a 34 pin PCB edge connector. The dimensions for this connector are shown in figure 3-2. The pins are numbered 1 through 34 with the even numbered pins on the component side of the PCB. The odd numbered pins are on the non-component side. Pin 2 is located on the end of the PCB connector closest to the corner and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

#### 3.1.2 J2/P2 Connector

The dc power connector, J2, is a 4 pin AMP Mate-N-Lok connector (P/N 350211-1). The recommended mating connector, P2, is AMP P/N 1-480424-0 using AMP pins P/N 61473-1. J2, pin 1, is labeled on the component side of the PCB. Wire used should be #18 AWG. Figure 3-3 illustrates the J2 connector as seen on the drive PCB from the non-component side.

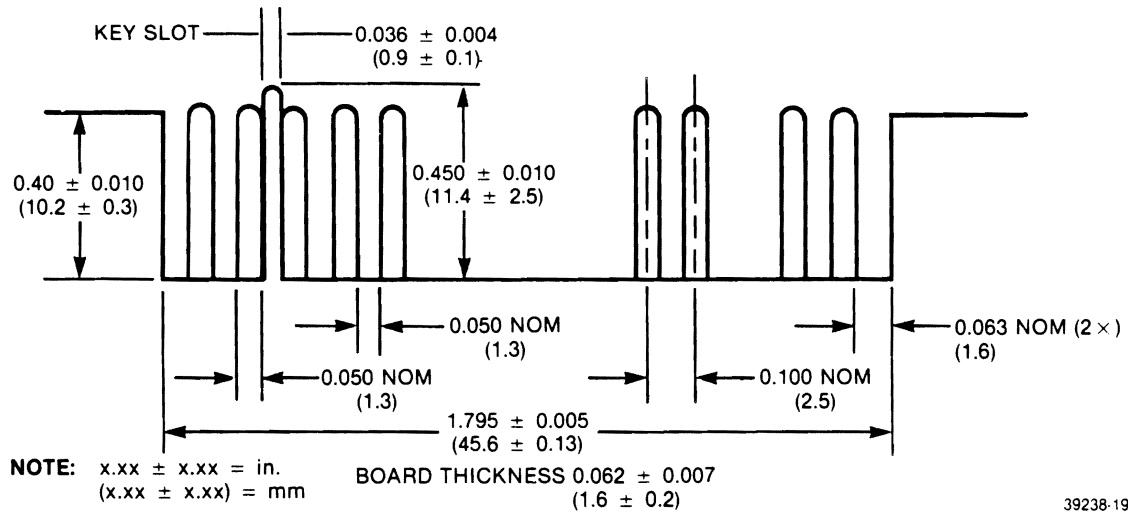


FIGURE 3-2. J1 CONNECTOR DIMENSIONS

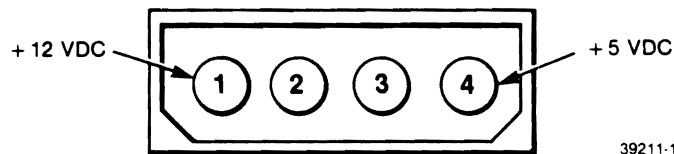


FIGURE 3-3. J2 CONNECTOR

### 3.2 FRAME GROUNDING

#### CAUTION

The SA455/465 must be frame grounded to the host system to ensure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good ac ground, a wire from the system ac frame ground must be connected to the SA455/465. For this purpose, a faston tab is provided on the drive near the motor control PCB where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.



## SECTION IV THEORY OF OPERATION

### 4.1 THEORY OF OPERATION

The SA455/465 floppy diskette drive electronics are packaged on one PCB which contains:

- a. Read/Write Amplifier and Transition Detector
- b. Spindle Motor Control
- c. Drive Select Circuits
- d. Index Detector Circuits
- e. Track Zero Circuits
- f. Track Accessing Circuits
- g. Power On Reset Control
- h. Write Protect Circuits
- i. Drive Status Circuits

The head positioning actuator moves the read/write head(s) to the desired track on the diskette. The head(s) is loaded onto the diskette when the door is closed.

The following paragraphs describe each of the above functions in detail.

### 4.2 READ/WRITE OPERATIONS

- a. The SA455/465 uses the double frequency non return to zero (NRZ) recording method.
- b. The read/write head, in general, is a ring with a gap and a coil wound at some point on the ring.
- c. During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil.
- d. During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface.

The SA455/465 drives use the double-frequency (2F) longitudinal NRZ method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, is provided by the using system. See figure 4-1.

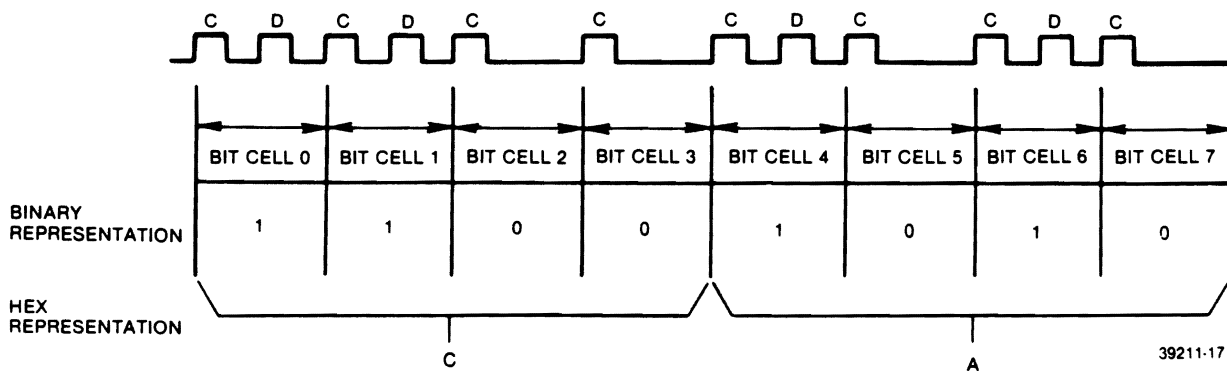


FIGURE 4-1. BYTE

The read/write head is a ring with a gap and a coil wound some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a longitudinal direction. See figure 4-2.

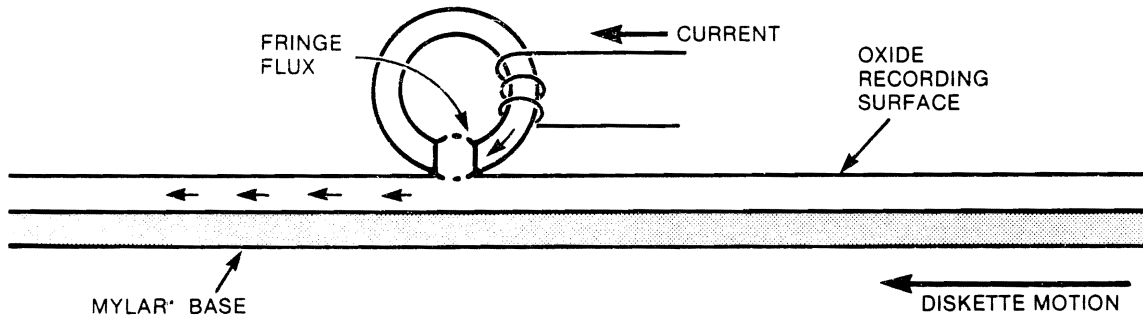


FIGURE 4-2. BASIC READ/WRITE HEAD

39211-18

The drive writes two frequencies: 1F 62.5 k Hz and 2F 125 k Hz. During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized one direction while the portion under the gap is magnetized in the opposite direction. This flux reversal represents a bit. See figure 4-3.

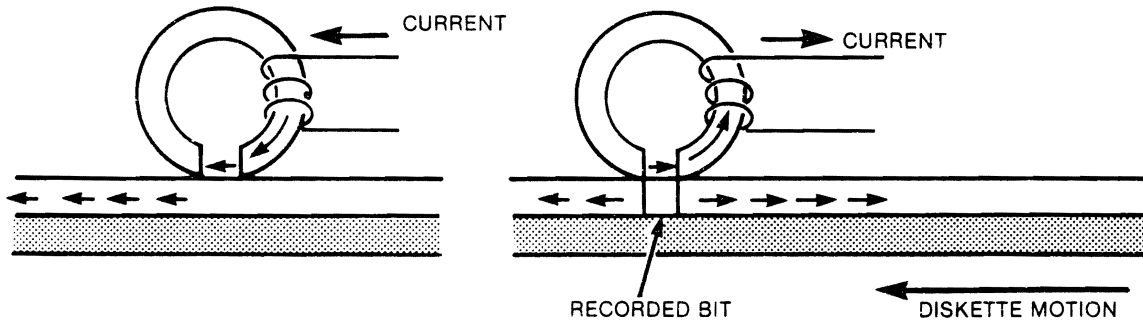


FIGURE 4-3. RECORDED BIT

39211-19

During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface. The gap first passes over an area that is magnetized in one direction and a constant flux flows through the ring and coil. The coil registers no output voltage at this point. When a recorded bit passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See figure 4-4.

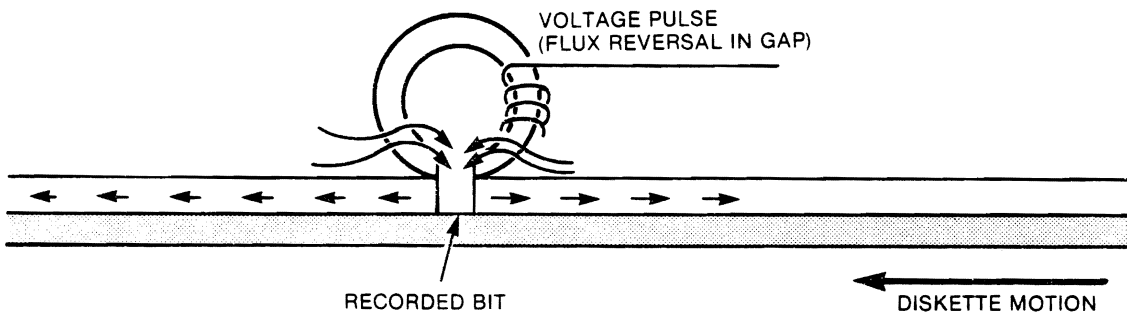
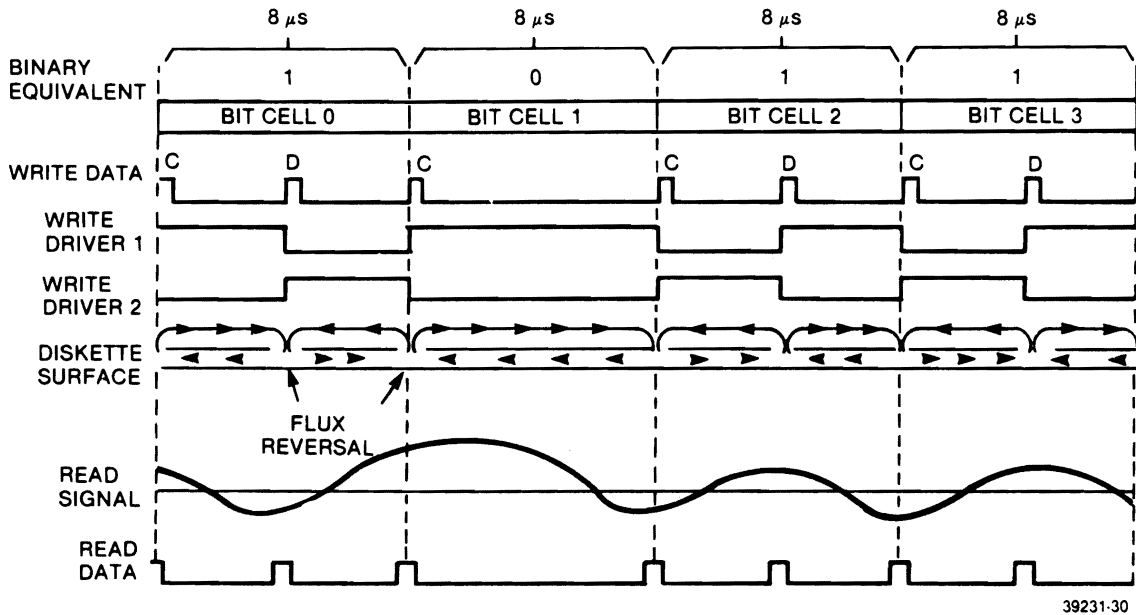


FIGURE 4-4. READING A BIT

39211-20

These flux reversals produce an FM waveform which transmits data to and from the diskette. See figure 4-5.

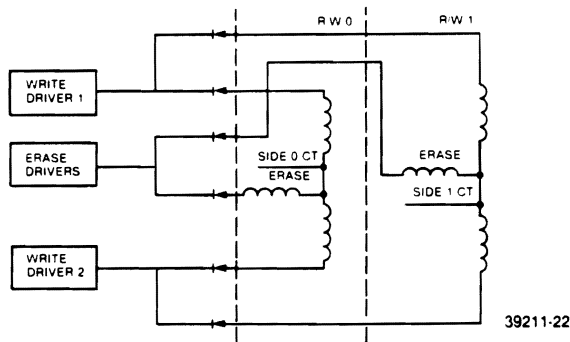


**FIGURE 4-5. 1F AND 2F RECORDING FLUX AND PULSE RELATIONSHIP**

### 4.3 READ/WRITE HEAD

- The ceramic read/write heads each contain three coils.
- When writing, the head erases the outer edges of the track to ensure that the data recorded will not exceed the 0.012 in. (SA455) or 0.006 (SA465) track width.

The read/write head contains three coils. Two read/write coils are wound on a single core, center tapped, and one erase coil is wound on a yoke that spans the track being written. The read/write and erase coils are connected as shown in figure 4-6.



**FIGURE 4-6. READ/WRITE HEADS**

During a write operation, the erase coil is energized. This causes the outer edges of the track to be trim erased so that the track being recorded will not exceed the 0.012 in. (SA455) or 0.006 in. (SA465) track width. Tunnel erasing allows for minor deviations in read/write head current so as one track is recorded, it will not "splash over" to adjacent tracks.

Each bit written will be directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. This will cause a change in the flux pattern for each bit. The current through either of the read/write coils will cause the old data to be erased as new data is recorded.

During a read operation, the direction of flux changes on the diskette surface as it passes under the gap and current is induced into one of the windings of the read/write head. This results in a voltage output pulse. When the next data bit passes under the gap, another flux change takes place in the recording surface. This causes current to be induced in the other coil, producing another voltage output pulse of the opposite polarity.

#### 4.4 WRITE CIRCUIT OPERATION

- The write data trigger flips with each pulse on the WRITE DATA line.
- The write data trigger alternately drives one or the other of the write drivers.
- WRITE GATE allows write current to flow to the write driver circuits if the diskette is not write protected.
- Write current sensed allows erase coil current.
- Heads are selected by grounding the appropriate center tap.

WRITE DATA pulses (clock and data bits) are supplied by the using system. The write trigger "flips" with each pulse. The outputs are fed to alternate write drivers.

WRITE GATE and NOT WRITE PROTECT are ANDed together and will cause write current to flow to the write driver circuits, which in turn causes the center tap switch to close and erase current to flow after the turn on delay of 400  $\mu$ sec.

The output of one of the write drivers allows write current to flow through one half of the read/write coil. When the write trigger "flips," the other write driver provides write current to the other half of the read/write coil.

The removal of WRITE GATE causes the turn off delay circuit to time out for 1.1 ms. At the end of the delay, the center tap switch opens and the erase current source is turned off. See figure 4-7.

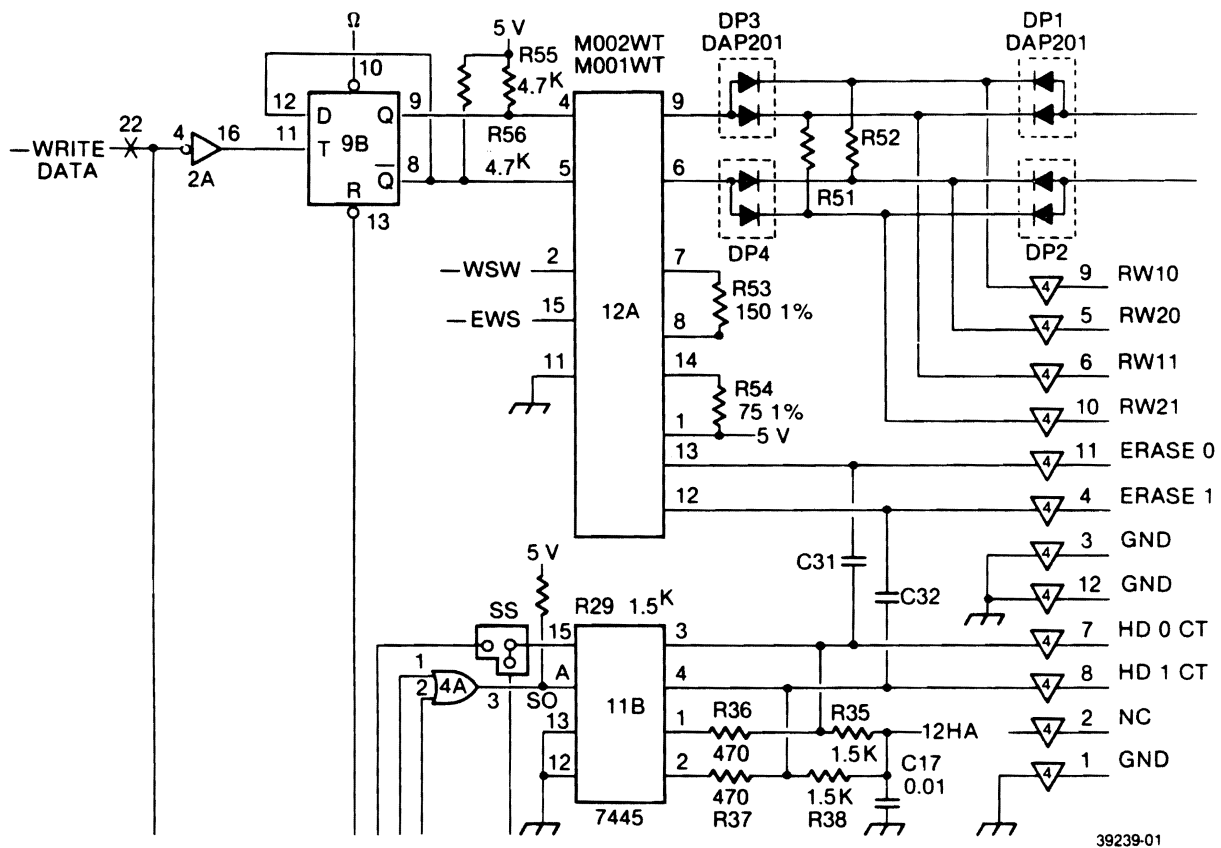


FIGURE 4-7. WRITE CIRCUIT

## 4.5 READ CIRCUIT OPERATION

- a. Duration of all read operations is under control of the using system.
- b. As long as the drive is selected and WRITE GATE is not active, the read signal is amplified and shaped and the square wave signals are sent to the interface as READ DATA.

When the using system requires data from the diskette drive, the using system must select the head and disable WRITE GATE. The read signal is then fed to the amplifier section of the read circuit. After amplification, the read signal is fed to a filter where the out of band noise is removed. The read signal is then fed to the differentiator amplifier.

Since a clock pulse occurs at least once every  $8 \mu\text{s}$  and data bits are present once every  $4 \mu\text{s}$ , the frequency of the READ DATA varies (FM encoding only). The read signal amplitude decreases as the frequency increases. Note the signals in figure 4-8. The differential amplifier will amplify, differentiate, limit, and digitize the read signals (sine waves).

The drive has no data separator, only a pulse standardizer for the READ DATA signal.

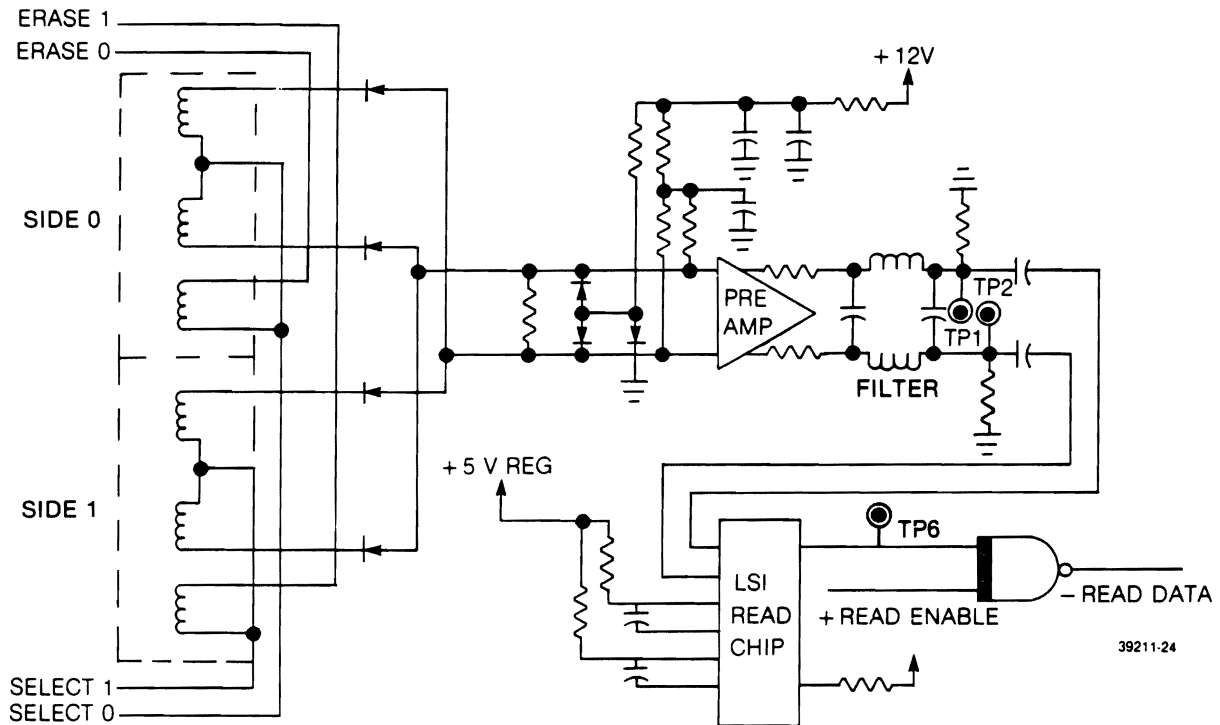


FIGURE 4-8. READ CIRCUIT

## 4.6 DRIVE MOTOR CONTROL

- a. Start/Stop
- b. Speed Control
- c. Over Current Protection
- d. Speed Adjustment

The motor used in the SA455/465 is a dc drive motor with a separate motor on and off interface line. After activating the MOTOR ON line, a 500 ms delay must be introduced to allow proper motor speed before reading or writing.

When MOTOR ON is activated at pin 16 of the interface, the mode will start by means of current flow through the motor windings. The motor speed control utilizes an integral brushless tachometer. The output voltage signal from this tachometer is compared to a voltage/frequency reference level. The output from the voltage/frequency comparator will control the necessary current to maintain a constant motor speed of 300 rpm. Motor speed adjustment changes the voltage reference through a potentiometer.

## 4.7 INDEX DETECTOR

Each time an index or sector hole is moved past the index photo detector, a pulse is formed. This pulse is present on the interface as index/sector pin 8. Without a diskette in the drive, the output line will be low and the using system must look for a transition to be a valid signal. The detector output is fed into a schmidt trigger with a level trigger latch back to maintain pulse stability while shaping the pulse. With output enable true, this pulse will be on the interface as a negative going pulse. See figure 4-9.

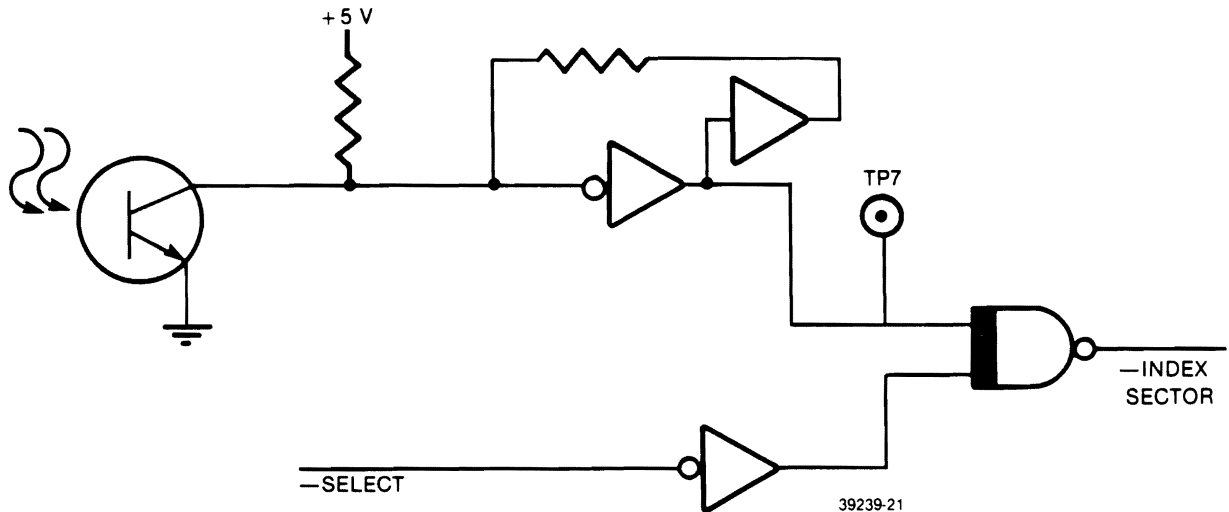


FIGURE 4-9. INDEX DETECTOR

## 4.8 TRACK ZERO INDICATION

Track 00 signal (pin 26) is provided to the using system to indicate when the read/write head is positioned on track 00. The track 00 indication is provided when the flag attached to the head carriage passes between the photo transistor and the photo detector. On track, DRIVE SELECT is ANDed with the photo detector output. These conditions will cause a track 00 indication to the interface.

## 4.9 TRACK ACCESSING

- Stepper Motor (Four Phase)
- Stepper Control Logic
- Reverse Seek
- Forward Seek

Seeking the read/write head from one track to another is accomplished by selecting the desired direction utilizing the DIRECTION SELECT interface line, loading the read/write head, and pulsing the STEP line. Multiple track accessing is accomplished by repeated pulsing of the STEP line with WRITE GATE inactive until the desired track has been reached. Each pulse on the STEP line will cause the read/write head to move one track either in or out, depending on the DIRECTION SELECT line.

### 4.9.1 Stepper Motor

The four phase stepper motor turns the head actuator cam in two step increments per track for the 455 and one step increments for the 465. The band actuator and capstan move the heads track to track.

Two current modes are automatically enabled. The first step pulse will enable full current to the stepper motor. Within 35 ms after that last step pulse is issued, stepper motor current is automatically decreased to approximately 50% of its full value.

### 4.9.2 Stepper Control

During power on reset time, the stepper control counter is reset to zero. This causes phases -B and -A to be energized in the stepper. Figures 4-10 and 4-11 show the stepper control logic and timing.

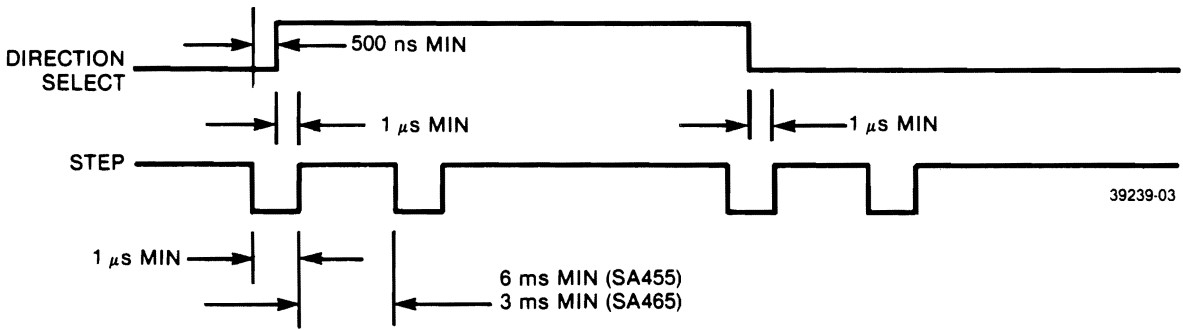


FIGURE 4-10. STEPPER TIMING

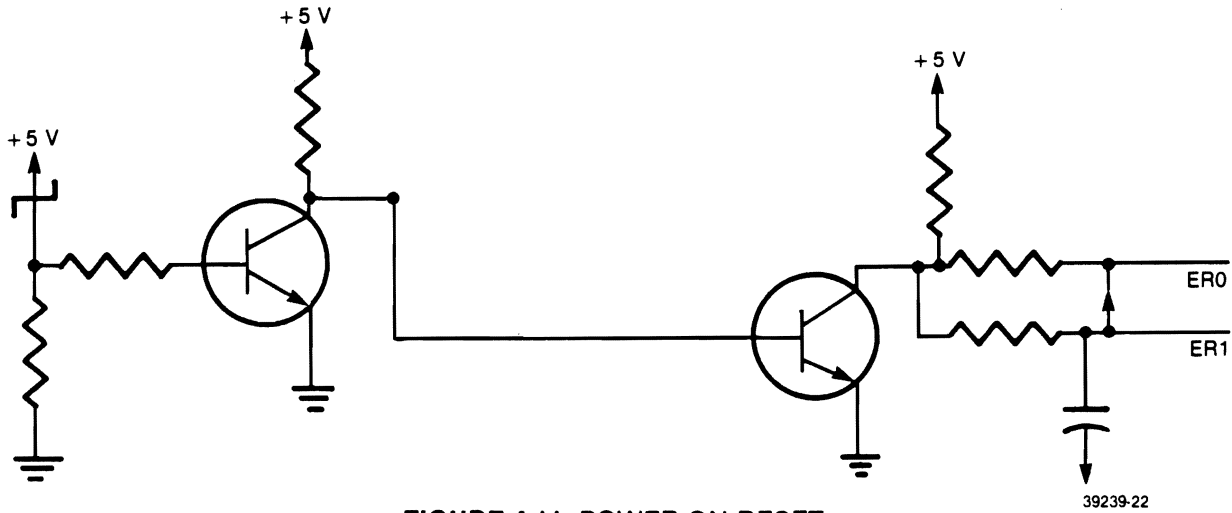


FIGURE 4-11. POWER ON RESET

#### 4.10 DRIVE SELECT

The SA455/465 is configured to operate alone in a single drive system. It can be easily modified to operate with other drives in a daisy chained multiplexed drive system. This is done by selecting the specific drive address and jumpering the appropriate DRIVE SELECT line. See figure 4-12.

The "MX" option is used for single drive systems. By shorting "MX," the I/O lines are always enabled.

The "MS" option allows the motor to be enabled from DRIVE SELECT.

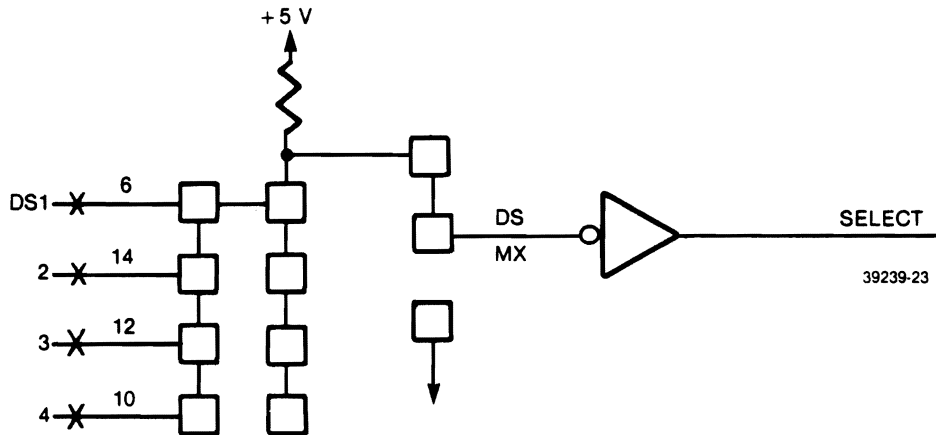


FIGURE 4-12. DRIVE SELECT

#### 4.11 WRITE PROTECT

This interface signal is provided by the drive to indicate to the user when a write protected diskette is installed. The signal is logical 0 level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface. If the "WP" trace is cut, writing to the diskette is inhibited unless a write protect label is installed over the notch. See figure 4-13.

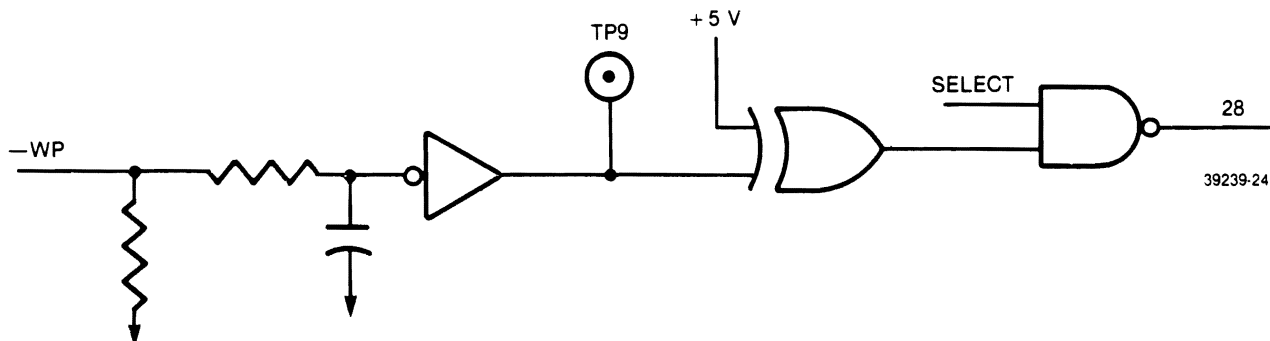


FIGURE 4-13. WRITE PROTECT

#### 4.12 READY

This interface signal gives the user an indication that a diskette is inserted correctly in the drive and the door is closed. The READY signal is active, at a logical 0 level, when all of the following conditions are met:

- a. The door is closed.
- b. The door has not been opened since the drive was last deselected and timed out 500 ms.
- c. Two INDEX/SECTOR pulses have been sensed since the previous conditions were met.

If the READY signal is inactive, the user may deselect and then select the drive to test READY again; if the door had previously been disturbed but is now closed, READY will activate upon sensing an INDEX/SECTOR pulse.



## SECTION V MAINTENANCE

### 5.1 MAINTENANCE EQUIPMENT

#### 5.1.1 Alignment Diskette

The alignment diskette is used for verifying and adjusting the SA455/465. Two alignment diskettes are available. The SA455/465 has two read/write heads and requires written information on both surfaces. The SA128 (48 tpi) alignment diskette should be used when performing service checks on the SA455. The SA465 requires the SA126 (96 tpi) alignment diskette.

The following adjustments and checks can be made using the SA128/126 alignment diskettes.

	<b>SA455-SA128</b>	<b>SA465-SA126</b>
a. Read/Write Head Radial Alignment	TRK 33	TRK 64
b. Index Photo Detector Alignment	Set at TRK 38 Verified at TRK 01	Set at TRK 76 Verified at TRK 02
c. Track 00 Head Position	TRK 00	TRK 00
d. Azimuth Angle (not field adjustable)	TRK 33	TRK 64
e. 125 k Hz Signal Recorded to Check Head Position on Inside Track	TRK 34	TRK 79

Caution should be used not to destroy prerecorded alignment tracks. The write protect tab must be installed to prevent accidental writing on the alignment diskette. If the write protect option is used, remove the write protect tab.

#### 5.1.2 Exerciser PCB

The exerciser PCB can be used in a stand alone mode, built into a test station, or used in a test for field service.

The exerciser will enable the user to make all adjustments and check outs required on the SA455/465 minidiskette drive. It has no intelligent data handling capabilities but can write a 2F 125 k Hz signal which is the recording frequency used for amplitude checks on the SA455/465 drive. The exerciser can start and stop the drive motor, and enable read in the SA455/465 to allow checking for proper read back signals.

### 5.1.3 Special Tools

The following special tools are available for performing maintenance on the SA455/465.

Description	Part Number
SA128 Alignment Diskette	54573
SA126 Alignment Diskette	54382
Exerciser PCB	54157
Head Cable Extender	54578
Phillips Screw Drivers	Medium and Small
Oscilloscope	Textronix 465 or equivalent

## 5.2 DIAGNOSTIC TECHNIQUES

### 5.2.1 Introduction

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment. Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

### 5.2.2 "Soft Error" Detection and Correction

Soft errors are usually caused by:

- Airborne contaminants that pass between read/write heads and disk. Usually these contaminants can be removed by cartridge self-cleaning wiper.
- Random electrical noise that usually lasts for a few microseconds.
- Small defects in written data and/or track not detected during write operation may cause soft errors during read.
- Improper grounding of power supply, drive, and/or host system. Refer to SA455/465 OEM manual (P/N 39238) for proper grounding requirements.
- Improper motor speed.

The following procedures are recommended to recover from the above mentioned soft errors:

- Reread track 10 times or until such time as data is recovered.
- If data is not recovered after using step (a), access head to adjacent track in same direction previously moved, then return to desired track.
- Repeat step (a).
- If data is not recovered, error is not recoverable.

### 5.2.3 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and check operation must be done. If the write operation is not successful after 10 attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error persists, the diskette should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

### 5.2.4 Read Error

Most errors that occur will be "soft errors." In these cases, performing an error recovery procedure will recover the data.

### 5.2.5 Seek Error

- a. Stepper malfunction.
- b. Carriage binds.
- c. To recover from a seek error, recalibrate to track 00 and perform another seek to the original track or do a read ID to find on which track the head is located.

## 5.3 TROUBLE-SHOOTING

Figures 5-1 through 5-5 provide trouble-shooting procedures for the SA455/465.

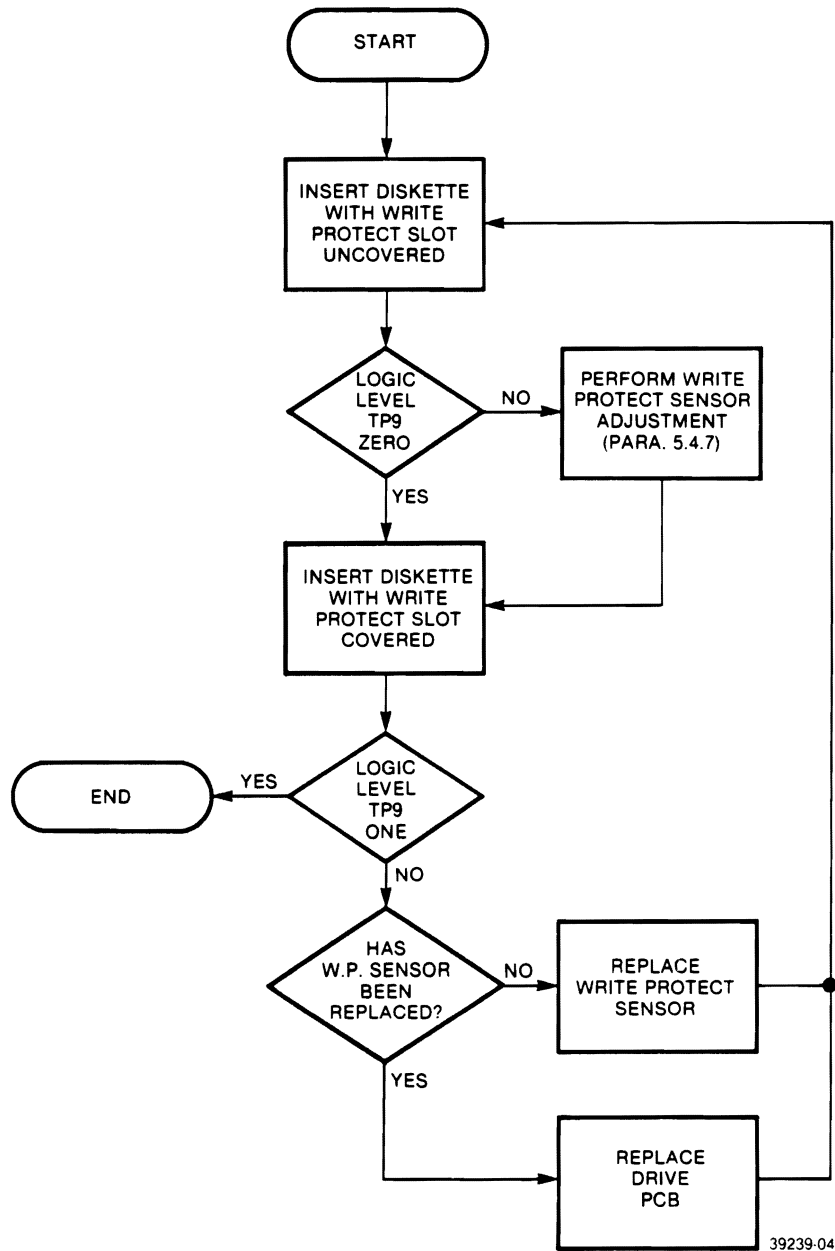
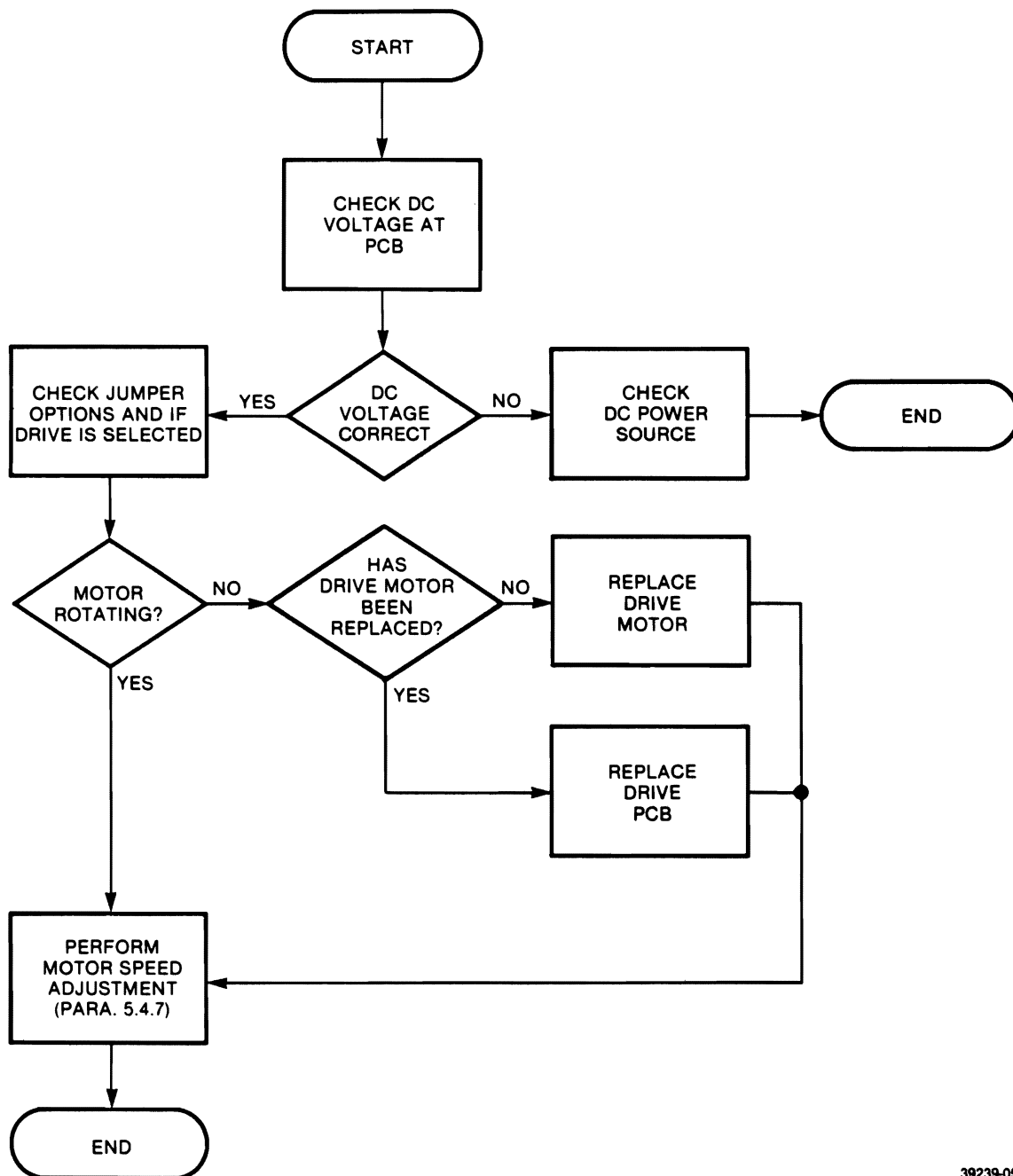
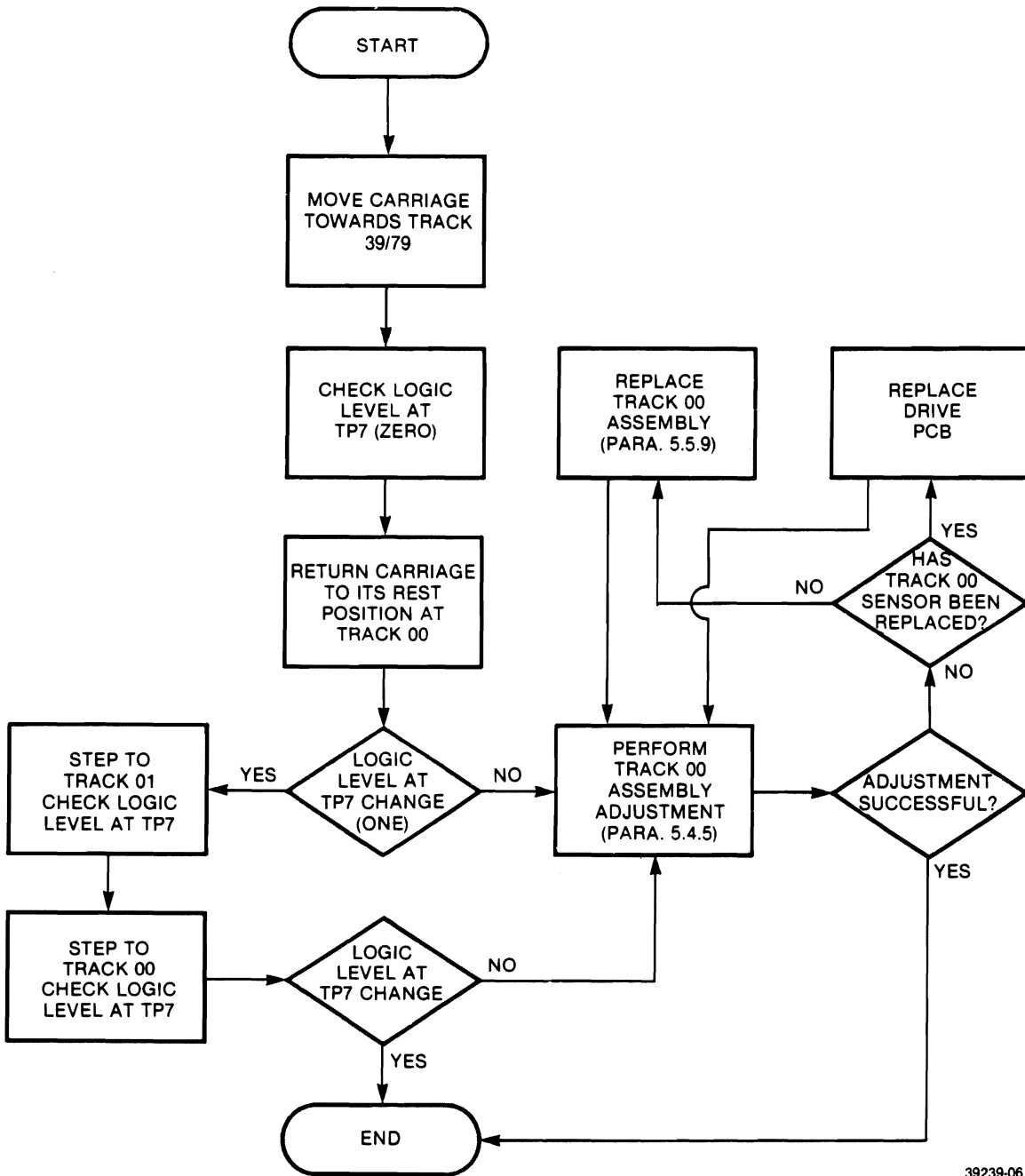


FIGURE 5-1. WRITE PROTECT INOPERATIVE



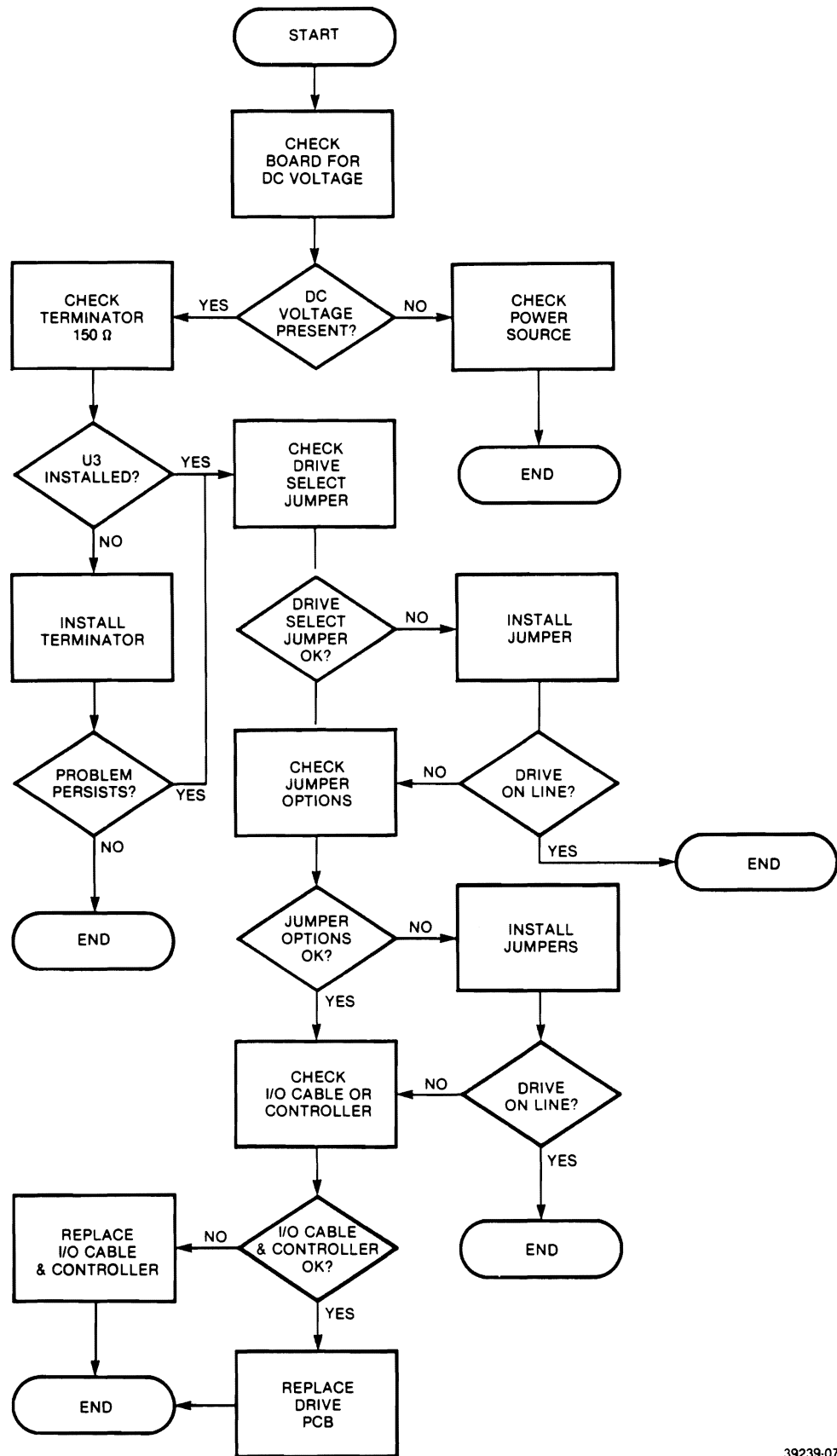
39239-05

FIGURE 5-2. DISKETTE NOT ROTATING



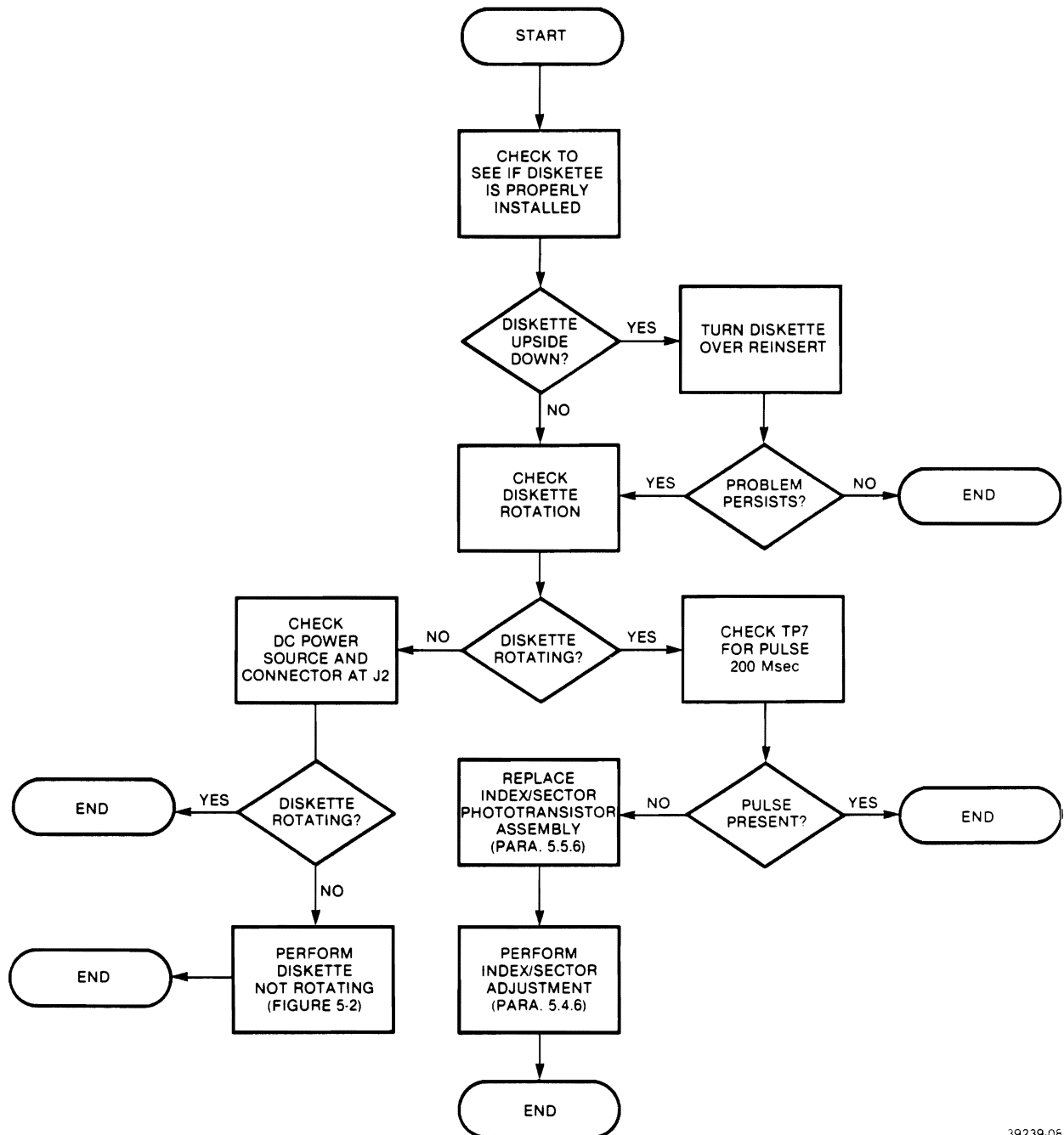
39239-06

FIGURE 5-3. TRACK 00 INDICATOR INOPERATIVE



39239-07

FIGURE 5-4. DRIVE NOT COMING ON LINE



39239-06

**FIGURE 5-5. INDEX PULSE INOPERATIVE**

## 5.4 ADJUSTMENTS

### 5.4.1 Head Radial Alignment

#### NOTE

The SA465 read/write head assembly is aligned at factory and adjustment of head to head alignment is not field adjustable.

- a. Insert alignment diskette (SA455 = SA128) (SA465 = 126).

#### NOTE

Alignment diskette should be at room conditions for at least 24 hours before alignment checks.

- b. Select drive and step head(s) to track 16 (SA455) or track 64 (SA465).
- c. Sync oscilloscope external negative on TP7 (—INDEX). Set time base to 20 msec per division. This will display over one revolution.
- d. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set inputs to ac, ADD, and invert one channel. Set vertical deflection to 50 mV/division.
- e. Amplitude of two lobes must be within 70% of each other (80% for 465). If lobes do not fall within specification, continue on with procedure (see figure 5-6).

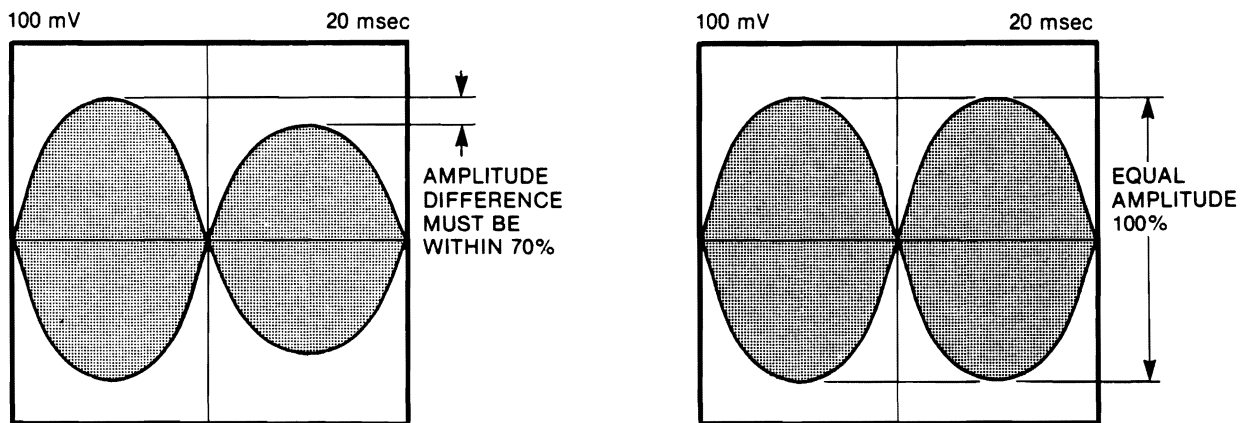


FIGURE 5-6. ALIGNMENT LOBES

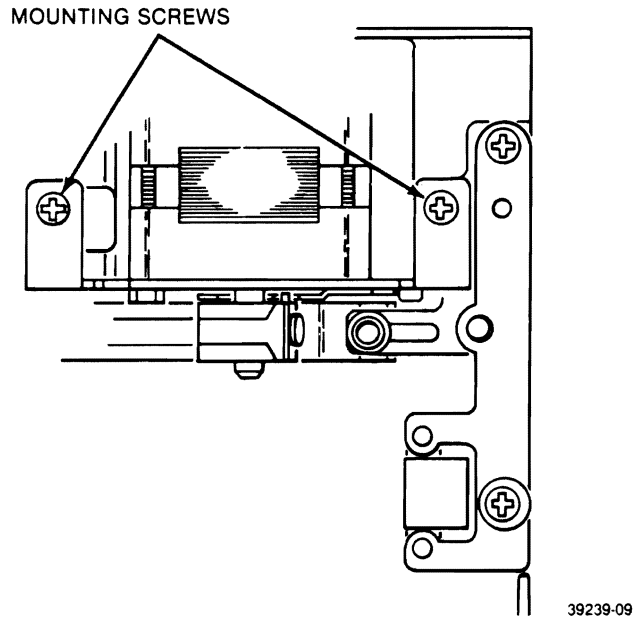
39239-25

- f. Loosen two mounting screws, which hold stepper motor to base casting (see figure 5-7).
- g. Adjust stepper motor.
- h. When lobes are of equal amplitude, tighten motor plate mounting screws (see figure 5-7).
- i. Check adjustment by stepping off track and returning. Check in both directions and readjust as required.
- j. Whenever head radial alignment has been adjusted, track 00 detector must be checked (paragraph 5.4.4).



## CAUTION

When tightening mounting screws, pressure **must** be applied to the rear of the step motor through the rectangular hole in the side of the casting to keep the motor bracket against the registering surfaces of the casting. Failure to do this will angle the band positioner causing track-to-track problems.

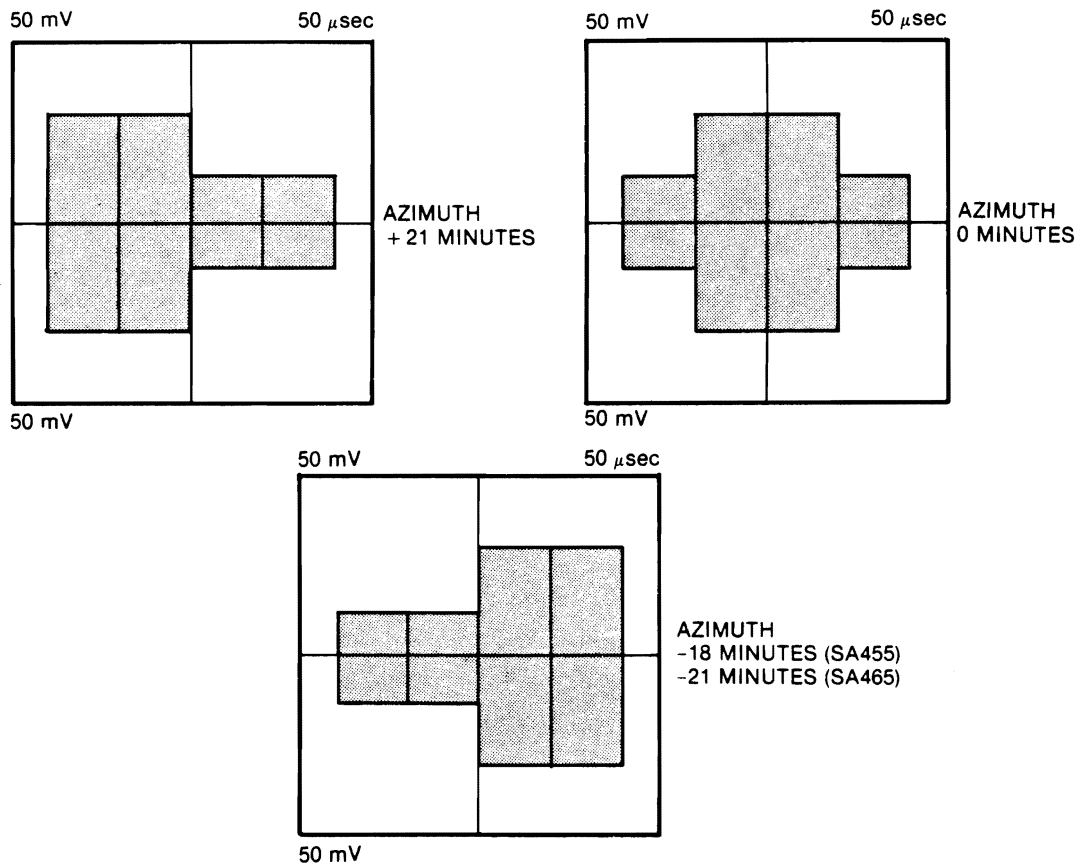


**FIGURE 5-7. STEPPER MOTOR MOUNTING SCREWS**

### 5.4.2 Read/Write Head(s) Azimuth Check

The azimuth is not field adjustable. If after performing this check the waveform on the oscilloscope is not within  $\pm 21$  minutes, replace the read/write head(s) assembly.

- a. Install alignment diskette (SA455 = SA128) (SA465 = SA126).
- b. Select drive and step to track 33 (SA455) or track 64 (SA465).
- c. Sync oscilloscope external negative on TP7. set time base to 0.5 msec per division.
- d. Connect one probe to TP1 and other to TP2. Invert one channel and ground probes to PCB. Set inputs to ac, ADD, and 50 mV per division.
- e. Compare waveform to figure 5-8. If not within range shown, replace read/write head assembly.



**FIGURE 5-8. AZIMUTH CHECK**

39239-10

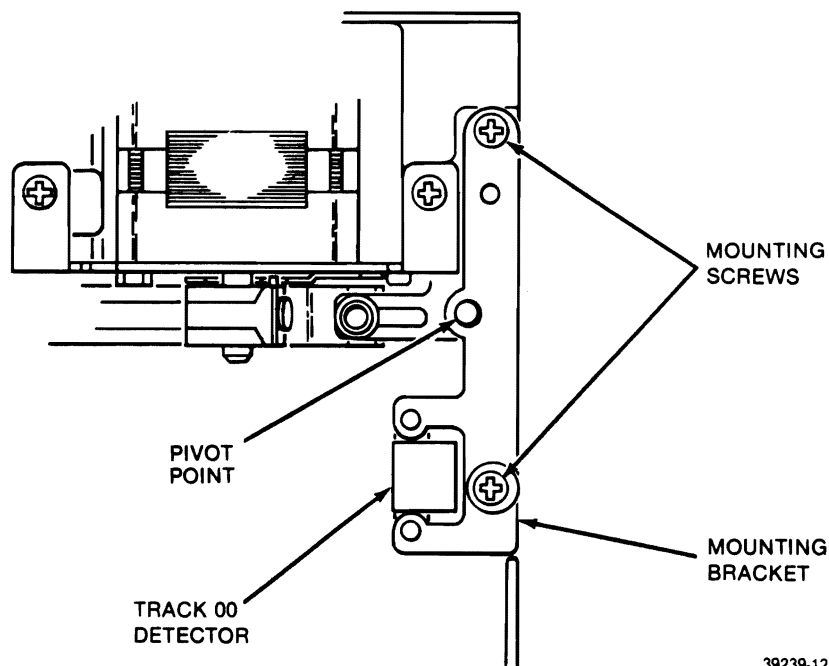
### 5.4.3 Head Amplitude Check

These checks are only valid when writing and reading back as described below. Ensure the diskette used for this check is not “worn” or otherwise shows evidence of damage on either side.

- a. Install good media.
- b. Start motor.
- c. Select drive and step to track 39 (SA455) or track 79 (SA465).
- d. Sync oscilloscope external on TP7 (+Index); connect one probe to TP2 and TP1 on drive PCB. Ground probes to PCB, ADD, and invert one input. Set volts per division to 50 mV and time base to 20 msec per division.
- e. Select head 0 and write a 2F pattern on entire track. Average minimum amplitude peak-to-peak should be 100 mV.
- f. Select head 1 and write a 2F pattern on entire track. Average minimum amplitude peak-to-peak should be 100 mV.
- g. If either head fails to meet minimum amplitude specifications, continue with procedure.
- h. Install fresh media and recheck.
- i. Check motor speed as per paragraph 5.4.6.
- j. With oscilloscope in “chop” mode, verify that output exists at both TP1 and TP2. If one TP has no output, or significantly less output than other, turn head cable connector over at J4. Should same TP have little or no output, PCB is faulty and needs replacing. If opposite TP now exhibits problem, head assembly is at fault, and should be replaced. Refer to paragraph 5.5.3.

#### 5.4.4 Track Zero Detector Assembly Adjustment

- a. Apply power to drive and install alignment diskette SA128 or SA126.
- b. Select drive and step to track 00.
- c. Sync oscilloscope external negative on TP7 (—Index). Set time base to 20 msec per division.
- d. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set input to ac. ADD, and invert one channel. Set vertical deflection to 100 mV/division.
- e. The 125 k Hz signal recorded should be observed at this time.
- f. If 125 k Hz signal is not present, step forward one track at a time and verify 125 k Hz signal is present. Step only five tracks.
- g. Step back towards track 00 detector and verify presence of 125 k Hz signal. Repeat stepping until signal is found.
- h. Once 125 k Hz signal is present on oscilloscope, carriage is located at track 00. Disconnect probes from TP1, TP2, and TP7. Connect one channel to TP8 and set input to dc. Set vertical deflection to 2 V per division. Trigger oscilloscope on selected input channel.
- i. Step to track 01 and verify that TP8 goes to zero.
- j. If not, loosen track 00 bracket.
- k. Set drive to seek alternately between tracks 00 and 01.
- l. Adjust eccentric until a 50% duty cycle is obtained (see figure 5-9).
- m. Tighten track 00 bracket and recheck timing.
- n. If same signal is obtained, remove alignment diskette, power down drive, and reinstall PCB. If same signal is not obtained, repeat steps k-n.



**FIGURE 5-9. TRACK ZERO ADJUSTMENT**

### 5.4.5 Index/Sector Timing Adjustment

- a. Insert alignment diskette SA128 or SA126.
- b. Start motor and select head 0.
- c. Step carriage to track 01 (SA455) or track 02 (SA465).
- d. Sync oscilloscope external positive on TP7 (+Index). Set time base to  $50 \mu\text{sec}/\text{division}$ .
- e. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set inputs to ac, ADD, and invert one channel. Set vertical deflection to  $500 \text{ mV}/\text{division}$ .
- f. Observe timing between start of sweep and first data pulse. This should be  $200 + 200/-100 \mu\text{sec}$ . If timing is not within tolerance, continue on with adjustment. See figure 5-10.
- g. Loosen mounting screw in index detector block until assembly is just able to be moved. See figure 5-11.
- h. Step carriage to track 38 (SA455) or track 76 (SA465).
- i. Observing timing, adjust detector until timing is  $200 + 200/-100 \mu\text{sec}$ . Ensure that detector assembly is against registration surface on hub frame.
- j. Tighten mounting screw.
- k. Step carriage to track 01 (SA455) or track 02 (SA465).
- l. Recheck timing.
- m. Repeat for head 1.

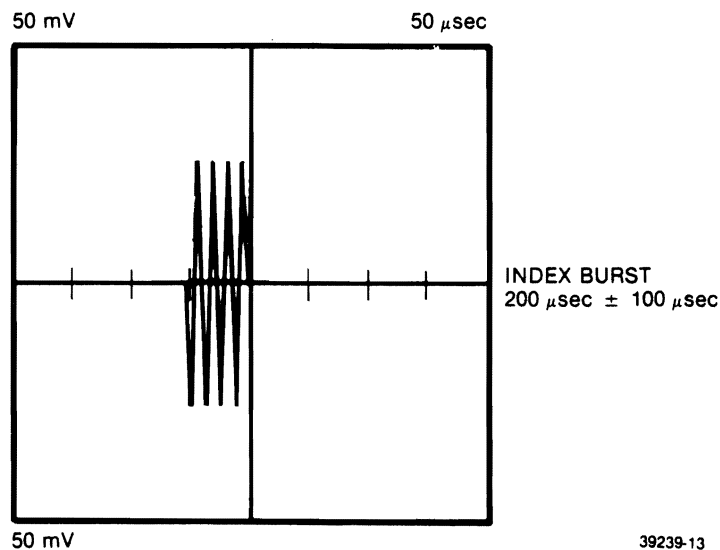
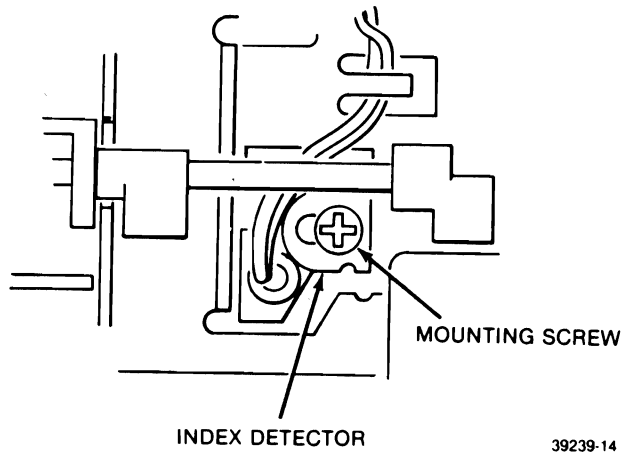


FIGURE 5-10. INDEX BURST



**FIGURE 5-11. INDEX DETECTOR**

**5.4.6 Motor Speed Adjustment (Using a Frequency Counter)**

This adjustment is not recommended for the field.

- a. Install SA128/126 or SA154/155 diskette; start motor and step to track 32.
- b. Connect frequency counter to TP7 (+ Index) on drive PCB.
- c. Adjust pot located on the motor PCB for  $5 \pm 0.05$  Hz (Period =  $200 \pm 2$  ms).

**5.4.7 Write Protect Detector**

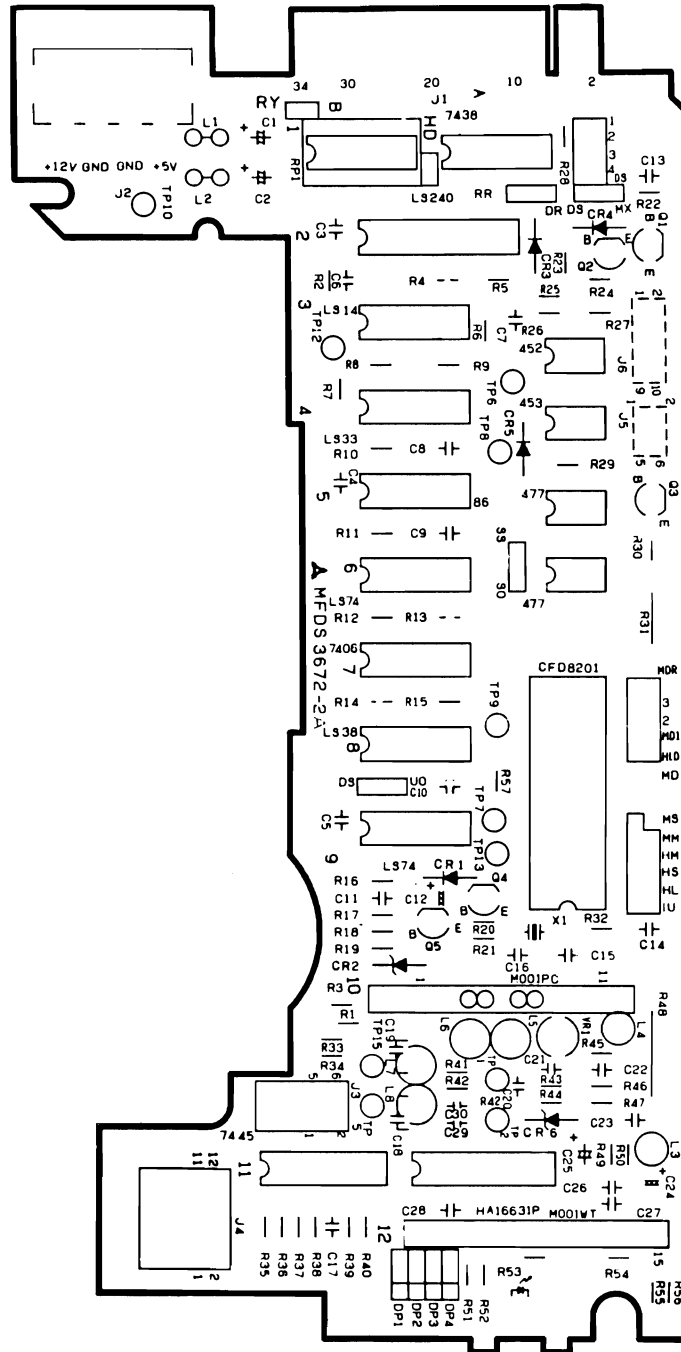
- a. Insert diskette into drive. Write protect notch must be open.
- b. Set oscilloscope to AUTO SWEEP, 2 V/div. Monitor TP9.
- c. Check to see if logic level changes when diskette is removed.

**5.4.8 Test Points On Drive PCB**

Test points for the drive PCB are as follows:

1	+ Read Data	9	Write Protect
2	—Read Data	10	Ground
5	Signal Ground	12	Step Pulse
6	Digital Read Data	13	Motor On
7	Index	15	Ground
8	Track 00		

See figure 5-12 for test point locations.



39239-18

FIGURE 5-12. PCB COMPONENT LOCATIONS, P/N'S 25284 AND 25286

## **5.5 REMOVALS AND REPLACEMENTS**

### **5.5.1 Faceplate Latch**

- a. Open door. Remove door latch.
- b. Remove mounting screw on each side of faceplate. Pull faceplate forward and away from drive casting.
- c. No re-adjustment is required after replacement.

### **5.5.2 Direct Drive Motor Assembly**

This assembly is not recommended for field replacement.

### **5.5.3 Head and Carriage Assembly**

This assembly is not recommended for field replacement.

### **5.5.4 Stepper Motor and Actuator Assembly**

This assembly is not recommended for field replacement.

### **5.5.5 Clamp Hub**

- a. Remove PCB.
- b. Open door.
- c. Remove clamp assembly front and rear screws.
- d. To reinstall: Position hub clamp with spacer and spring in place onto spindle hub. (Large end of spring is placed against hub frame.)
- e. Press hub frame down towards spindle until hub shaft protrudes through mounting hole in hub frame.
- f. Reinstall faceplate. Readjustment is not required.

### **5.5.6 Write Protect Sensor and Index Detector**

- a. Remove connector from PCB.
- b. Remove mounting screw from write protect assembly. This will free assembly.
- c. Remove index detector screw to free detector.
- d. Reverse instructions to reinstall.

### **5.5.7 Track Zero Photo Detector**

- a. Remove PCB and shields from drive.
- b. Remove: white wire from J6 Pin 2.  
green wire from J6 Pin 1.  
yellow wire from J6 Pin 10.
- c. Loosen mounting bracket screws.
- d. Remove two screws securing LED housing to track 00 plate.
- e. To reinstall, reverse above procedure.
- f. Adjust as directed in paragraph 5.4.5.

## 5.6 RECOMMENDED INCOMING RECEIVING INSPECTION

### 5.6.1 Necessary Equipment

All Shugart drives are 100% adjusted and tested before leaving the factory. It is only necessary to inspect for shipping damage on receipt of drives.

Inspection should be simple and test equipment kept to a minimum. Shugart recommends the following equipment.

- a. SA809 Exerciser (P/N 54157)
- b. Exerciser Instruction Manual (P/N 50686)
- c. Power Supply for Exerciser and Drive (+5, +12 V)
- d. Oscilloscope
- e. SA128/126 Alignment Diskette
- f. SA455/465 Service Manual (P/N 39239-0)

### 5.6.2 Procedure

- a. Unpack drive and inspect for physical shipping damage.
- b. Make sure all power is off.
- c. Attach exerciser cables to appropriate drive connectors.
- d. Power up.
- e. Insert alignment diskette (SA455 = SA128, SA465 = SA126).
- f. Set track addresses of 00 and 39 (SA455) or 79 (SA465) into exerciser.
- g. Select drive.
- h. Start motor and let drive seek automatically for 5 minutes.
- i. Check that activity light is on.
- j. Using this SA455/465 Service Manual and the Exerciser Instruction Manual as guides, perform the following checks:
  - Index Timing Adjustment (paragraph 5.4.6).
  - Head Radial Alignment, Sides 0 and 1 (paragraph 5.4.1).
  - Track Zero Switch is on at track 00 and off at 01 and 02.
- k. Remove alignment diskette and insert SA154/155 diskette.
- l. Seek to track 39 (SA455) or track 79 (SA465) and write a 2F signal. Minimum read back should be 90 mV.
- m. Check write protect sensor adjustment (paragraph 5.4.8).
- n. Power off.
- o. Remove connectors and repack drive.

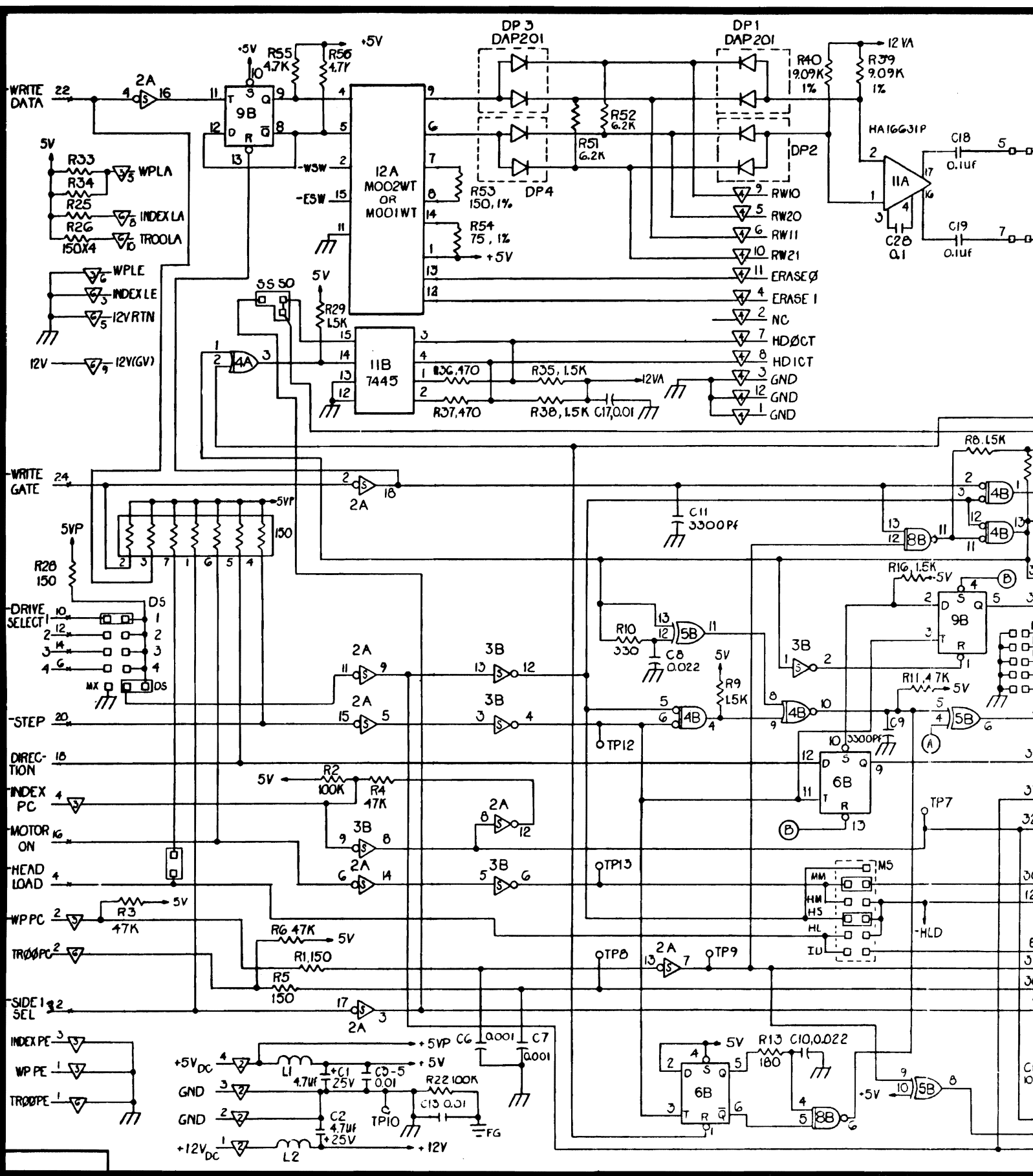
This procedure verifies that the critical functions of the drive are working properly (i.e., the drive will read and write, the disk will rotate at the proper speed, and critical adjustments are within specification).



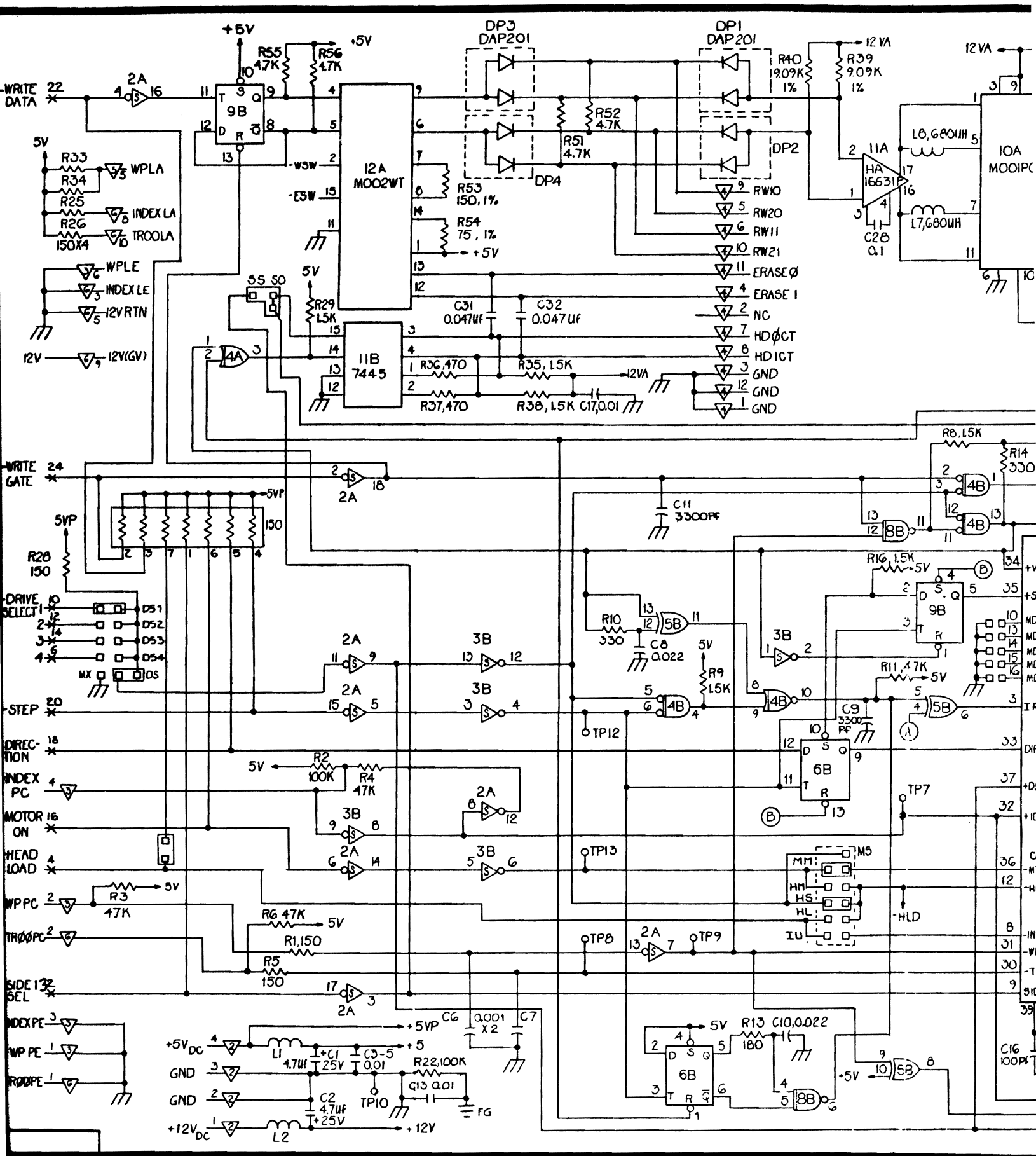
## **SECTION VI**

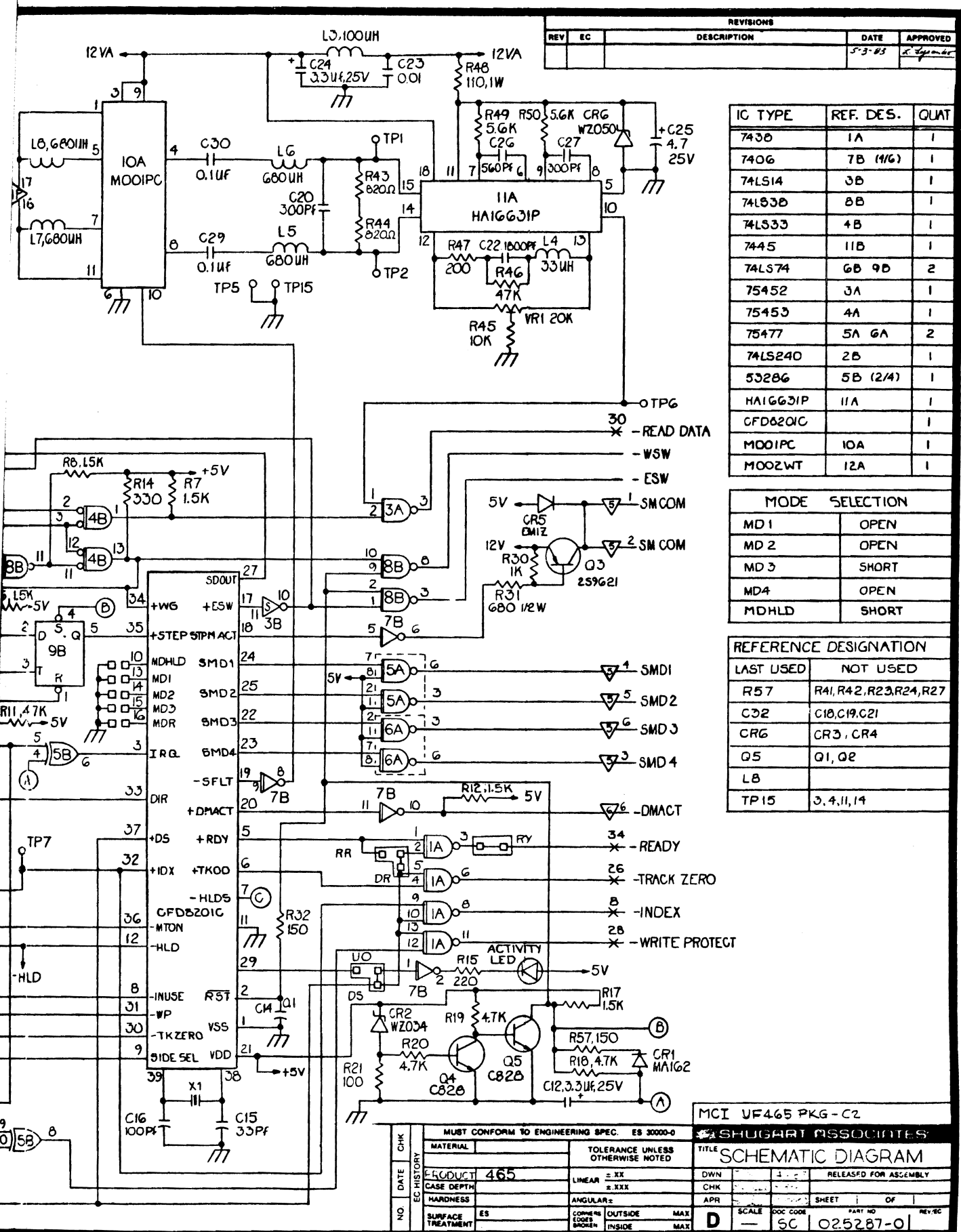
### **SCHEMATIC DIAGRAMS**

The following schematic diagram is furnished as an aid to malfunction analysis of PCB's 25284 (SA455) and 25286 (SA465).









REVISIONS			
REV	EC	DESCRIPTION	DATE
			5-3-83
			<i>[Signature]</i>

IC TYPE	REF. DES.	QUAT
7430	1A	1
7406	7B (1/6)	1
74LS14	3B	1
74LS30	8B	1
74LS33	4B	1
7445	11B	1
74LS74	6B 9D	2
75452	3A	1
75453	4A	1
75477	5A 6A	2
74LS240	2B	1
53286	5B (2/4)	1
HAIGGJIP	11A	1
CFD620IC		1
MOOIPC	10A	1
MOOZWT	12A	1

MODE SELECTION	
MD 1	OPEN
MD 2	OPEN
MD 3	SHORT
MD 4	OPEN
MDHLD	SHORT

REFERENCE DESIGNATION	
LAST USED	NOT USED
R57	R41, R42, R23, R24, R27
C32	C18, C19, C21
CR6	CR3, CR4
Q5	Q1, Q2
LB	
TP15	3, 4, 11, 14

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		ASHUGART ASSOCIATES	
TITLE SCHEMATIC DIAGRAM		RELEASED FOR ASSEMBLY	
PRODUCT 465	LINEAR ±.XX	DWN	1
CASE DEPTH	±.XXX	CHK	
HARDNESS	ANGULAR ±	APR	
SURFACE TREATMENT ES	CORNERS OUTSIDE MAX	SCALE	SHEET OF
	EDGES BROKEN INSIDE MAX	D	5C
		SCALE	025287-0

FIGURE 6-2. SCHEMATIC DIAGRAM, P/N 25286 6-5/6-6 (blank)

## **SECTION VII ILLUSTRATED PARTS CATALOG**

### **7.1 DESCRIPTION**

The Illustrated Parts Catalog (IPC) is arranged so that the figure will always precede the parts listing and, when possible, will appear directly above the parts list or on the left hand page immediately preceding it.

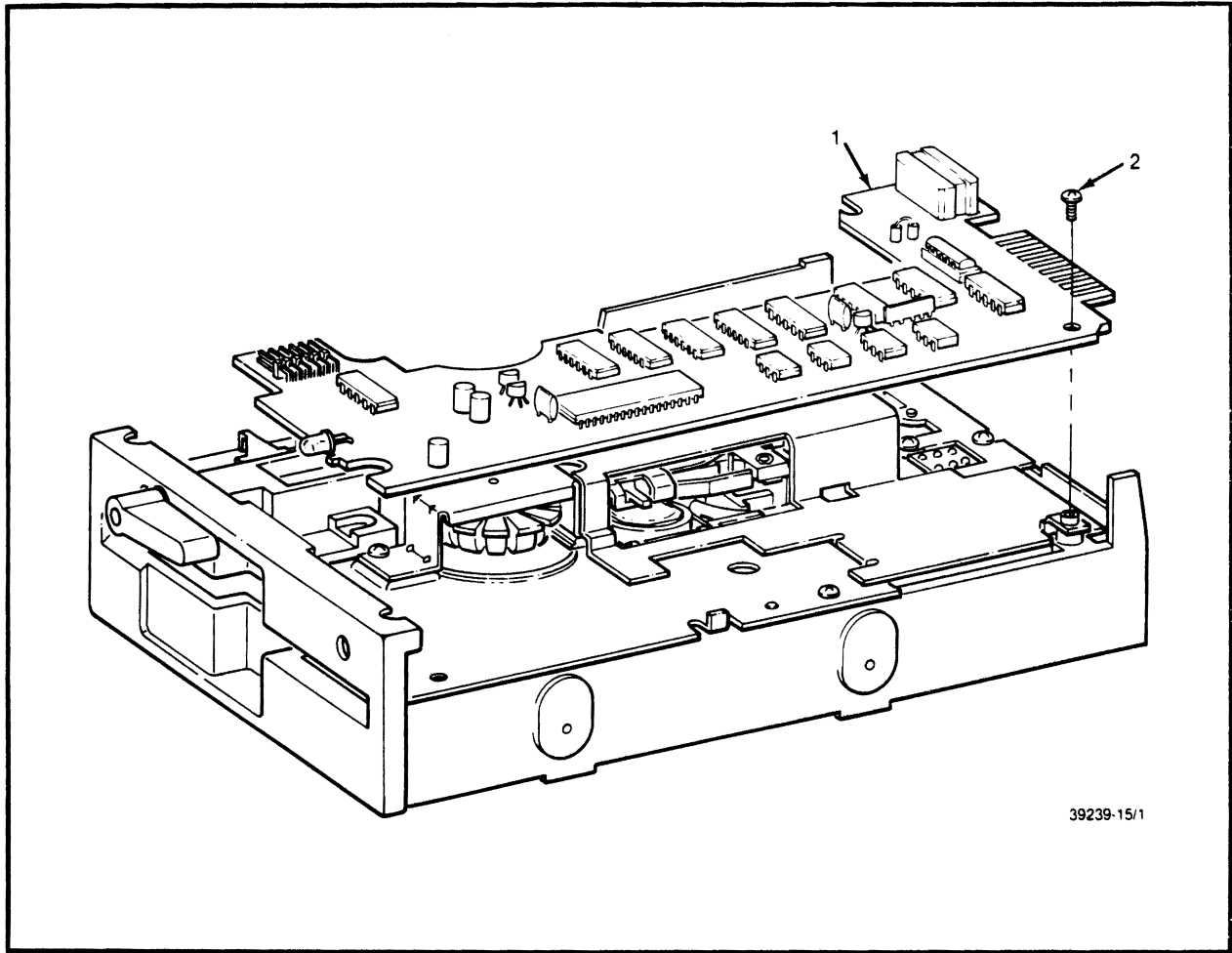
The first number in the list will always refer to the figure number. The second number will refer to the reference number of the part within the figure.

Part numbers enclosed in parentheses refer to parts belonging to a Next Higher Assembly (NHA) and are of importance only to those customers with alternate assemblies. Following the descriptions of these parts, the designation NHA P/N \_\_\_\_\_ gives the part number of the assembly to which they pertain. When applicable to the customer's assembly, these alternate parts will be used in lieu of the part listed directly above them. Assume that the quantity per assembly for these alternate parts is the same unless otherwise listed.

When an assembly is referred to within a figure and a further breakdown is shown on another figure, then the referenced figure will be called out.

### **7.2 QUANTITY PER ASSEMBLY**

The quantity listed is the quantity used on the major assembly. Major assemblies themselves will not have a quantity listed.



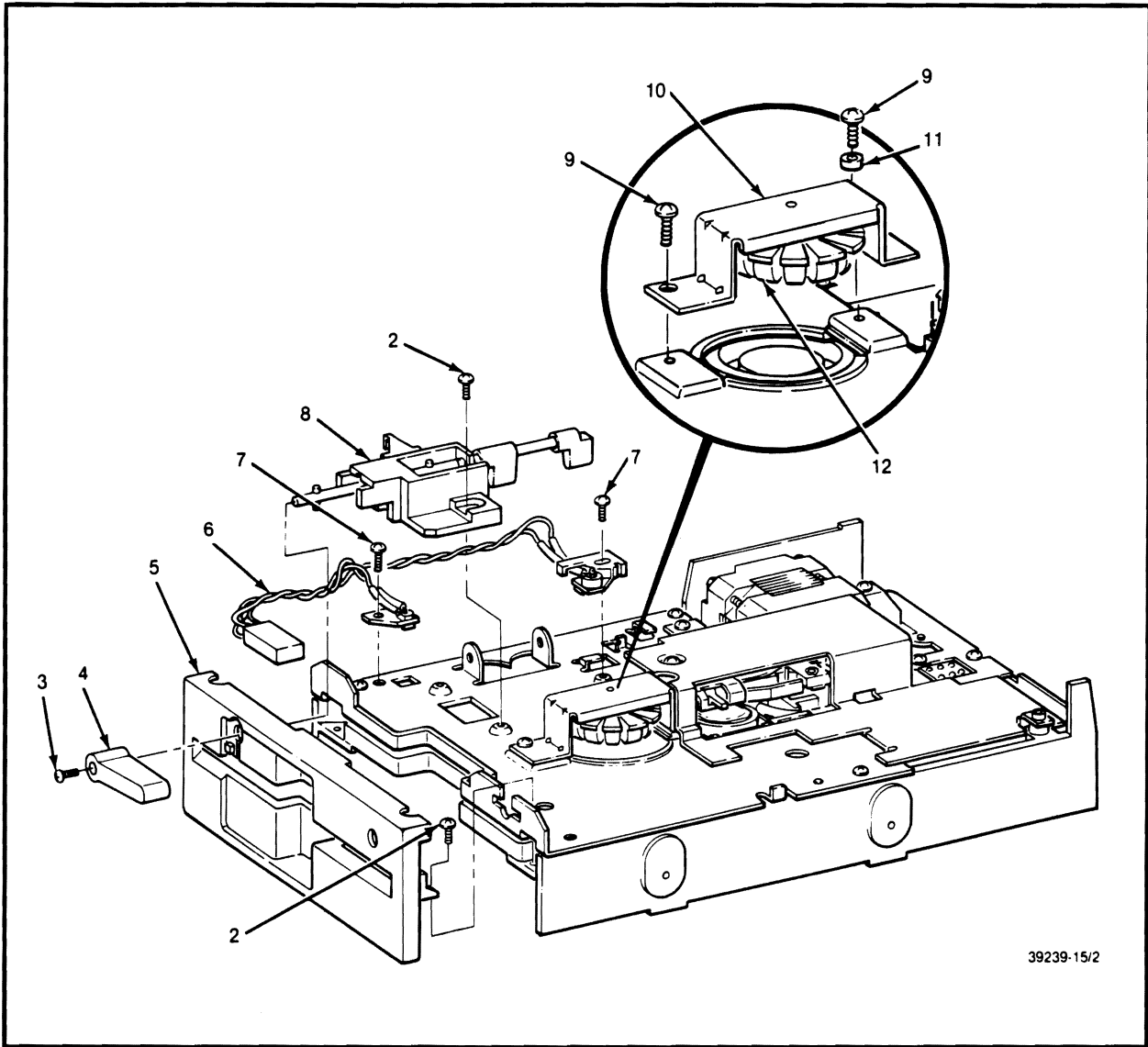
39239-15/1

**FIGURE 7-1. SA455/465 BASIC DRIVE ASSEMBLY (SHEET 1 OF 4)**

**SA455/465 BASIC DRIVE ASSEMBLY**

<b>REFERENCE NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY</b>
Ref	51756	SA455/465 MINIFLOPPY™ DRIVE	
1	25284	SA455 PCB	1
	25286	SA465 PCB	1
2	11477	SCREW	2





**FIGURE 7-1. SA455/465 BASIC DRIVE ASSEMBLY (SHEET 2 OF 4)**

**SA455/465 BASIC DRIVE ASSEMBLY (CONT.)**

<b>REFERENCE NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY</b>
3	11464	SCREW	1
4	51782	CLAMP HANDLE	1
5	52446	FACE PLATE	1
6	54758	WRITE PROTECT/INDEX DETECTOR	1
7	11475	SCREW	2
8	51896	GUIDE SHAFT ASSEMBLY	1
9	11450	SCREW	2
10	51898	CLAMP CAM ASSEMBLY	
11	51788	SPACER	1
12	54765	COLLET	1

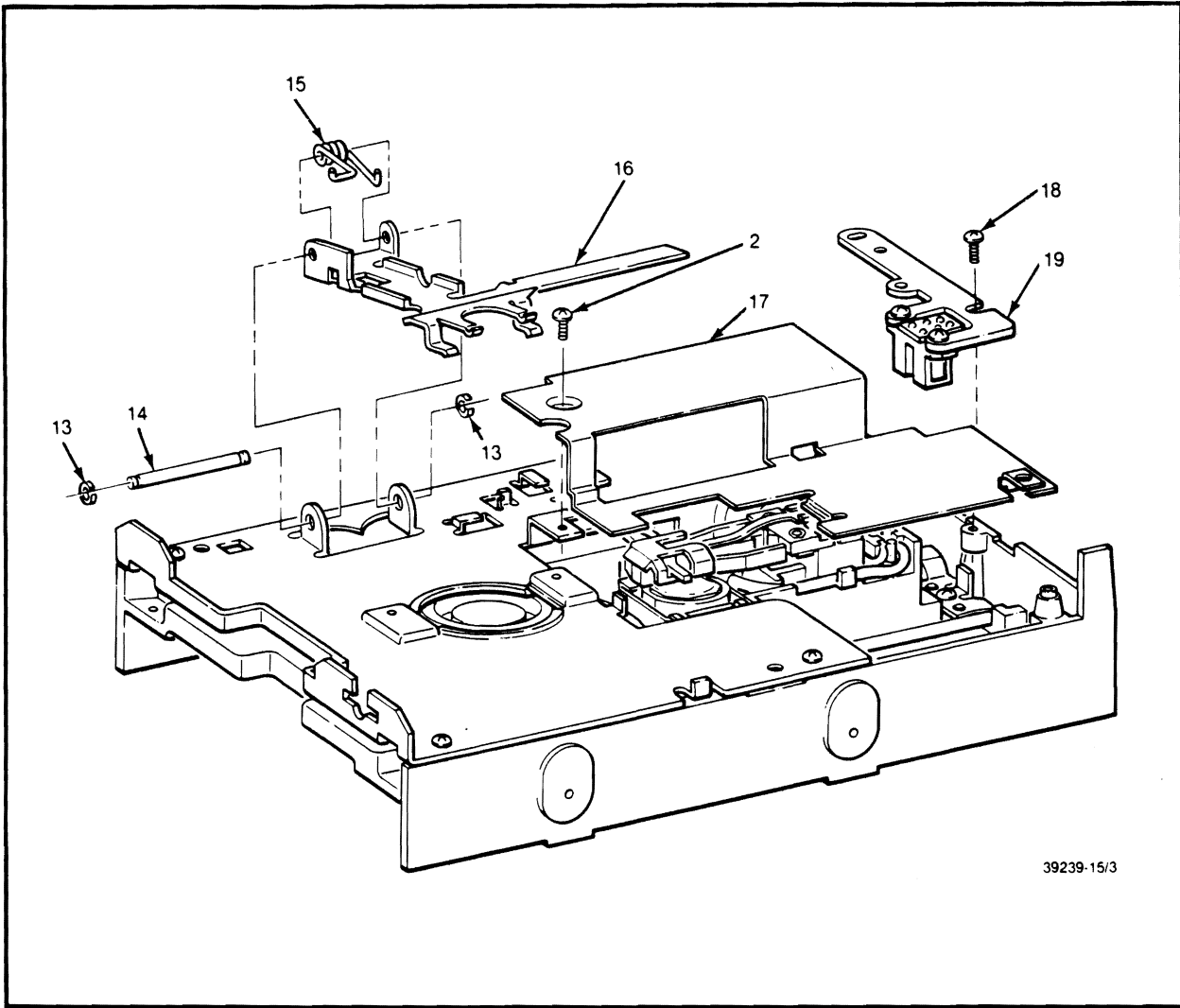
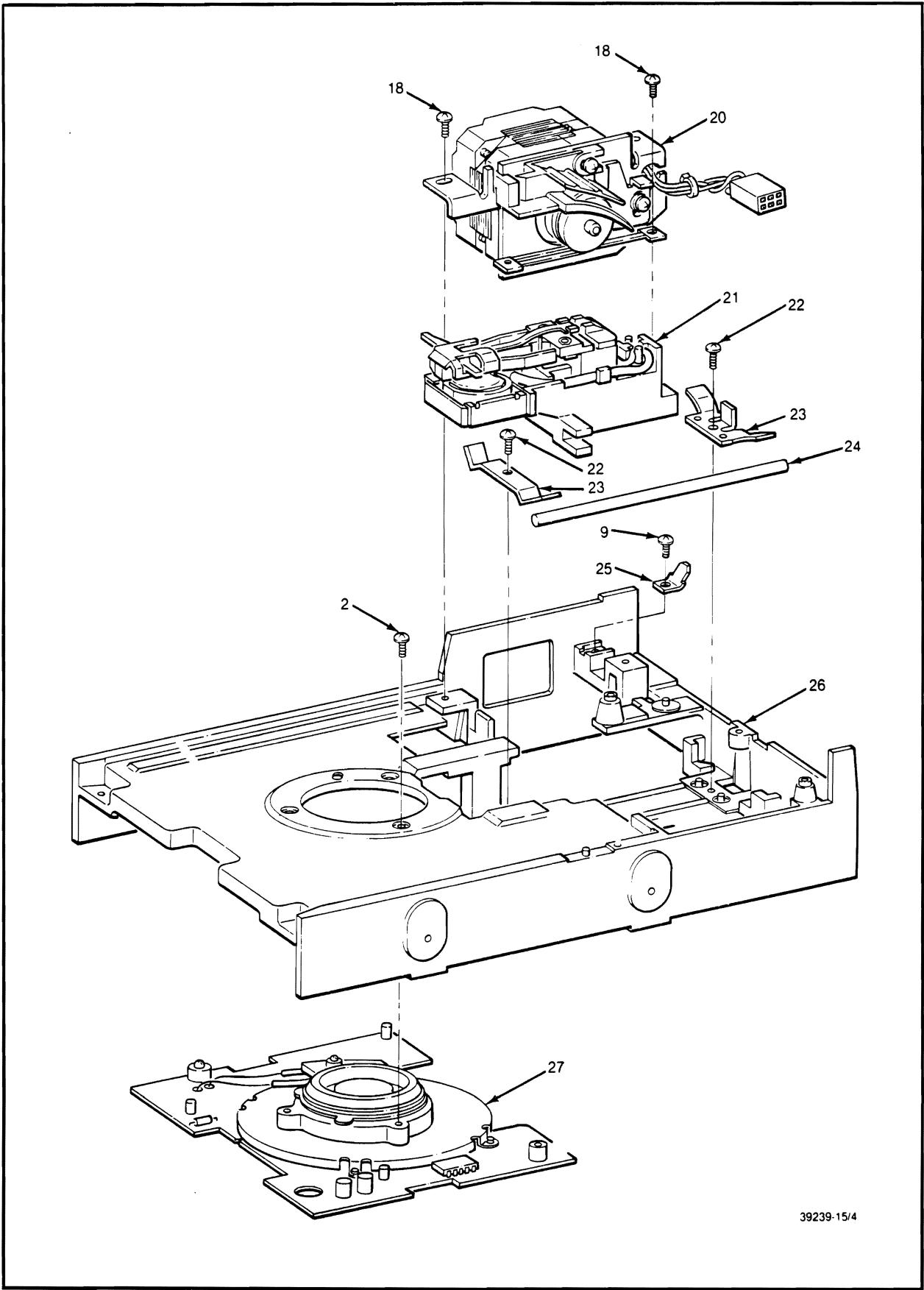


FIGURE 7-1. SA455/465 BASIC DRIVE ASSEMBLY (SHEET 3 OF 4)

**SA455/465 BASIC DRIVE ASSEMBLY (CONT.)**

<b>REFERENCE NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY</b>
13	11461	E-RING	2
14	51785	LIFT SHAFT	1
15	51784	LIFT SPRING	1
16	51786	LIFTER	1
17	54768	SHIELD PLATE	1
18	11468	SCREW	1
19	54762	TRACK 00 SENSOR	1



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FIGURE 7-1. SA455/465 BASIC DRIVE ASSEMBLY (SHEET 4 OF 4)

**SA455/465 BASIC DRIVE ASSEMBLY (CONT.)**

<b>REFERENCE NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY</b>
20	51754	STEPPER ASSEMBLY	1
21	54773	SA455 HEAD CARRIAGE ASSEMBLY	1
	54814	SA465 HEAD CARRIAGE ASSEMBLY	1
22	11476	SCREW	2
23	51895	CLAMP, Guide Rod	2
24	51801	GUIDE ROD	2
25	11456	FASTEN TAB	1
26	51757	BASE	1
27	51800	DRIVE MOTOR	1

**TABLE 7-1. REFERENCE NUMBER TO PART NUMBER CROSS REFERENCE**

<b>Part Number</b>	<b>Reference Number</b>
11450	1-9
11456	1-32
11461	1-23
11464	1-3
11468	1-18
11475	1-7
11476	1-22
11477	1-2
25284	1-1
25284	1-2
51754	1-26
51757	1-33
51771	1-36
51782	1-4
51783	1-9
51784	1-17
51785	1-24

<b>Part Number</b>	<b>Reference Number</b>
51786	1-18
51788	1-14
51800	1-34
51801	1-30
51895	1-23
51896	1-8
51898	1-13
52446	1-5
54758	1-6
54762	1-22
54765	1-15
54768	1-20
54773	1-27
54814	1-24

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### 7.3 RECOMMENDED SPARE PARTS STOCKING GUIDE

The spare parts stocking guide is broken down into three levels. These levels are: Site or Field Support Engineer, Branch Office, and Depot or Headquarters. The quantities listed assume that the Site is replenished by the Branch immediately and the Branch replenished by the Depot within 30 days.

The inventories that the levels can maintain are:

Site	1 to 20 machines
Branch	1 to 100 machines
Depot	
Depot only parts	Unlimited
Branch replenishment	Same as Branch ratio

Table 7-2 shows the spare parts required to support the SA455/465 in the field.

**TABLE 7-2. SA455/465 SPARE PARTS STOCKING GUIDE**

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT
25284	PCB, SA455	1	3	4
25286	PCB, SA465	1	3	4
51781	LOCK CAM			2
51782	CLAMP HANDLE	1	4	4
51783	LOCK SPRING	1	2	2
51784	LIFTER SPRING	1	2	2
51785	LIFTER SHAFT		2	2
51896	GUIDE SHAFT ASSEMBLY			2
51899	CLAMP BEARING			2
52445	STEPPER MOTOR			2
52446	FACE PLATE		2	3
54755	FACE PLATE (FULL HEIGHT)		2	3
54758	WRITE PROTECT/INDEX DETECTOR ASSEMBLY	1	3	3
54762	TRACK 00 ASSEMBLY	1	3	3
54765	COLLET ASSEMBLY		2	2
54768	SHIELD PLATE		1	2
54770	SPINDLE MOTOR			2
54771	GUIDE ROD			2
54773	SA455 HEAD CARRIAGE		2	3
54814	SA465 HEAD CARRIAGE		2	3

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