1.1 GENERAL

Toshiba Personal Computer T1000 (hereinafter referred to as T1000) is a portable personal computer which is compatible with IBM PC situated at higher rank of portable computer than Toshiba T1100. It provides many powerful functions in spite of its compact size and internal battery pack. Hardware of the T1000, most of IC chips are C-MOS type so that the power consumption is very little and Gate Array chips are applied so that it is very compact and light weight.

The T1000 is composed of as follows:

System PCB (Printed curcuit board)
3.5-inch floppy disk drive
LCD (Liquid crystal display)
Keyboard

The system PCB has a power supply function.
A 3.5-inch floppy disk drive (FDD) is double-sided, double-density, double-track with storange capacity of 720 kilobytes (formatted). The high-resolution liquid crystal display (LCD) with pixels of 640 in columns and 200 in rows.
The keyboard has 82 keys. For most applications it can be used exactly like a standard typewriter keyboard.

The T1000 provided connecting to the optional devices at the rear panel and left side panel of the system. There are six connectors such as a parallel printer, an RGB direct drive CRT display, an external FDD, an external key pad and an RS-232C device.

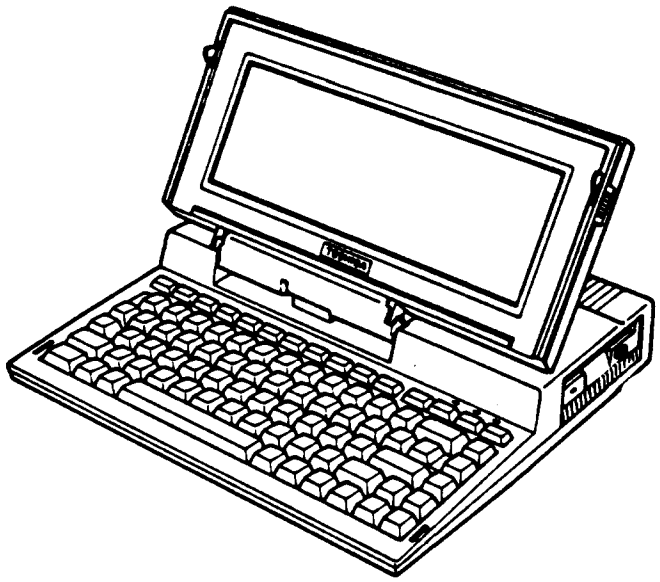


FIGURE 1-1 T1000 Personal Computer

1.2 SYSTEM PCB

System PCB is composed of the following devices:

- Central processor: CPU (80C88) (5 MHz)

- Memory
  System memory ... 512 kbytes
  BIOS ROM ... 32 kbytes
  Video RAM ... 16 kbytes

- MS-DOS ROM (Version 2.11)

- System support element (T7885)
  TOSHIBA super integration LSI (T7885) has various functions such as; clock generator (CG, equivalent to 82C84), bus controller (BC, equivalent to 82C88), programmable interrupt controller (PIC, equivalent to 82C59), floppy disk controller (FDC, equivalent to uPD765), programmable interval timer (PIT, equivalent to 82C53), direct memory access controller (DMAC, equivalent to 82C37), and programmable peripheral interface (PPI, equivalent to 82C55).

- Keyboard controller: KBC (80C50)

- RS232C controller (8250)

- Gate array
  I/O controller gate arrey
  I/O driver gate arrey
  Display controller gate arrey

1.2.1 Jumper straps

The system PCB has five jumper straps; PJ17, PJ18, PJ19, PJ20 and PJ21.

The following figure shows location of the jumper straps.

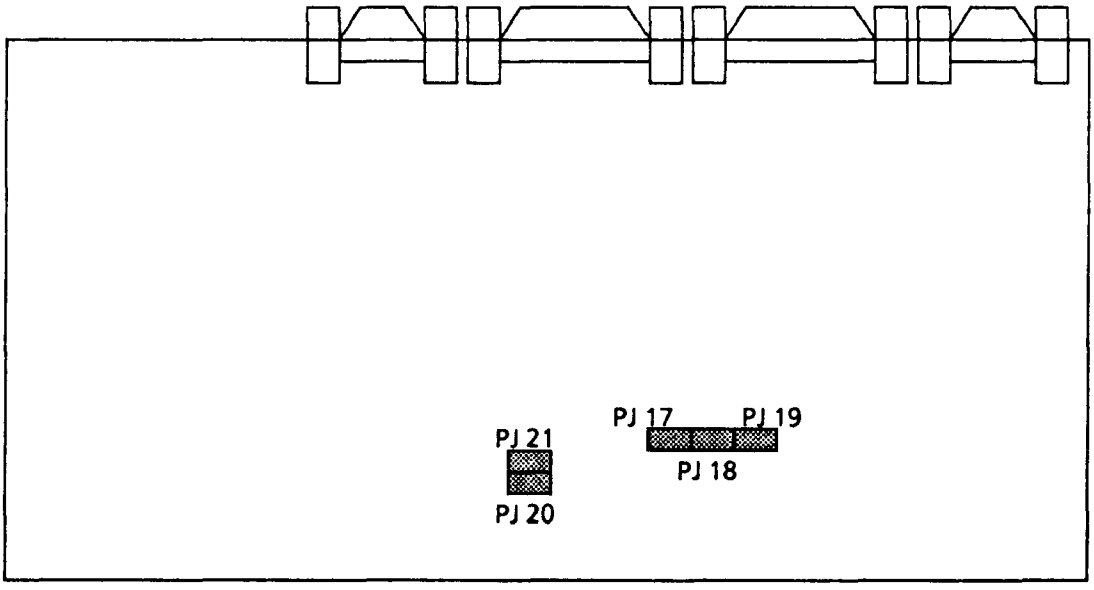
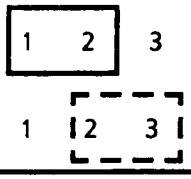
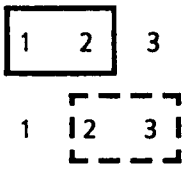
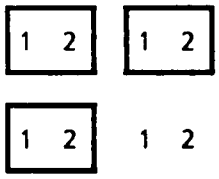


FIGURE 1-2 Jumper Straps Location

The following table shows function of the jumper straps.

TABLE 1-1 Jumper Straps Functions

Jumper	Pins	Description
PJ17		To use a 4 Mbits EPROM. To use a 1 Mbit and 2 Mbits EPROM.
PJ 18 PJ 19		To change a DOS-ROM package pin. 24 pin is output enable and 2 pin is AD 16. 24 pin is AD 16 and 2 pin is output enable.
PJ20 PJ 21		Displays a normal font. Displays a North Europian (Denmark) font.

1.3 3.5-INCH FLOPPY DISK DRIVE

The floppy disk drive (FDD) used in the T1000 is high performance, high reliable, slim sized FDD for 3.5-inch floppy disks with recording capacity of 1 Mbyte (unformatted) in double-sided, double density and 135 tracks per inch operation. The specifications are as following table.

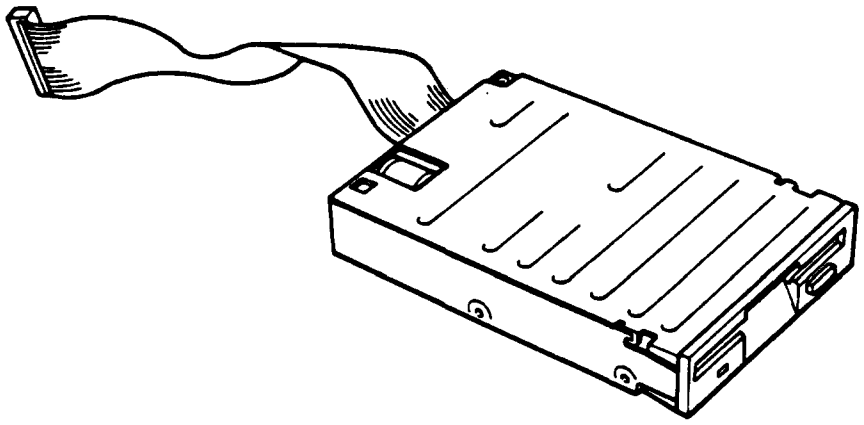


FIGURE 1-3 3.5-inch FDD

TABLE 1-2 3.5-inch Floppy Disk Drive Specifications

Item	Specifications
Storage Capacity (kilobytes)	1000 (unformatted) 720 (formatted)
Number of Heads	2
Number of Track per Side	80
Track to Track Access (milliseconds)	6
Head Settling Time (milliseconds)	15
Track Density (tracks per second)	135
Motor Start-up Time (milliseconds)	500
Data Transfer Rate (kilobits per second)	250
Rotational Speed (revolutions per minute)	300
Recording Method	MFM (Modified frequency modulation)

1.6 KEYBOARD

The keyboard is mounted on the system and has 82 keys. These consist of 48 standard keys, 10 function keys, 10 cursor keys, 13 functional keypads, and Fn key.
The keyboard is just a key matrix built up by the above keys. The keyboard is connected to the keyboard controller on the system PCB through a 25-pin flat cable.

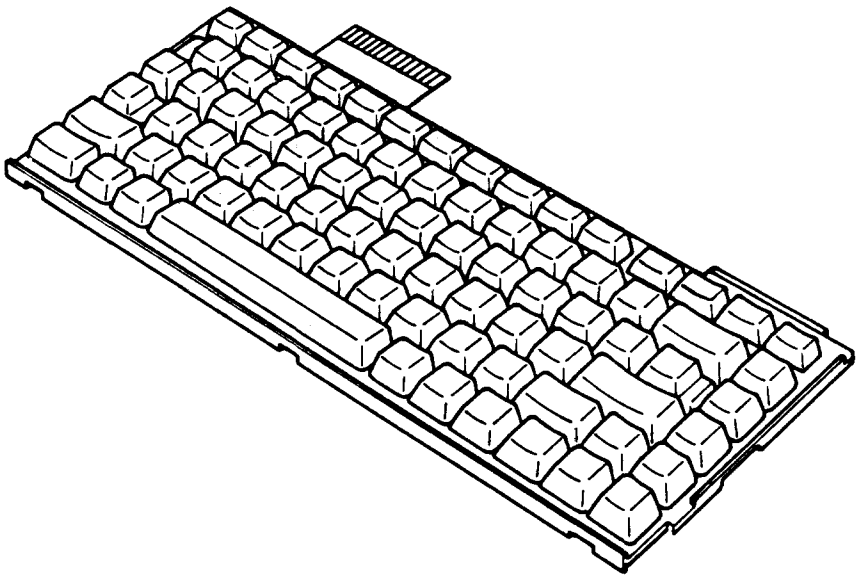


FIGURE 1-4 Keyboard

1.7 LIQUID CRYSTAL DISPLAY

The liquid crystal display (LCD) is a graphics type display unit which has a resolution of 640 in horizontal (or column) by 200 in vertical (or row) directions. This unit is composed of the display panel, power supply and driver circuits. This receives timing pulses, four-bit data signals, +5V dc and -22V dc power inputs and a contrast control input from the system PCB. All timing pulses and data signals are TTL level compatible. Specifications are as following table.

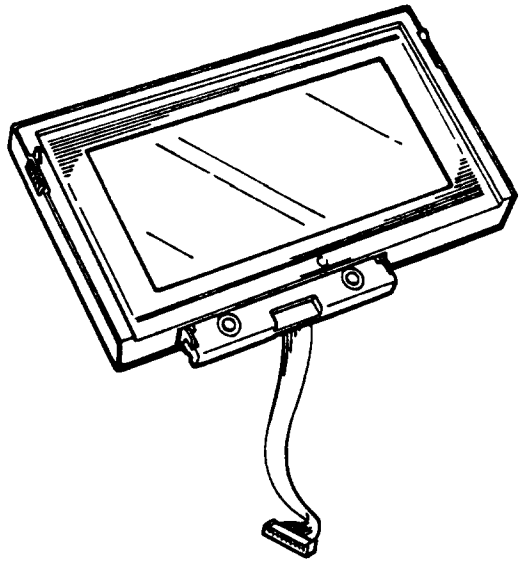


FIGURE 1-5 Liquid Crystal Display

TABLE 1-3 Liquid Cristal Display Spesifications

Item	Specification
Outline Dimension (mm)	273.0 (W) x 97.6 (H) x 12.0 Max (D)
Number of Dots	640 x 200 dots
Number of characters	80 x 25 (2000) Characters (8 x 8 dot format, alpha-numeric)
Clear Viewing Area (mm)	250.0 (W) x 83.0 (H)
Dot Size (mm)	0.345 (W) , 0.345 (H)
Dot Pitch (mm)	0.375 (W) , 0.375 (H)
Weight (gram)	350

2.1 GENERAL

These problem isolation procedures are used to isolate defective FRUs (field replaceable units) to be replaced. FRUs consist of the following:

1. Power Supply
2. System PCB
3. FDD
4. Keyboard
5. LCD

See PART 4 for detailed replacement procedures instructions. Test program operations are described in PART 3.

The following items are necessary for carrying out the problem isolation procedures.

1. T1000 Diagnostics disk
2. Phillips screwdriver
3. Work disk (for FDD testing)
4. Cleaning disk kit (for FDD testing)
5. Multimeter
6. Printer port LED

The problem isolation flowchart described in part 2.2 can be used to determine the necessary isolation procedures to be followed when there is a problem with the T1000.

2.2 PROBLEM ISOLATION FLOWCHART

This flowchart is used as a guide for determining which FRU is defective. Please confirm the following before performing the flowchart procedures.

1. No disk is in the FDD.
2. The ac adapter is disconnected.
3. All optional equipment is disconnected.

See next page.

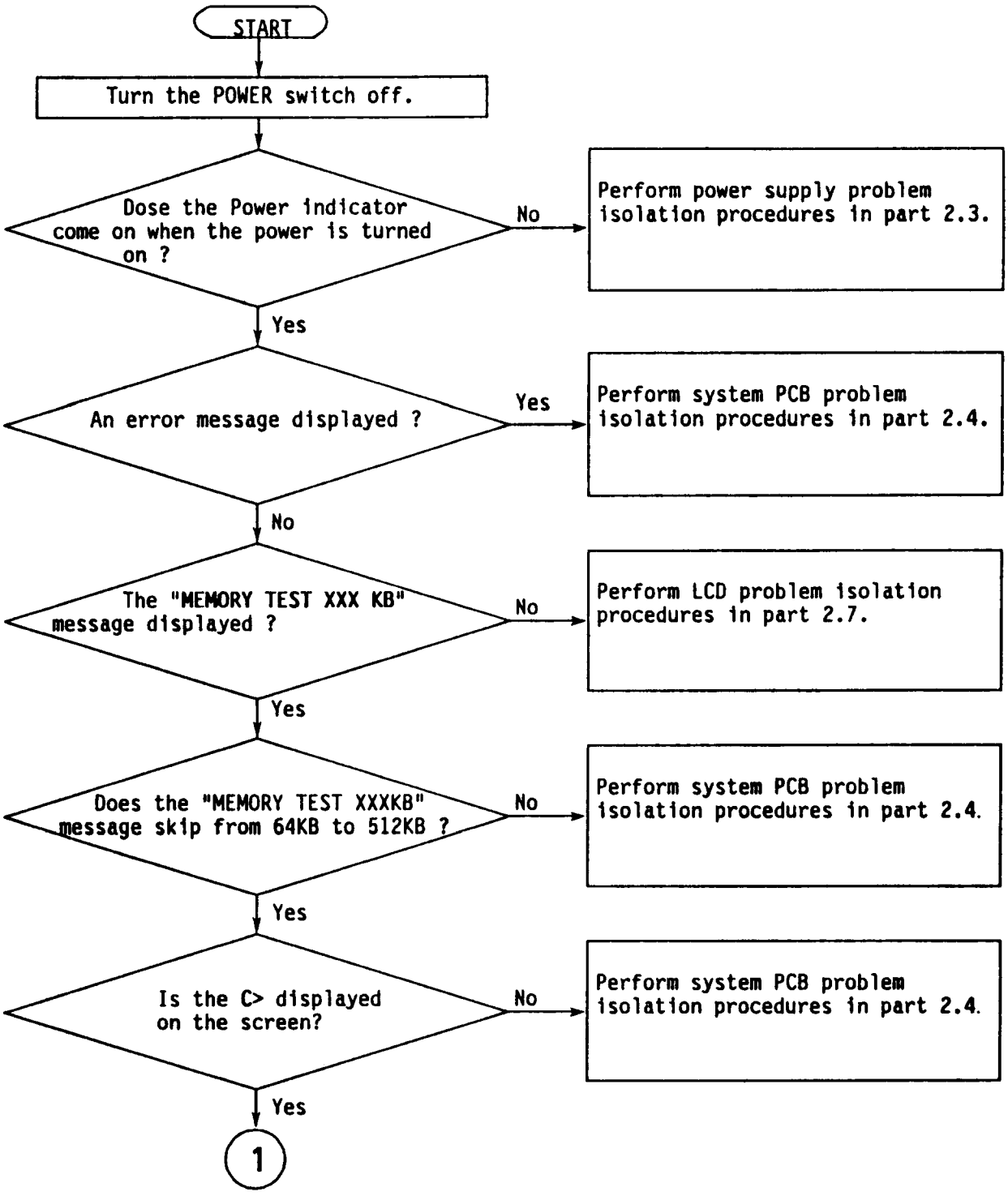
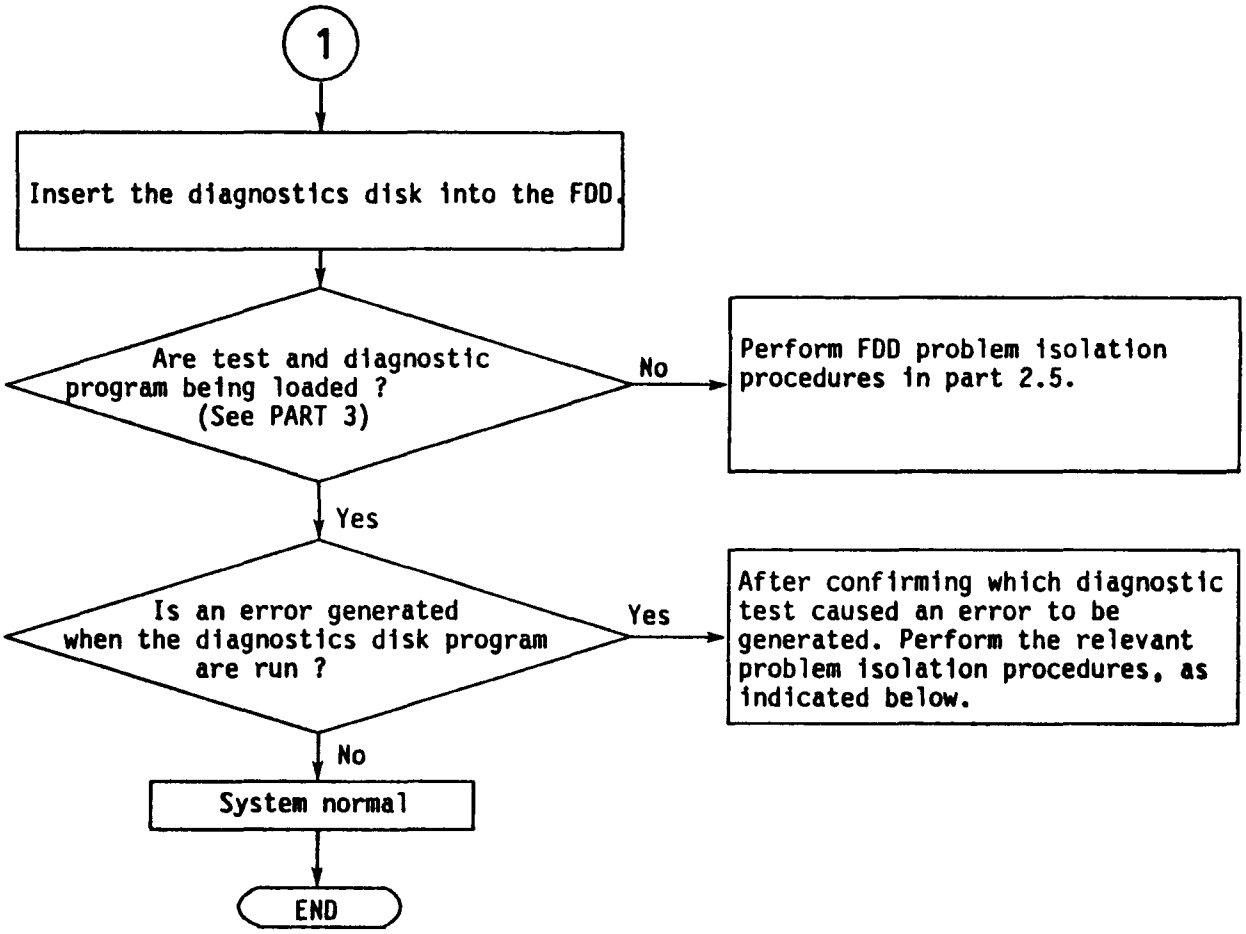


FIGURE 2-1 Problem Isolation Flowchart



1. If an error is generated on the system test, memory test, display test and real time test, go to system PCB isolation procedures in part 2.4.

2. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.6.

3. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

2.3 POWER SUPPLY ISOLATION PROCEDURES

This section describes how to determine whether the power supply is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Battery Check

PROCEDURE 2: Input Voltages Check

PROCEDURE 3: Connector Check

PROCEDURE 4: Low Battery detection Volume Adjustment

PROCEDURE 5: Battery Pack Replacement

PROCEDURE 1

Battery Check

1. Turn the POWER switch off.

2. Disconnect the ac adapter.

3. Turn the POWER switch on. If the Low Battery indicator red lights, plug the ac adapter into the DC IN 9V jack. If the indicator then changes to green, then battery pack is normal and you should go to PROCEDURE 2.; if it remains red, replace the ac adapter. If it still remains lit red, go to PROCEDURE 2.

4. If the Low Battery indicator doesn't light in red and Power indicator green lights, go to PROCEDURE 3.

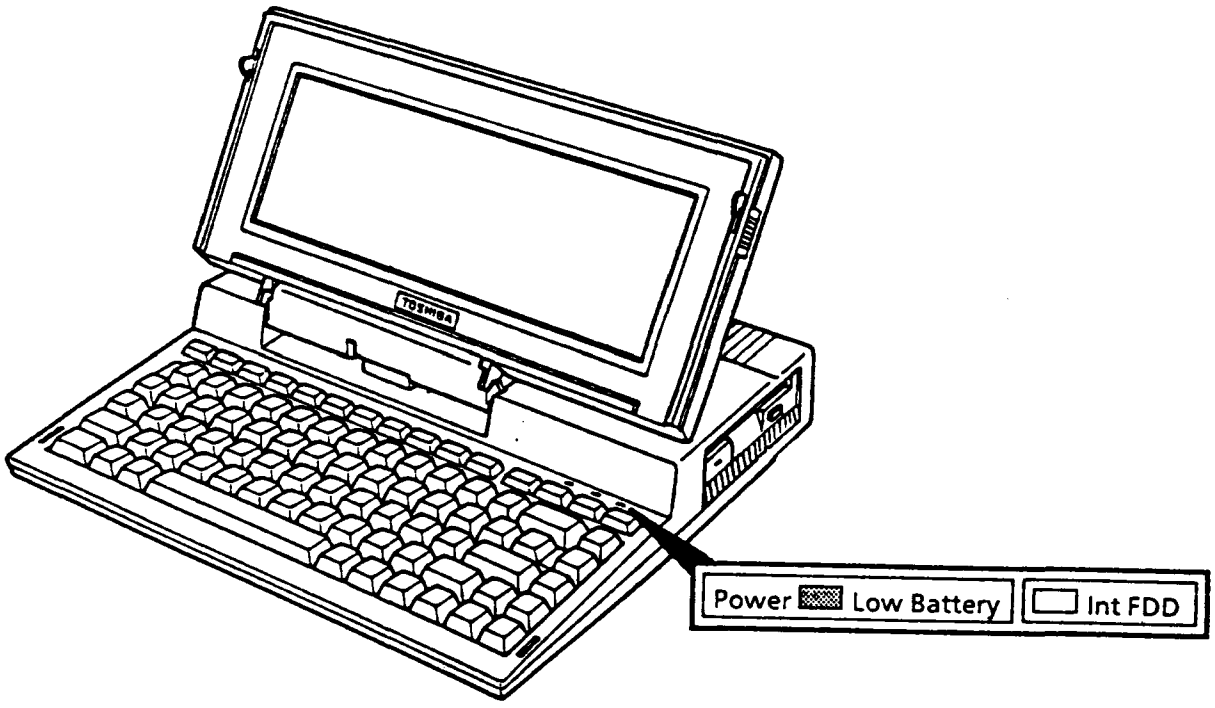


FIGURE 2-2 Battery Check

PROCEDURE 2

Connector Check

1. Turn the POWER switch off.

2. Remove the top cover assembly. (Refer to part 4.2.)
   If the system has an optional modem card, remove the modem card. (Refer to part 4.13.)

3. If the battery connector (PJ 10) is connected properly, go to PROCEDURE 3; if it is not connected properly, reconnect it.

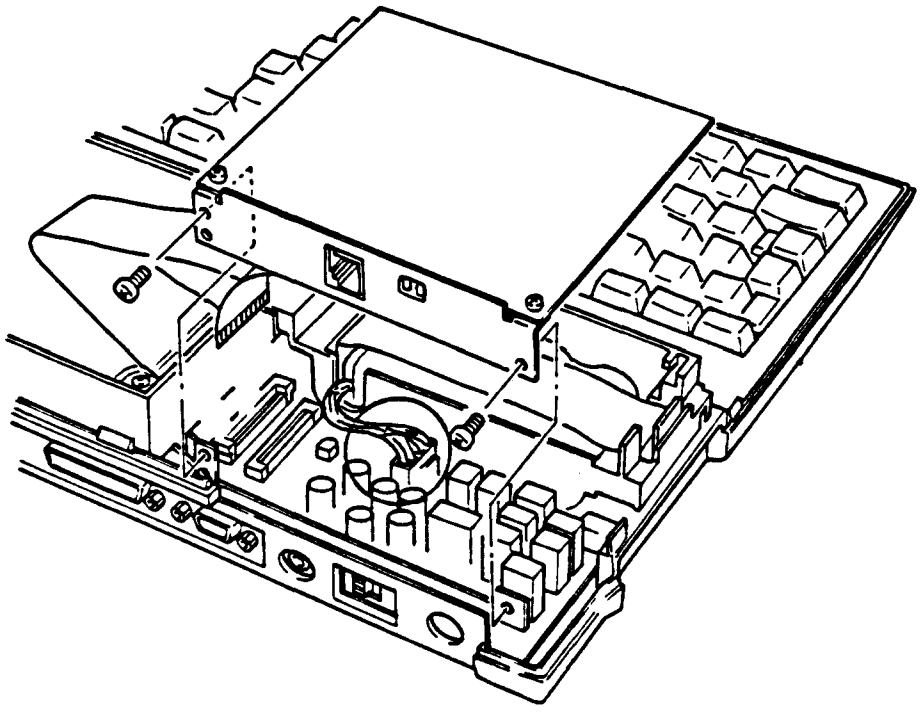


FIGURE 2-3 Battery Connector

PROCEDURE 3

Battery Pack Output Voltages

1. Plug ac adapter into the DC IN 9V jack, then turn the POWER switch on.

2. Use a multimeter to confirm that the battery pack output voltages for the battery connector conform to the values given in the following table.

3. If the voltages conform to the values given in the table, the battery pack is normal. go to PROCEDURE 4.

4. If the voltages do not conform to the those given in the table, go to PROCEDURE 5.

TABLE 2-1 Battery Pack Output Voltages

CONNECTOR	PIN NUMBER		VOLTAGE (Vdc)		
	+ lead	- lead	Normal	Min	Max
PJ 10	1, 2	3, 4	+ 5	+ 4.8	+ 5.5

PROCEDURE 4

Low Battery Detection Volume Adjustment

1. Use a multimeter to confirm that the output voltages for the PJ 23 on the system PCB conform to the values given in the following table.

2. If the voltage conforms to the values given in the table, go to PROCEDURE 5.

3. If the voltage does not conform to that given in the table, adjust the VR2 on the system PCB by a Phillips screwdriver.

TABLE 2-2 PJ 23 Adjustment

CONNECTOR	PIN NUMBER		VOLTAGE (Vdc)	
	+ lead	- lead	Min	Max
PJ 23	2	1	+ 2,18	+ 2,19

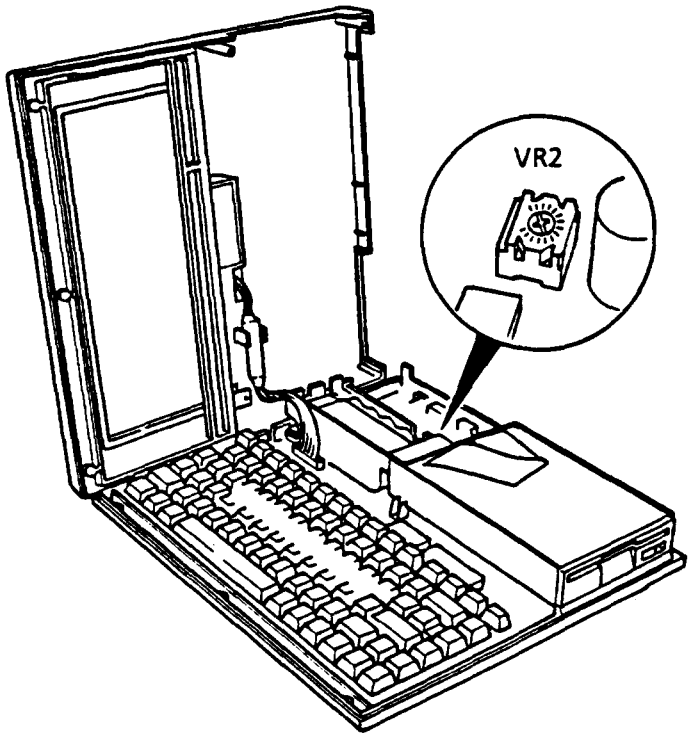


FIGURE 2-4 VR2 Adjustment

PROCEDURE 5

Battery Pack Replacement

1. Turn the POWER switch off.

2. Replace the battery pack. (Refer to part 4.5.)

3. If normal operation is restored after replacing the battery pack, the battery pack was defective.

4. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

2.4 SYSTEM PCB ISOLATION PROCEDURES

This section describes how to determine whether the system PCB is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Message Check

PROCEDURE 2: Printer Port LED Check

PROCEDURE 3: Jumper Straps Check

PROCEDURE 4: Test Program Execution

PROCEDURE 5: System PCB Replacement

NOTE: Before carrying out any of these procedures, make sure that there is not a floppy disk in the FDD.

PROCEDURE 1

Message Check

1. Turn the POWER switch on.

2. If the following message is displayed on the screen, go to PROCEDURE 4.

```
Toshiba Personal Computer MS-DOS Version 2.11/R2A

   (c) Copyright Toshiba Corporation 1983, 1987
   (c) Copyright Microsoft Corporation 1981, 1984

Expanded Memory Maneger Version 3.20
No EMS port
COMMAND Version 2.11V

C>echo off
  It is now February 26 1987,13:10:52.64
C>
```

3. If the above message is not displayed, check to see if any of the following messages are displayed.

TABLE 2-2 Error Messages

KEYBOARD ERROR
FDD ERROR
OPTION ROM ERROR
RTC ERROR

4. If any of the above messages are displayed, go to PROCEDURE 3.

5. If none of the above messages are displayed, go to PROCEDURE 2.

PROCEDURE 2

Printer Port LED Check

1. Turn the POWER switch off.
2. Plug the printer port LED into the PRT (printer) connector on the back of the unit.
3. Turn the POWER switch on while watching the printer port LED.
   The printer port LED will light at the same time that the POWER switch is turned on.
4. Read the final LED status as a hexadecimal value from left to right.
5. If the final LED status matches any of the error status and OK status values in the following table, go to PROCEDURE 4.
6. If the final LED status is **FEH**, go to PROCEDURE 2 and continue.

TABLE 2-3 Printer Port LED Error Status and OK Status

Test Name	Error Status	OK Status
BIOS ROM test	01H	11H
Timer (82C53) test	02H 03H	12H
DMAC (82C37) test	04H 05H	14H
RAM R/W test (first 16kbytes)	06H 07H	16H
PIC (82C59) test	08H 09H 0AH 0BH	1BH
Video RAM test	0CH	
Display controller test	0DH 0EH	

PROCEDURE 3

Jumper Strap Check

1. Turn the POWER switch off.
2. Remove the top cover assembly. (Refer to part 4.2.)
3. Confirm that the jumper straps status is normal. (Refer to part 1.2.1.)
4. If the jumper strap status is normal, go to PROCEDURE 4.
5. If the jumper strap status is not normal, set them correctly.

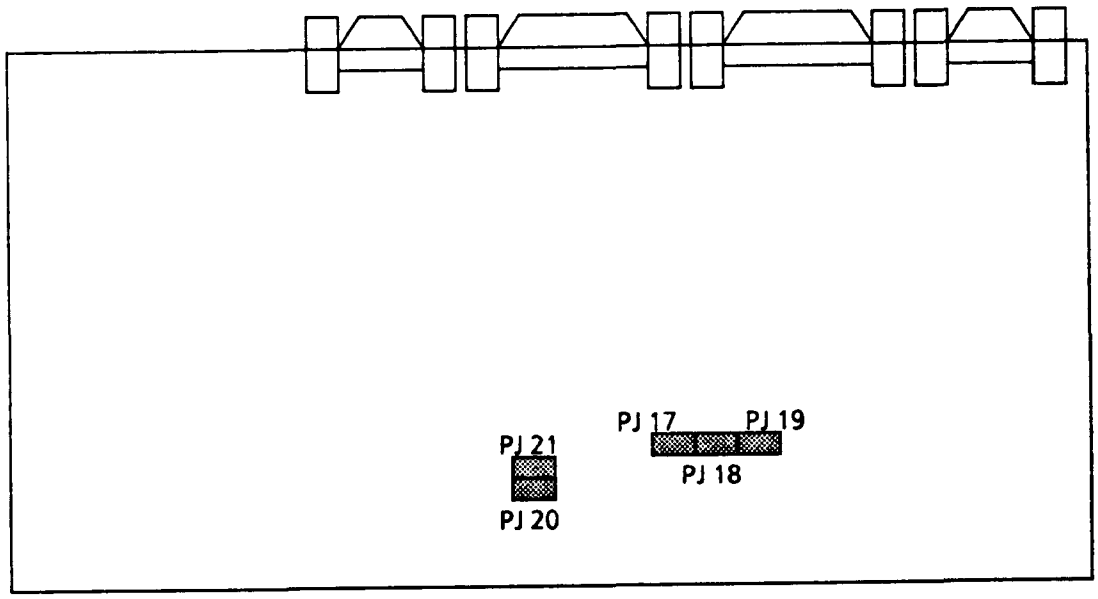


FIGURE 2-5 System PCB Jumper Straps

PROCEDURE 4

Test Program Execution

1. Execute the following test program. (See PART 3 TEST AND DIAGNOSTICS.)

    1. System test
    2. Memory test
    3. Keyboard test
    4. Display test
    5. Floppy disk test
    6. Real time test

2. If an error is generated on the system test, memory test, display test and real time test, go to PROCEDURE 5.

3. If an error is generated on the floppy disk test, go to FDD isolation procedures in part 2.5.

4. If an error is generated on the keyboard test, go to keyboard isolation procedures in part 2.6.

PROCEDURE 5

System PCB Replacement

1. Replace the system PCB. (Refer to part 4.8)

2. If normal operation is restored after replacing the PCB, the previous PCB was defective.

3. If normal operation is not restored, another FRU is probably defective. The defective unit must be isolated and replaced.

2.5 FLOPPY DISK DRIVE ISOLATION PROCEDURES

This section describes how to determine whether the floppy disk drive is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Test and Diagnostic Program Loading Check

PROCEDURE 2: Message Check

PROCEDURE 3: Head Cleaning

PROCEDURE 4: FDD Test Execution

PROCEDURE 5: FDD Connector Check

PROCEDURE 6: New FDD connection

PROCEDURE 1

Test and Diagnostic Programs Loading Check

1. Turn the POWER switch off.
2. Insert the diagnostics disk into the FDD.
3. Turn the POWER switch on.
4. If loading occurs normally, go to PROCEDURE 3. (See PART 3 to determine if loading has occurred normally.)
5. If loading has not occurred normally, go to PROCEDURE 2.

PROCEDURE 2

Message Check

1. When the diagnostics disk is inserted into the FDD and the POWER switch is turned on, the following message should appear.

(a)

```
Toshiba Personal Computer MS-DOS Version 2.11 / RXX

   (C) Copyright  Toshiba  Corporation 198X,198X
   (C) Copyright  Microsoft Corporation 198X,198X

COMMAND Version 2.11V

C>echo off
  It is now February 26 1987,13:10:52,64
C>
```

(b)

```
Non-System disk or disk error
Replace and press any key when ready
```

2. If the above messages is displayed, the contents of the floppy disk are damaged, or some other disk than the diagnostics disk has been inserted into the FDD. Change the diagnostics disk. If loading then occurs, go to PROCEDURE 4; if loading does not occur, go to PROCEDURE 3.

3. If the above messages appears, go to PROCEDURE 5.

PROCEDURE 3

Head Cleaning

1. Turn the POWER switch off.
2. Insert the cleaning disk to the FDD.
3. Turn the POWER switch on, then will clean the head of the FDD.
4. Remove the the cleaning disk from the FDD.
5. If normal operation is restored after cleaning the head, go to PROCEDURE 4.
6. If normal operation is not restored, go to PROCEDURE 5.

PROCEDURE 4

FDD Test Execution

1. Run the floppy disk test which is indicated in the Diagnostic Test Menu.

2. If an error is generated during the floppy disk test, an error code and status will be displayed as indicated in the following table. Go to PROCEDURE 6.

3. If no error is generated, the FDD is normal.

TABLE 2-4 FDD Error Statuses

CODE	STATUS
01	Bad Command
02	Address Mark Not Found
03	Write Protected
04	Record Not Found
06	Media removed on dual attach card
08	DMA Overrun Error
09	DMA Boundary Error
10	CRC Error
20	FDC Error
40	SEEK ERROR
60	FDD not drive
80	Time Out Error (Not Ready)
EE	Write buffer error

PROCEDURE 5

FDD Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 9V jack.
2. Remove the top cover assembly. (Refer to part 4.2.)
3. If the FDD cable is connected to the system PCB securely, go to PROCEDURE 6.
4. If the above connections are not secure, reconnect them.

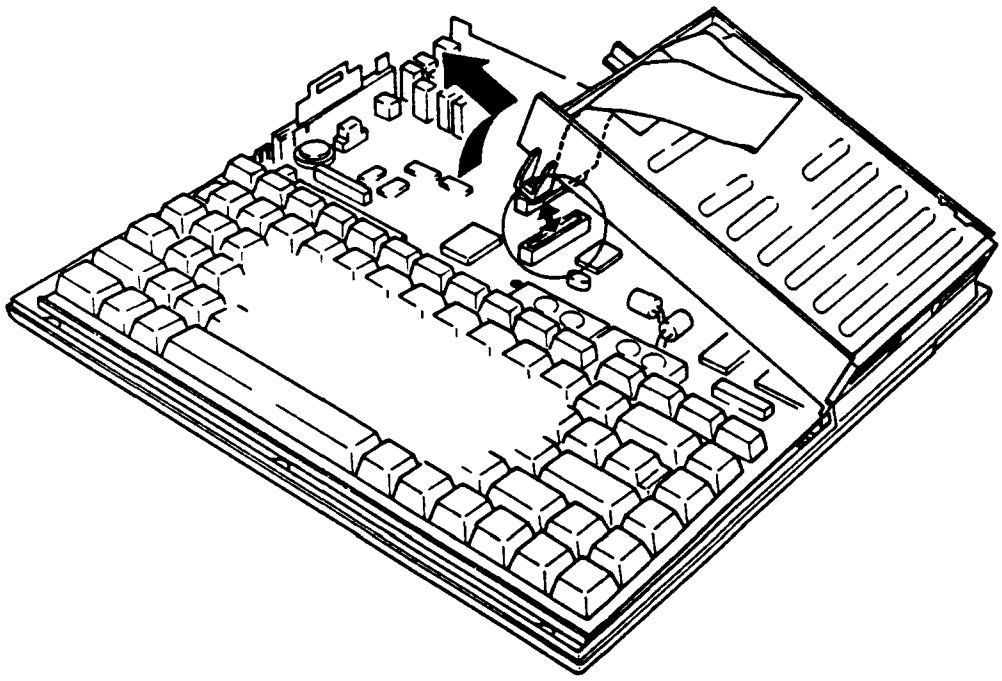


FIGURE 2-6 FDD Connector Check

PROCEDURE 6

New FDD Connection

1. Turn the POWER switch off.
2. Remove the FDD. (Refer to part 4.7.)
3. Connect the new FDD to the FDD connector, then other connectors too.
4. Turn the POWER switch on.
5. If normal operation is restored after connect the new FDD, the previous FDD was defective. Assemble the system.
6. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

2.6 KEYBOARD ISOLATION PROCEDURES

This section describes how to determine whether the keyboard is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Input Check

PROCEDURE 2: Keyboard Test Execution

PROCEDURE 3: Connector Check

PROCEDURE 4: New Keyboard Connection

PROCEDURE 1

Input Check

1. Load the diagnostics disk, DOS ROM or the MS-DOS system disk.

2. When a prompt (A, B, C, etc.) appears on the screen, hit any of the white keys on the keyboard (any character or the space bar). If the character you hit appears on the screen, go to PROCEDURE 2.

3. If the character does not appear, go to PROCEDURE 3.

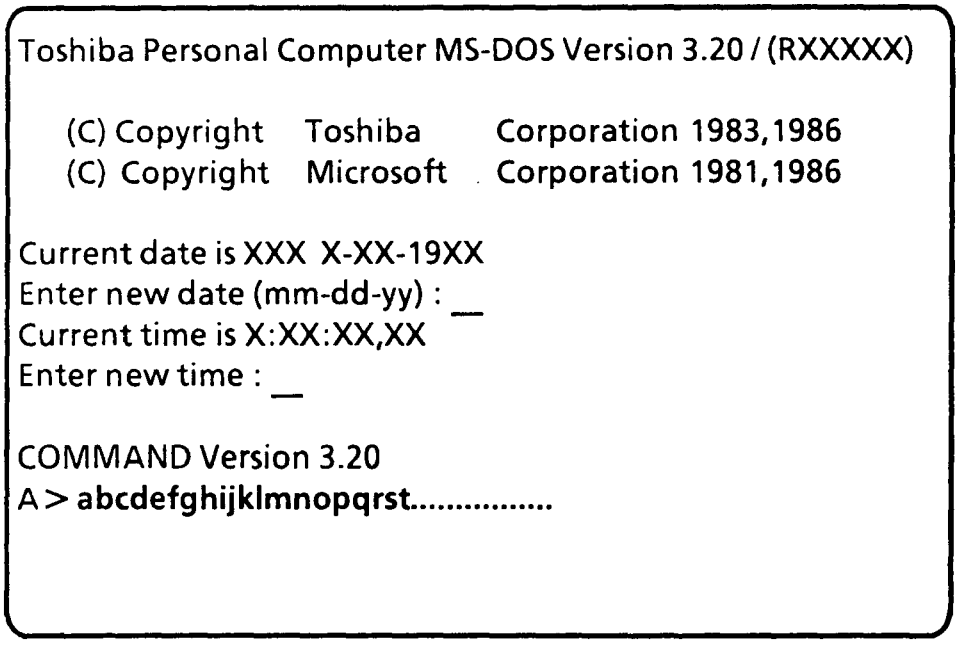


FIGURE 2-7 Keyboard Input Check

PROCEDURE 2

Keyboard Test Execution

1. Insert the diagnostics disk into the FDD and load the test and diagnostics programs. (Refer to PART 3.)

2. Run the keyboard test which is indicated in the diagnostics test menu.

3. If an error is generated during the test, go to PROCEDURE 3.

4. If no error is generated during the test, the keyboard is normal.

PROCEDURE 3

Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 9V jack.

2. Remove the top cover assembly. (Refer to part 4.2)

3. Lift up the keyboard and check that the keyboard cable is connected securely to the system PCB. If it is connected securely, go to PROCEDURE 4.

4. If it is not connected securely, reconnect it.

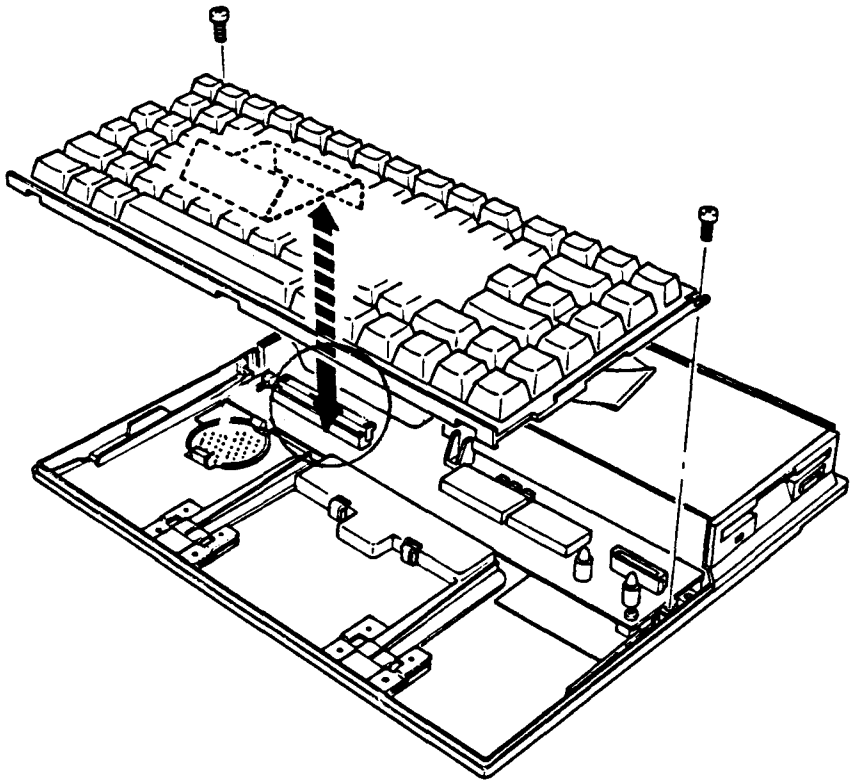


FIGURE 2-8 Keyboard Connector Check

PROCEDURE 4

New Keyboard Connection

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 9V jack.
2. Remove the keyboard unit. (Refer to part 4.4.)
3. Connect the new keyboard to the system PCB.
4. If normal operation is restored after connect the keyboard, the previous keyboard was defective. Assemble the system.
5. If normal operation is not restored, system PCB is probably defective. Refer to part 2.4.

2.7 LCD ISOLATION PROCEDURES

This section describes how to determine whether the LCD is defective or not. The procedures below are outlined in the following pages. They should be performed in the order indicated.

PROCEDURE 1: Display Check

PROCEDURE 2: LCD Contrast Check

PROCEDURE 3: Display Test Execution

PROCEDURE 4: System PCB Connector Check

PROCEDURE 5: LCD Module Connector Check

PROCEDURE 6: New LCD Cable Connection

PROCEDURE 7: New LCD Module Connection

PROCEDURE 1

Display Check

1. Turn the POWER switch off.

2. After turning the POWER switch on again, the following message should appear in the upper left-hand corner of the screen:

MEMORY TEST XXXKB

3. If the message appears, go to PROCEDURE 2.

4. If the message does not appear, first do the following:

   (a) Confirm that the contrast knob is adjusted correctly.

   (b) Confirm that the display is not on an external CRT.

   After confirming (a) and (b) above, perform steps 1 and 2 again. If the message still fails to appear, go to PROCEDURE 3.

PROCEDURE 2

LCD Contrast Check

1. Turn the contrast knob, then confirm that the screen becomes changed darker or brighter.

2. If the screen is changed darker or brighter, power supply inputs voltage to the LCD module. Go to PROCEDURE 7.

3. If the screen is not changed, go to PROCEDURE 4.

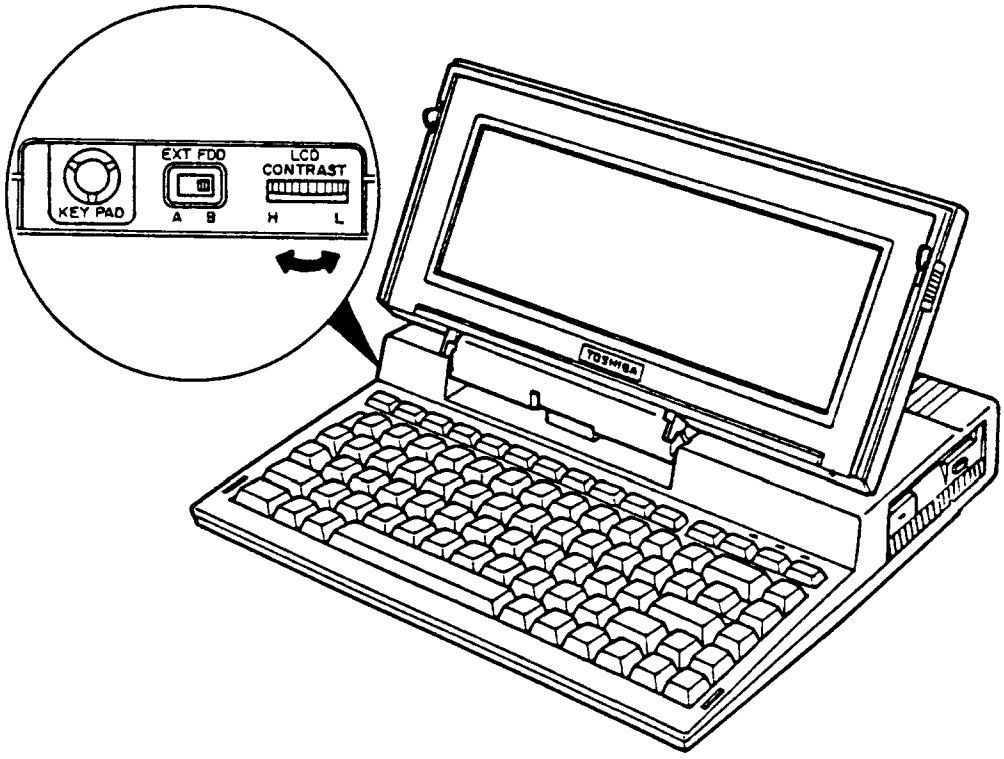


FIGURE 2-9 LCD Contrast Check

PROCEDURE 3

Display Test Execution

1. Insert the diagnostics disk into the FDD and run the test and diagnostics programs.

2. If an error is generated during the display test from the diagnostics test menu, the system PCB is probably defective. Refer to part 2.4.

3. If no error is generated, the display controller on the system PCB is normal.

PROCEDURE 4

System PCB Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 9V jack.
2. Remove the top cover assembly. (Refer to part 4.2.)
3. Confirm that the LCD cable is connected securely to the system PCB connector (PJ 14).
4. If the cable is connected securely, go to PROCEDURE 4.
5. If it is not connected securely, reconnect it.

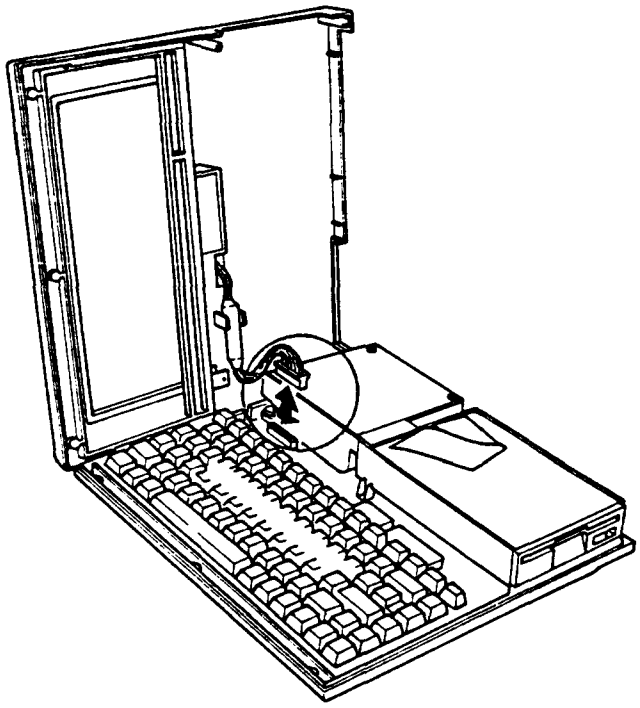


FIGURE 2-10 System PCB Connector Check

PROCEDURE 5

LCD Module Connector Check

1. Turn the POWER switch off and disconnect the ac adapter from the DC IN 9V jack.
2. Take out the LCD module (Refer to part 4.10.) and confirm that the LCD cable is connected securely to the module.
3. If the cable is connected securely, go to PROCEDURE 6.
4. If the cable is not connected securely, reconnect it.

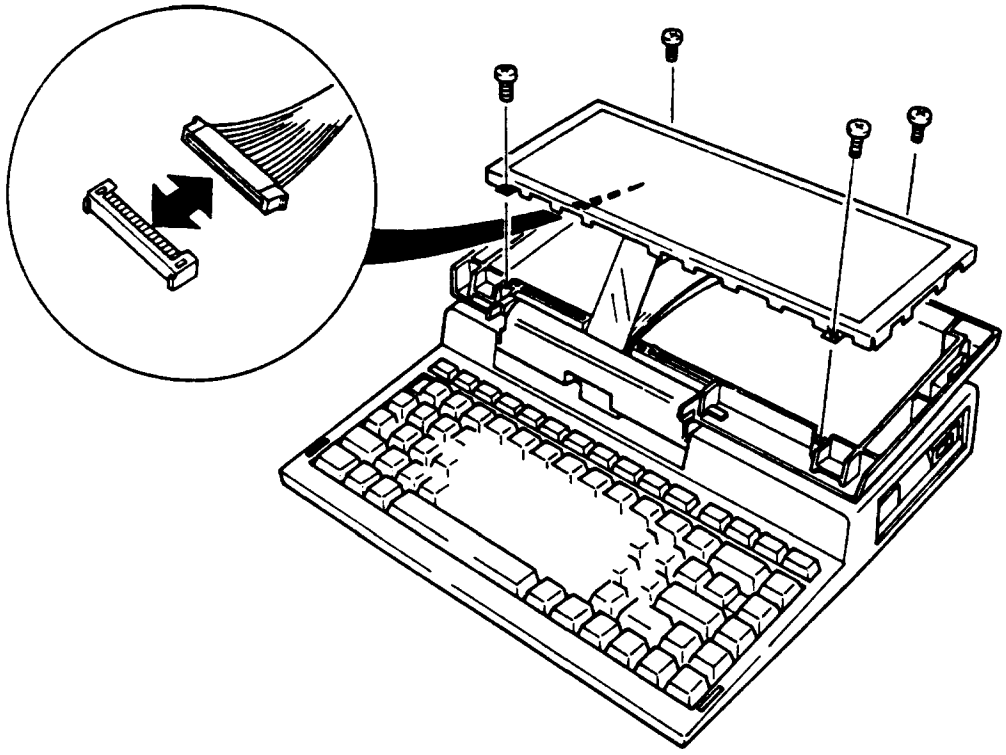


FIGURE 2-11 LCD Module Connector Check

PROCEDURE 6

New LCD Cable Connection

1. Connecte the new LCD cable to the system PCB and LCD module.
2. If normal operation is restored after replacing the LCD module, the previous LCD cable was defective. Assemble the system.
3. If normal operation is not restored, LCD module is probably defective. Go to PROCEDURE 7.

PROCEDURE 7

LCD Module Connection

1. Connect a new LCD module and LCD cable to the system PCB.

2. If normal operation is restored after replacing the LCD module, the previous LCD module was defective. Assemble the system.

3. If normal operation is not restored, system PCB is probably defective. System PCB is probably defective. Refer to part 2.4.

3.1 GENERAL

This part explains test and diagnostic programs. The purpose of the test and diagnostic programs is to check the functions of all hardware modules of the T1000 Personal Computer.
There are 13 programs; they are composed of two modules: the service program module (DIAGNOSTICS MENU) and test program module (DIAGNOSTIC TEST MENU).
The service program module is composed of 5 tasks:

1. HEAD CLEANING
2. LOG UTILITIES
3. RUNNING TEST
4. FDD UTILITIES
5. SYSTEM CONFIGURATION

The test program module is composed of 8 test as follows:

1. SYSTEM TEST
2. MEMORY TEST
3. KEYBOARD TEST
4. DISPLAY TEST
5. FLOPPY DISK TEST
6. PRINTER TEST
7. ASYNC TEST
8. REAL TIMER TEST

The following items are necessary for carrying out the test and diagnostic programs.

1. T1000 Diagnostics disk
2. MS-DOS system disk
3. Work disk (formatted)
4. Cleaning disk kit
5. Printer wraparound connector
6. RS232C wraparound connector

The service engineer utilizes these programs to isolate problems by selecting the appropriate program and operation procedures described in the part 3.2 OPERATIONS.

3.2 OPERATIONS

1. Insert the diagnostics disk in the floppy disk drive and turn the POWER switch on.

2. Input **TESTCE10** for the **A>** prompt and press Enter.

3. The following display will appear.

```
TOSHIBA personal computer T1000 DIAGNOSTICS
Version 0.02 (C) copyright TOSHIBA Corp. 1987

DIAGNOSTIC  MENU :

   1 - DIAGNOSTIC TEST
   2 -
   3 -
   4 - HEAD CLEANING
   5 - LOG UTILITIES
   6 - RUNNING TEST
   7 - FDD UTILITIES
   8 - SYSTEM CONFIGURATION
   9 - EXIT TO MS-DOS

PRESS [1] - [9] KEY
```

Detailed explanations of the service programs and the operations are given in parts 3.13 to 3.17.

4. Press 1 key then Enter. The following display will appear.

```
TOSHIBA personal computer T1000 DIAGNOSTICS
version 0.02 (C) copyright TOSHIBA Corp. 1987

DIAGNOSTIC  TEST MENU :

    1 - SYSTEM TEST
    2 - MEMORY TEST
    3 - KEYBOARD TEST
    4 - DISPLAY TEST
    5 - FLOPPY DISK TEST
    6 - PRINTER TEST
    7 - ASYNC TEST
    8 - REAL TIMER TEST
   88 - FDD & HDD ERROR RETRY COUNT SET
   99 - EXIT TO DIAGNOSTICS MENU

PRESS [1] - [9] KEY
```

If you want to set the FDD error retry count, type 88 then press Enter. The following message will appear.
If don't execute the operation, FDD error retry count is once.

FDD Error retry count ?

You can set the error retry count of the floppy disk test.

Type 99 then press Enter. Return to the DIAGNOSTICS MENU.

When select the FLOPPY DISK TEST, the following messages will appear.

Test drive number select (1:FDD1,2:FDD2,0:FDD1&2) ?

Media in drive#1 mode (1:360k,2:360k-1.2M/720k,3:1.2M,4:720k) ?

5. After pressing the test number (1 to 8) of the DIAGNOSTIC TEST MENU, the following display (sample) will appear.

```
TEST NAME                                    XXXXXXX

SUB TEST    : XX
PASS COUNT  : XXXXX       ERROR COUNT :  XXXXX
WRITE DATA  : XX          READ DATA   :  XX
ADDRESS     : XXXXX       STATUS      :  XXX

SUB-TEST MENU  :

01 - ROM CHECKSUM
 :   :
 :   :
99 - Exit to DIAGNOSTIC TEST MENU

SELECT SUB-TEST NUMBER ? _
TEST LOOP (1:YES/2:NO) ? _
ERRR STOP (1:YES/2:NO) ? _
```

6. Select the subtest number. Type the subtest number then press the Enter. The following message will appear.
When select the KEYBOARD TEST, the following message will not appear.

TEST LOOP (1:YES/2:NO) ?

When select the (YES);
At each time a test cycle ends, it increments the pass counter by one and repeats the test cycle..
When select the (NO);
At the end of a test cycle, it terminares the test execution and exits to the subtest menu.

7. Type the 1 or 2 then press Enter. The following message will appear.

ERROR STOP (1:YES/2:NO) ?

When select the (YES);
When an error occurs, it displays the error status and stops the execution of the test program. The operation guide displays on the right side of the display screen.
When select the (NO);
When an error occurs, it displays the error status then it increments the error counter by one and goes to the next test.

8. Type the 1 or 2 then press the Enter. The test program will run. Each subtest names described in the part 3.3.

9. When stop the test program, press Ctrl + Break keys then return to the DIAGNOSTICS MENU.

10. When error occors on the test program, the following message will appear.

ERROR STATUS NAME **[[HALT OPERATION]]**
1: Test End
2: Continue
3: Retry

1: Terminates the test program execution and exits to the subtest menu.
2: Continues the test.
3: Retry the test.

The error code and error status names described in part 3.12.

3.3 SUBTEST NAMES

The following table shows subtest name of the test program.

TABLE 3-1 Subtest Names

#	TEST NAME	SUBTEST#	TEST ITEMS
1	SYSTEM	01	ROM checksum
		02	MS-DOS ROM checksum
2	MEMORY	01	RAM constant data
		02	RAM address pattern data
		03	RAM refresh
		04	Backup RAM
		05	EMS function
3	KEYBOARD	01	Pressed key display
		02	Tenkey pad display
		03	Pressed key code display
4	DISPLAY	01	VRAM read/write
		02	Character attributes
		03	Character set
		04	80*25 Character display
		05	320*200 Graphics display
		06	640*200 Graphics display
		07	Display page
		08	"H" pattern display
		09	Special attribute test
5	FDD	01	Sequential read
		02	Sequential read/write
		03	Random address/data
		04	Write specified address
		05	Read specified address
6	PRINTER	01	Ripple pattern
		02	Function
		03	Wrap around
7	ASYNC	01	Wrap around (channel - 1)
		02	Wrap around (channel - 2)
		03	Point to point (send)
		04	Point to point (receive)
		05	Card modem loopback
		06	Card modem on-line test
		07	Dial tester test
9	REAL TIMER	01	Real time
		02	Real time carry

3.4 SYSTEM TEST

Subtest 01 ROM checksum (Execution time: 1 second)

This test performs the ROM checksum test on the system PCB.
(Test extent: F0000H to FFFFFH 64 Kbytes)

Subtest 02 MS-DOS ROM checksum (Execution time: 2 seconds)

This test performs the MS-DOS ROM checksum test on the system PCB.
(Test extent: A0000H to AFFFFH every 64 kbytes)
(Size: 256/512 kbytes)

3.5 MEMORY TEST

Subtest 01 RAM constant data (Execution time: 90 seconds)

This test writes constant data to Memory, and then reads and compares them with the original data.
The constant data are "FFFFH", "AAAAH", "5555H", "0101H" and "0000H".

Subtest 02 RAM address pattern data (Execution time: 28 seconds)

This test makes the segment address and offset address by XORing, and then writes the address pattern data and reads and compares them with the original data.

Subtest 03 RAM refresh (Execution time: 50 seconds)

This test writes constant data in 256 bytes length to Memory, and then reads and compares it with the original data. The constant data are "AAAAH" and "5555H". A certain interval time will be taken between the write and the read operations.

Subtest 04 Backup RAM (Execution time: 3 second)

This test writes data (FFH, AAH, 55H, 00H) to the backup memory (160 bytes) in the KBC (Keyboard controller); then read it the data out and compares it to the original data.
This test makes the offset address by XORing, and then writes the address pattern data and reads and compares them with the original data.

Subtest 05 EMS function (Execution time: 16 seconds; 384 kbytes)

CAUTION: The contents of the EMS (Expanded memory specification) will be erased when this test is run. After the test, enter the MS-DOS SETUP10 command, to set the EMS space. (See the OWNER'S manual for details).

Note: If the system doesn't have a expanded memory card (optional), this test cannot be executed.

Run the same test as subtest 04 for the EMS memory (384 kbytes) page frame address (D0000H) and the block select register (03H). This is performed for every 64kbytes.
Operations for the test is as follows.

1. After executing the test, the following message will appear.

   Warning: The contents of the EMS will be destroyed
   Press [Enter] key.

2. Press the Enter then the following message will appear.

   [EMS port = XXXH, BLOCK# = X, PAGE = XXXXX]

3. Automatically return to the subtest menu of the MEMORY TEST.

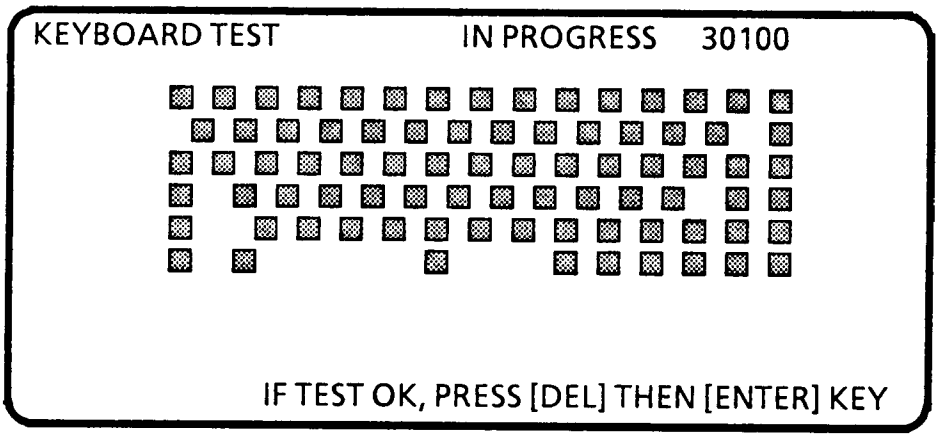
3.6 KEYBOARD TEST

Subtest 01 Pressed key display

Note: Execute the test when Num-lock key is off. If this key is on, the test cannot be carried out.

When the keyboard layout (as shown below) is drawn on the display, press a certain key and check whether the corresponding key on the screen is changed to the character "*".
When the same key again, it becomes to be the original state so that it is able to confirm the self-repeat function.
The following three keys are exceptions, and each key is changed to the character "*" only when it is pressed, and if released, it gets bach to the original state.

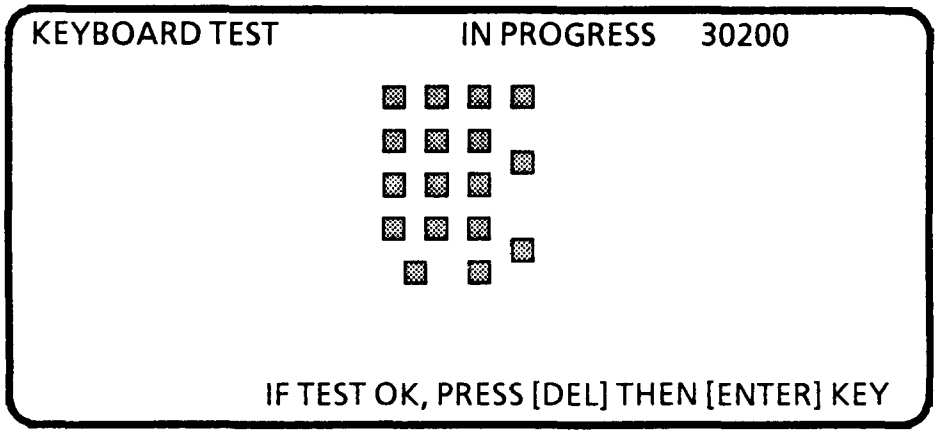
Ctrl key, Shift key, Alt key



Subtest 02 Tenkey pad display

Note: This test can be executed only when the Tenkey pad is connected to the key pad connector.

When the keyboard layout is drawn on the display, press a certain key of the tenkey pad, and confirm that the corresponding key on the display is changed to the character "*".
When the same key is pressed again, it gets back to the original stats so that it is able to confirm the self-repeat function.



Subtest 03 Pressed key code display

Scan code, character code, and key top name are displayed on the screen by pressing a certain key as shown below.
Some keys such as Ins, Caps lock, Num lock, Scroll lock, Alt, Ctrl, and shift key blink on the screen when each one is pressed.
Each scan code, character code and key top name described in the TABLE 3-2.(Next page)

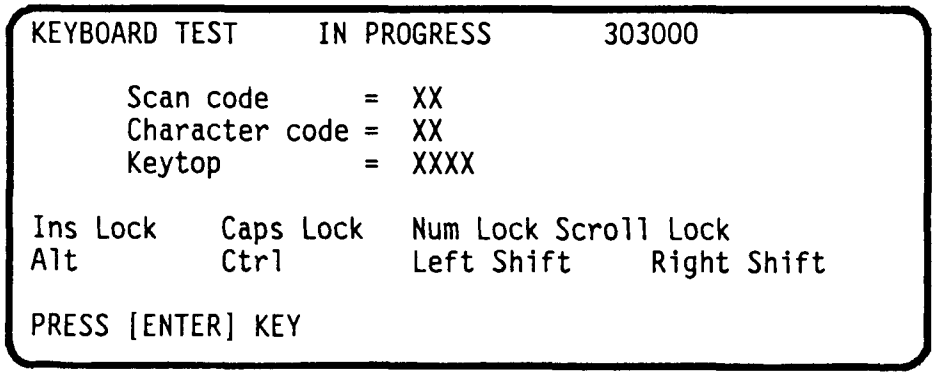


TABLE 3-2 Scan Code, Character Code, and Key Top Name

KEY TOP	SCAN CODE	CHARACTER CODE
`	29	60
1	02	31
2	03	32
3	04	33
4	05	34
5	06	35
6	07	36
7	08	37
8	09	38
9	0A	39
0	0B	30
-	0C	2D
=	0D	3D
\	2B	5C
←–	0E	08
–→	0F	09
q	10	71
w	11	77
e	12	65
r	13	72
t	14	74
y	15	79
u	16	75
i	17	69
o	18	6F
p	19	70
[	1A	5B
]	1B	5D
a	1E	61
s	1F	73
d	20	64
f	21	66
g	22	67
h	23	68
j	24	6A
k	25	6B
l	26	6C
;	27	3B

TABLE 3-2 Scan Code, Character Code, and Key Top Name

KEY TOP	SCAN CODE	CHARACTER CODE
'	28	27
z	2C	7A
x	2D	78
c	2E	63
v	2F	76
b	30	62
n	31	6E
m	32	6D
,	33	2C
.	34	2E
/	35	2F
Space	39	20
F2	3C	00
F4	3E	00
F6	40	00
F8	42	00
F10	44	00
F1	3B	00
F3	3D	00
F5	3F	00
F7	41	00
F9	43	00
Esc	01	1B
Home	47	00
←	4B	00
End	4F	00
Uper	48	00
Lower	50	00
Pg Up	49	00
→	4D	00
Pg Dn	51	00
Del	53	00
Sys Req	85	00
Prt Sc	37	2A
-	4A	2D
+	4E	2B

3.7 DISPLAY TEST

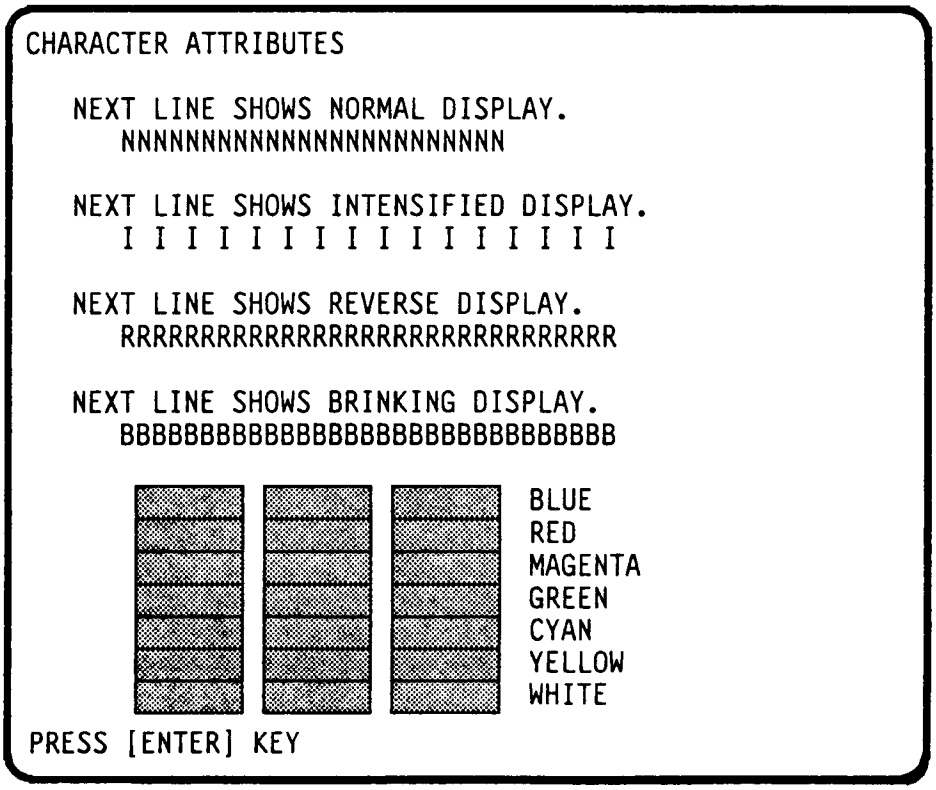
Subtest 01 VRAM read/write (Execution time: 1 second)

This test writes constant data (FFFFH, AAAAH, 5555H, 0000H) and address data to the video RAM; it then reads the data out and compares it the original data.

Subtest 02 Character attributes (Execution time: 1 second)

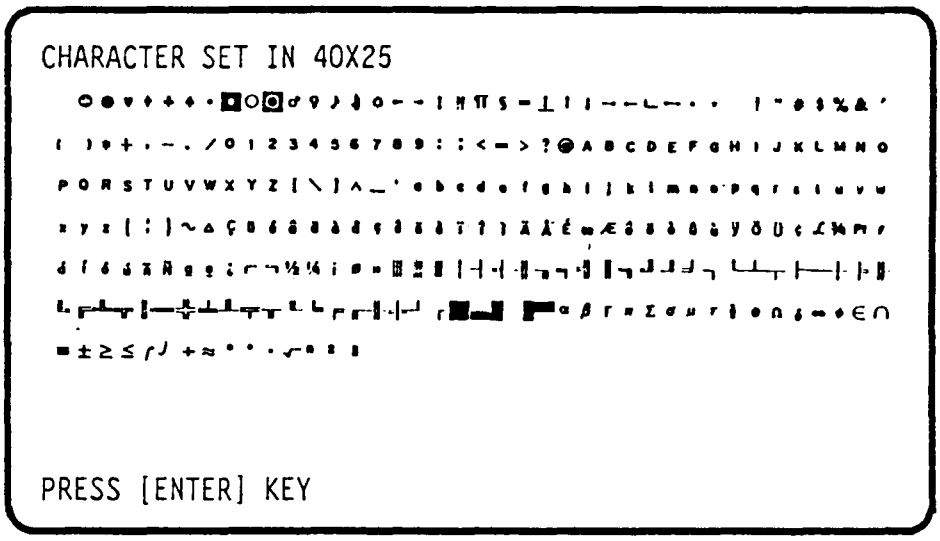
This test is for checking the various types of displays:

Normal Display
Intensified Display
Reverse Display
Blinking Display
In the case of color displays, all seven colors used (blue, red, magenta, green, cyan, yellow, white) are displayed. The background and foreground colors can then be checked for brightness. The display below appears on the screen when this test is run.



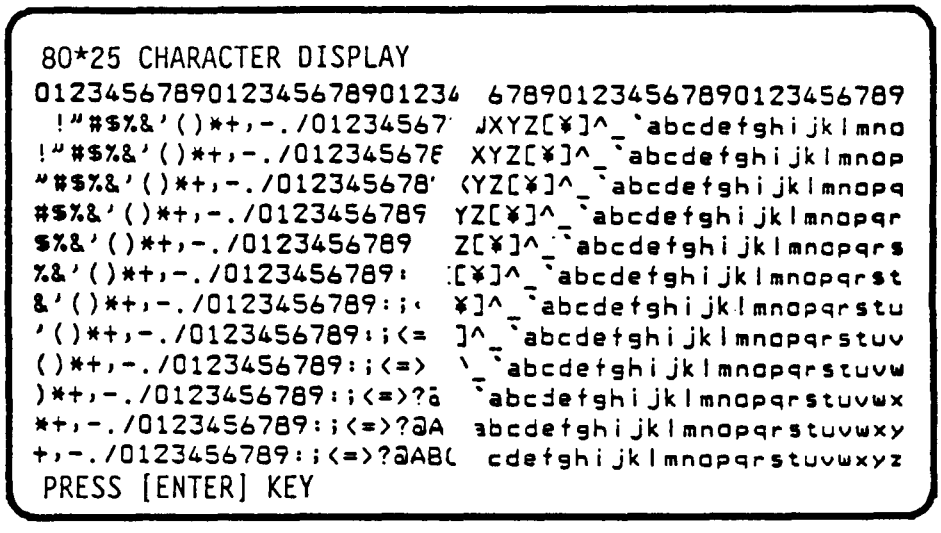
Subtest 03 Character set (Execution time: 1 second)

In this test the character code (00H to FFH) characters are displayed in the 40 x 25 pixel mode as shown below.



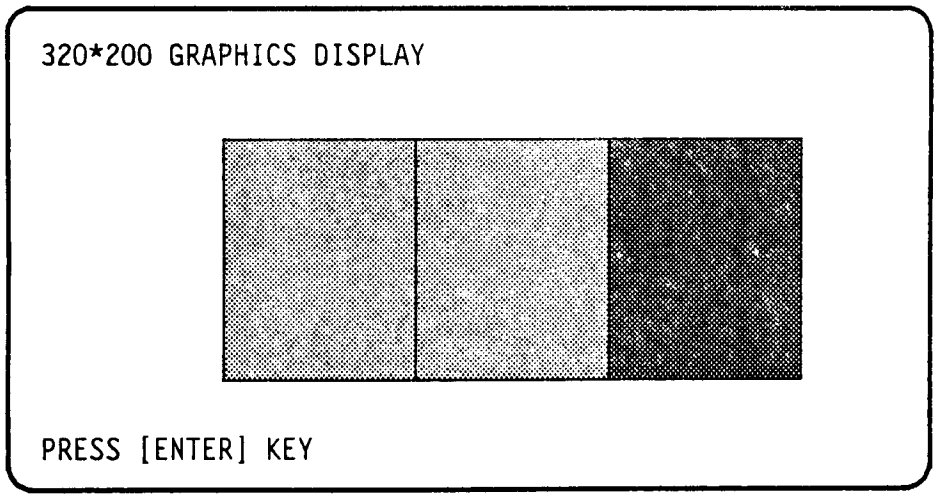
Subtest 04 80*25 Character display (Execution time: 1 second)

In this test the shift caracters are displayed in the 80 x 25 pixel mode as shown below.



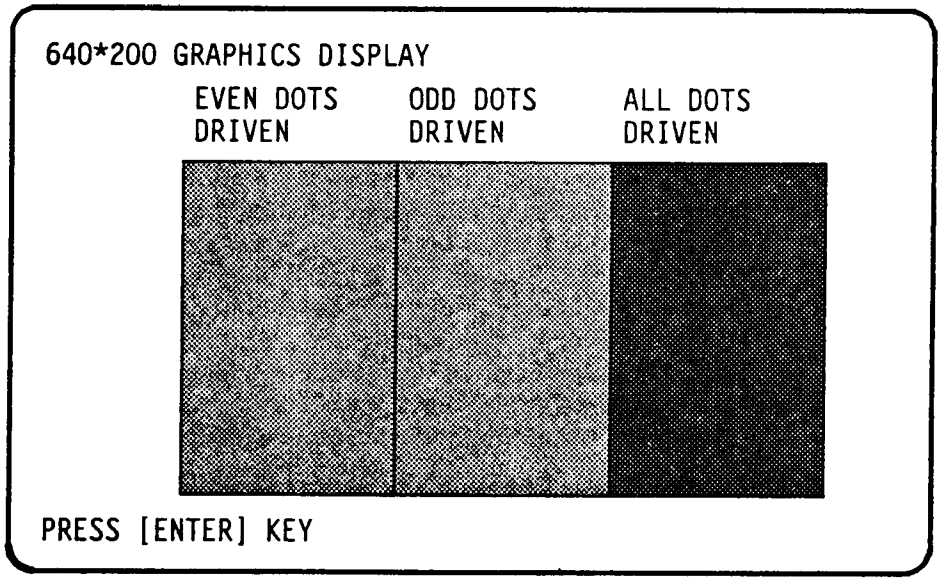
Subtest 05 320*200 Graphics display (Execution time: 3 seconds)

This test displays two sets of color blocks for the color display in the 320 x 200 dots graphics mode as shown below.



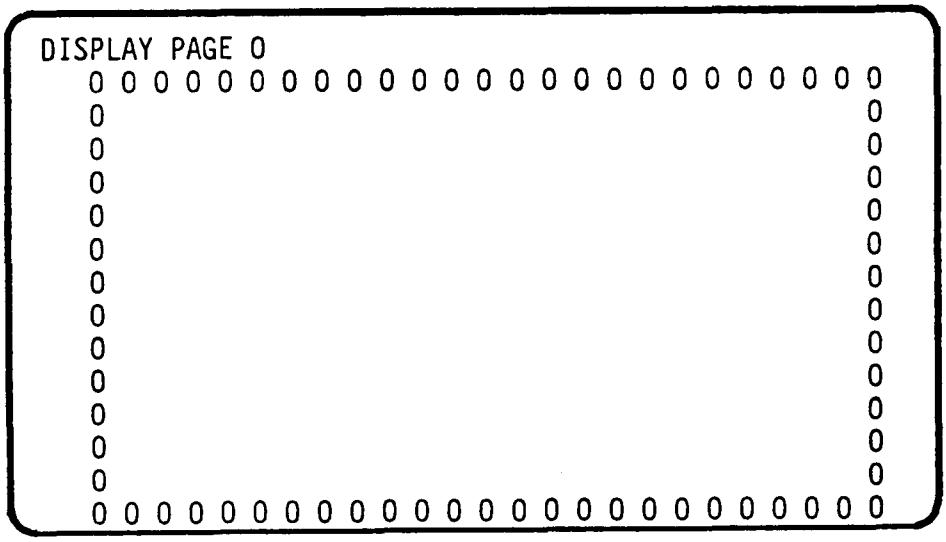
Subtest 06 640*200 Graphics display (Execution time: 3 seconds)

This test displays the color blocks for the black and white display in the 640 x 200 dot graphics mode as shown below.



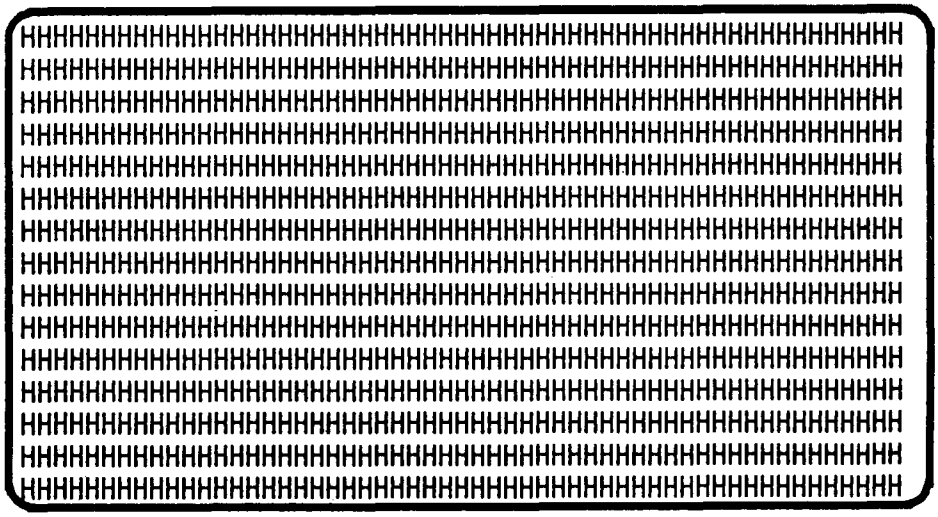
Subtest 07 Display page (Execution time: 15 seconds)

This test confirms that the pages can be changed in order (page 0 to page 7) in the 40 x 25 pixel mode.



Subtest 08 "H" pattern display (Execution time: 1 second)

This test displays H characters on the entire screen, as shown below.



Subtest 09 Special attribute test

This test executes the following test.
1. EXT/FDD SW test
2. Attribute special test

Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
[ EXT FDD select SW test ]

      Change "EXT FDD" SW ! = [[[ XXX ]]]


Press [ENTER] KEY
```

   Confirm that the above message **[[[XXX]]]** changes when it is specified by EXT FDD switch.

2. After pressing the Enter, the following message will appear.

```
[ FONT change test ]

   Press [ Fn + -> ] key !


Press [ENTER] KEY
```

   Confirm that the font of the above message cheages by pressing the Fn + -> keys.

3. After pressing the Enter, the following message will appear.

```
[ Attribute special test ]

 (1) FG(non-zero),  BG(zero)   ,R18(bit1,0) ... Double

 (2) FG(non-zero) NE BG(non-zero),R18(bit3,2) ...


PRESS [ENTER] KEY
```

   Confirm that the character font changes by pressing Enter.

5. After pressing Enter, return to the subtest menu of the DISPLAY TEST.

3.8 FLOPPY DISK TEST

CAUTION: Before running the floppy disk test prepare a formatted work disk and remove the diagnostics disk then insert the work disk to the FDD.

Subtest 01 Sequential read (Execution time: 63 seconds)

This test performs a cyclic redundancy check with a continuous read operation of all track on a floppy disk.
2D (Double-sided, double density): Track 0 to 39
2DD (Double-sided, double density, double track): Track 0 to 79

Subtest 02 Sequential read/write (Execution time: 130 seconds)

This test writes data to all tracks (as defined above) continuously and then reads the data out and compares it to original data.
(The data pattern is B5ADADH repeated.)

Subtest 03 Random address/data (Execution time: 12 seconds)

This test writes random data to random address on all tracks (as defined in subtest 01) and then reads the data out and compares it with the original data.

Subtest 04 Write specified address (Execution time: 1 second)

This test writes data specified by keyboard to tracks, heads, and address specified by the keyboard.

Subtest 05 Read specified address (Execution time: 1 second)

This test reads data from tracks, heads, and address specified by keyboard.

3.9 PRINTER TEST

CAUTION: A printer (IBM compatible) must be looked up to the system in order to execute the test.

Subtest 01 Ripple pattern (Execution time: 110 seconds)

This test prints character for code 20H through 7EH line by line while shifting one character to the right at the beginning of each new line.

```
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmn
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmno
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnop
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopq
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqr
%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrs
&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrst
'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrstu
()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrstuv
)*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrstuvw
*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmnopqrstuvwx
```

Subtest 02 Function (Execution time: 15 seconds)

This test prints out various print type as shown below.

Normal Print
Double Width Print
Compressed Print
Emphasized Print
Double Strike Print
All Characters Print

```
   PRINTER TEST
1.  THIS LINES SHOWS NORMAL PRINT.
2.  THIS LINE SHOWS DOUBLE WIDTH PRINT.
3.  THIS LINE SHOWS COMPRESSED PRINT.
4.  THIS LINE SHOWS EMPASIZED PRINT.
5.  THIS LINE SHOWS DOUBLE STRIKE PRINT.
  ALL CHARACTERS PRINT

 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[¥]^_`abcdefghijklmn
opqrstuvwxyz{|}~
```

Subtest 03 Wrap around (Execution time: 1 second)

Note: A printer wraparound connector is necessary for executing this test. Wiring diagram of the printer wrap around connector described in the part 3.18.

Checks the data, control, and status lines with the printer wrap around connector.

3.10 ASYNC TEST

For subtest 01 to subtest 05, transmission is done as follows in the communication.

Speed: 9600 BPS
Data: 8 bits + parity (EVEN)
1 stop bit
20H to 7EH

Subtest 01 Wrap around (channel 1) (Execution time: 1 second)

Note: An RS232C wrap around connector must be connected to channel 1 to execute this test. RS232C wrap around connector wiring diagram described in part 3.18.

Performs a data send/receive test with the wrap around connector for the channel 1.

Subtest 02 Wrap around (channel 2) (Execution time: 1 second)

Performs the same test as subtest 01 for the channel 2.

Subtest 03 Point to point (send) (Execution time: 1 second)

Note: This test can be executed on condition that the both send and receive sides are set in the same condition, and also connected together by RS232C direct cable (Wiring diagram described in part 3.18.). Subtest 03 must be executed together with subtest 04 and vice versa.

In this test, the data (20H to 7EH) are sent as one block from one side to the other, and then returned from the later one to the first side again.
This test is used to check wheter the returned data are same as the original ones.

Subtest 04 Point to point (receive) (Execution time: 1 second)

This test is exactly the same as subtest 03 except that the data flow is completely opposite.

Subtest 05 Card modem loopback (Execution time: 5 seconds)

Note: If there is no modem card in the system, this test can not be executed.

This test is used to check whether the data, which is from the modem to the RS232C inside the system, is same as the original data which had first been sent to the modem card.

Subtest 06 Card modem on-line test (Execution time: 10 seconds)

Note: After the system is connected to the PBX, unless the receive side is in the same status as the send side, the test cannot be executed.

In this test, first some data are sent to the modem card from the RS232C inside the system, then the data is again sent to the other system through the PBX (Private Branch Exchange).
This test is used whether the returned data from the other system are same as the original data.

Subtest 07 Dial tester test (Execution time: 60 seconds)

Note: To execute this test, a dial tester must be connected to the system.

This test is carried out by sending the pulse dial and tone dial twice automatically.

[Pulse dial]: "1-2-3-4-5-6-7-8-9-0-1-2"
[Tone dial]: "1-2-3-4-5-6-7-8-9-*-0-#"

3.11 REAL TIMER TEST

Subtest 01 Real time

A new data and time can be input during this test when the current data and time are displayed. Operations for the test is as follows.

1. After executing the test, the following message will appear.

```
REAL TIME TEST                          901000

   Current date:  XX-XX-XXXX
   Current time:  XX:XX:XX

   Enter new date:

PRESS [ENTER] KEY TO EXIT TEST
```

2. If current date is not correct, input the current new date. Press the Enter, the **Enter new time:** message will appear.

3. If current time is not correct, input the current new time. Press the Enter, return to the subtest menu of the REAL TIME TEST.

Subtest 02 Real time carry

CAUTION: When this test is executed, the current data and time is erased.

This test checks whether the real-time clock increments the time displayed cerrectly (month, day, year, hour, minute, second).

3.12 ERROR CODE AND ERROR STATUS NAMES

The following table shows the error code and error status names.

TABLE 3-3 Error Code and Error Status Names

DEVICE NAME	ERROR CODE	ERROR STATUS NAME
EVERYTHING	FF	Compare error
SYSTEM	01	ROM Checksum Error
MEMORY	01	Parity Error
FDD	01	Bad Command
	02	Address Mark Not Found
	03	Write Protected
	04	Record Not Found
	06	Media removed on dual attach card
	08	DMA Overrun Error
	09	DMA Boundary Error
	10	CRC Error
	20	FDC Error
	40	SEEK ERROR
	60	FDD not drive
	80	Time Out Error (Not Ready)
	EE	Write buffer error
PRINTER	01	Time Out
	08	Fault
	10	Select Line
	20	Out Of Paper
	40	Power off
	80	Busy Line
RS232C	01	DSR Off Time Out
	02	CTS Off Time Out
	04	RX EMPTY Time Out
	08	TX BUFFER FULL Time Out
	10	Parity Error
	20	Framing Error
	40	Overrun Error
	80	Line Status Error
	88	Modem Status Error
	33	NO CARRIER (CARD MODEM)
	34	ERROR (CARD MODEM)
	36	NO DIAL TONE (CARD MODEM)

3.13 HEAD CLEANING

3.13.1 Program description

This program executes head loading and seek/read operations for head cleaning. A cleaning kit is necessary for cleaning the FDD head.

3.13.2 Operations

1. After pressing 4 and Enter to select from the DIAGNOSTICS MENU, the following message will appear.

```
HEAD CLEANING

Mount cleaning disk(s) on drive(s).
Press any key when ready.
```

2. After the above message appears, remove the Diagnostics disk, insert the cleaning disk, and press any key.

3. When the following message appears, FDD head cleaning will begin.

```
HEAD CLEANING

Mount cleaning disk(s) on drive(s).
Press any key when ready.
     Cleaning start
```

4. When cleaning is finished, the display automatically returns to the DIAGNOSTICS MENU.

3.14 LOG UTILITIES

3.14.1 Program description

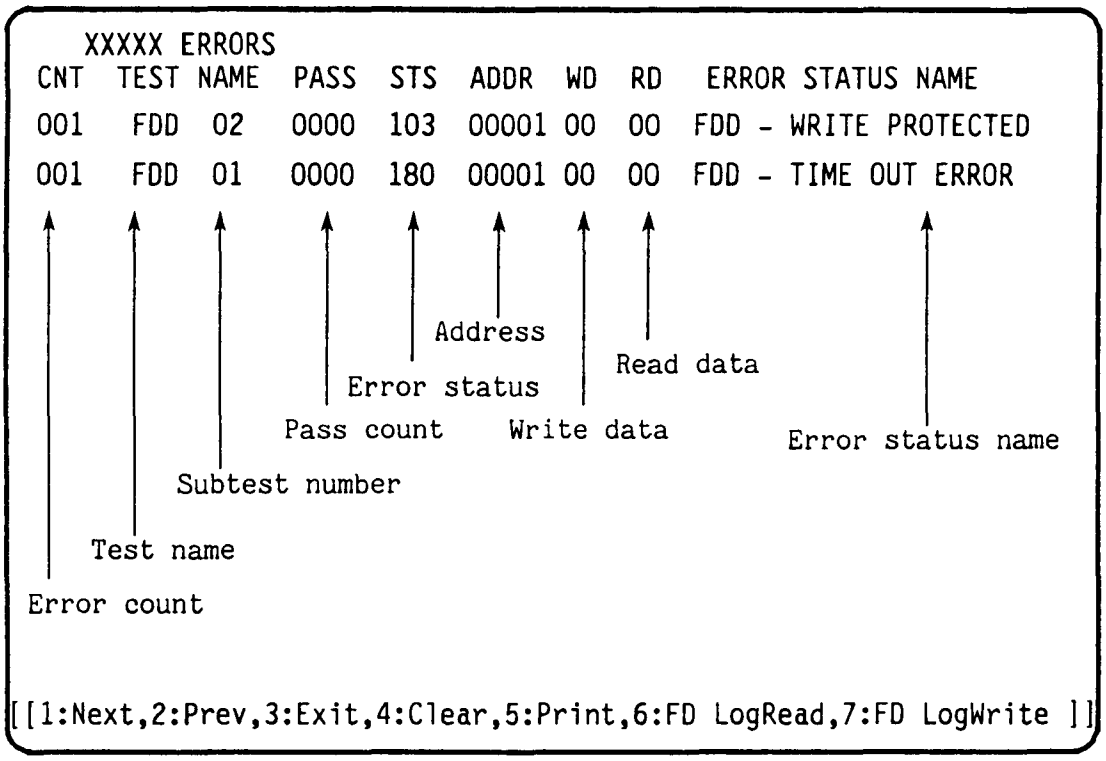
This program logs error information generated, while a test is in progress; the information is stored in the RAM.
However if the POWER switch is turned off the error information will be lost. The error information itself is displayed as the following.

1. Error count (CNT)
2. Test name (TEST)
3. Subtest number (NAME)
4. Pass count (PASS)
5. Error status (STS)
6. Address (FDD, HDD 1 or memory; ADDR)
7. Write data (WD)
8. Read data (RD)
9. Error status name

This program can store data on a floppy disk or output information to a printer.

3.14.2 Operations

1. After pressing 5 and Enter to select from the DIAGNOSTICS MENU, the error information logged in the RAM or on the floppy disk is displayed as shown below.



2. Error information to be displayed on the screen can be manupulated with the following key operation.

   The 1 key scrolls the display to the next page.
   The 2 key scrolls the display to the previous page.
   The 3 key returns the display to the DIAGNOSTIC MENU.
   The 4 key erases all error log information in RAM.
   The 5 key outputs error log information to a printer.
   The 6 key reads log information from a floppy disk.
   The 7 key writes log information to a floppy disk.

3.15 RUNNING TEST

3.15.1 Program description

This program automatically runs the following tests in sequence.

1. System test (subtest number 01, 02)
2. Memory test (subtest number 01, 02, 03, 04)
3. Display test (subtest number 01 to 07)
4. FDD test (subtest number 02)
5. Printer test (subtest number 03)
6. Async test (subtest number 01)

When running an FDD test, this system automatically decides whether there are one or two FDDs.

3.15.2 Operations

CAUTION: Do not forget to load a work disk. If a work disk is not loaded, an error will be generated during FDD testing.

1. Remove the diagnostics disk and insert the work disk into the floppy disk drive.

2. After pressing 6 and Enter to select from the DIAGNOSTIC MENU, the following message will appear.

   Printer wrap around test (Y/N) ?

3. Select whether to execute the printer wraparound test (Yes) or not (No). Type the desired Y or N and press Enter key. (If Y is selected, a wraparound connector must be connected to the printer connector on the back of the unit.) The following message will appear.

   Async wrap around test (Y/N) ?

4. Select whether to execute the test (Yes) or not (No). Type the desired Y or N and press Enter Key. (If Y is selected, an RS232C wraparound connector must be connected to the COMMS connector on the back of the unit.)

5. This program is repeated continuously. To stop the program, press Ctrl + Break key.

3.16 FDD UTILITEIS

3.16.1 Program description

These programs format and copy floppy disks, and display dump list for both the FDD and the HDD.

1. **FORMAT**

This program can format floppy disk (5.25"/3.5") as follows.

(a) **2D:** Two-sided, double-density, 48 TPI, MFM mode, 512 bytes, 9 sectors/track.
(b) **2DD:** Two-sided, double-density, double-track, 96 TPI, MFM mode, 512 bytes, 15 sectors/track.
(c) **2HD:** Two-sided,high-density, double-track, 96/135 TPI, MFM mode, 512 bytes, 15 sectors/track.

2. **COPY**

This program copies floppy disks.

Copy with one FDD (Drive A)
Copy with two FDDs (Drive A to Drive B)

3. **DUMP**

This program display the contents of floppy disks (both 3.5" and 5.25") and hard disks (designated sectors).

3.16.2 Operations

1. After pressing 7 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear before program execution.

```
[FDD UTILITIES]

   1 : FORMAT
   2 : COPY
   3 : DUMP
   9 : EXIT TO DIAGNOSTICS MENU

PRESS [1] - [9] KEY
```

2. **FORMAT** Selection

(1) When **FORMAT** is selected, the following message appears.

```
DIAGNOSTICS - FORMAT
Drive number select (1:A, 2:B) ? _
```

(2) Select a drive number. Type the number and the following message will then appear.

Type select (1:2D-04D,2:2D-08DE,3:2HD-08DE,4:2DD-2DD)

(3) Select a media-drive type number. Type the number and the following message will appear.

```
Warning : Disk data will be destroyed.

Insert work disk in to drive A :
Press any key when ready.
```

(4) Remove the diagnostics disk from the FDD and insert the work disk; press any key.
The **Format start** message will appear; formatting is then executed. After the floppy disk is formatted, the following message will appear.

Format complete
Another format (1:Yes/2:No) ?

(5) If you type 1 and press Enter key, the display will return to the message in (3) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

3. **COPY** Selection

(1) When **COPY** is selected, the following message will appear.

```
DIAGNOSTICS - COPY
Type select (1:2D-04D,2:2D-08DE,3:2HD-08DE,4:2DD-2DD) ?_
```

(2) Select a media/drive type number. Type the number. The following message will then appear.

```
Insert source disk into drive A :
Press any key when ready.
```

(3) Remove the diagnostics disk from the FDD and insert the source disk; press any key. The **Copy started** message will then appear. After that, the following message will appear.

```
Insert target disk into drive A :
Press any key when ready.
```

(4) Remove the source disk from the FDD and insert the work disk (formatted); press any key. When coping can not be done with one operation, message (2) is displayed again. Repeat the operation. After the floppy disk has been copied, the following message will appear.

```
Copy complete
Another copy (1:Yes/2:No) ?
```

(5) If you type 1 the display will return to the message in (1) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

4. **DUMP** Selection

(1) When **DUMP** is selected, the following message will appear.

```
[HDD&FLOPPY DISK DATA DUMP]
format type select (0:2DD,1:2D,2:2HD,3:HDD) ? _
```

(2) Select a format type number. Type the number. If 3 is selected, the dump lists for the hard disk are displayed automatically.

0: Display a dump list for a floppy disk (2DD)
1: Display a dump list for a floppy disk (2D).
2: Display a dump list for a floppy disk (2HD).
3: Displays a dump list for a hard disk.

(3) If 0, 1, or 2 is selected, the following message will appear.

Select FDD number (1:A/2:B) ?

(4) Select an FDD drive number; the following message will then appear.

```
Insert source disk into drive A :
Press any key when ready.
```

(5) Remove the diagnostics disk from the FDD and insert a source disk; press any key. The **Track number ??** message will then appear. Type the track number and press Enter.

(6) The **Head number ?** message will then appear. Type the head number and press Enter.

(7) The **Sector number ??** message will then appear. Type the sector number and press Enter. The dump list for the floppy disk will be displayed.

(8) After a dump list appears on the screen, the **Press number key (1:up,2:down,3:end) ?** message will appear.

1. Displays the next sector dump.
2. Displays a previous sector dump.
3. Displays the following message.

Another dump (1:Yes/2:No) ?

(9) If you type 1 the display will return to the message shown after (4) above. If you type 2 the display will return to the DIAGNOSTICS MENU.

3.17 SYSTEM CONFIGURATION

3.17.1 Program description

This program displays the following system configuration.

1. Memory size
2. Display type
3. Floppy disk drive number
4. Async port number
5. Hard disk drive number
6. Printer port number

3.17.2 Operations

After pressing 8 and Enter key to select from the DIAGNOSTICS MENU, the following display will appear.

```
SYSTEM CONFIGURATION :

 * - 512KB MEMORY
 * - LCD
 * - 1 FLOPPY DISK DRIVE(S)
 * - 1 ASYNC ADAPTOR
 * - 1 PRINTER ADAPTOR




PRESS [ENTER] KEY
```

Press Enter key to return to the DIAGNOSTICS MENU.

3.18 WIRING DIAGRAM

1. Printer wrap around connector

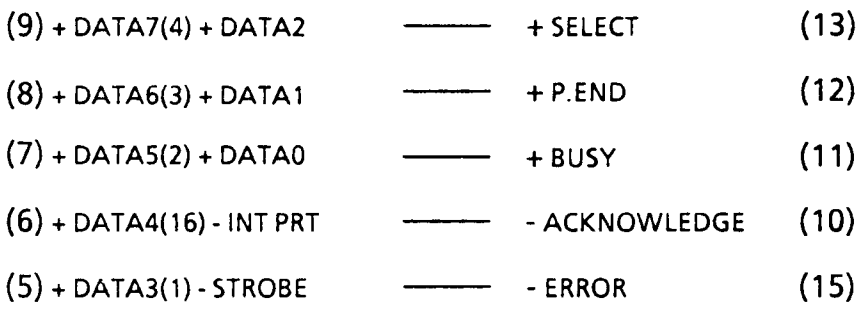


FIGURE 3-1 Printer Wrap Around Connector

2. RS232C Wrap around connector

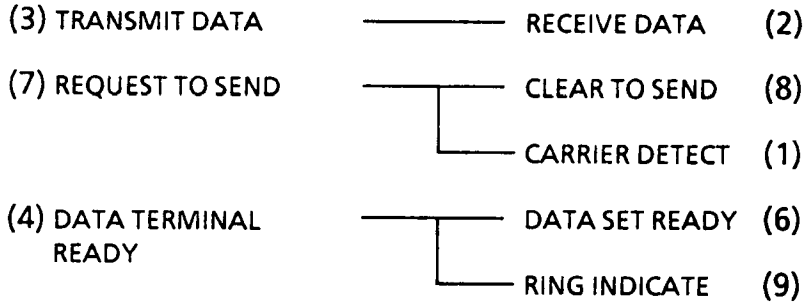


FIGURE 3-2 RS232C Wrap Around Connector

3. RS232C direct cable (9-pin to 9-pin)

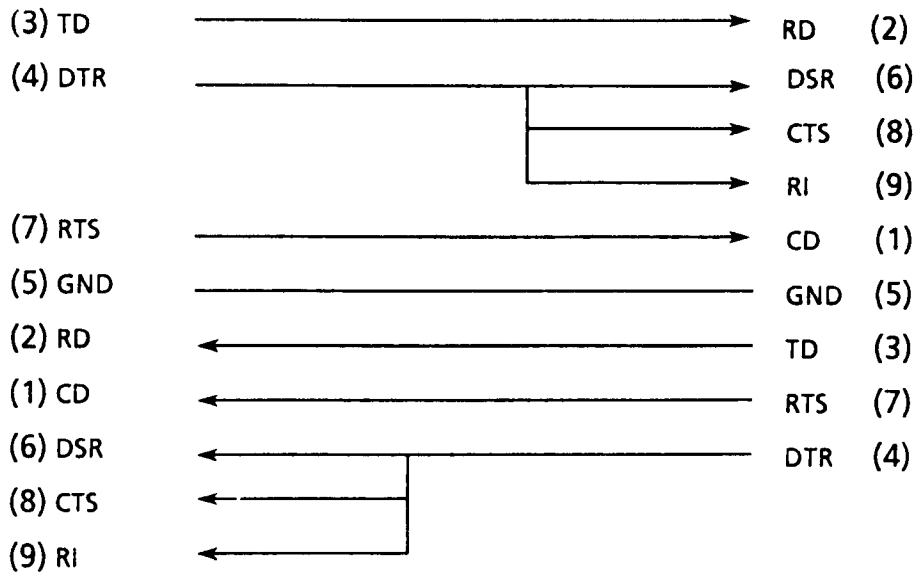


FIGURE 3-3 RS232C Dilect Cable (9-pin to 9-pin)

4. RS232C dilect cable (9-pin to 25-pin)

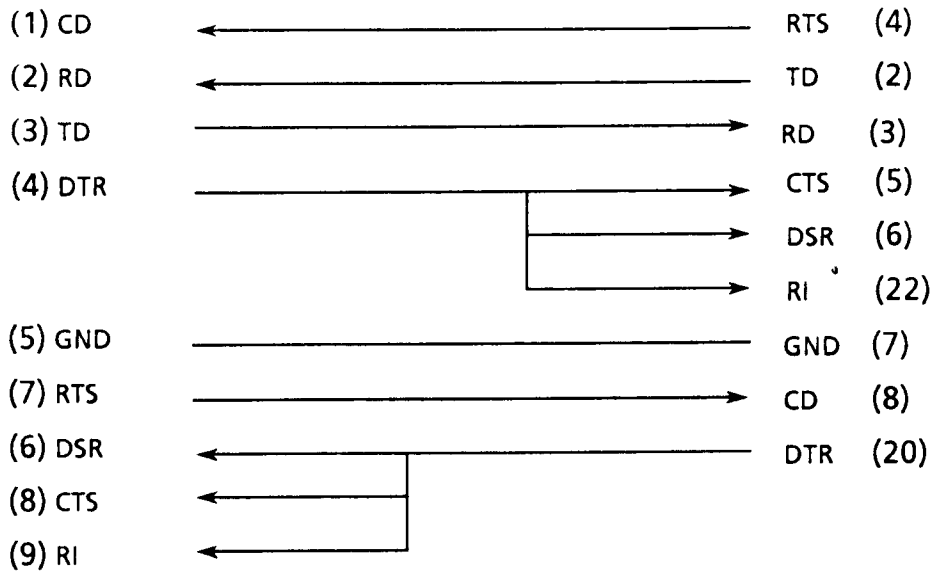


FIGURE 3-4 RS232C Dilect Cable (9-pin to 25-pin)

4.1 GENERAL

This section gives a detailed description of the procedures used to replace FRUs (field replaceable units).

FRUs consist of the following:

1. Top Cover Assembly
2. Keyboard Unit
3. Speaker
4. Battery Box
5. Battery Assembly
6. FDD (Floppy Disk Drive) Box
7. FDD
8. System PCB
9. LCD Mask
10. LCD Module
11. LCD Cover Subassembly

The following points must be kept in mind:

1. The system should never be disassembled unless there is a problem (abnormal operation, etc.).
2. Only approved tools may be used.
3. After deciding the purpose of replacing the unit, and the procedures required, do not carry out any other procedures which are not absolutely necessary.
4. Be sure to turn the POWER switch off before beginning.
5. Be sure to disconnect the ac adapter and all external cables from the system.
6. Follow only the fixed, standard procedures.
7. After replacing a unit, confirm that the system is operating normally.
8. Even if the POWER switch is turned off, the system is still supplied with electric current by the battery. During maintenance activity, you should take enough care so that no short circuit will occur on the system PCB.

Tools needed for unit replacement:

1. Phillips Screwdriver
2. Tweezers

4.2 REMOVING/REPLACING THE TOP COVER ASSEMBLY

The top cover consists of the top cover (A), LCD mask (B), LCD module (C) and LCD cover (D).

NOTE: Replacement procedures for these items are detailed in parts 4.9 to 4.12.

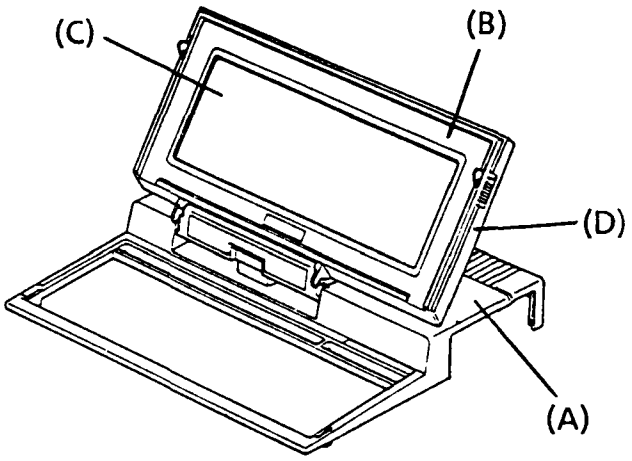


FIGURE 4-1 Top Cover Assembly

1. Confirm that the POWER switch is off.

2. Turn the unit upside down and remove the six screws (E) from the base subassembly.

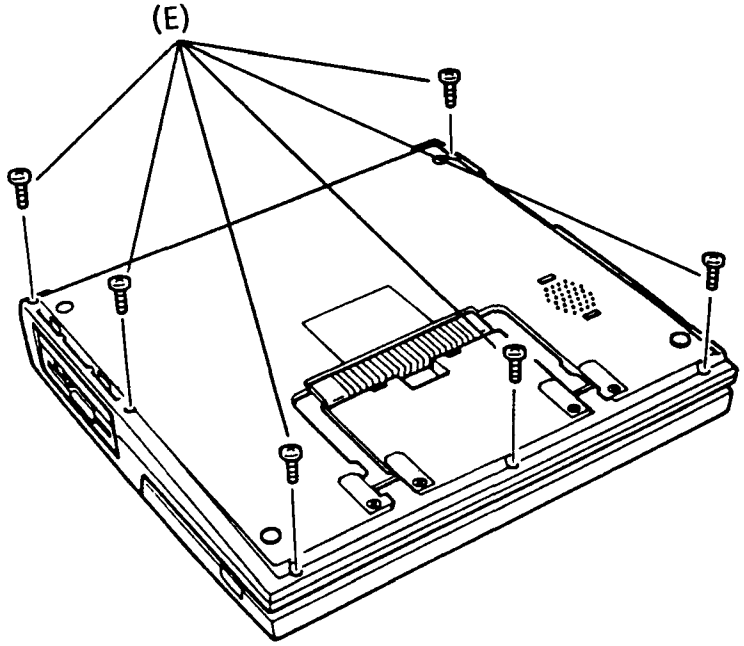


FIGURE 4-2 Removing the Screws from the Base Subassembly

3. Open the LCD by sliding the two side latches (F) forward while pulling upward.

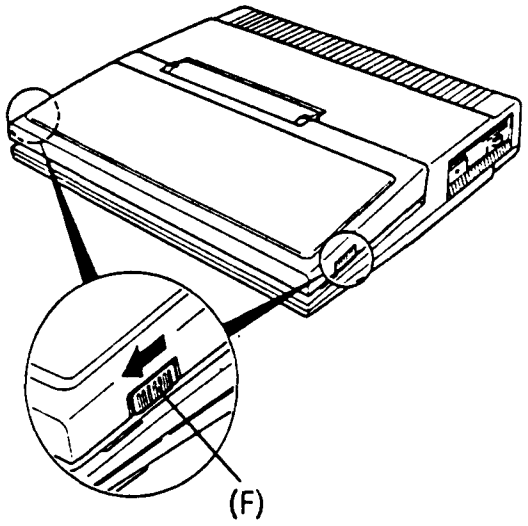


FIGURE 4-3 Opening the LCD

4. The top cover can now be lifted and separated from the base subassembly. Once the top cover assembly is separated from the base subassembly it should be stood on its side to the left of the unit.

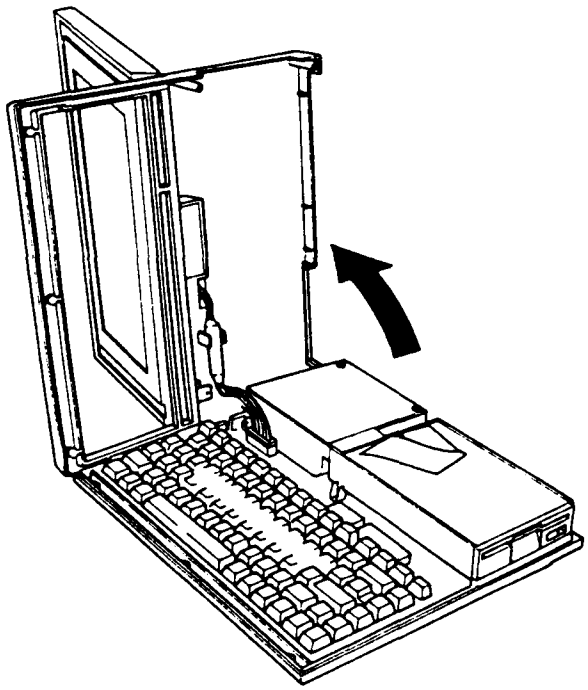


FIGURE 4-4 Removing the Top Cover Assembly from the Base Subassembly

5. To reassemble the unit, remount the top cover assembly on the base subassembly and follow the above procedures in reverse.

4.3 DISCONNECTING THE TOP COVER ASSEMBLY

1. Confirm that the POWER switch is off.
2. Remove the top cover assembly as directed in part 4.2.
3. Disconnect the LCD cable (A) from the system PCB (B).

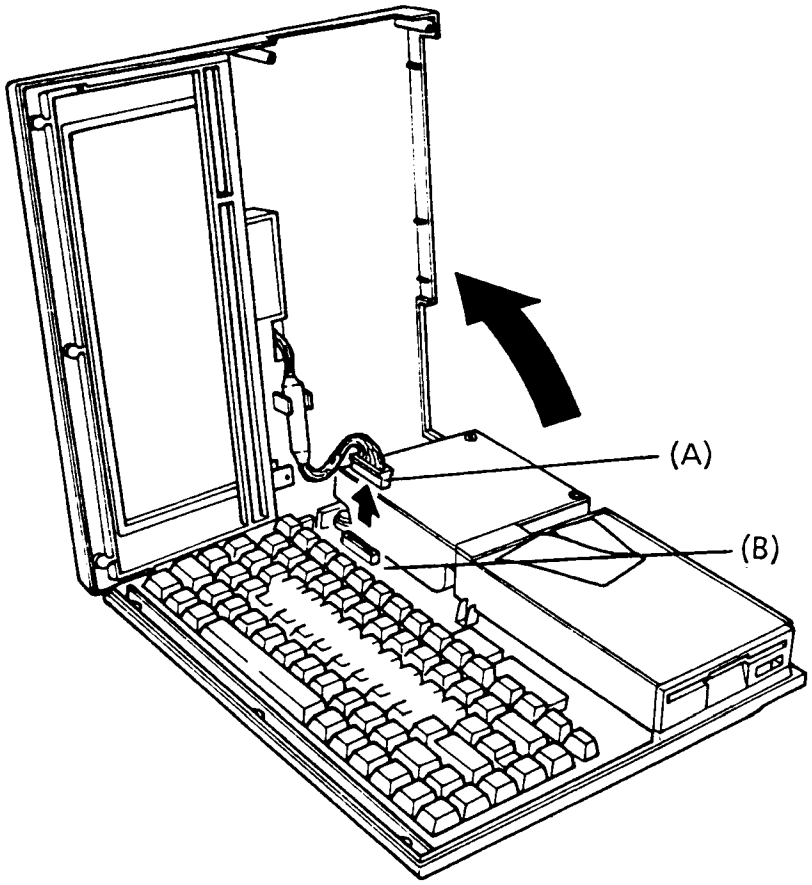


FIGURE 4-5 Disconnecting the Top Cover Assembly

4. To install a new top cover assembly, follow the above procedures in reverse.

4.4 REMOVING/REPLACING THE KEYBOARD UNIT AND SPEAKER

1. Confirm that the POWER switch is off.
2. Remove the top cover assembly as directed in part 4.2.
3. Remove the two screws (A) and lift the keyboard unit out.
4. Release the pressure plate (B) of connector PJ 12 to disconnect the keyboard cable from the system PCB.
5. Remove the speaker (C) by pushing the plastic latch (D) outward until the speaker can be pulled out.

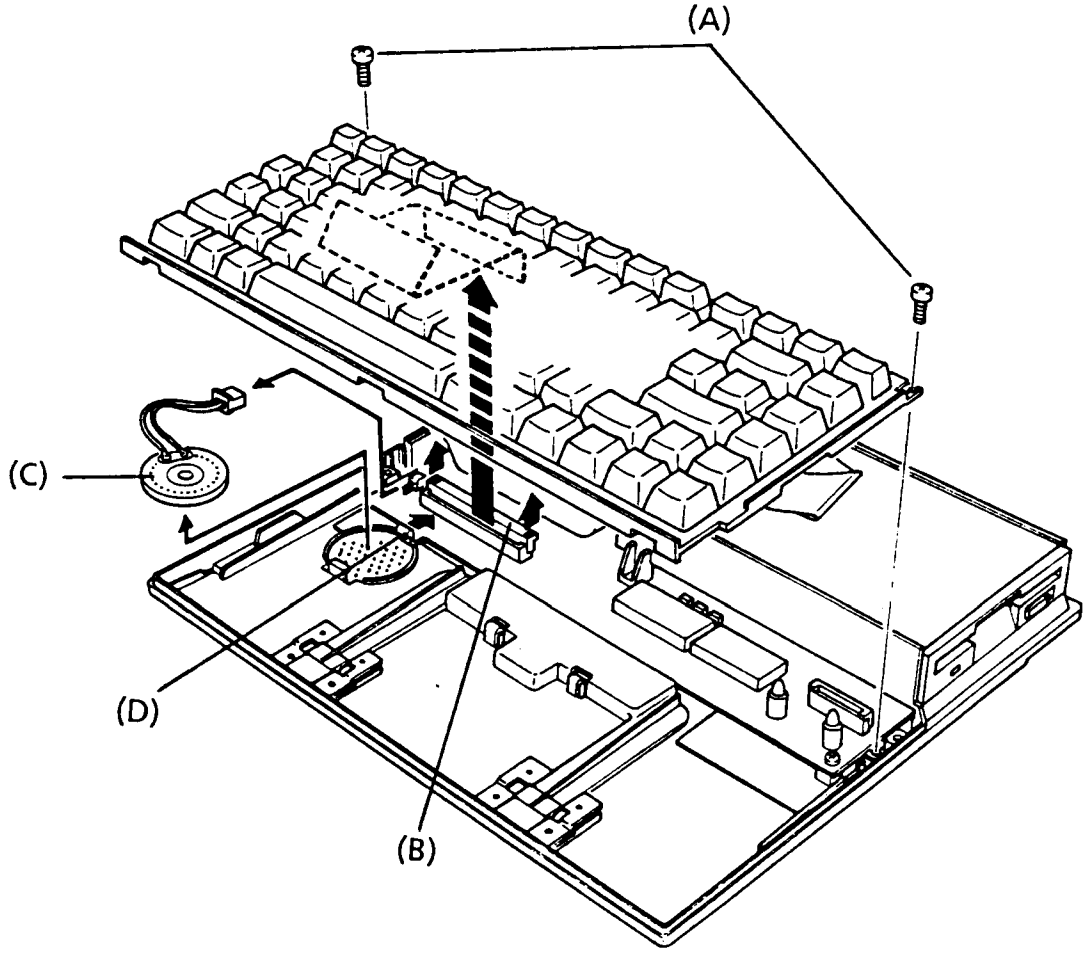


FIGURE 4-6 Removing the Keyboard Unit and Speaker

4. To install a new keyboard unit, follow the above procedures in reverse.

4.5 REMOVING/REPLACING THE BATTERY ASSEMBLY AND BATTERY BOX

1. Confirm that the POWER switch is off.
2. If the system has an optional modem card, remove the modem card as directed in part 4.13.
3. Disconnect the battery cable (A) from the system PCB (B).
4. Remove the single screw (C) from the battery holder (D).
5. Lift the battery holder out and remove the battery assembly.
6. Push the plastic latch (E) in and lift the battery box (F) out.

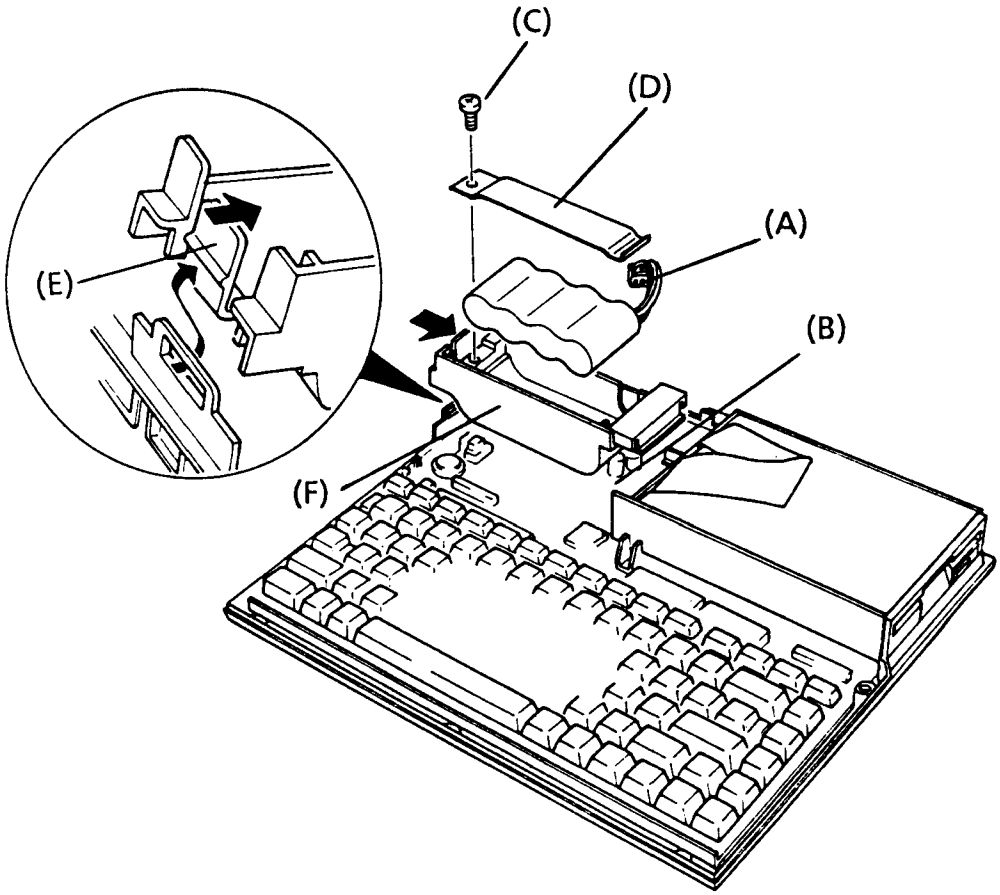


FIGURE 4-7 Removing the Battery Assembly and Battery Box

7. To install a new battery assembly and battery box, follow the above procedures in reverse.

4.6 REMOVING/REPLACING THE FDD (FLOPPY DISK DRIVE) BOX

1. Confirm that the POWER switch is off.
2. Remove the battery box as directed in part 4.5.
3. Remove the three screws (A) holding the FDD box (B) in place.
4. Disconnect the FDD cable (C) from the system PCB (D).
5. Lift the FDD box up and away from the system PCB.

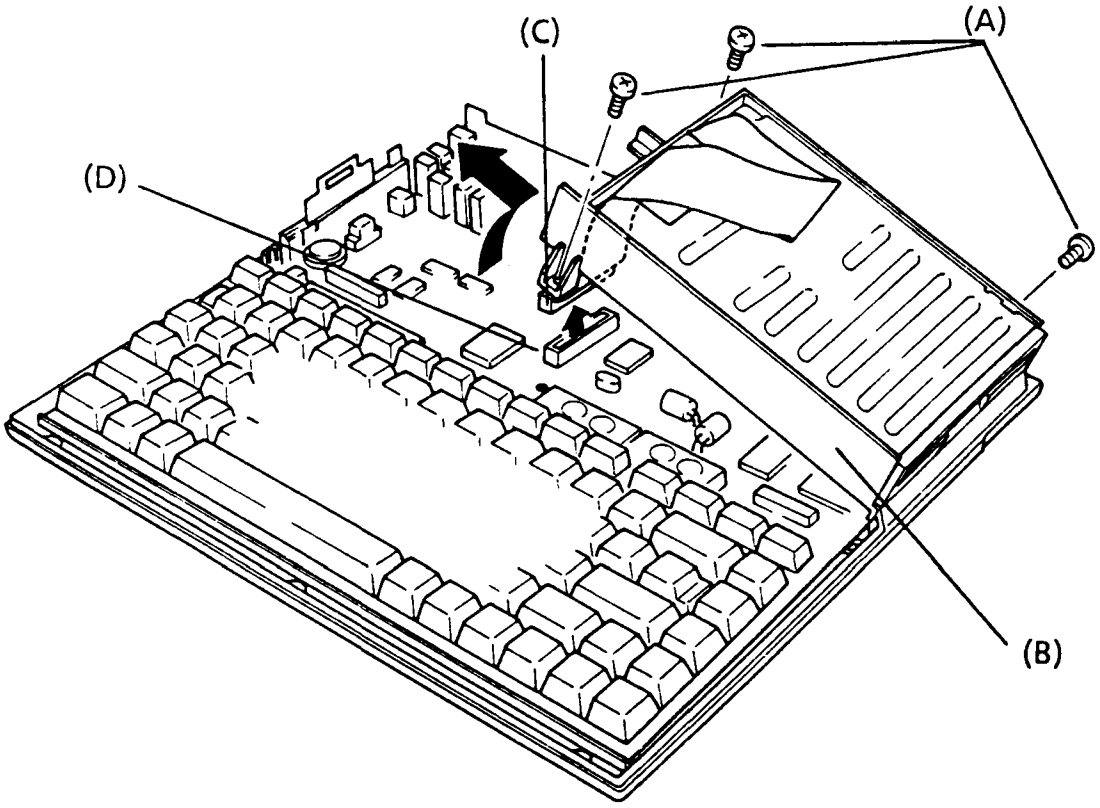


FIGURE 4-8 Removing the FDD Box

6. To install a new FDD box, follow the above procedures in reverse.

4.7 REMOVING/REPLACING THE FDD (FLOPPY DISK DRIVE)

1. Confirm that the POWER switch is off.
2. Remove the FDD box as directed in part 4.6.
3. Remove the three flatheaded countersunk screws (A) and the grounding plate (B) from the bottom of the FDD box (C).
4. Lift the FDD out of the FDD box.

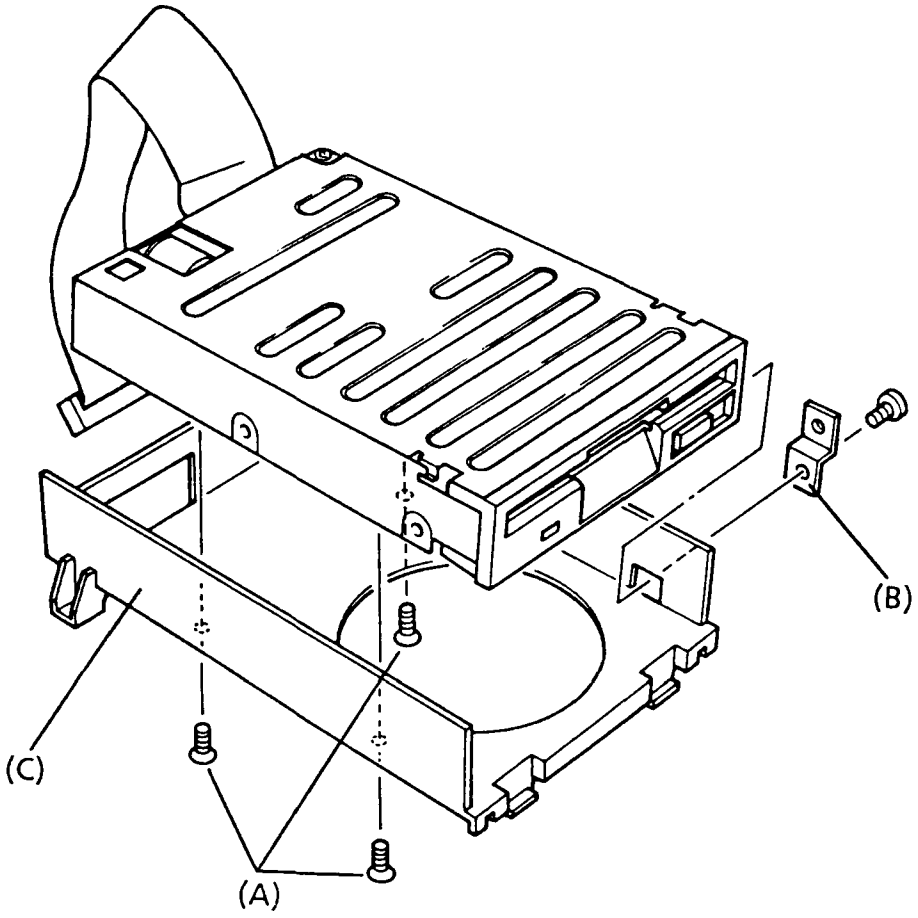


FIGURE 4-9 Removing the FDD

5. To install a new FDD, follow the above procedures in reverse.

4.8 REMOVING/REPLACING THE SYSTEM PCB

1. Confirm that the POWER switch is off.

2. Remove the keyboard unit, battery box, and FDD box as directed in parts 4.4, 4.5, and 4.6. If the system unit has an expanded memory card, remove the card as directed in part 4.14.

3. Disconnect the speaker cable (A) from the system PCB (B).

4. Remove the four screws (C) from the system PCB and lift the board out.

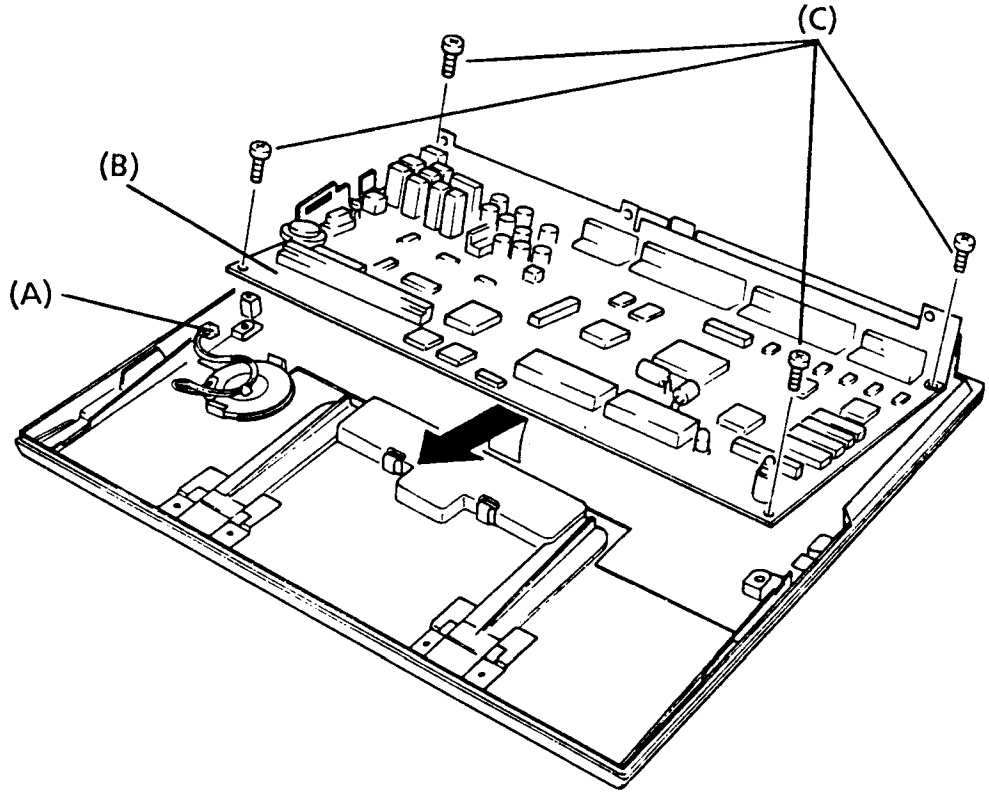


FIGURE 4-10 Removing the System PCB

5. To install a new system PCB, follow the above procedures in reverse.

4.9 REMOVING/REPLACING THE LCD MASK

1. Confirm that the POWER switch is off.

2. Open the LCD by sliding the two side latches (A) forward while pulling upward.

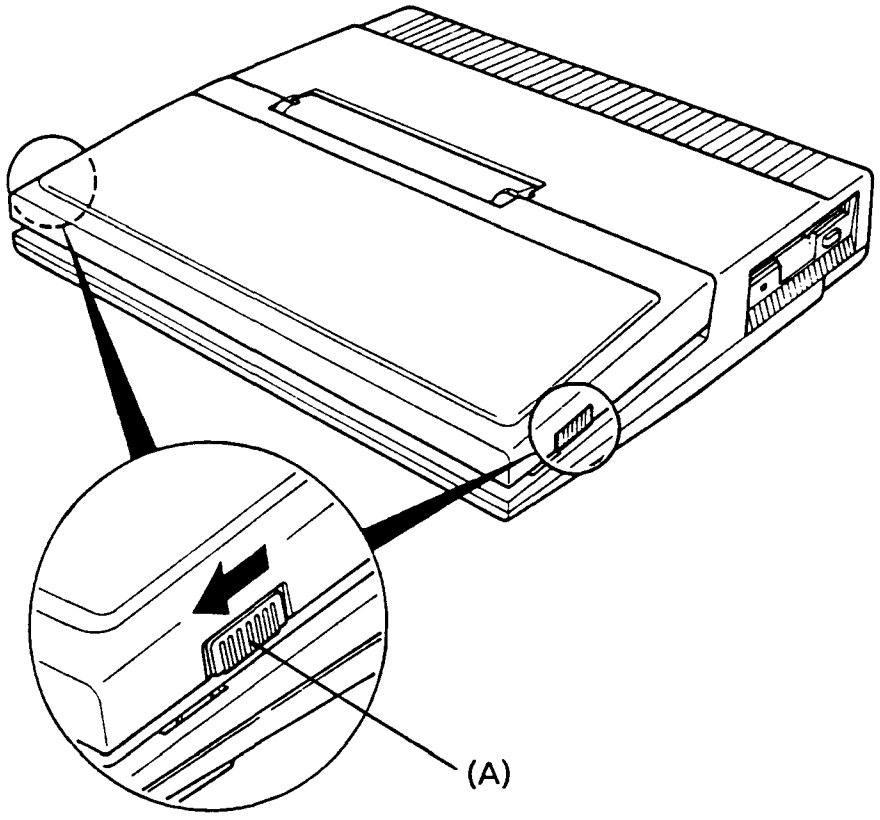


FIGURE 4-11 Opening the LCD

3. Using tweezers or a fine-pointed instrument, peel off the TOSHIBA label (B) and keep it in a clean place.

4. Remove the single flatheaded countersunk screw (C) and take the LCD mask (D) off by pulling it slightly forward and upward.

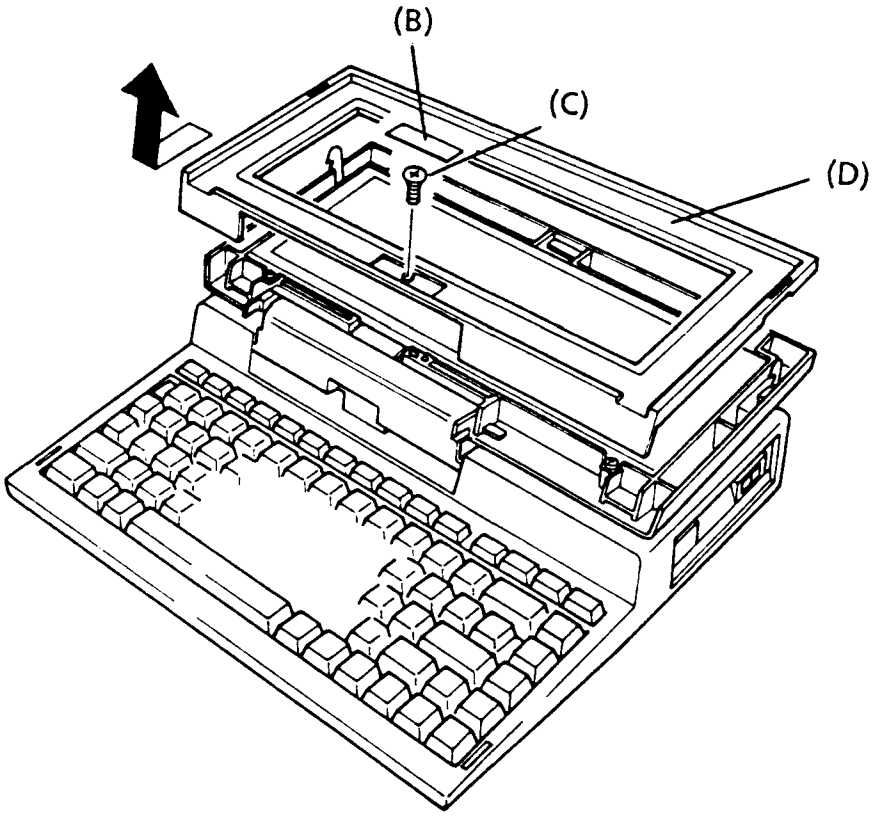


FIGURE 4-12 Removing the LCD Mask

5. To install a new LCD mask, follow the above procedures in reverse.

4.10 REMOVING/REPLACING THE LCD MODULE

1. Confirm that the POWER switch is off.
2. Remove the LCD mask from the LCD as directed in part 4.9.
3. Remove the four screws (A) on the LCD module (B).
4. Disconnect the LCD cable (C) from the LCD module.

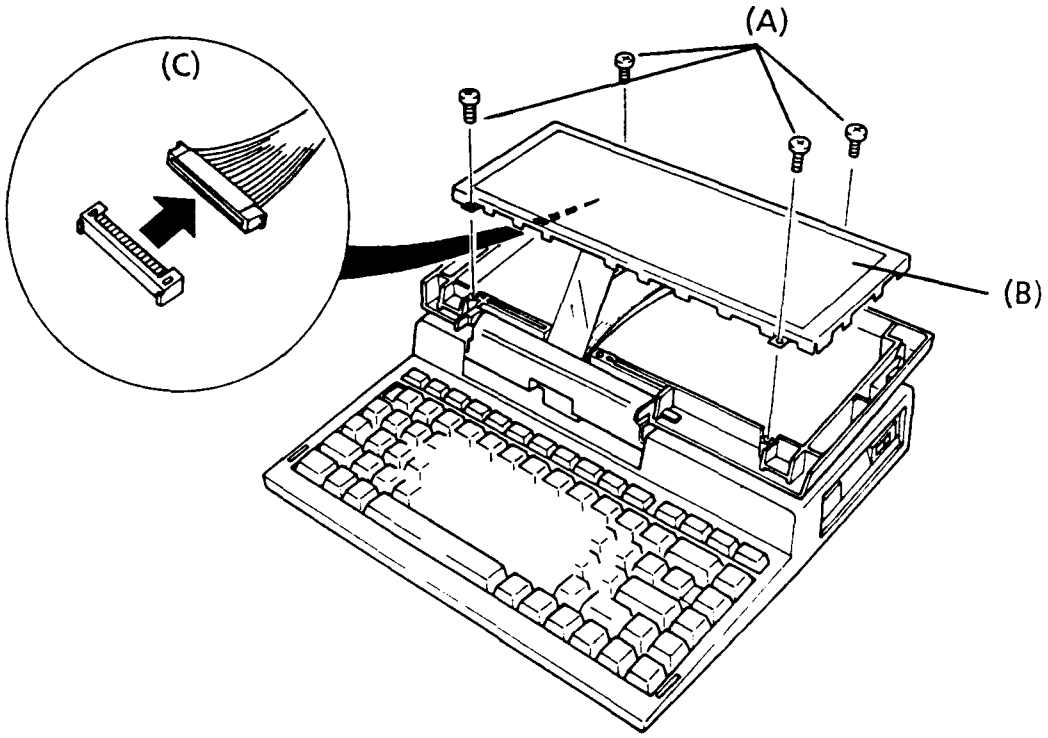


FIGURE 4-13 Removing and Disconnecting the LCD Module

5. To install a new LCD module, follow the above procedures in reverse.

4.11 REMOVING THE LCD COVER SUBASSEMBLY

1. Confirm that the POWER switch is off.

2. Remove the LCD mask and LCD module as directed in parts 4.9 and 4.10.

3. Using tweezers or a fine-pointed instrument, peel off the hinge label (A) and remove the two screws (B) that it conceals. Keep the label in a clean place.

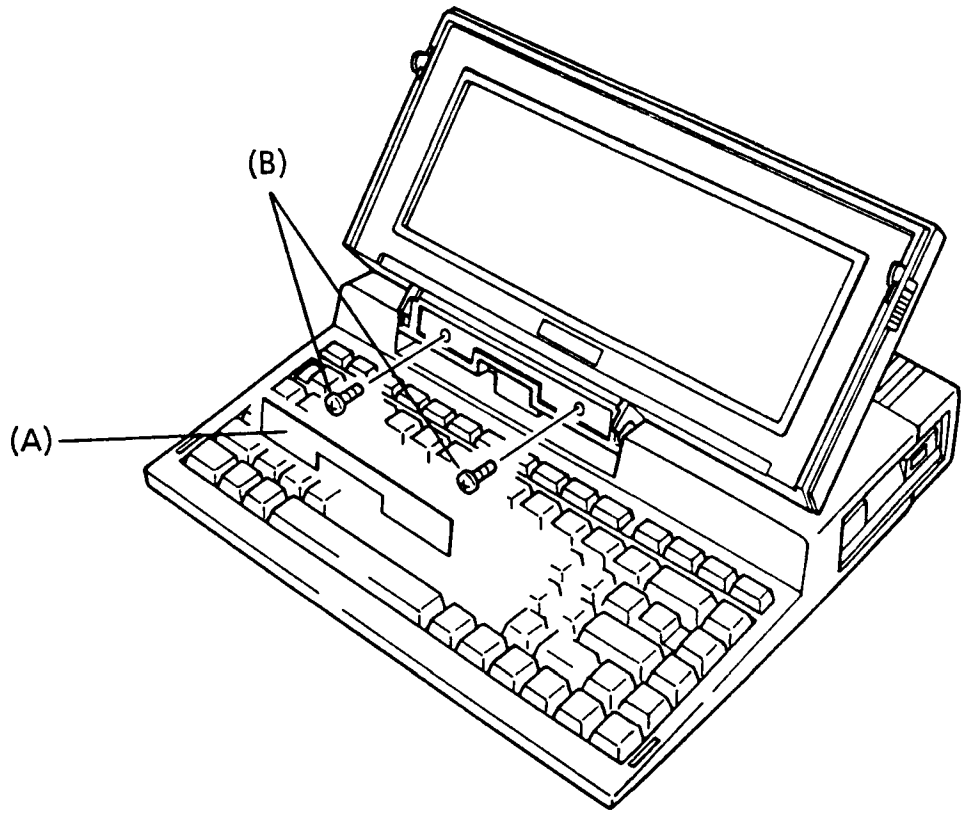


FIGURE 4-14 Removing the LCD Cover Subassembly Screws

4. Move the LCD cover subassembly (C) forward again to free it from the unit's top cover (D).

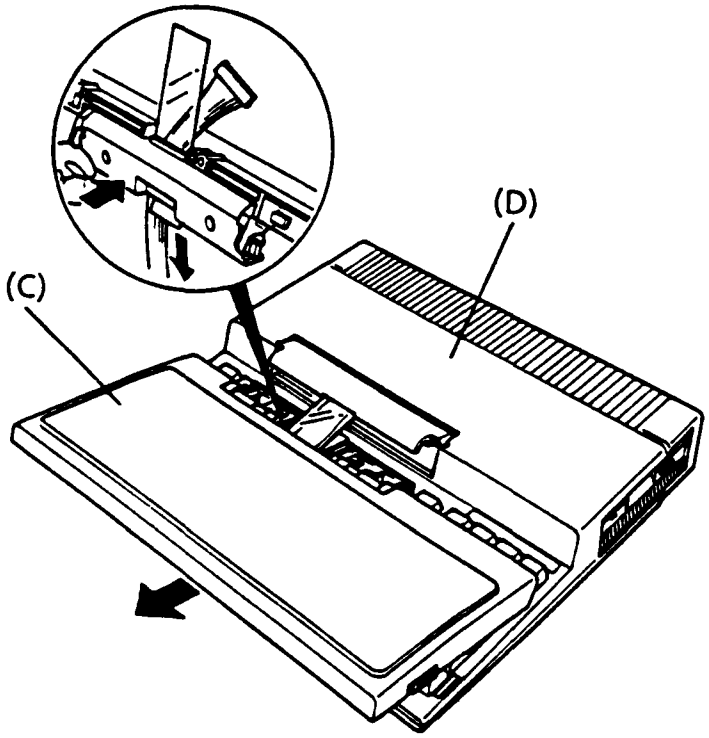


FIGURE 4-15 Removing the LCD Cover Subassembly

5. Remove the hinge cover (E) and the torsion bar (F) from the top cover.

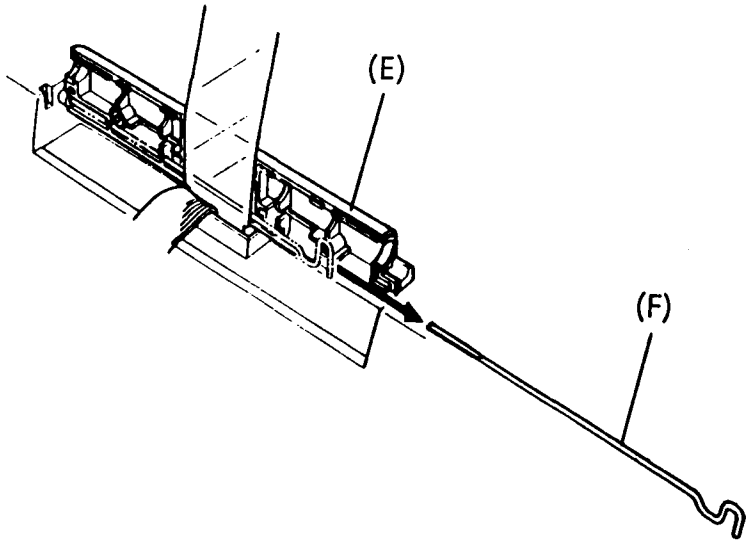


FIGURE 4-16 Removing the Hinge Cover and Torsion Bar

6. Replacement procedures are described in part 4.12.

4.12 REPLACING THE LCD COVER SUBASSEMBLY

1. Confirm that the POWER switch is off.

2. Insert the torsion bar (A) into the hole (B) provided in the top cover. Make sure that the torsion bar is fully seated before proceeding; the hooked portion should be positioned vertically.

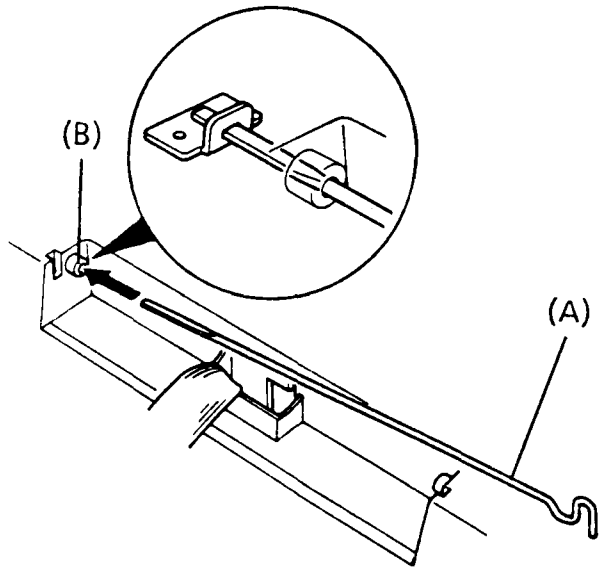


FIGURE 4-17 Inserting the Torsion Bar

3. Insert the short end of the hinge cover plastic cable shield (C) into the main unit; the torsion bar must be seated in the hinge cover between the cover and the shield. The hinge cover itself should be seated on the two pirot ends (D).

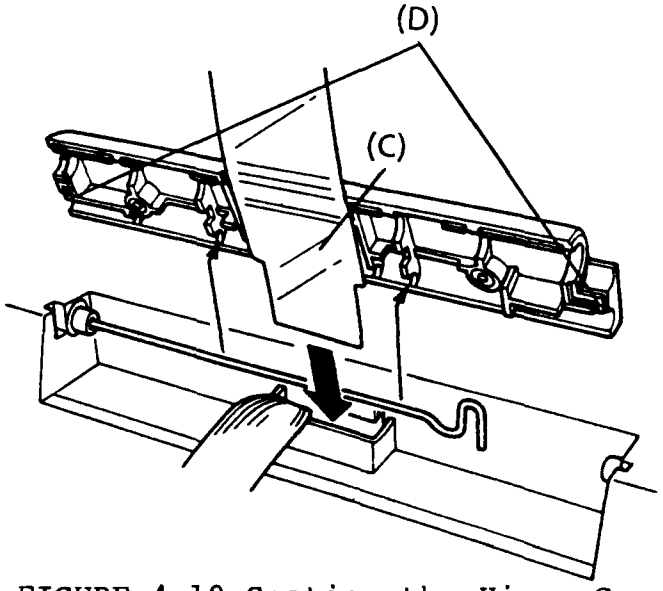


FIGURE 4-18 Seating the Hinge Cover

4. Insert the long end of the hinge cover cable shield into the LCD cover (E).

5. Insert the short end of the LCD cover cable shield into the main unit. The cable should be sandwiched between the two shields (F).

6. While feeding the long end of the hinge cover cable shield into the LCD cover, seat the LCD cover subassembly under the two dowel ends (G).

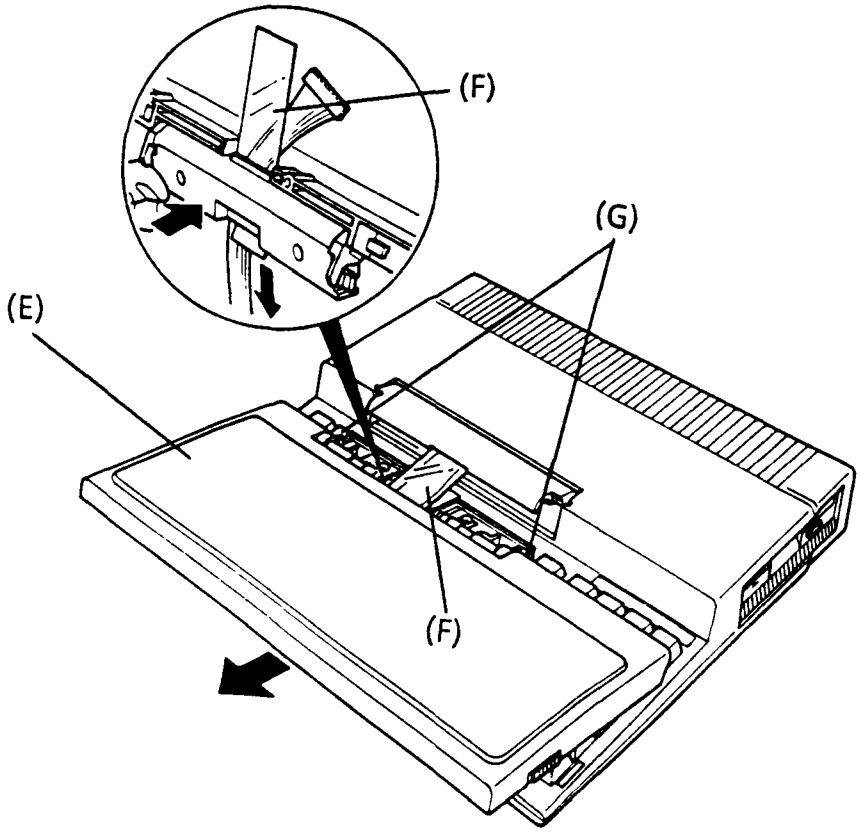


FIGURE 4-19 Seating the LCD Cover

7. Rotate the LCD cover assembly to a vertical position while constantly maintaining pressure to prevent separation of the hinge cover and the LCD cover. Insert and tighten down the two LCD cover screws to complete the replacement procedure.

8. As directed in part 4.11 reassemble the LCD cover subassembly

4.13 REMOVING/REPLACING THE MODEM CARD (OPTIONAL)

1. Confirm that the power switch is off.
2. Remove the top cover assembly as directed in part 4.2.
3. Remove the two screws (A) at the back of the unit.
4. Release the pressure plate (B) of connector PJ 7 (C) to disconnect the modem cable (D) from the system PCB.
5. Lift the modem card (E) out.

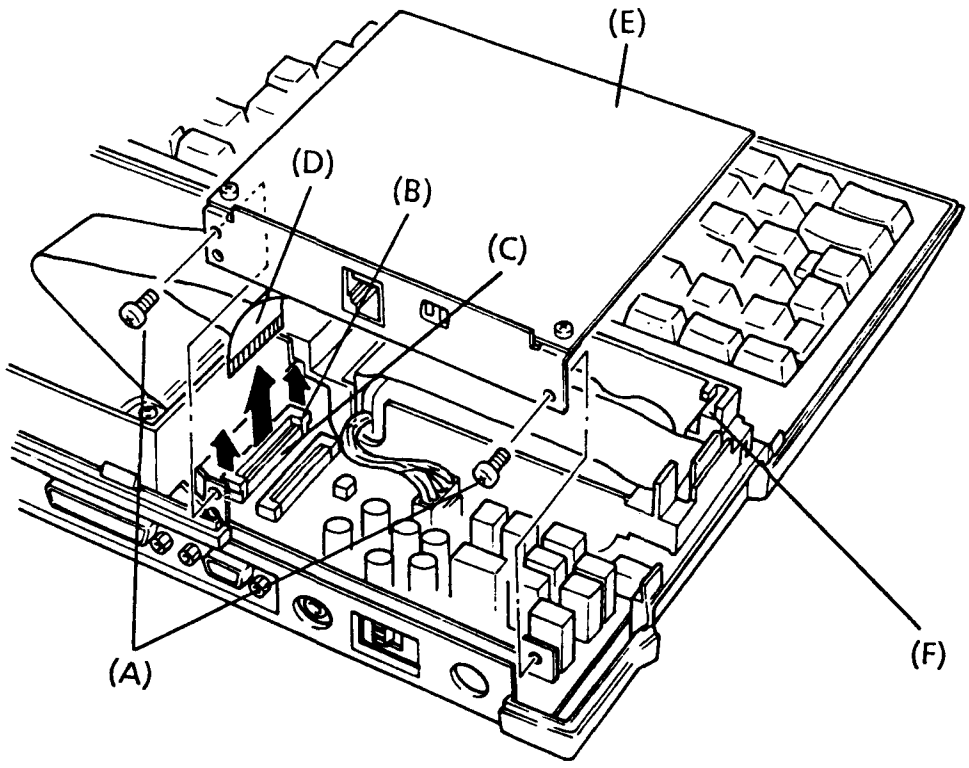


FIGURE 4-20 Removing the Modem Card

6. To install a new modem card, follow the above procedures in reverse.
   Note: The modem card must be inserted into the slots (F) before it is fightened down.

4.14 REMOVING/REPLACING THE EXPANDED MEMORY CARD (OPTIONAL)

CAUTION: The expanded memory contents will remain in the old expanded memory. If desired, transfer the contents of the old expanded memory onto a floppy disk before replacing the memory card.
Before replacing the expanded memory card, disconnect the battery cable from the system PCB.

1. Confirm that the power switch is off.

2. Remove the top cover assembly as directed in part 4.2.

3. Pull out the expanded memory card (A) from the system PCB (B).

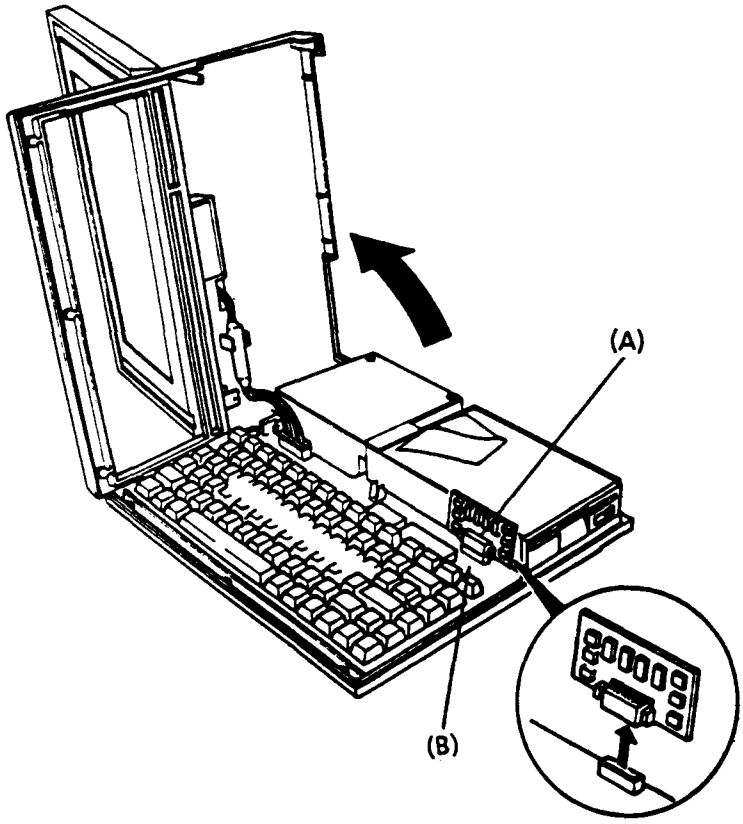


FIGURE 4-21 Removing the Expanded Memory Card

4. To install a new expanded memory card, follow the above procedures in reverse.

5.1 SYSTEM UNIT

5.1.1 Inside the system unit

(A) LCD

(B) Top cover assembly

(C) Keyboard unit

(D) Battery pack

(E) 3.5-inch floppy disk drive

(F) System PCB

(G) Speaker

(H) Base subassembly

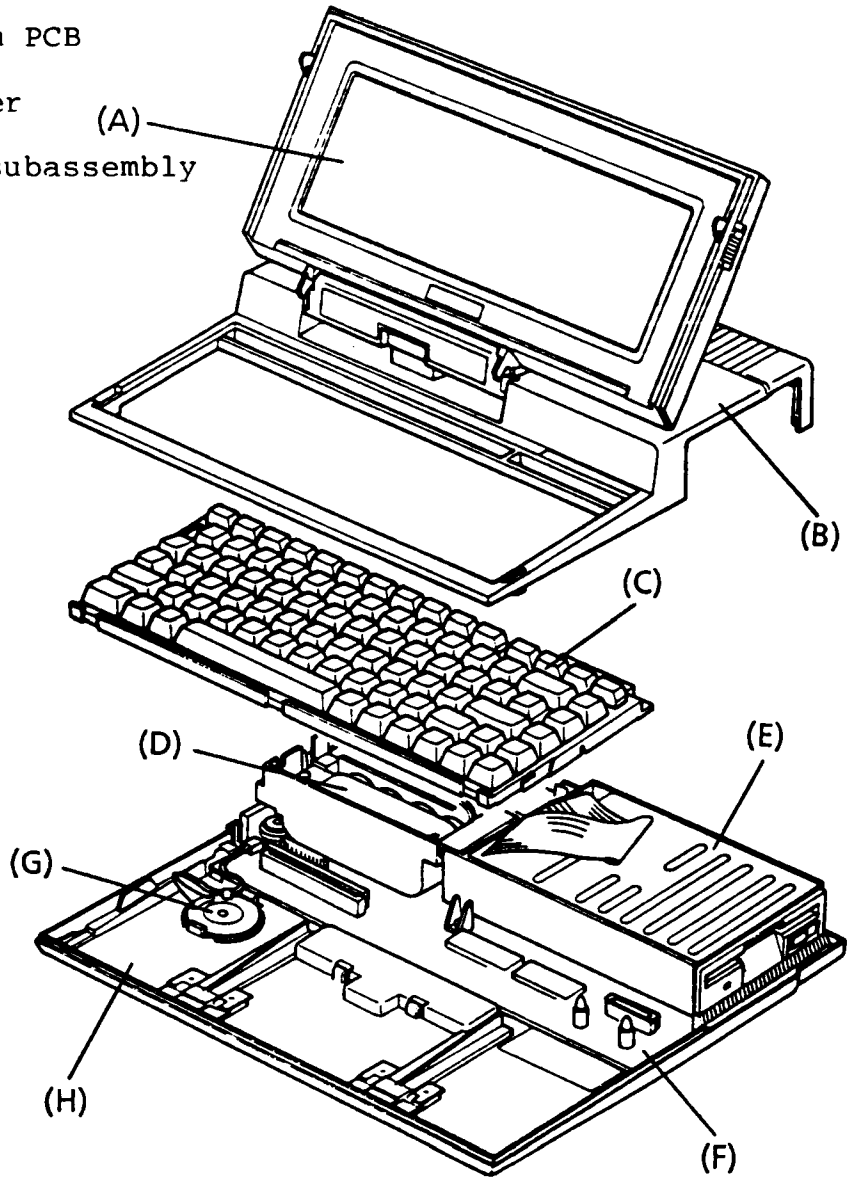


FIGURE 5-1 Inside the System Unit

5.1.2 Rear panel

(A) COMMS connector (9-pin D-shell)

(B) Printer connector (25-pin D-shell)

(C) EXT FDD connector (25-pin D-shell)

(D) RGB connector (9-pin D-shell)

(E) COMP connector (2-pin)

(F) Power switch

(G) DC IN jack (dc 9V)

(H) Expansion slot

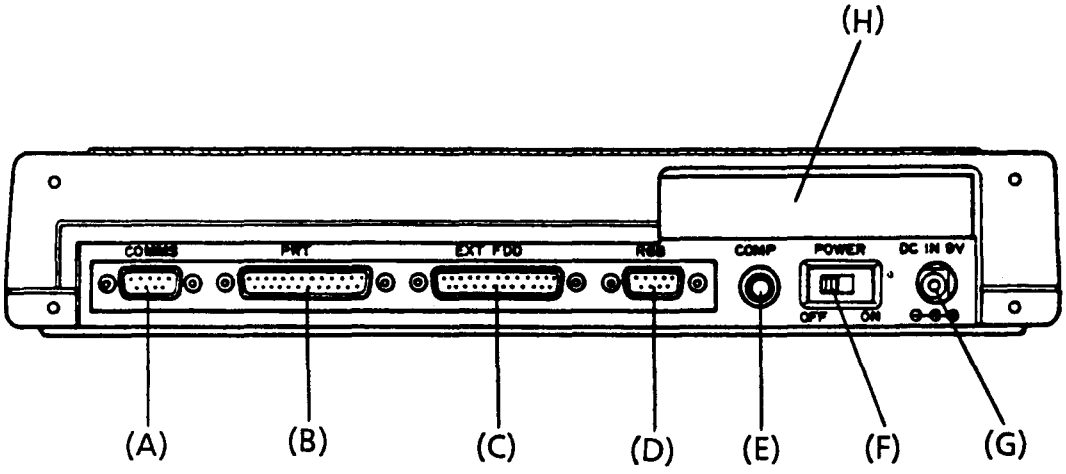


Figure 5-2 Rear Panel

5.1.3 Left side the system unit

(A) Key pad connector (2-pin)

(B) EXT FDD switch

(C) LCD contrast knob

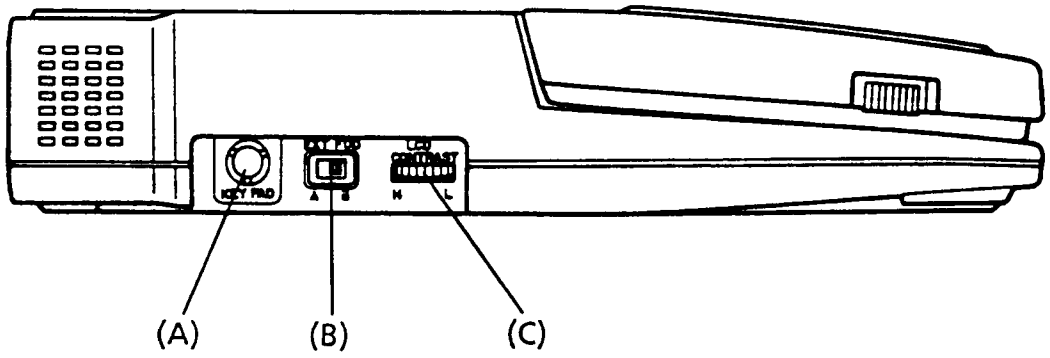


FIGURE 5-3 Left Side the System Unit

5.2 SYSTEM PCB

5.2.1 System PCB connectors

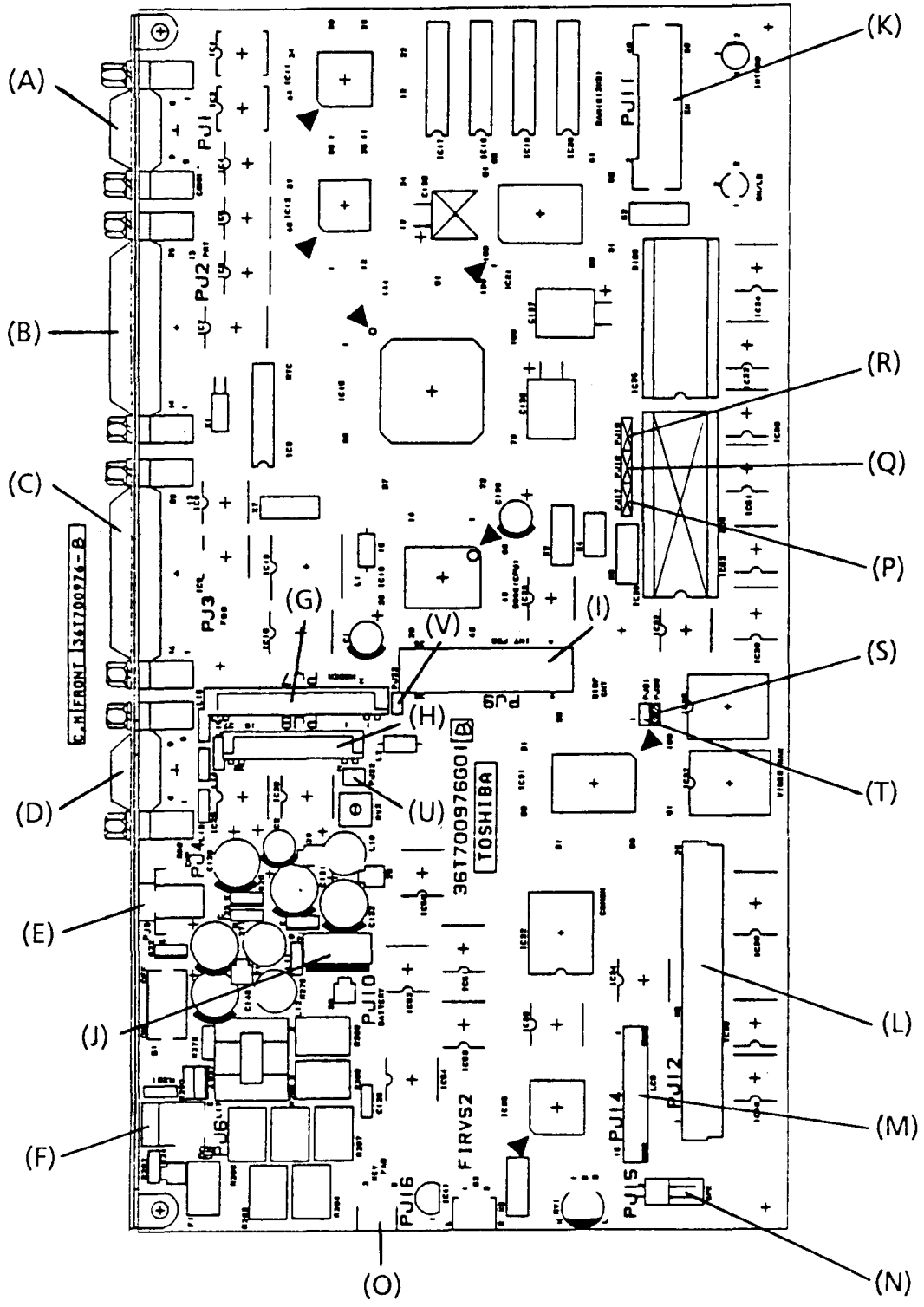


FIGURE 5-4 System PCB Connectors

(A) PJ 1 COMMS connector (9-pin D-shell)

(B) PJ 2 Printer connector (25-pin D-shell)

(C) PJ 3 EXT FDD connector (25-pin D-shell)

(D) PJ 4 RGB connector (9-pin D-shell)

(E) PJ 5 COMP connector (2-pin)

(F) PJ 6 DC IN jack (2-pin)

(G) PJ 7 Modem connector (27-pin)

(H) PJ 8 Expansion bus connector (20-pin)

(I) PJ 9 FDD connector (26-pin)

(J) PJ 10 Battery connector (4-pin)

(K) PJ 11 Expanded memory connector (40-pin)

(L) PJ 12 Keyboard connector (25-pin)

(M) PJ 14 LCD connector (15-pin)

(N) PJ 15 Speaker connector (2-pin)

(O) PJ 16 Key pad connector

(P) PJ 17 Jumper strap (EPROM)

(Q) PJ 18 Jumper strap (DOS-ROM)

(R) PJ 19 Jumper strap (DOS-ROM)

(S) PJ 20 Jumper strap (Font)

(T) PJ 21 Jumper strap (Font)

(U) PJ 22 Not used.

(V) PJ 23 Test point (Low Battery)

5.2.2 System PCB ICs

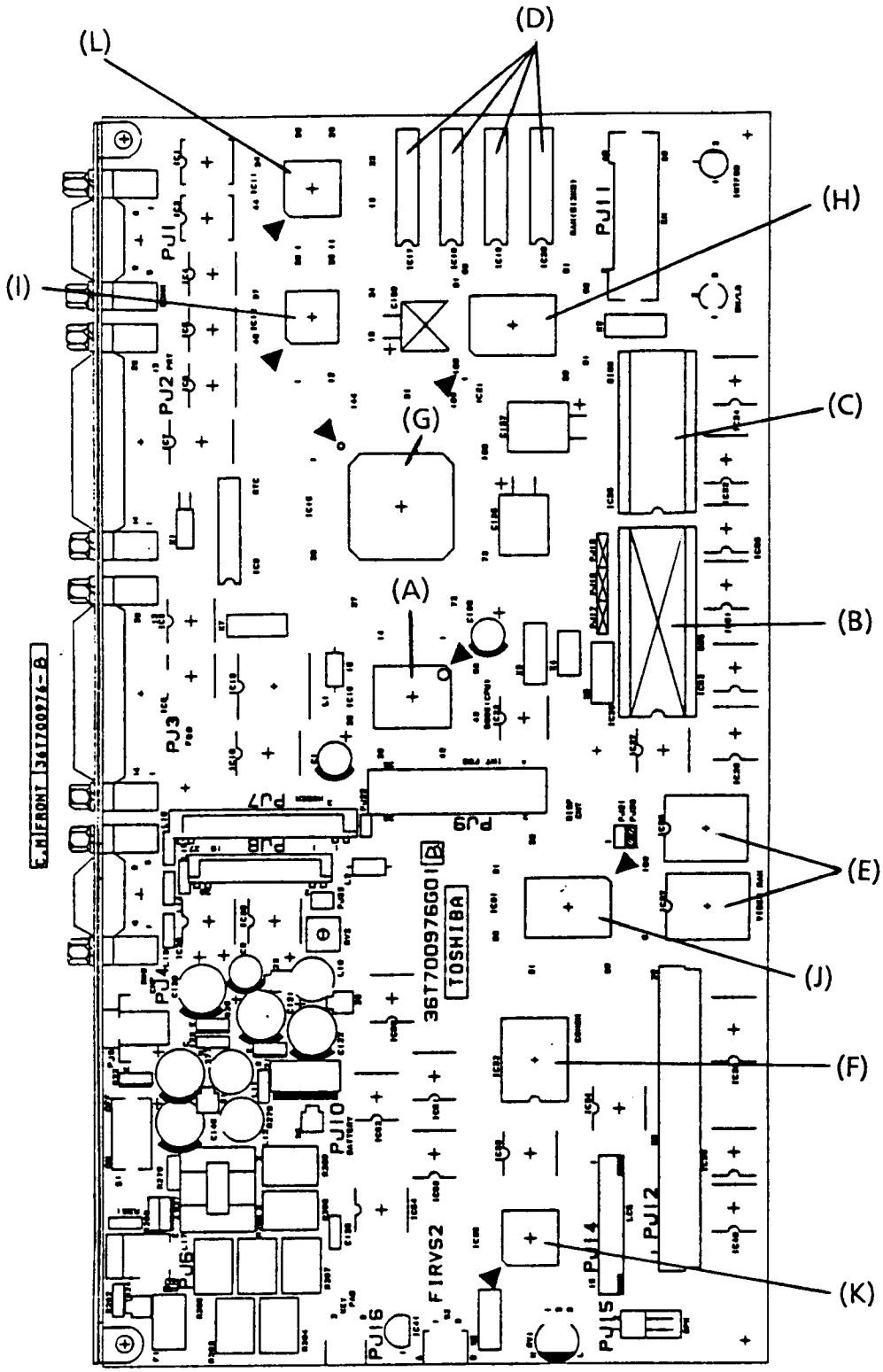


FIGURE 5-5 System PCB ICs

(A) CPU: Central processor (80C88)

(B) DOS ROM

(C) BIOS ROM

(D) System RAM (512 kbytes)

(E) Video RAM

(F) CG ROM

(G) Gate Array (Super integration: SI T7885)

(H) Gate Array (I/O controller)

(I) Gate Array (I/O driver)

(J) Gate Array (Display controller)

(K) Keyboard controller (80C50)

(L) RS232C controller (8250)

5.3 CONNECTORS

5.3.1 Printer connector

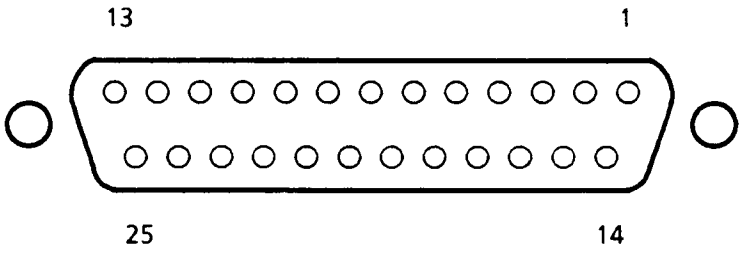


FIGURE 5-6 Printer Connector

TABLE 5-1 Printer Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	STROB0	O	- STROBE
2	PD01	O	+ DATA BIT 0
3	PD11	O	+ DATA BIT 1
4	PD21	O	+ DATA BIT 2
5	PD31	O	+ DATA BIT 3
6	PD41	O	+ DATA BIT 4
7	PD51	O	+ DATA BIT 5
8	PD61	O	+ DATA BIT 6
9	PD71	O	+ DATA BIT 7
10	ACK0	I	- ACKNOWLEDGE
11	BUSY1	I	+ BUSY
12	PE1	I	+ PAPER END
13	SELEC1	I	+ SELECT
14	AUTFD0	O	- AUTO FEED
15	ERROR0	I	- ERROR (FAULT)
16	PINT0	O	- PRINTER INITIALIZE
17	SLIN0	O	- SELECT INPUT
18-25	GND		GROUND (0 V)

5.3.2 EXT FDD connector

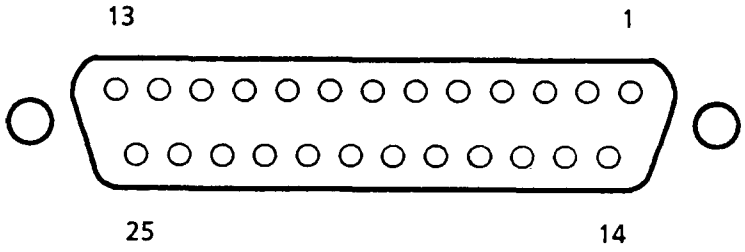


FIGURE 5-7 EXT FDD Connector

TABLE 5-2 EXT FDD Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	EFRDY0	I	- EXTERNAL DRIVE READY
2	EINDX0	I	- EXTERNAL INDEX
3	ETRAC0	I	- EXTERNAL TRACK ZERO
4	EWPRT0	I	- EXTERNAL WRITE PROTECTED
5	EFDAT0	I	- EXTERNAL READ DATA
6	DSKCHG0	I	-DISK CHANGE
7 - 9	-		(NOT USED)
10	ESEL0	O	- EXTERNAL DRIVE SELECT
11	EMON0	O	- EXTERNAL MOTOR ON
12	EDATA0	O	- EXTERNAL WRITE DATA
13	EGATE1	O	+ EXTERNAL WRITE GATE
14	LOWDNS0	O	- LOW DOWN
15	ESIDE0	O	- EXTERNAL SIDE SELECT
16	EFDRC0	O	- EXTERNAL DIRECTION
17	ESTEP0	O	- EXTERNAL STEP
18-23	GND		GROUND (0 V)
24	EF2DD1	I	+ 2DD DRIVE
25	GND		GROUND (0 V)

5.3.3 RGB connector

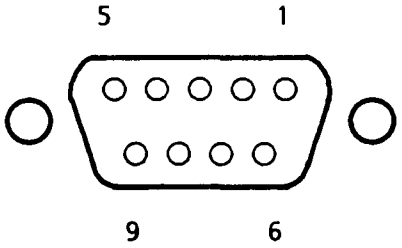


FIGURE 5-8 RGB Connector

TABLE 5-3 RGB Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1, 2	GND		GROUND (0 V)
3	CRV1	O	+ R (RED) VIDEO
4	CGV1	O	+ G (GREEN) VIDEO
5	CBV1	O	+ B (BLUE) VIDEO
6	CIV1	O	+ I (INTENSITY) VIDEO
7			(NOT USED)
8	CHSY1	O	+ HORIZONTAL SYNC
9	CVSY1	O	+ VERTICAL SYNC

5.3.4 COMMS connector

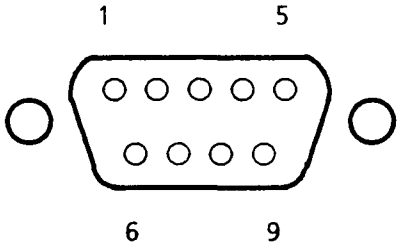


FIGURE 5-9 COMMS Connector

TABLE 5-4 COMMS Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	P26CP	O	COMPOSITE VIDEO
2	GND		GROUND (0 V)

5.3.5 COMP connector

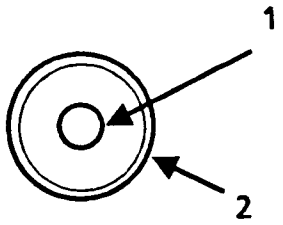


FIGURE 5-10 COMP Connector

TABLE 5-5 COMP Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	DCD1	I	+ DATA CARRIER DETECT
2	RD0	I	- RECEIVE DATA
3	SD0	O	- SEND DATA
4	DTR1	O	+ DATA TERMINAL READY
5	GND		GROUND (0 V)
6	DSR1	I	+ DATA SET READY
7	RTS1	O	+ REQUEST TO SEND
8	CTS1	I	+ CLEAR TO SEND
9	RI1	I	+ RING INDICATOR

5.3.6 Key pad connector

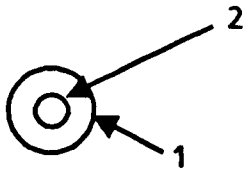


FIGURE 5-11 Key Pad Connector

TABLE 5-6 Key Pad Connector Signal Names

PIN	SIGNAL	I/O	DESCRIPTION
1	GND		GROUND (0 V)
2	TENKEY 1	I/O	+ TENKEY

5.4 KEYBOARD LAYOUT

5.4.1 USA version

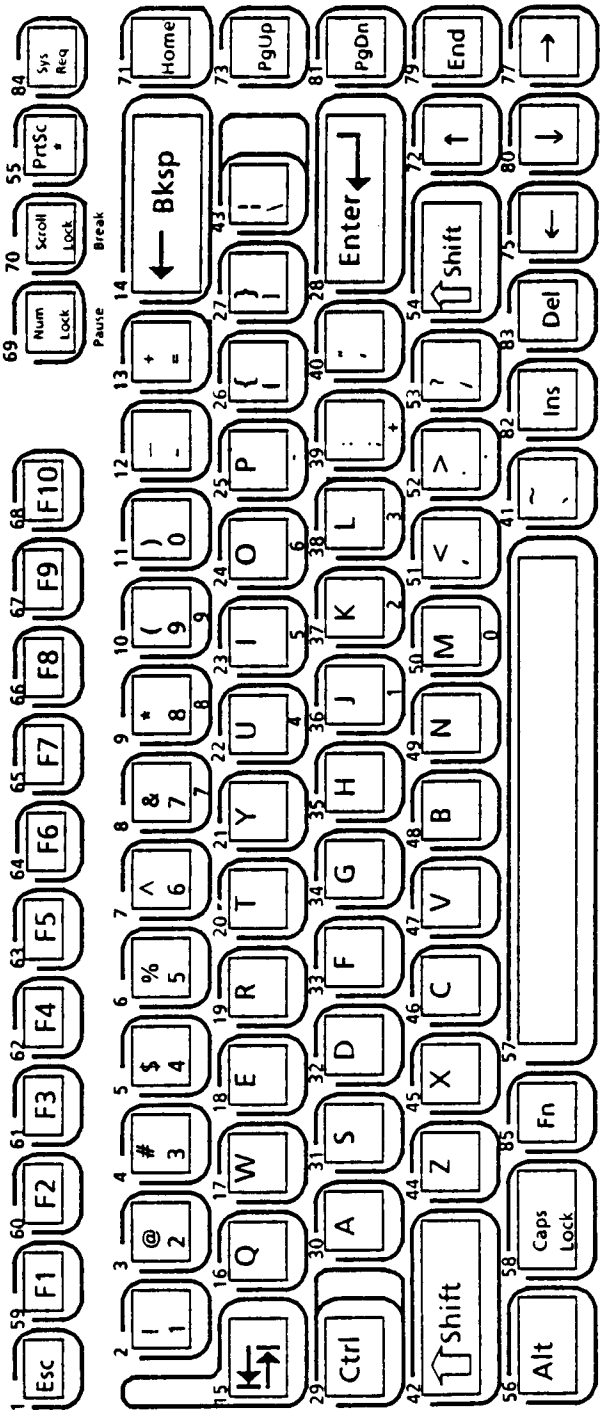


FIGURE 5-12 USA Version

5.4.2 England version

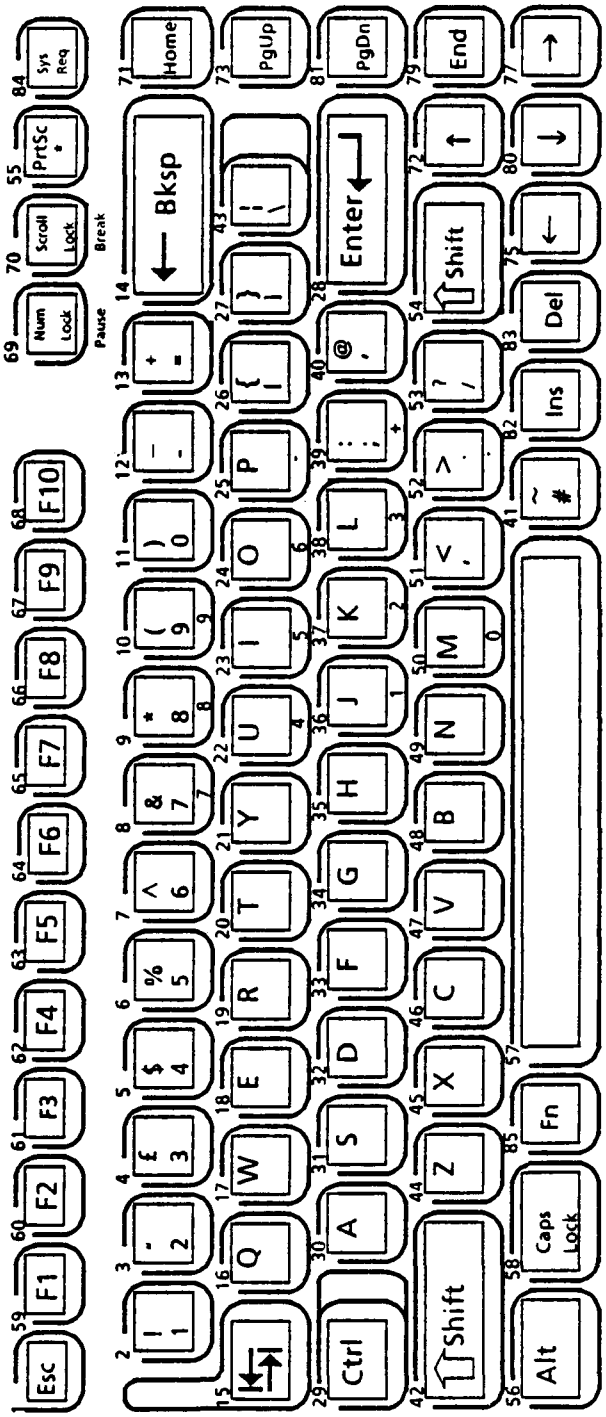


FIGURE 5-13 England Version

5.4.3 German version

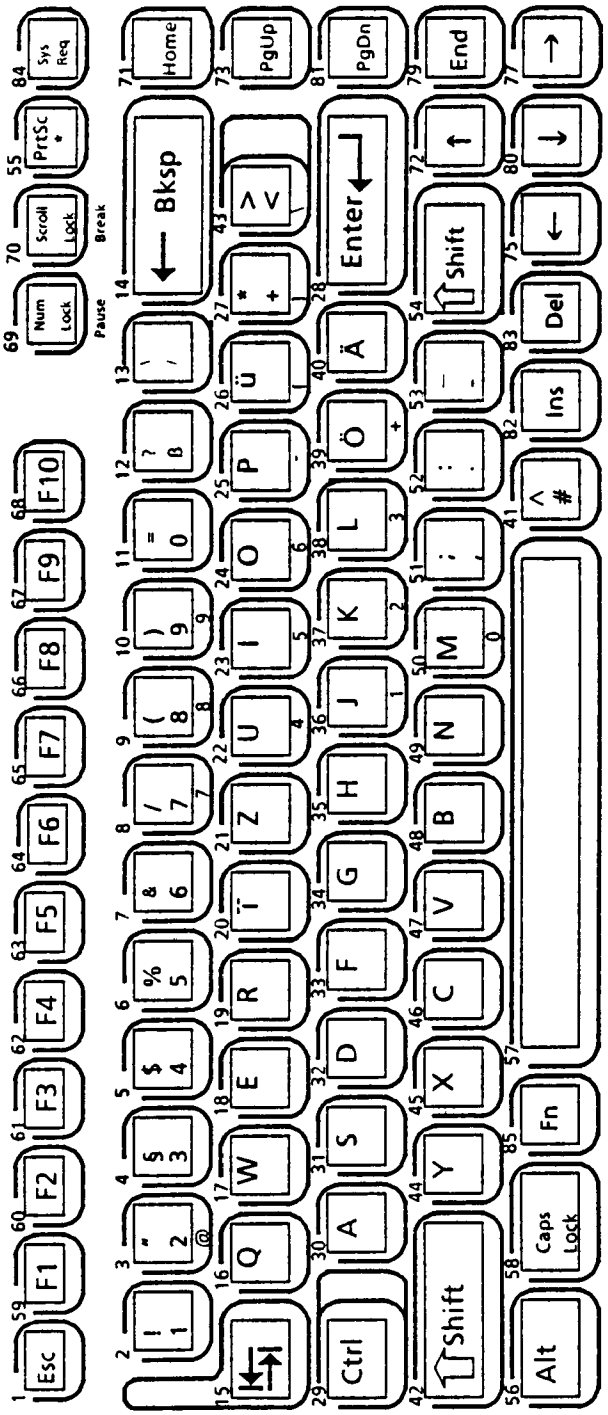


FIGURE 5-14 German Version

5.4.4 France version

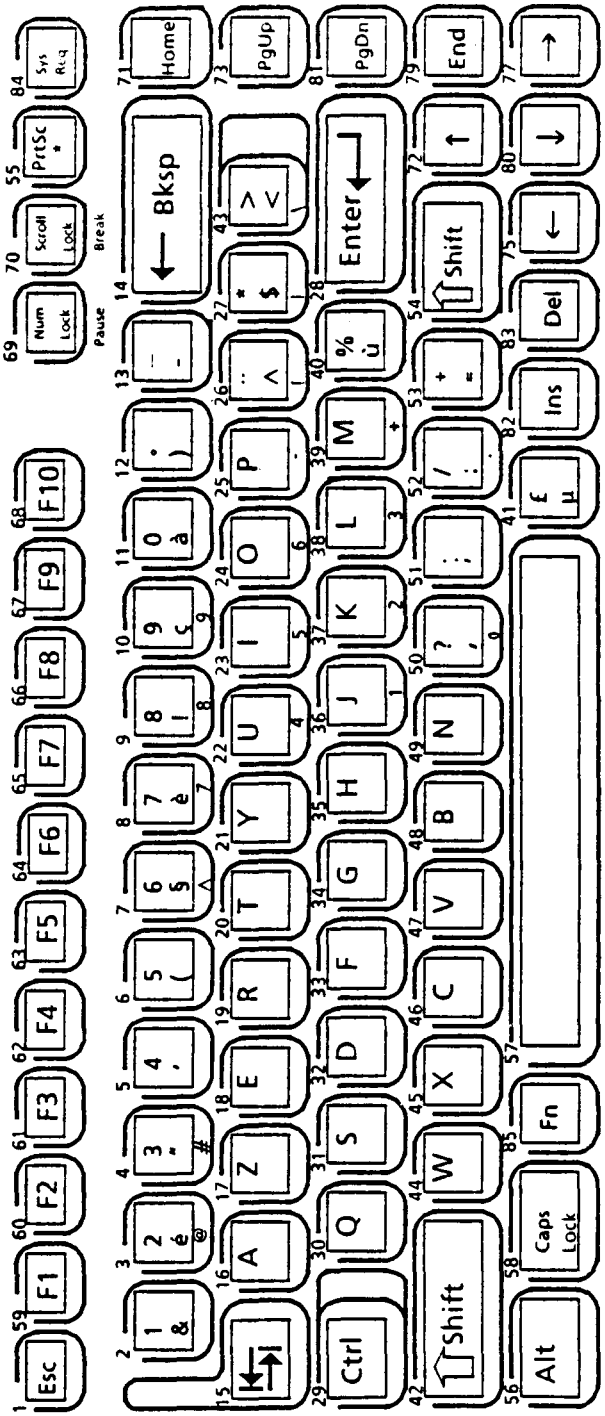


FIGURE 5-15 France Version

5.4.5 Spain version

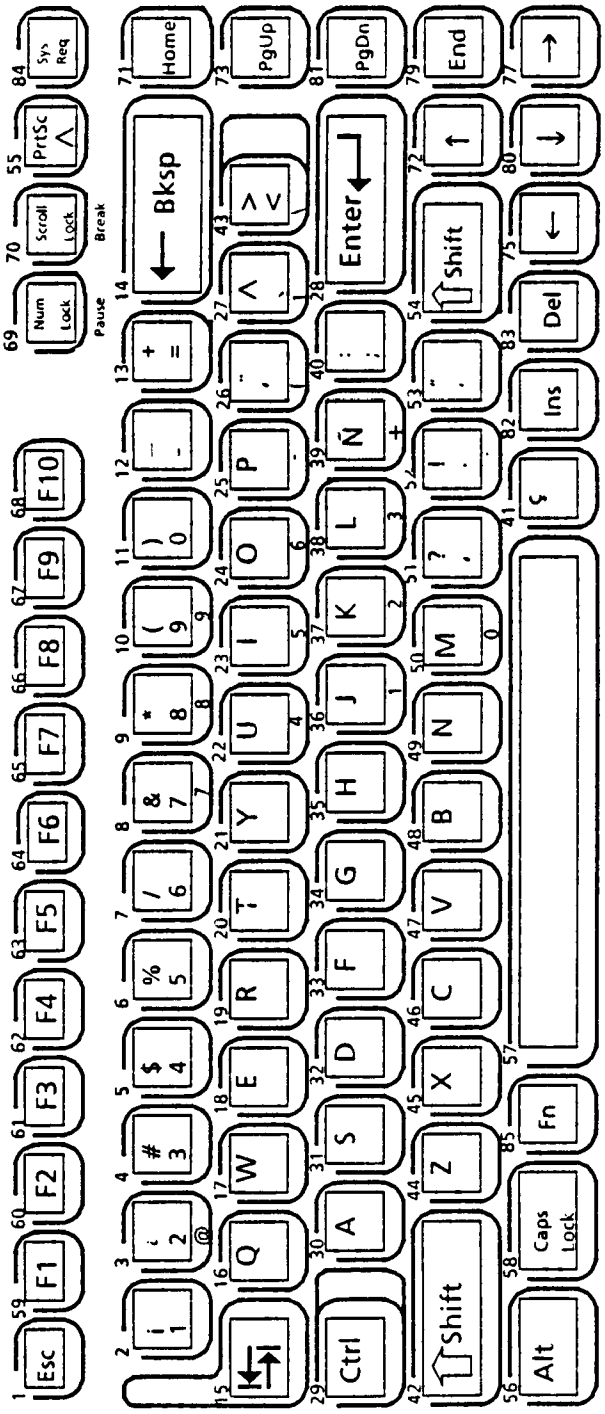


FIGURE 5-16 Spain Version

5.4.6 Italy version

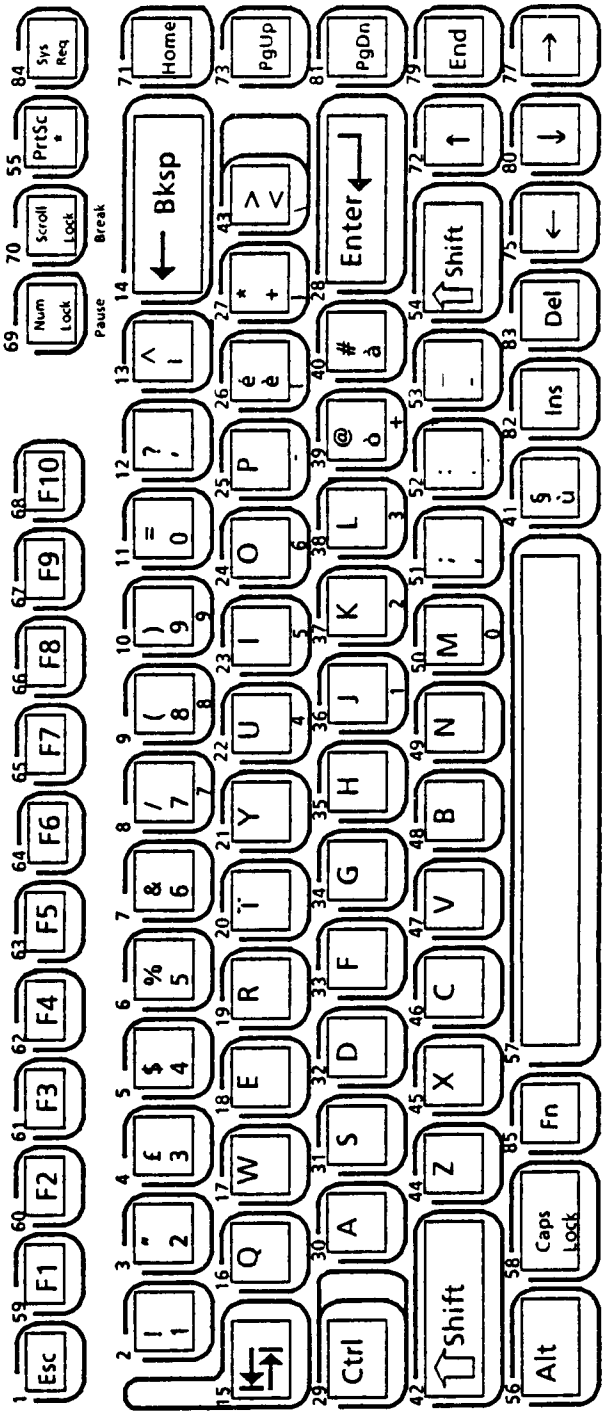


FIGURE 5-17 Italy Version

5.4.7 Scandinavia version

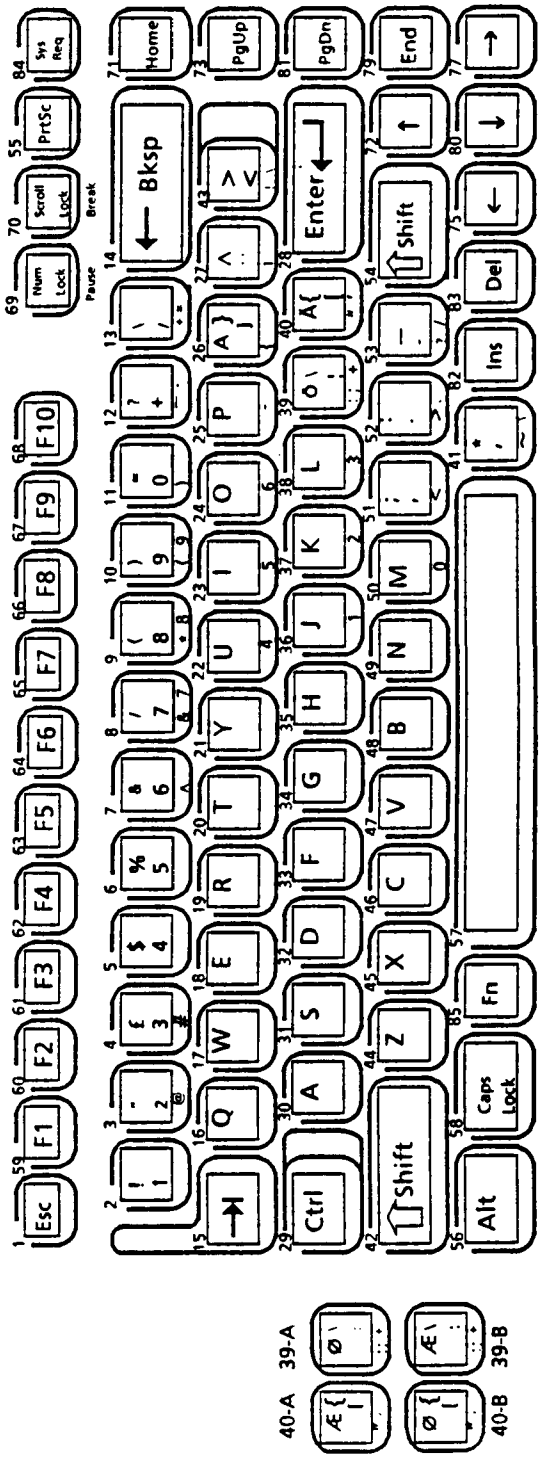


FIGURE 5-18 Scandinavia Version

5.4.8 Switzerland version

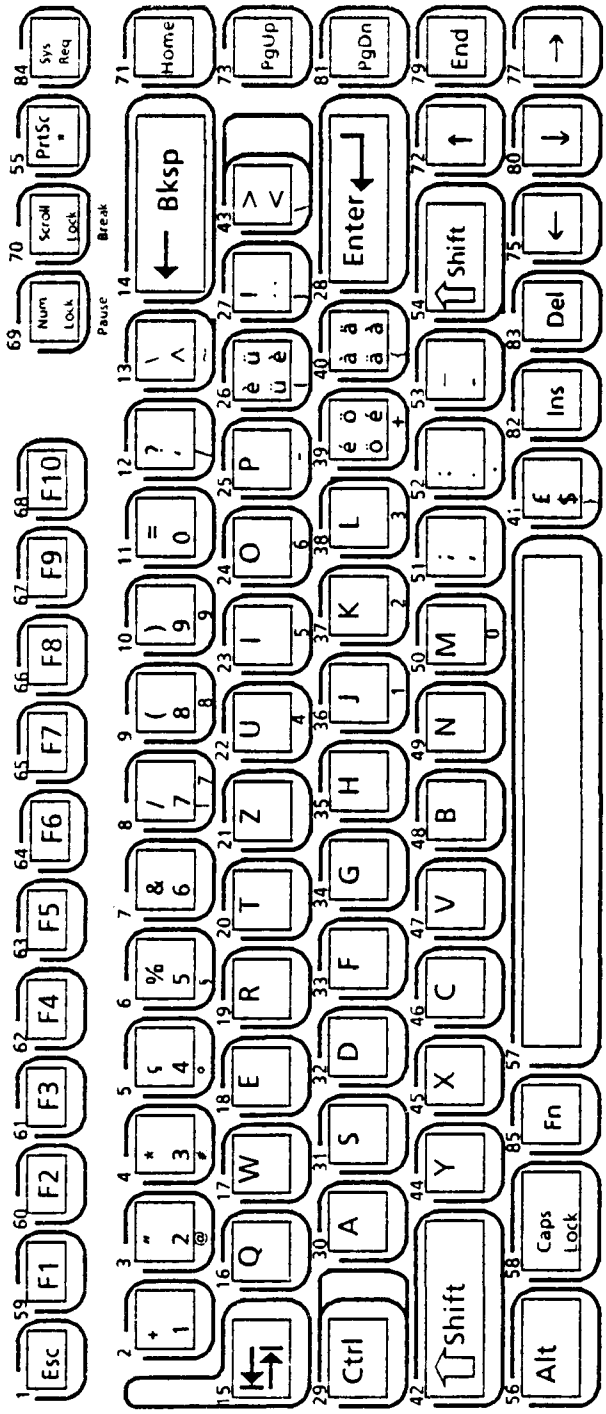


FIGURE 5-19 Switzerland Version

5.4.9 Keycap number

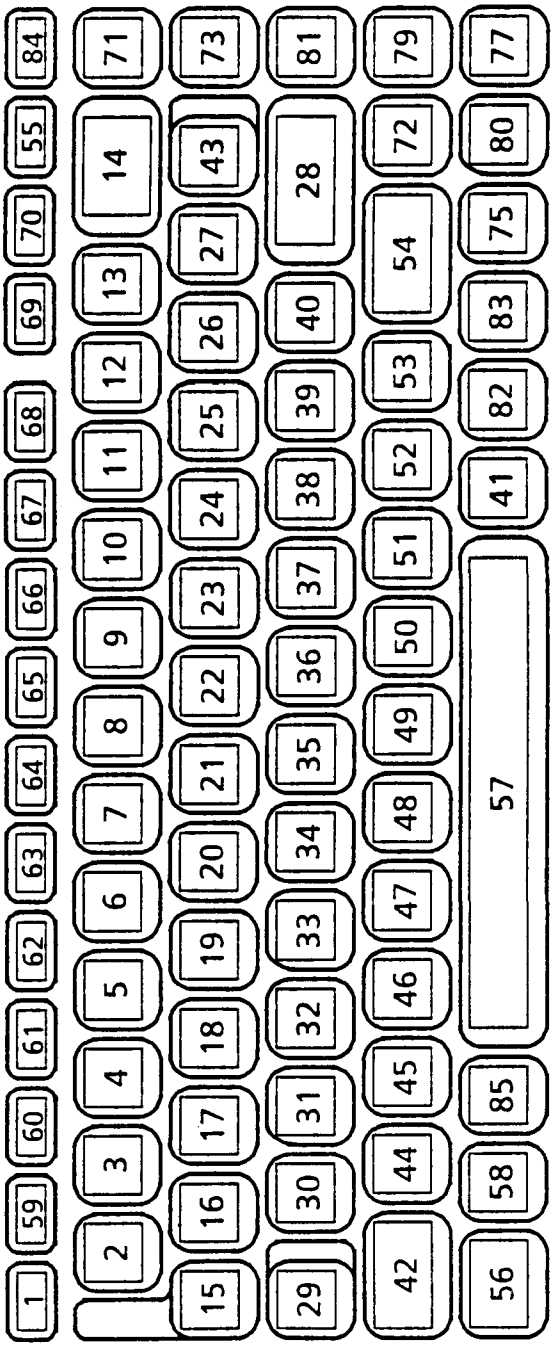
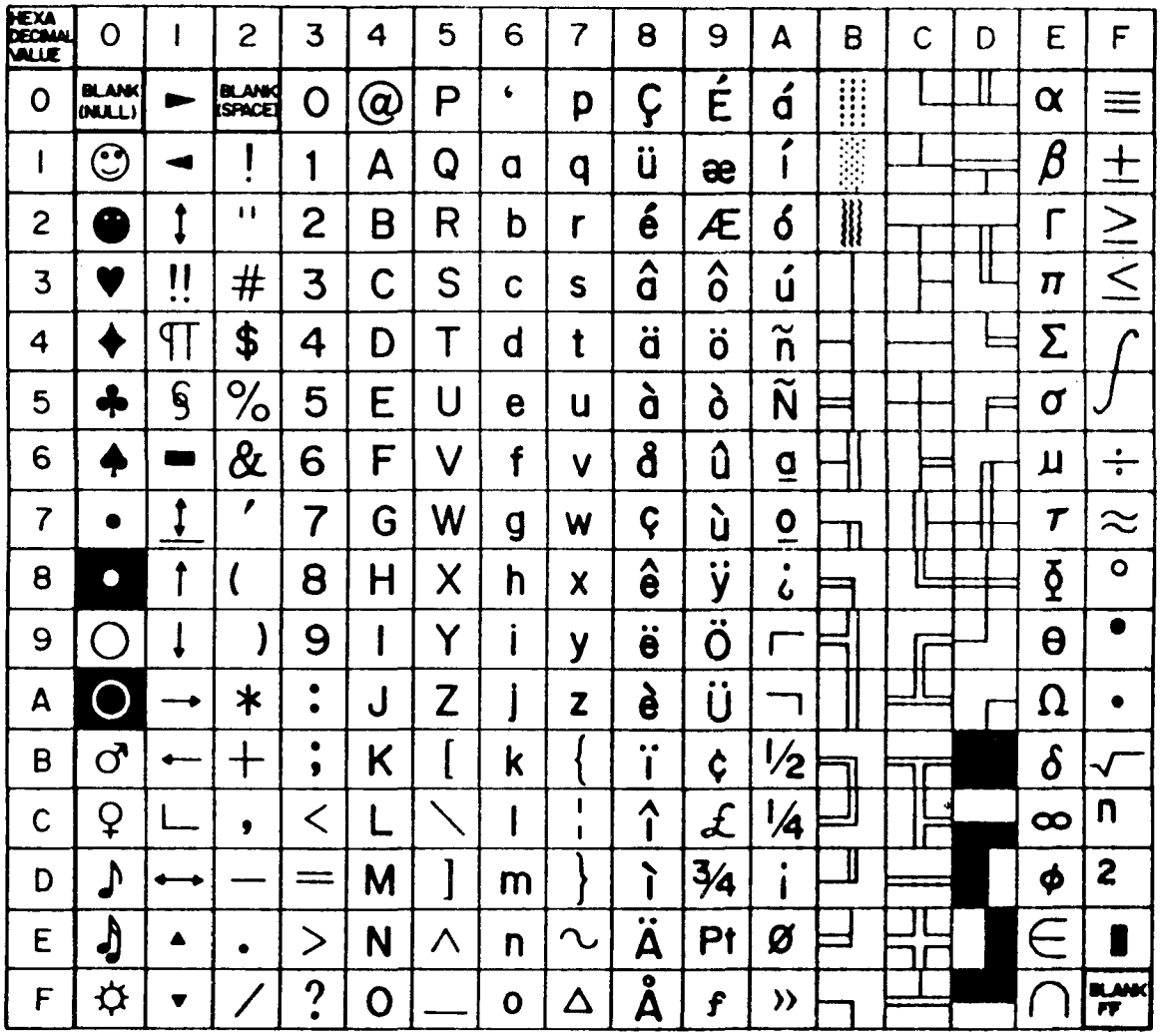


FIGURE 5-20 Keycap Number

5.5 DISPLAY CODE

TABLE 5-7 Display Code



APPENDIX A

SUPER INTEGRATION - T7885, T7885A

A.1 GENERAL

The super integration (T7885, or T7885A) is the system LSI that configures the 16-bit personal computer T1000, which uses the 80C88 for its microprocessor.

T7885 contains 144 pins for its functions, and is composed of various components, the detailed explanation about which is given in A.3.

Following is the list of main components and functions that T7885 or T7885A contains.

(1) Clock Generation (8284)
(2) 8088 Bus Controller (8288)
(3) 8088 Interrupt Controller (8259)
(4) Memory & I/O Address Control
(5) System Bus Control
(6) DMA Controller (82C37)
(7) Keyboard Interface
(8) Speaker Interface
(9) External Bus Controller
(10) Floppy Disk Controller (8565)

A.2 BLOCK DIAGRAM

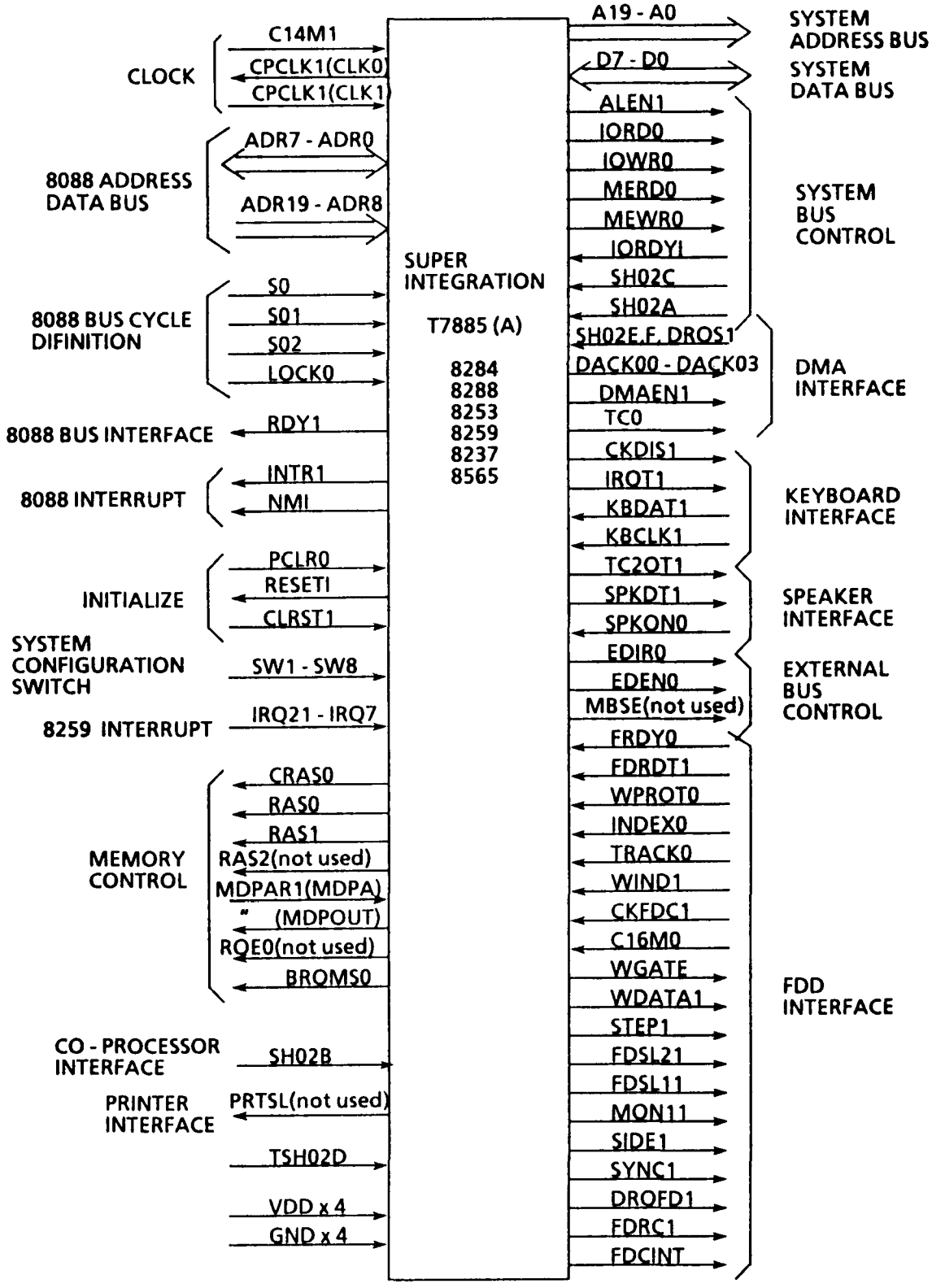


FIGURE A-1 Block Diagram

A.3 **PIN DESCRIPTION**

TABLE A-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1	I	RQFDC	DRQFD1 (DMA REQUEST FROM FDC) This is a DMA request signal from FDC, and is assigned to DREQ2 inside the G.A. It needs pulling-up outside the GA.
2	O	FDCINT	FDC INTERRUT REQUEST This is a signal to indicate that FDC is requiring the interrupt service. In the non-DMA mode, this signal is output per byte, and in the DMA mode, it is output when command operation is completed. It is connected to the IR6 interrupt pin inside the G.A.
3	I	$FDC	CKFDC1 (CLOCK FDC) This signal is the clock for the floppy disk controller
4	I	WIND	WIND1 (WINDOW) This is the signal generated in the VFO circuit, and is used to sample FDRDT signal.
5	O	SYNC	SYNC1 This is a signal to designate the operation mode of the VFO circuit. When this signal is "1", read operation is enabled, and when "0", it is disabled.
6	O	SIDE	SIDE1 (SIDE SELECT) This is a signal used to select the head of either side 0 or side 1. When this signal is "0", head 0 is selected, and when "1", head 1 is selected.
7	O	FDRC	FDRC1 (FDC DIRECTION) This is a signal to designate moving direction of the head. When this signal is "0", the direction is outward, and when "1", inward.
8~11	O	DACK0 ~ DACK3	DACK00 ~ DACK03 (DMA ACKNOWLEDGE) This is the signal that notifies each peripheral of the fact that DMA service is acknowledged. When DACK0 is active, it indicates that refresh cycle is being performed.

Pin	I/O	Symbol	Signal name and Description
12	O	EOP	TC0 (TERMINAL COUNT) This signal is output when DMA channel has reached the terminal count.
13~15	I	DREQ1 ~DREQ3	SHO2E, SHO2F, DRQS1 (DMA REQUEST) These are the DMA request signals input from the I/O devices for DMA service. These signals must be kept the same status until its acknowledged signal DACK is activated. They correspond to DREQ1 ~ 3 signals.
16	-	CAS0	FDCLK1 (4MHz FDC CLOCK OUT in the T7885A) In the T7885, this pin is not used and must be kept open.
17	-	CAS1	NO CONNECT
18~19	I		POWER + 5Vcc is supplied through these pins.
20	-	CAS2	NO CONNECT This pin is not used, and must be kept open .
21	O	INTR	INTR1 (INTERRUPT REQUEST) This signal is connected to the INTR pin of the 80C88 processor. This signal corresponds to INT signal output from the 8259.
22~27	I	IR2~IR7	IRQ21 ~ IRQ7 (INTERRUPT REQUEST) These signals correspond to the IR input signal of the 8259. Unused pins must be externally pulled up by the resistance of more than 10k Ohms.These are input asynchronously. An internal request is executed by raising an IR input (low to high), and holding it high until it is acnowledged (Edge Triggered Mode), or just by a high level of on an IR input (Level Triggeres Mode).
28	-	MAST	SH02G (NO CONNECT) This pin is not used, and must be kept free.

Pin	I/O	Symbol	Signal name and Description
29	I	CLKI	PROCESSOR CLOCK IN This signal is used in the T7885 as the clock for bus controller, DMA controller, and as the timer clock with a quarter of the desired frequency.
30	O	ALE	ALEN1 (ADDRESS LATCH ENABLE) This is a timing signal output from the bus controller to latch the addresses output from the 80C88 processor.
31	O	MER	MERD0 (MEMORY READ) This is a memory tread timing signal, and is output during the DMA cycle or processor cycle. This signal is output also during refresh cycle.
32	O	MEW	MEWR0 (MEMORY WRITE) This is a memory write timing signal, and is output during the DMA cycle or processor cycle.
33	O	IOR	IORD0 (IO READ) This is an I/O read timing signal, and is output during the DMA or processor cycle.
34	O	IOW	IOWR0 (IO WRITE) This is an I/O write timing signal, and is output during the DMA or processor cycle.
35~37	I	S0 S1 S2	S00, S01, S02 (STATUS) These signals are connected to the pins S0, S1, and S2 of the 8088 processor respectively. Status signals are active from T4 clock high-level to T2 through T1. When READY signal of the 80C88 is at high level, with the clock level of T3 or TW, this signal becomes the passive state of (1,1,1), and is used for bus controller.

Pin	I/O	Symbol	Signal name and Description
38	O	READY	READY1 (PROCESSOR READY) This signal is connected to the READY pin of the 80C88 processor, and notifies the processor of the fact that data transmission between the GA and I/O or memory has completed.
39	O	CLK0	CPCLK1 (PROCESSOR CLOCK OUT) This is a processor clock used inside the 80C88 processor and the T7885. This is connected to the CLKI pin.
40	O	RESET0	RESET1 (RESET OUT) This is a reset signal used to initialize the system. This signal is connected to the RESET pin of the 80C88, and is normally connected to the RESETI pin of this GA itself.
41	I	RESET	PCLR0 This signal is used to reset.
42	I	EFI	C14M1 (EXTERNAL FREQUENCY) This signal is an external clock signal used to output CPCLK1signal. Three times the required clock frequency should be supplied.
43~50	IO	A0~A7	ADR0 ~ ADR7 (ADDRESS DATA BUS) These signals are connected to the AD0 through AD7 pins of the 80C88 processor. In T1 cycle of the 8088 processor, memory / I/O address is input, and in T2, T3, TW1, and T4 cycles, data can be input or output. Address information is latched inside the processor.
51~55	I	A8 ~ A12	ADR8 ~ ADR12 (ADDRESS BUS) These signals are connected to the address lines A8~A12 of the 80C88 processor. Memory /I/O address is output in T1 cycle. The address information is latched inside the processor.
56~57	I	GND	GROUND These are the pins for grounding.

Pin	I/O	Symbol	Signal name and Description
58~64	I	A13 ~A19	ADR13 ~ ADR19 (ADDRESS BUS) These signals are connected to the address lines A13~A19 of the 80C88 processor. Memory/I/O address is output in T1 cycle. The address information is latched inside the processor.
65	I	LOCK	LOCK0 This signal is connected to LOCK of the 80C88 processor . When this signal is active, DMA cycle is not enabled as other masters are prohibited from latching the bus.
66	I	TE	TSH02D (TEST ENABLE) This is the signal used to test this LSI independently of the system. When used within the system, it must be connected to the grouding terminal.
67	I	IORDY	IORDY1 (IO CHANNEL READY HIGH) This signal is usually at high level, but it is to put to low when memory cycle or I/O cycle is extended.
68	I	CRTRDY	SH02A (I/O CHANNEL READY LOW) This signal is usually at low level, but it is to put to high when memory cycle or I/O cycle is extended.
69	I	NPNPI	SH02B (NUMERIC PROCESSOR INTERRUPT) This is an interrupt signal input from the co-processor.
70	I	IOCHK	SH02C (I/O CHANNEL CHECK) This is a parity error signal for external memory and I/O divices. In this system, this signal is not used.

Pin	I/O	Symbol	Signal name and Description
71	I	MDPOUT	MDPAR1 (MEMORY DATA PARITY OUT) This is a parity bit output signal from the memory system. When this signal is input, parity check is executed inside the G.A. Parity check is not carried out in this system.
72	O	MDPA	MDPAR1 (MEMORY DATA PARITY IN) This is a parity bit to be sent to the memory system. Parity generation is executed inside the G.A. Parity check is not carried out in this sytem.
73 74	O	ROE0 ROE1	BROMS0 (ROM OUTPUT ENABLE 0,1) These are ROM read-out timing signals, which are output for reading the memory. ROE0 becomes active when memory address F0000H~F7FFFH is accessed to be read out. This signal is not used. in this system. ROEI becmes active when memory address F8000H~FFFFFH is accessed to be read out.
75	O	CRAS	CRAS0 (ROW ADDRESS STROBE) This is a RAS timing signal for dynamic RAM, which is output whenever memory is accessed. This is output also during the refresh cycle.
76 77 78	O	RAS0 RAS1 RAS2	RAS0, 1, 2 (ROW ADDRESS DECODE 0, 1, 2) RAS0 is activated when memory address 00000H~3FFFFH is accessed, or during the refresh cycle. RAS1 is activated when memory address 40000H~7FFFFH is accessed, or during the refresh cycle. RAS2 is not used in this system.
79	O	NMI	NON-MASKABLE INTERRUPT This signal is not used in this system.

Pin	I/O	Symbol	Signal name and Description
80	O	EDIR	EDIR0 (EXTERNAL DIRECTION) This is a direction control signal, which is generated when the external driver/receiver is installed as the data bus buffer . When this signal is "1", it indicates the output direction, and when "0", it means input direction.
81	O	EDEN	EDEN0 (EXTERNAL DATA ENABLE) This is a signal to enable the output of the external data when the external driver/receiver is installed as the data bus buffer. Normally it is in the state of "Enable". When I/O port of the G.A is read out during the processor cycle, it is inactivated.
82	O	PRTSL	PRINTER CHIP SELECT This is a chip select signal for the parallel printer controller. When the CPU accesses the address 378H~37FH, this signal becomes active.
83	O	AEN	DMAEN1 (ADDRESS ENABLE) When this signal AEN is active, it means that DMA has occupied the bus. During the DMA data transfer, the processor or other devices are prohobited from using the bus.
84	O	MBSE	MEMORY BUS ENABLE This is a signal used to control the output of the data buffer of the DRAM. This signal is not used in this system.
85	I	READY	FRDY0 (FDD READY) This is a signal used to indicate that the FDD is ready to read or write.
86	I	FDRDT	FDRDT1 (FDD READ DATA) This is a Read data signal from the floppy disk through the external VFO circuit. This signal is activated inside the G.A with the signal READY.

Pin	I/O	Symbol	Signal name and Description
87	I	WPROT	WPROT0 (WRITE PROTECT) This signal is used to indicate that the inserted disk is disabled from writing. This signal is enabled inside the G.A, with the signal RWSEK.
88	I	INDEX	INDEX0 This signal is used to indicate the starting point of each track. This signal is activated inside the G.A with READY signal .
89	I	TRACK	TRACK0 This signal indicates that the read/write head is at "track0". This is activated inside the G.A with the signal RWSEK.
90~91	I	VDD	POWER 5Vdc power is supplied through these pins.
92	I	16MHz	C16M0 This is 16MHz clock signal, and is used for the precomp. circuit or for write clock.
93	O	WGAT	WGAT0 (WRITE GATE) When this signal is "1", write operation is enabled, and when "0", read operation is enabled.
94	O	WDAT	WDATA1 (WRITE DATA) This is the data signal written on the disk.
95	O	STEP	STEP1 This is a signal to move the head and is used with the signal FDCDRC. This is activated with the signal RWSEK inside the G.A.
96~97	O	SEL1,SEL2	FDSL11, FDSL21 (DRIVE SELECT) These are the drive select signals.
98	O	MON	MON11 (MOTOR ON) This is the signal to turn the spindle motor.
99~ 118	O	AO0 ~ AO19	A0 ~ A19 (ADDRESS BUS) Addresses from the processor or those from DMA are output by these signals.

Pin	I/O	Symbol	Signal name and Description
119 ~123 & 126 ~128	IO	D0~D7	SD0 ~ SD7 (DATA BUS) During the processor or DMA cycle , the transferred data between the processor and memory or between DMA and I/O ports are input or output through these buses.
129	O	CLKDIS	CKDIS1 (CLOCK DISABLE) This is a signal to prohibit the KBCLK signal sent from the keyboard. This signal is output from the bit 6 of the parallel port B.
130	O	SPKDAT	SPKDT1 (PORT B BIT 1) This is a gate signal for speaker output. When the bit 1 of the Port B is set to "1", it becomes active, and enables the speaker output.
131	I	SPKON	SPKON1 (SPEAKER ON) This signal enables the speaker output, and is input to the bit 4 of the parallel port C.
132	O	IRIS	IRQT1 (INTERRUPT REQUEST) When the data from the keyboard is received, this signal is activated. When the bit 7 of the parallel port B is "1", IRQ1 is inactivated. When this signal becomes active, IR (Interrupt Request) also becomes active inside the G.A.
133	I	KBDAT	KBDAT1 (KEY BOARD DATA) This signal indicates the data input from the keyboard. These data are converted to parallel ones.
134	I	KBCLK	KBCLK1 (KEY BOARD CLOCK) This signal is related to the clock input from the keyboard, and is used to get the timing for receiving the keyboard data.
135	I	RESET1	CLRST1 (RESET IN) There is a reset signal used to initialeze this G.A (T7885).

Pin	I/O	Symbol	Signal name and Description
136 ~143	I	W1 ~ W8	DIP-SWITCH These are 8-bit input signals to designate the system configuration. These signals are read out by the 80C88 processor, by which the state of the system configuration is judged.
144	O	OUT2	TC2OT1 (OUT2) This signal corresponds to OUT2 signal of the 8253 CH2, and is used to adjust the tone of the speaker.

A.4 **FUNCTION OF THE MAIN COMPONENTS**

A.4.1 Clock generator

CPCLK1 is the basic clock signal for the 80C88 processor. It is one third of the frequency obtained by C14M1 signal (EFI pin).

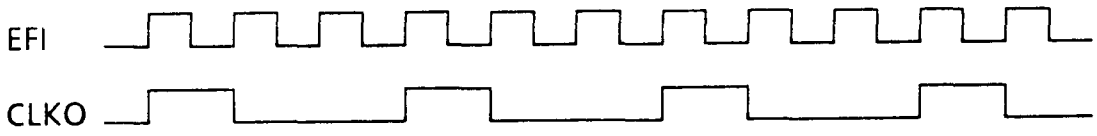


FIGURE A-2 Clock Signal

CPCLK1 signal is connected to the CLKI pin (pin No. 29). CLKI signal is used as the clock that controls the bus and DMA operation.
This signal is output to the timer controller after being reduced to a quarter of its frequency.

A.4.2 8088 Bus controller (READY)

This signal is connected to the READY pin of the 80C88 CPU, and is used to inform that the data transfer with the memory or with I/O devices has finished.
The output timing of this signal varies depending on what kind of data transfer is being done.
The following explains some example of the bus timing.
When the 80C88 processor transfers data with I/O devices, if IORDY and CRTRDY are active, the READY is issued as one wait cycle is asserted.

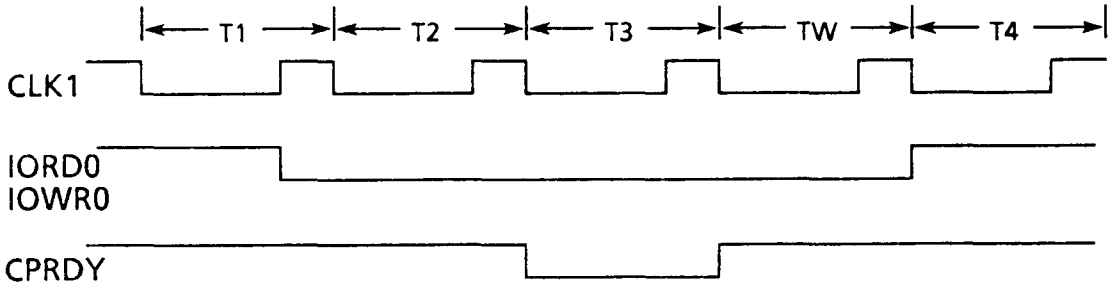


FIGURE A-3 Procssor I/O Cycle READY Timing

When more than one wait cycle is needed, IORDY1 or SH02A signal must be inactive.

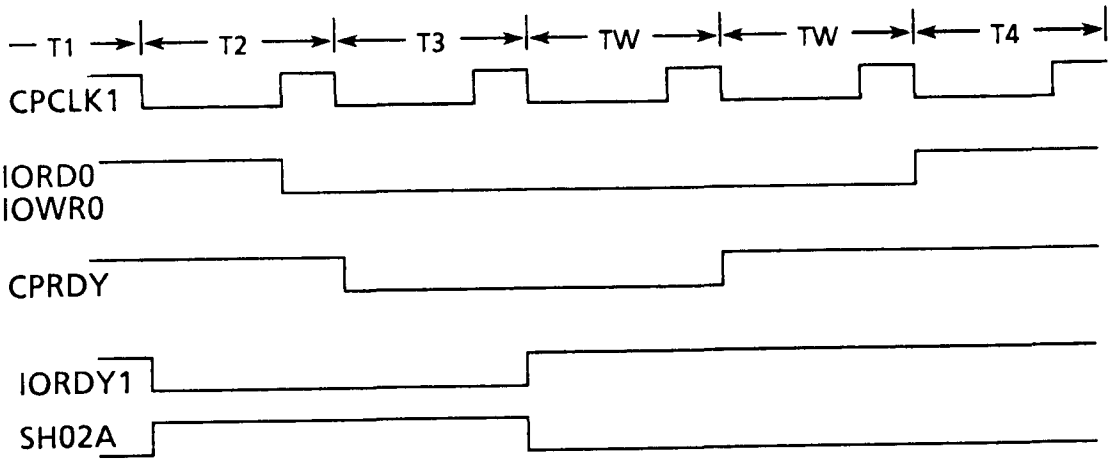


FIGURE A-4 READY Timing of I/O Cycle by IORDY1 or SH02A Signal

Memory data transfer by the 80C88 CPU terminates at "0" wait.

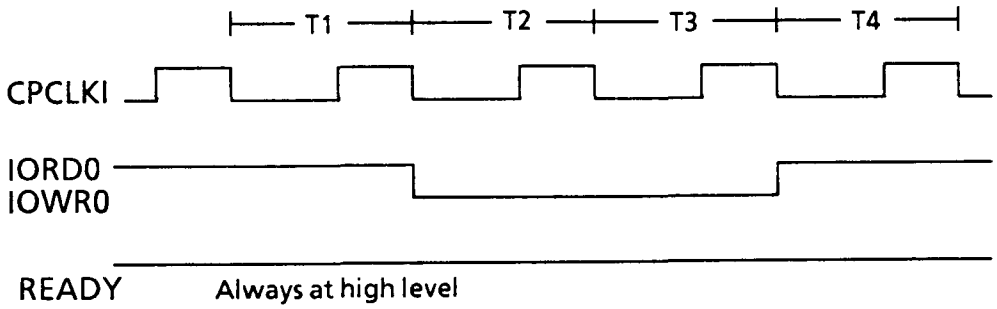


FIGURE A-5 Processor Memory Cycle READY Timing

When one or more wait cycle is needed, IORDY1 or SH02A signal must be inactive.

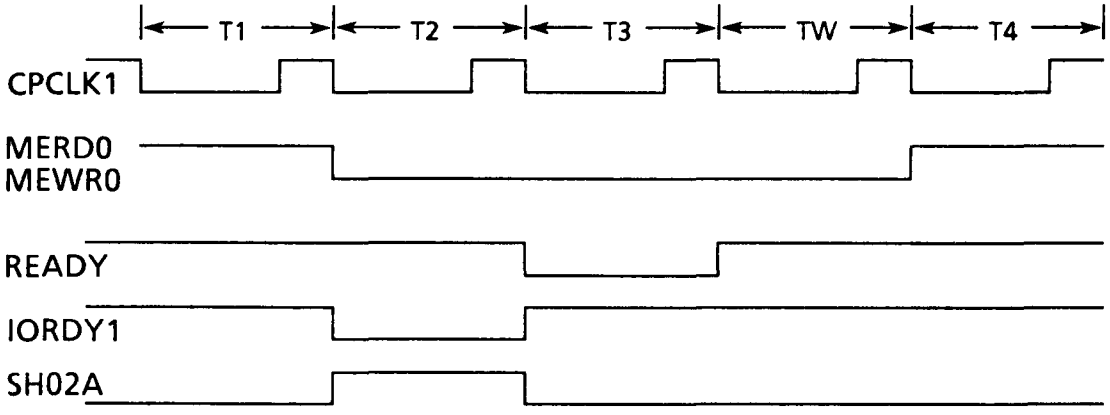


FIGURE A-6 READY Timing of Memory Cycle by IORDY1 or SH02A Signal

During the DMA cycle, READY signal is inactive.

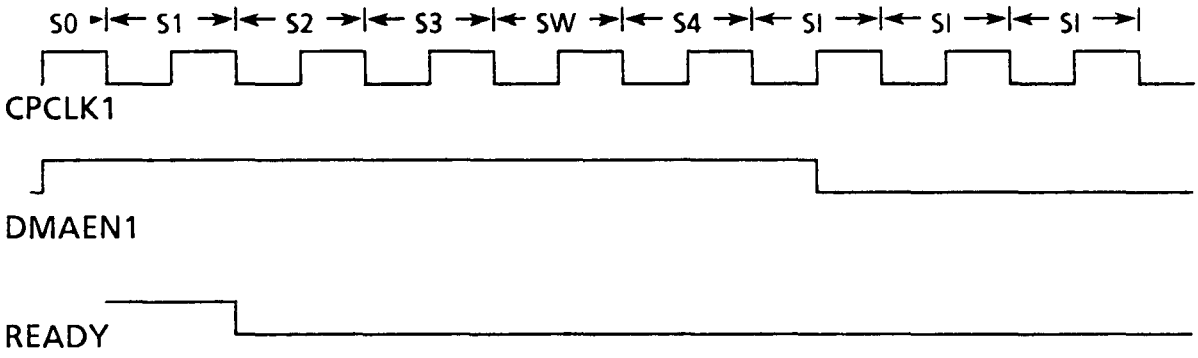


FIGURE A-7 READY in the DMA Cycle

A.4.3 80C88 interrupt

INTR1 signal

The following are the signals, if any of which becomes active and the internal interrupt controller is enabled, then INTR signal is generated.

- Interrupt request signals IR2-IR7 output from external devices
- IR1 or equivalent signal generated when the keyboard data is input
- IR0 generated when the internal timer activates output
- IR6 generated by FDCINT signal

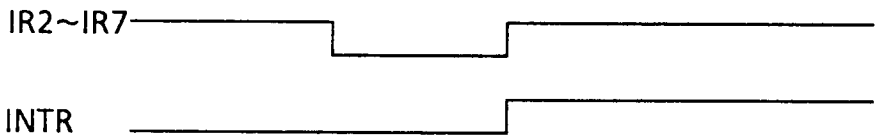


FIGURE A-8 INTR Signal

A.4.4 Memory control

a) CRAS0 signal

This is RAS timing signal output to the DRAM whenever the memory is accessed. It is also output during the refresh cycle.

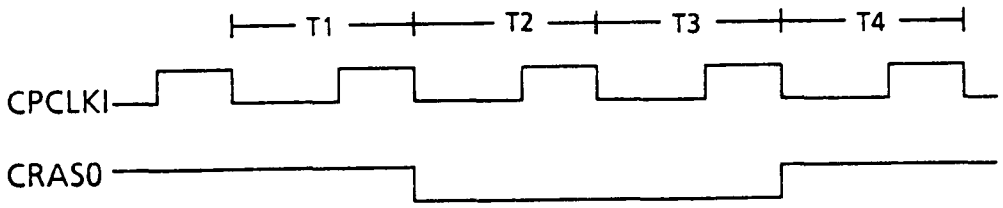


FIGURE A-9 CRAS0 during the Processor Cycle

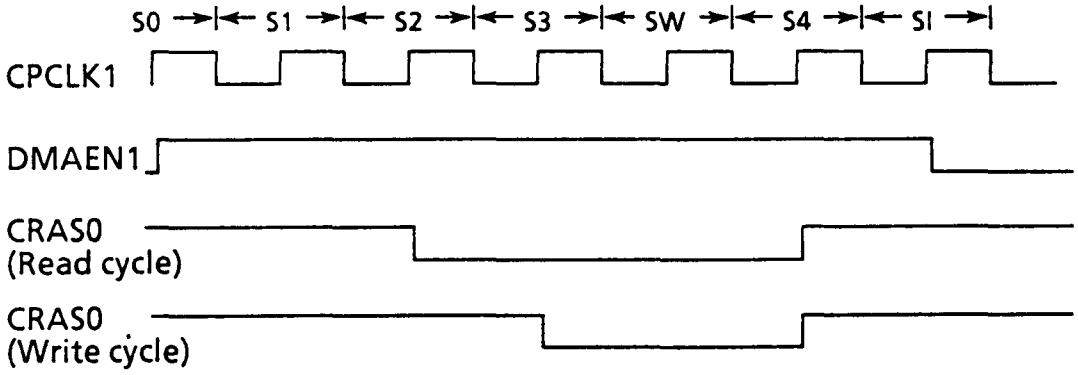


FIGURE A-10 CRAS0 during the DMA Cycle

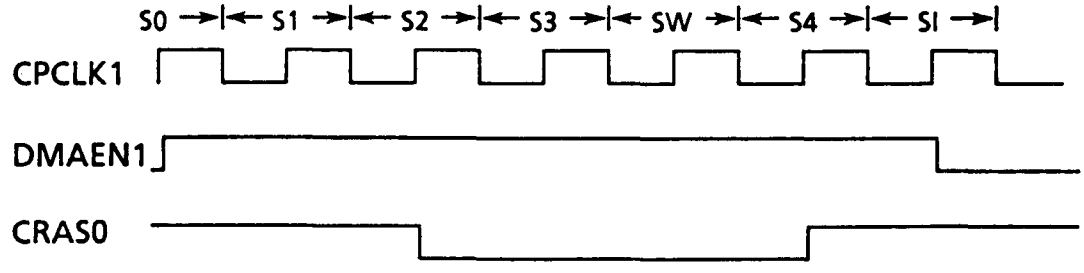


FIGURE A-11 CRAS0 during the Refresh Cycle

b) RAS0, RAS1, RAS2

These are the decoded address signals.

RAS0 (RAS01) becomes active when the memory address between 00000H-3FFFFH is addressed.
RAS1 (RAS11) becomes active when the memory address between 40000H-7FFFFH is addressed.
RAS2 (RA21) becomes active when the memory address between 80000H-9FFFFH is addressed. RAS2 is not used.
During the refresh cycle, all of these three signals become active.

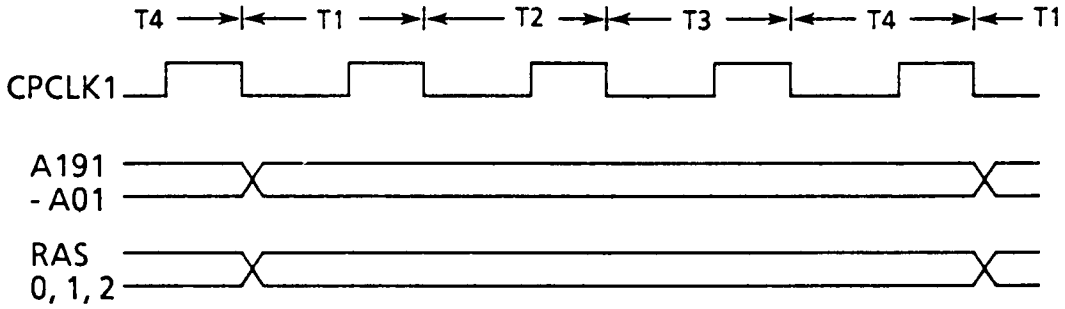


FIGURE A-12 RAS0, RAS1, RAS2 during Processor Cycle

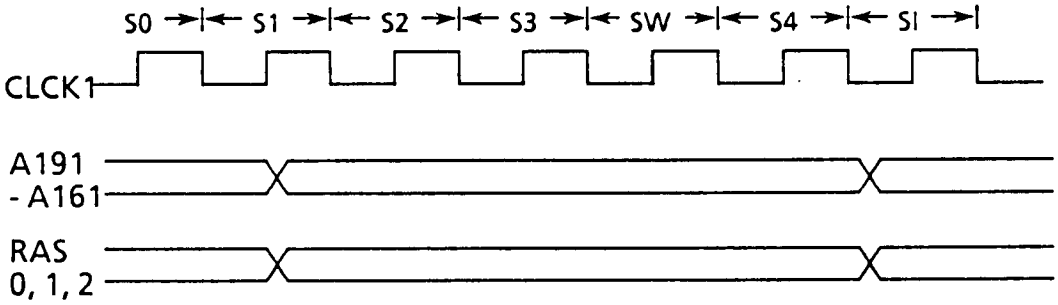


FIGURE A-13 RAS0, RAS1, RAS2 during the DMA Cycle

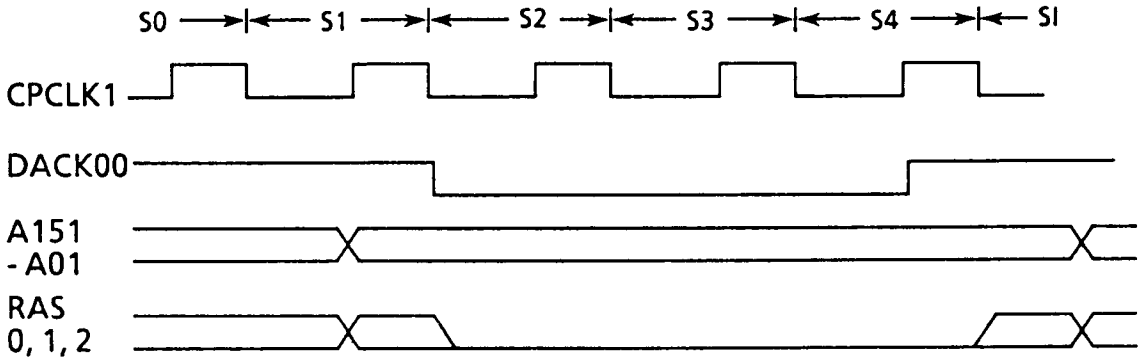


FIGURE A-14 RAS0, RAS1, RAS2 during the Refresh Cycle

c) ROE0, ROE1 (BROMS0)

This is the timing signal for reading out the ROM, and is output when the ROM is read out.
ROE0 becomes active when the address between F0000H-F7FFFH is read out, while ROE1 (BROMS0) becomes active when the address between F8000H-FFFFFH is read out. ROE0 is not used.

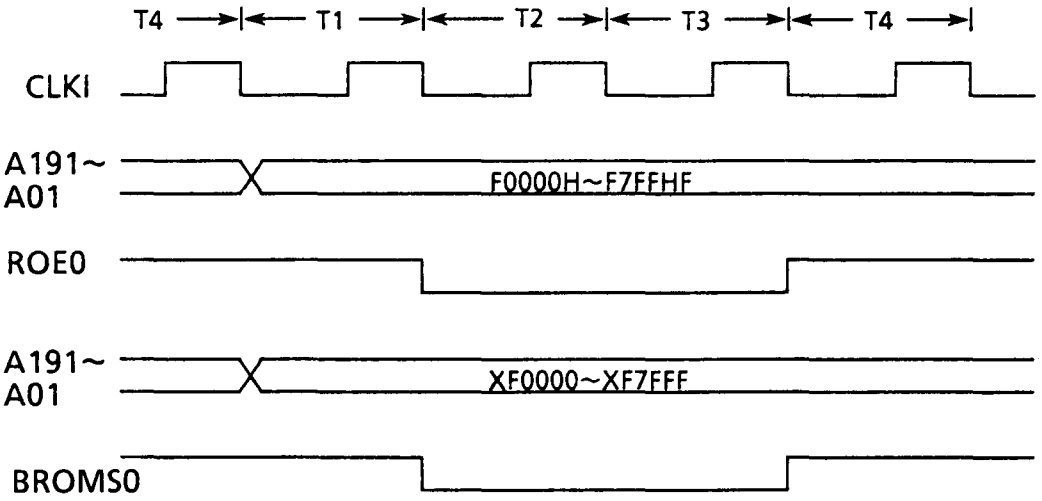


FIGURE A-15 ROE0, ROE1 Timing

A.4.5 System bus controller

a) ALE

This is the latch timing signal of the address from the processor, and is output by the bus controller. This signal is not used.

b) IORD0, IOWR0

These are I/O read/write timing signals, during the processor or DMA cycle.

c) MERD0, MEWR0

These are the memory read/write timing signals during the processor or the DMA cycle.

d) IORDY1, SH02A (CRTRDY)

These are READY signals used to extend the processor cycle or the DMA cycle.

e) IOCHK (SH02C)

This is a parity error signal to inform that there is some error in the expanded memory or other devices on the system bus.

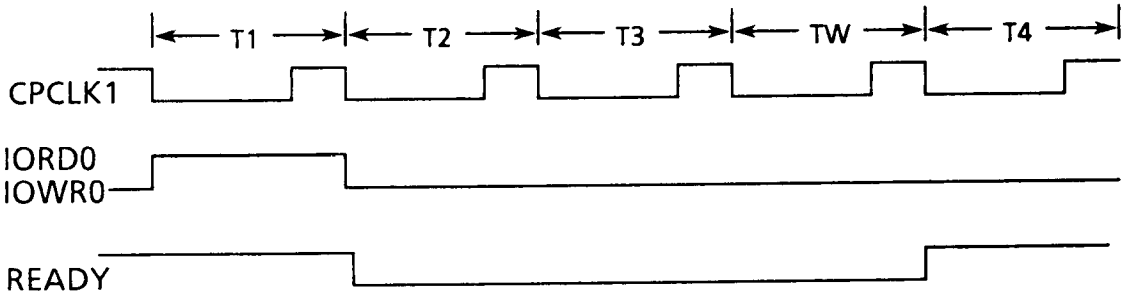


FIGURE A-16 ALE, IORD0, IOWR0 during the Processor Cycle when IORDY1 and SH02A are both active.

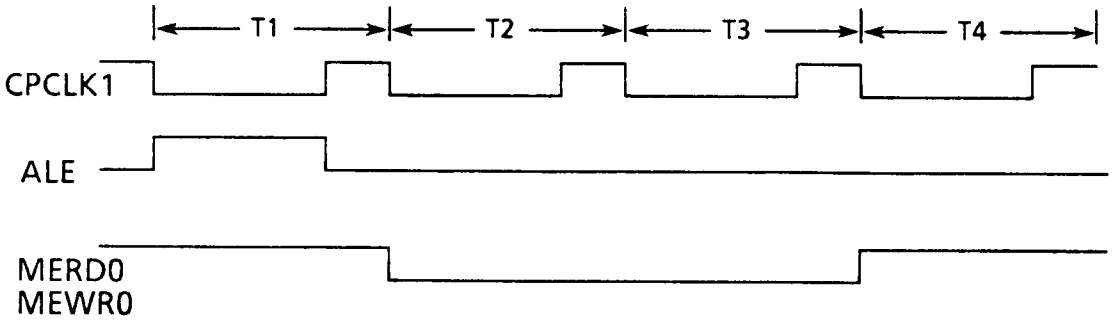


FIGURE A-17 ALE, MERD0, MEWR0, during the Processor Cycle when IORDY1 and SHO2A are both active.

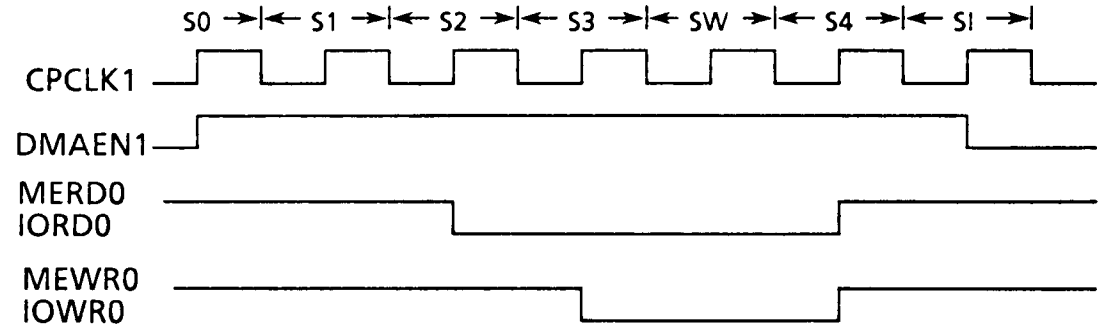


FIGURE A-18 IORD0, IOWR0, MERD0, MEWR0 during the DMA Cycle when IORDY1 and SHO2A are both active.

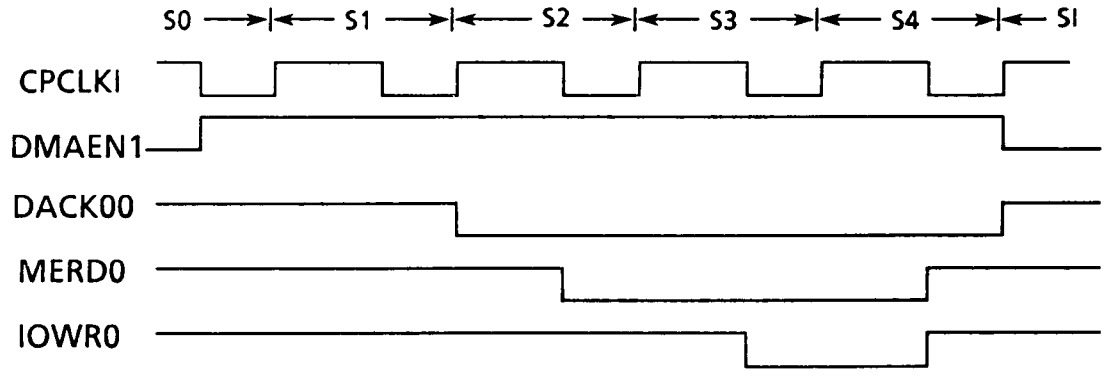


FIGURE A-19 MERD0, IOWR0 during the Refresh Cycle when IORDY1 and SHO2A are both active.

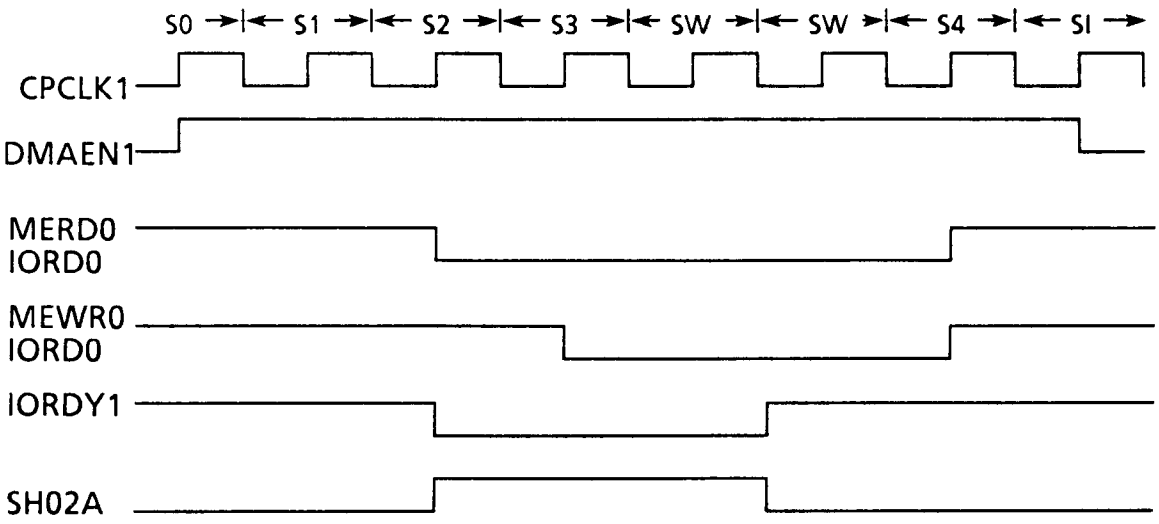


FIGURE A-20 IORDY1, SHO2A during more than one wait DMA Cycle

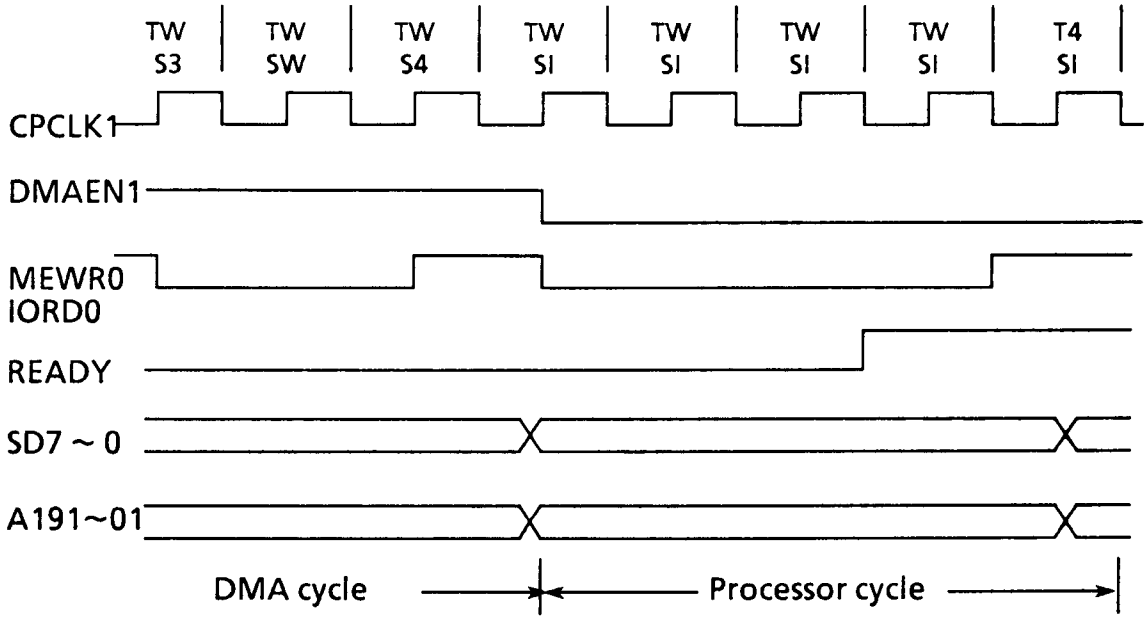


FIGURE A-21 Cycle Steal

A.4.6 DMA interface

a) DREQ1 - DREQ3

This is the signal that requires the DMA service, and when it is accepted, its acknowledging signal DACK becomes active.

b) DACK00-DACK30

This is the signal to indicate that the DMA service request is acknowledged.
DACK00 and DACK30 are used.

c) DMAEN1

This signal indicates that DMA has occupied the bus.

d) TC0

This signal becomes active when the DMA channel has come to the terminal count.

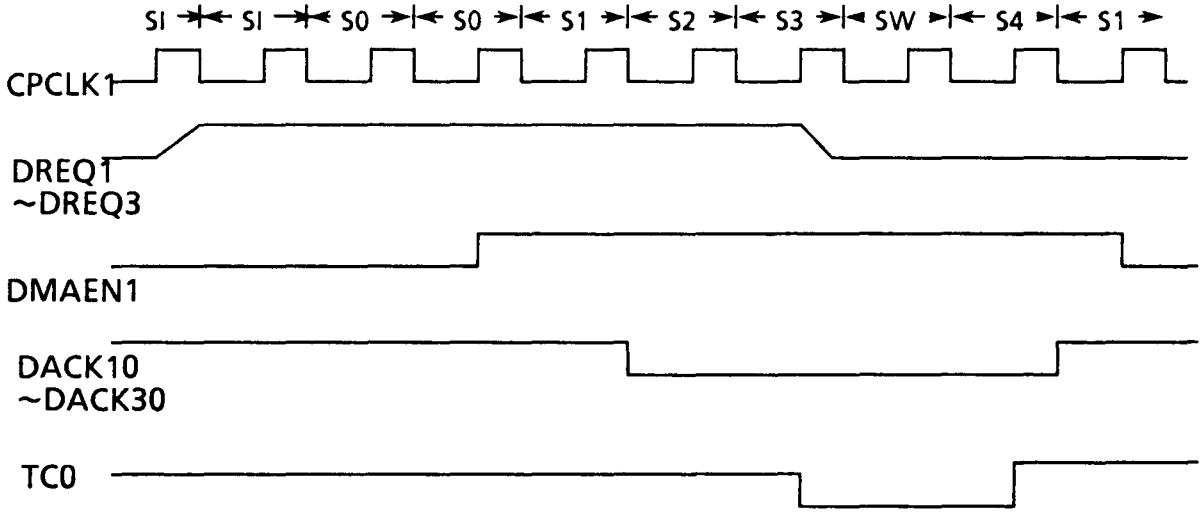


FIGURE A-22 DMA Interface Timing

A.4.7 Keyboard interface

This interface acquires data KBDAT1 from the keyboard and the timing signal KBCLK for this operation, and changes the serial data to the parallel one. When the data transfer to this interface is completed, IRQ1 signal is activated, and notifies of it to outside the interface, outputting the interrupt signal INTR to the processor.
The processor starts processing the data after accepting the interrupt, and during this process, it sets up bit 6 of the parallel port B, and disables KBCLK signal.

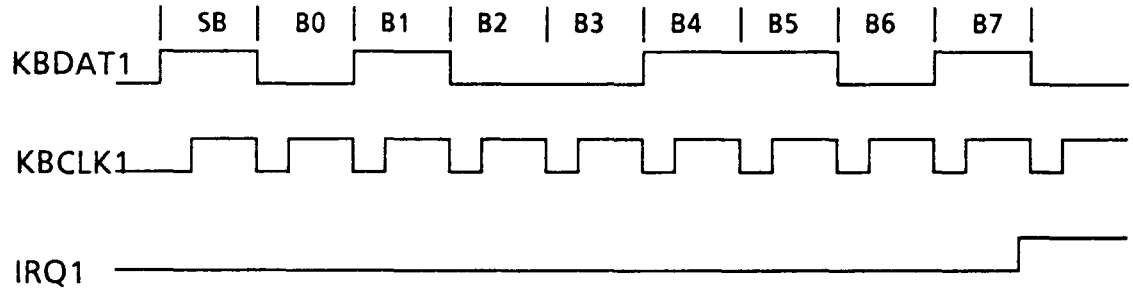


FIGURE A-23 KBDAT1, KBCLK1, IRQ1 Timing

SB ..... Start bit
BO ..... bit 0

The transition from high to low level of IRQ1 synchronizes the one from low to high level of CPCLK1 signal.

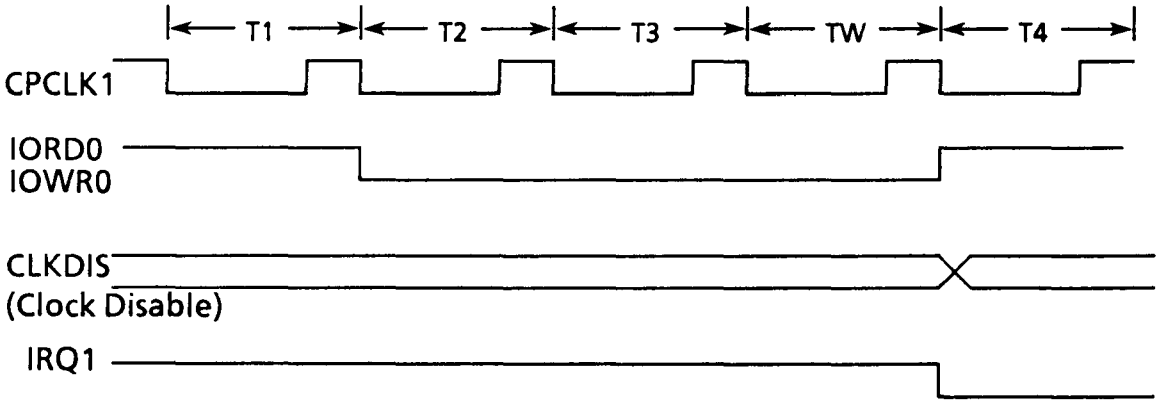


FIGURE A-24 IRQ1 Reset Timing

A.4.8 Speaker interface

TC2OT1 signal is used to adjust the tone of the speaker, when channel 2 of the timer is output. This signal is output at the transition of high to low level of CPCLK1 signal.
PB1 signal is output at the bit 1 of the port B, and activates the TC2OT1 signal externally.
SPKON0 is an input signal to confirm whether the speaker signal is correctly output after reinputting it, and is sent to the bit 4 of the port C.

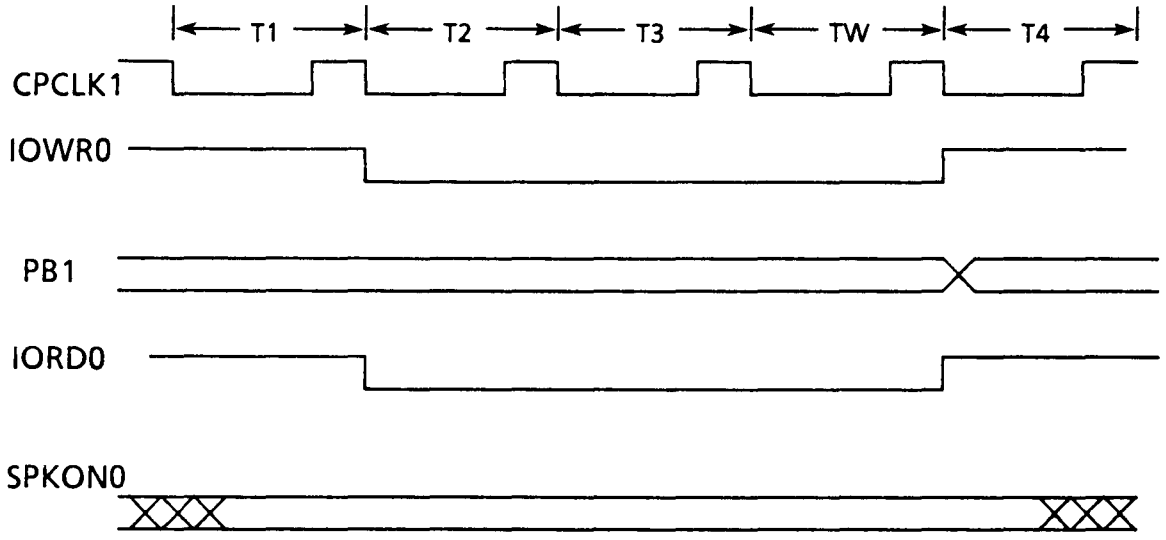


FIGURE A-25 Speaker Interface Timing

A.4.9 External bus controller

a) EDEN0, EDIR0

These signals control the output data and its destination on buffering the data bus, by setting the external bus driver receiver in the data buses SD7-SD0.
EDEN0 output control signal is inactivated during the processor cycle, when reading the I/O in the T7855 super integration.
EDIR0 destination control signal is inactivated, when the memory transmission between the external I/O devices and memory, during the DMA cycle or the processor reading cycle.

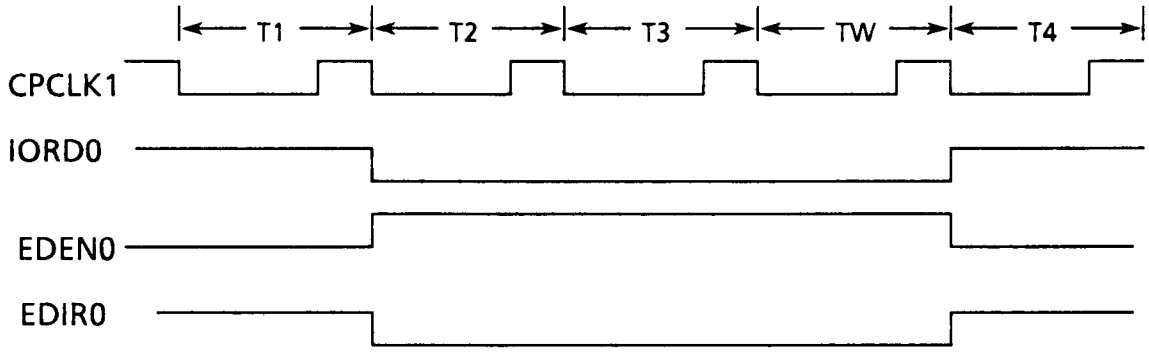


FIGURE A-26 EDEN0, EDIR0 during the Processor Cycle

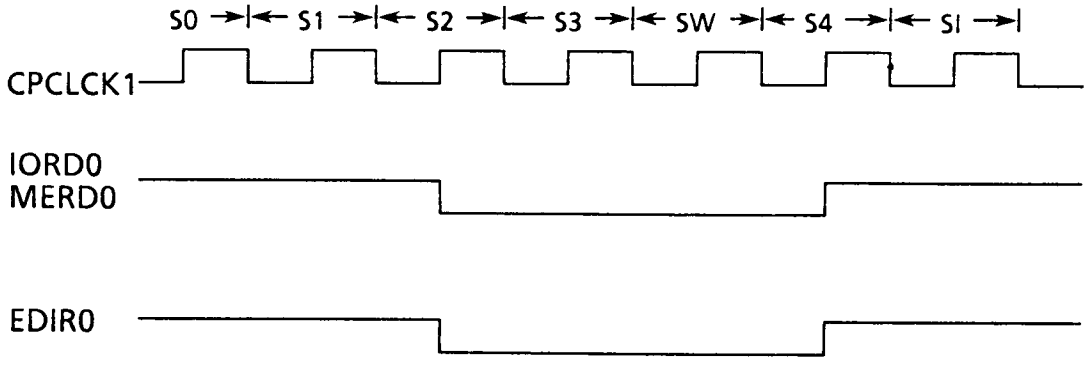


FIGURE A-27 EDIR0 during the DMA Cycle

b) MBSE0

This is the signal that controls the output of the data driver receiver of the DMA memory. The destination control is executed by MERD0 signal.
When the address between 00000H-9FFFFH is addressed, it is activated, but during the refresh cycle, it is inactivated.
This signal is not used in this system.

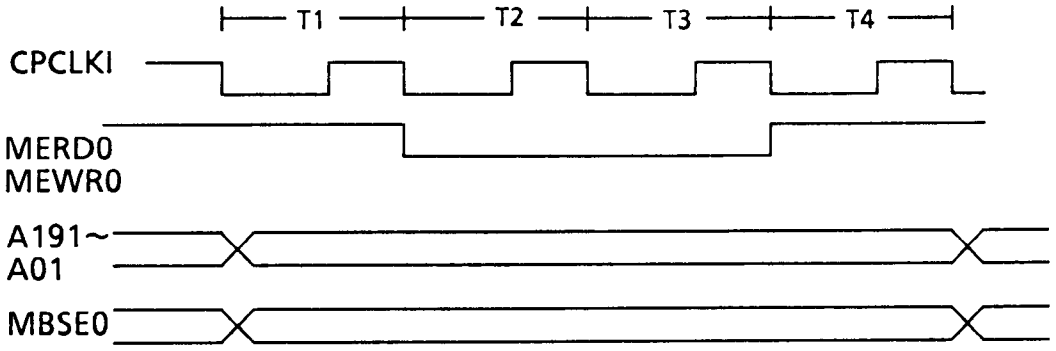


FIGURE A-28 MBSE0 during the Processor Cycle

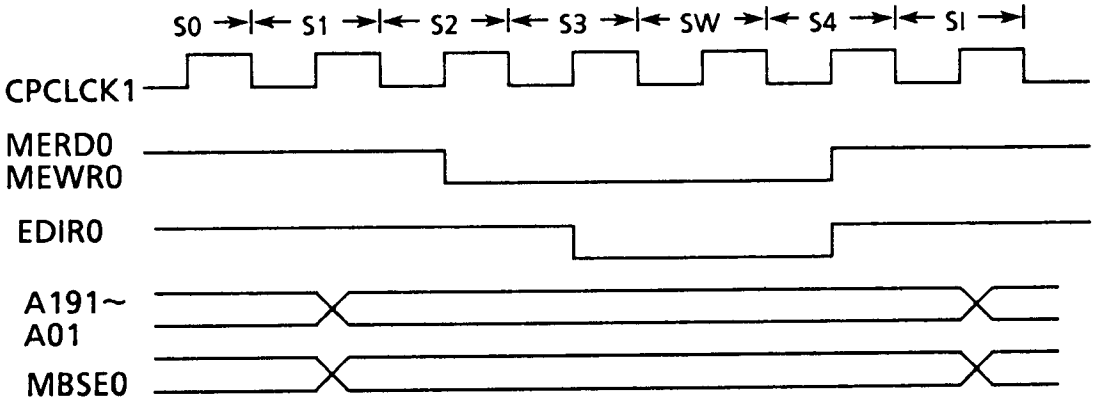


FIGURE A-29 MBSE0 during the DMA Cycle

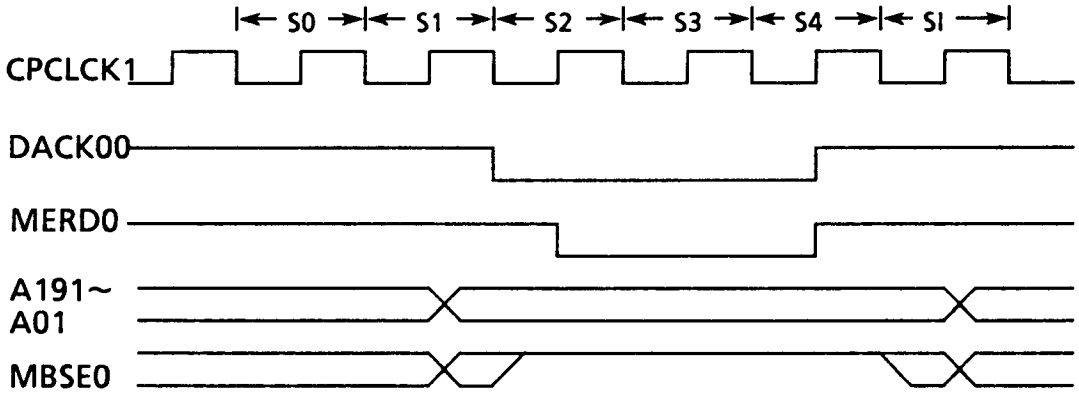


FIGURE A-30 MBSE0 during the Refresh Cycle

A.4.10 FDD interface

a) MON11, FDSL11, FDSL21

MON11 is the signal that turns the FDD spindle motor round, and FDSL11, FDSL21 are the drive selecting signals.
These three signals are output by setting the corresponding bis in FDD output register.
When bit 4 or bit 5 of the FDD output register is set, MON11 signal is activated.
FDSL11 is activated when bit 4 of the FDD output register is set and bit 1 and bit 0 are also both reset.
FDSL21 is activated when bit 5 and bit 0 are set and bit 1 is reset.

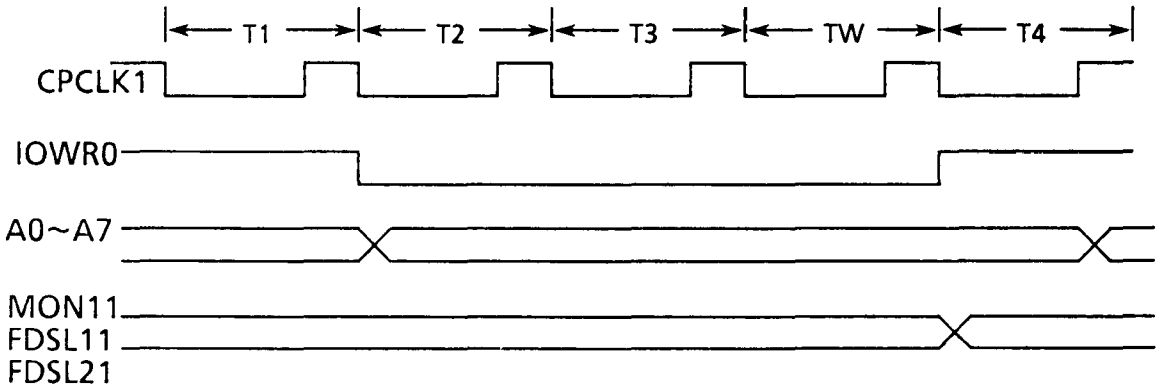


FIGURE A-31 MON11, FDSL11, FDSL21 Output Timing

b) CKFDC1

This is a clock signal for FDC and its frequency is 8MHz.

c) FRDY0, WPROT0, INDEX0, TRACK0

These signals are input from the drive unit.

d) SIDE1

This is a signal used to select either head "0", or "1" of the double sided drive. When this bit is "0", head "0" is selected.

e) STEP1, FDRC1

These signals are activated when seek opration is executed.

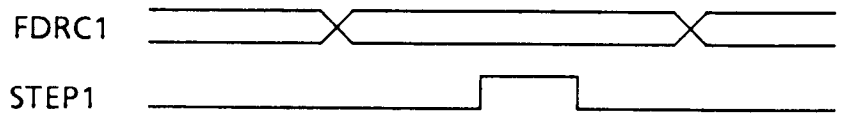


FIGURE A-32 Seek Operation

f) FDRDT1, WIND1, SYNC1

When read operation is executed, SYNC1 signal becomes "1", and WIND1 samples FDRDT1 signal which is composed of the data bit and clock bit.

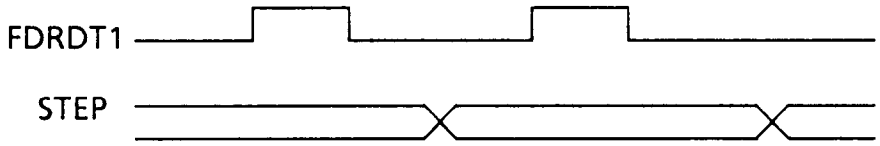


FIGURE A-33 FDC Read Operation

g) C16M0, WGAT0, WDATA1

When write operation is executed, these signals are activated. C16Mo is converted to 500KHz, and is used inside as a write clock.

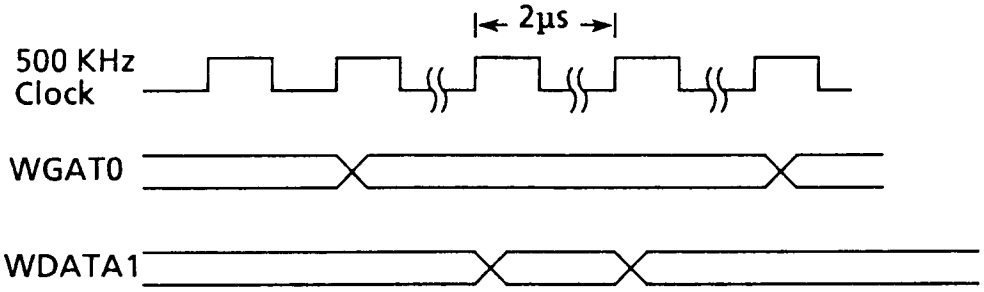


FIGURE A-34 FDD Write Operation

h) DRQFD1

This is the signal used to require the DMA service for FDD operation, and it corresponds to DREQ2 signal of the DMA Controller.
When the FDC receives the DACK20 signal from the DMA controller, it is inactivated.

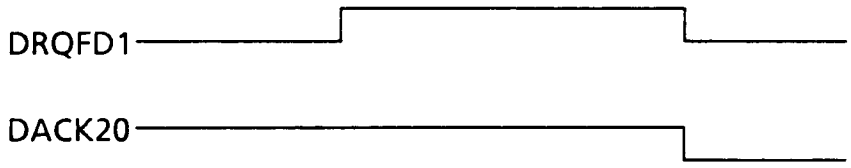


FIGURE A-35 FDC DMA Operation

i) FDC INT

This signal is output at each byte in the non-DMA mode, and is output at the end of the command operation in the DMA mode.
The output signal is connected to IR6 inside the G.A., and the DMA service request signal is output to the processor.
When the processor reads or writes the FDC, FDCINT is inactivated.

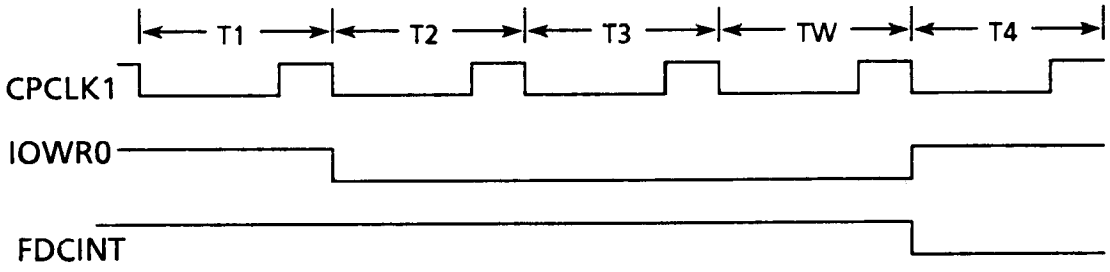


FIGURE A-36 FDCINT Reset Timing

A.4.11 I/O address map

a) I/O address inside the SI chip

TABLE A-2 I/O Address Map

Address	I/O
000H ~ 00FH	DMA Controller (equivalent to the 8237)
021H ~ 021H	Interrupt Controller
040H ~ 043H	Programmable Interval Timer (equivalent to the 8259)
060H	Port A
061H	Port B
062H	Port C
063H	Command / mode Regsiter
081H	DMA CH2 Page Register
082H	DMA CH3 Page Register
083H	DMA CH1 Page Register
0AH	NMI Mask Regsiter
378H ~ 37FH	Parallel Printer
3F0H, 3F1H, 3F4H, 3F5H	FDD Controller
3F2H, 3F3H, 3F6H, 3F7H	FDD Output Register

b) PRTSL

When an address between 378H-37FH is addressed, this signal is activated. In this system, this signal is not used.

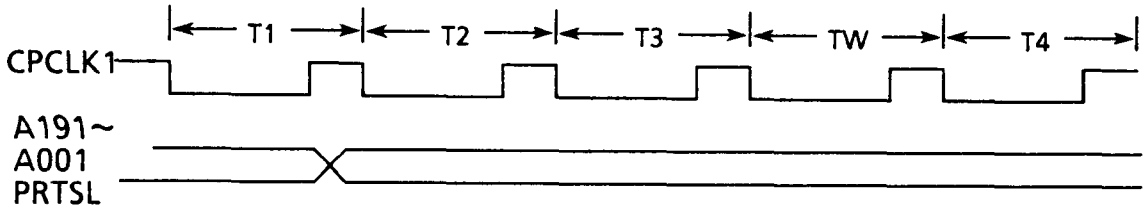


FIGURE A-37 PRTSL Timing

APPENDIX B

I/O CONTROLLER G.A.

B.1 GENERAL

I/O Controller Gate Array is composed of 100 pins and is used for T1000 personal computer.

This gate array includes the printer interface, I/O address decoder, various drivers, and so on.

Functions of the I/O controller are as follows.

(1) Printer Interface
(2) I/O Address Decoder
(3) System RAM Controller
(4) DOS ROM Controller
(5) System Support Port

Detailed explanation of each function is given in B.4.

B.2 **BLOCK DIAGRAM**

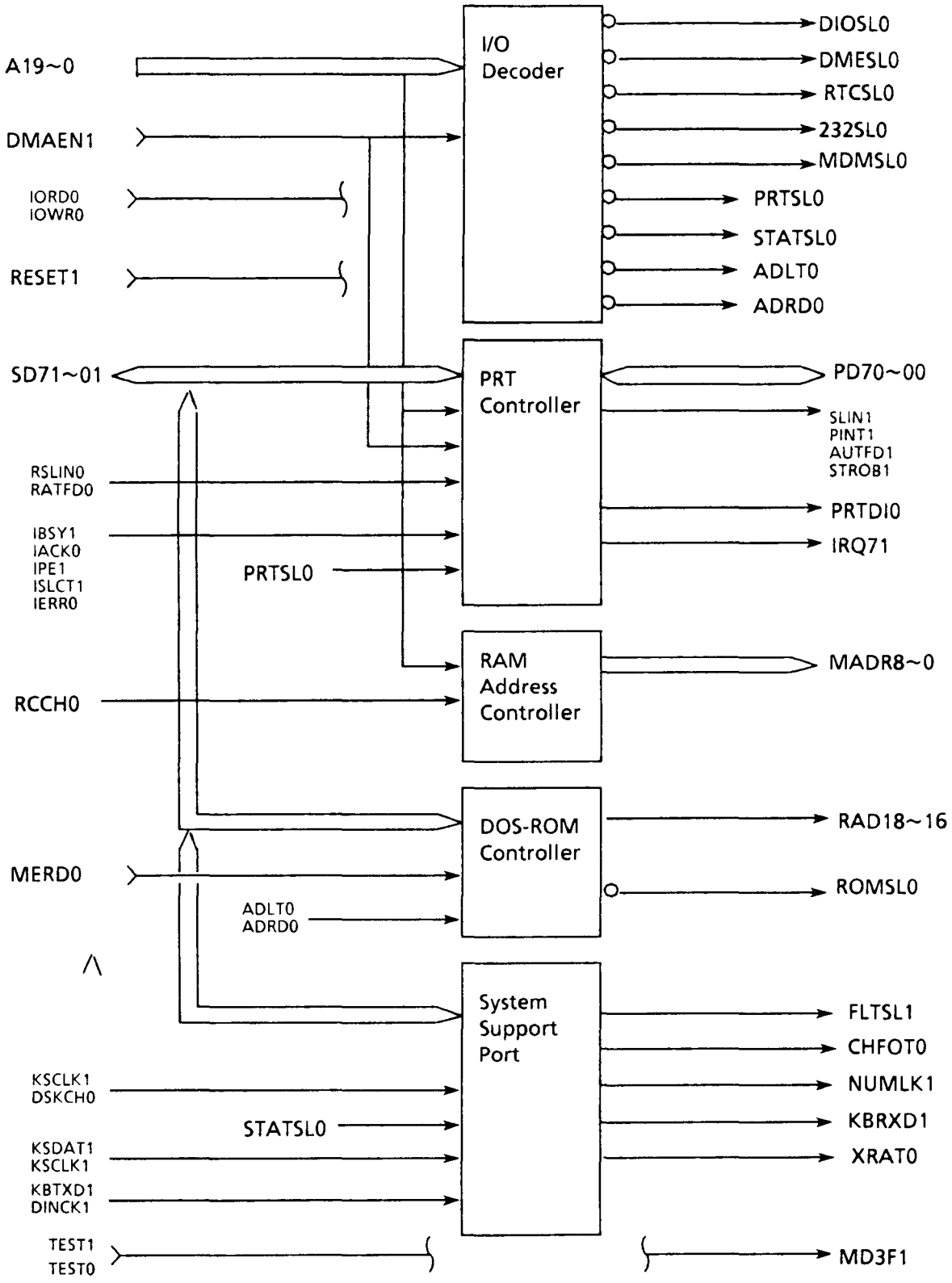


FIGURE B-1 I/O Controller Block Diagram

B.3 **PIN DESCRIPTION**

TABLE B-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1~ 23	I	A19~A0	A19~A10 + : Up to 1 Mbyte of address space is enabled by these address lines during the CPU/DMA cycle.
24	I	AEN	DMAEN1 + : During the DMA cycle, this signal is at high level ("1"), and during that of the CPU, this is at low level ("0").
25	I	MERD	MERD0 - : Read strobe for memory chips
26	I	DSKCH	DSKCH0 - : FDD disk change signal
27	I	IORD	IORD0 - : Read strobe for I/O devices
30	I	IOWR	IOWR0 - : Write strobe for I/O devices
31	O	MDMSL	MDMSL0 - : This signal is used to select I/O register of the modem. This signal is active when it is "0" (2F8H~2FFH / 3F8H~3FFH). Address conversion is executed by MD3F1.
32	O	DIOSL	DIOSL0 - : This signal is used to select I/O register of the display. This is active when it is "0". (3D0H~3DHF)
33	O	DMESL	DMESL0 - : This signal is used to select the display memory. This is active when it is "0" (B8000H~BFFFFH).
34	O	TIMSE	RTCSL0 - : This signal is used to select I/O register of the REAL TIMER. This is active when it is "0".

Pin	I/O	SYMBOL	Signa name and Description
35	O	232SL	232SL0 - : This signal is used to select I/O register of the RS232C. This is active when it is "0" (2F8H~2FFH / 3F8H~3FFH). Address conversion is executed by MD3F1.
36	O	DOSROM	ROMSL0 - : This is the CS signal for DOS-ROM. This signal is active when it is "0" (A0000~AFFFF). When bit 7 of the 0C8H register is "1", this signal is output.
37 ~ 39	O	RAD16 \ RAD18	RAD161, 171, 181 + : These signals correspond to the lines 18~16 (3bits) of the DOS-ROM. When an address between A0000 and AFFFF is selected, this signal is output. Bit allocation of the 0C8h register is as follows; Bit 6 ~3 : not used Bit 2 : RAD181 Bit 1 : RAD171 Bit 0 : RAD161
41	O	COM1/2	MDF31 + : When this signal is "1", 232SL0 signal selects the address between 2F8H and 2FFH, while MDMSL0 signal selects the one between 3F8H and 3FFH. When this signal is "0", 232SL0 signal selects the address between 3F8H and 3FFH, and MDMSL0 signal selects the one between 2F8H and 2FFH.
42	I	DINCK	DINCK1 + : This signal shows a clock output from the keyboard controller, and is used for data transmission between this controller and the keyboard controller.
43	I	KSCLK	KSCLK1 + : This signal shows the status data transfer clock from the keyboard controller. Data are transferred at the transition from high to low level.

Pin	I/O	SYMBOL	Signal name and Description
44	I	KSDAT	KSDAT1 + : This signal shows the status data from the keyboard controller. Data are transferred at the transition from high to low level of this clock.
45	I	KBTXD	KBTXD1 + : This signal shows a transmission line for the read data from the keyboard controller.
46	O	XRAT0	XRAT01 + : When an FDD operation is executed at high speed, this signal is "1".
47	O	NUML	NUMLK1 + : When the "Num Lock" key is pressed, this signal becomes "1", and is output to the keyboard controller. The content of bit 4 of the register is output. When reset operation is executed, this is "0",
48	O	DATFL	KBRXD1 + : This line is used to transfer data from the keyboard controller.
49	I	CLK	CPCLK1 + : CPU clock
50	I	TEST1	SH03A - : This pin is used to test the G.A. (Not used)
51	O	DCHE	FLTSL1 + : This signal is used for LCD selection, and when the signal is "1", the LCD is selected . When an external CRT is selected, the content of bit 6 of the register is inverted to be output. When this is "1", reset operation is executed.
52	O	FONT	CHFOT0 + : When double font is used, the signal is "1", and when single font is used, this signal is "0". Content of bit 5 of the register is inverted to be output. When reset operation is executed, this signal is "1".

Pin	I/O	SYMBOL	Signal name and Description
55	I	CLR1	RESET1 + : When this signal is "1", the system is reset. This is an input signal from the SI.
56	I	TEST0	SH03B - : This is the signal that puts the G.A into the Test mode. (Not used)
57	O	IRQ7	IRQ71 + : This is an interrupt signal of level 7, and is output to the 82C59.
58 ⌇ 66	I/O	D0~D7	SD01~SD71 + : These are the bidirectional data lines, and are used for data tranfer with the CPU.
67	I	ROWCOL	RCCH0 + : This is a signal used to convert the address (ROW/COLUMN) in outputting to the lines MADR 0~8.
68	O	MIN1	MIN1 + : This signal is not used in this system.
69 77	O	MAD0 ⌇ MAD8	MADR0~MADR8 + : This signal is used to output the address of the system RAM. When RCCH0 is "1", ROW : A0~A7, A16 are output. When it is "0", Column : A8~A15, A17 are output.
80 81	I	AUTFD, ISLIN	RATFD0, RSLIN0 These are wrap-around signals of AUTFD1 and SLIN1 signal which are issued by this GA.
82 ⌇ 86	I	ERROR, SELECT, PE, ACK, BSY	IERR0, ISLCT1, IPE1, IACK0, IBSY1, - : They are all status data input from the printer.

Pin	I/O	SYMBOL	Signal name and Description
87 ~ 91	O	STB, AUTF, PINT, SLIN	STROB1, AUTFD1, PINT1, SLIN1 + : These are output control signals to the printer. These signals are inverted when they are output to the printer.
92 ~ 99	I/O	PD0~7	OPD00~70 - : These are bidirectional data lines, and by these lines ; - The data to be output to the printer is inverted. - This can be used as the input mode. In this case, the input data is dealt with the same polarity as output mode.
100	O	PRTDIR	PRTDI0 + : When this signal is "1", eight bits of OPD*0 lines are in the output mode. When "0", the lines are in the input mode.

Notes: Pins 03, 28, 53, 78 are used for Vcc, and 04, 15, 29, 40, 54, 65, 79, 90 are used for GND.

B.4 **FUNCTION OF EACH COMPONENT**

B.4.1 Printer interface

B.4.1.1 Resisters and bits allocation

The printer interface uses I/O address between 378H and 37FH, and the bit allocation of the three resisters : Data resister, Status Port, and the control resister, is explained in the following tables.

	Port Address	DATA							
		7	6	5	4	3	2	1	0
Data Register	Write 378H	7	6	5	4	3	2	1	0
	Read 378H	7	6	5	4	3	2	1	0
Status Port	Read 379H	- BUSY	- ACK	PE	SEL-ECT	- ERR	-	-	-
Control Register	Write37AH	-	-	-	IRQEN	SLTIN	PINT	AUT-FD	STRB
	Read 37AH				IRQEN	SLTIN	PINT	AUT-FD	STRB
	Write 37FH								Bidir-EN

Table B - 2 Bit allocation of three Registers

Port Name	Port Address	I/O Address bit									
		A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Data Register	Write 378H	1	1	0	1	1	1	1	x	0	0
	Read 378H	1	1	0	1	1	1	1	x	0	0
Status Port	Read 379H	1	1	0	1	1	1	1	x	0	1
Control Register	Write37AH	1	1	0	1	1	1	1	x	1	0
	Read 37AH	1	1	0	1	1	1	1	x	1	0
	Write 37FH	1	1	0	1	1	1	1	x	1	1

a) Block diagram of the printer interface

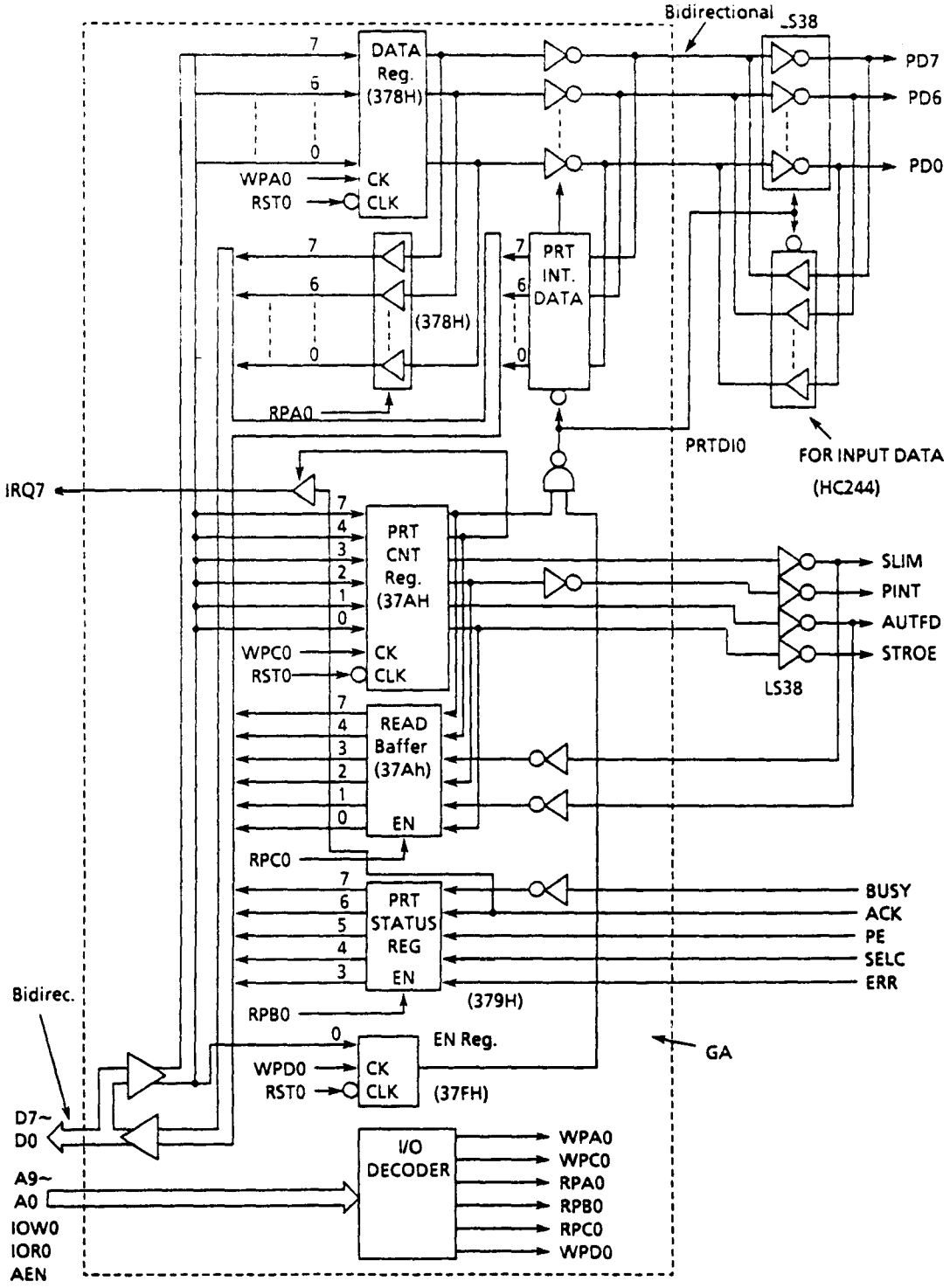


FIGURE B-2 Block Diagram

b) Data register

By RESET signal, this register is cleared.
At the transition from low to high level of the WPA0 signal, or of $\overline{IOWR}$ signal, 8-bit data is set on the data bus.

The set data is inverted and output to the data line of the printer port (in the case of the input mode, refer to B.3).

$$\overline{WPA0} = (378H) \cdot \overline{IOWR} \cdot \overline{AEN}$$

By the RPA0 signal, the above mentioned 8-bit data is output to the data bus.

$$\overline{RPA0} = (378H) \cdot \overline{IORD} \cdot \overline{AEN}$$

c) Printer controller register

By RESET signal, this register is cleared.
At the transition from low to high level of the WPC0 signal, or of $\overline{IOWR}$ signal, data of the lower 6-bit (5-0) on the data bus is set.

$$\overline{WPC0} = (37AH) \cdot \overline{IOWR} \cdot \overline{AEN}$$

By the RPC0 signal, the above mentioned 6-bit data on the input data as the response signal are output to the data bus.

$$\overline{RPC0} = (37AH) \cdot \overline{IORD} \cdot \overline{AEN}$$

d) Printer status register

By RPB0 signal, the input "Printer Status Data" is output to the 5-bit (7-3) data bus.

$$\overline{RPB0} = (379H) \cdot \overline{IORD} \cdot \overline{AEN}$$

e) Printer mode register

At the transition of high to low level of the RPD0 signal, the data bit 0 is input to the register.

$$\overline{RPD0} = (37FH) \cdot \overline{IOWR} \cdot \overline{AEN}$$

The data in the lines A9-A0 are decoded (except A2).

B.4.1.2 Bidirection of the printer data line

a) When outputting, the data contained in the Data Register is inverted to be output -- (when PRTD10 is at high level).

b) Input mode

When bit 7 of the 37AH (Printer control) register is "1", the data can be input -- (PRTD10 is low level).
This mode is effective only when bit "0" of the 37FH of the port is "1", and if "0", it is completely ignored.

B.4.2 I/O address decoder

I/O address decoder decodes the addresses A19-A0, and outputs the following signals;

DIOSL0 (Display I/O Register Select)
DMESL (Display Memory Select)
TIMSL (Real Timer Slect)
232CSL (RS232C Resister Select)
MDMSL (Modem Resister Select)

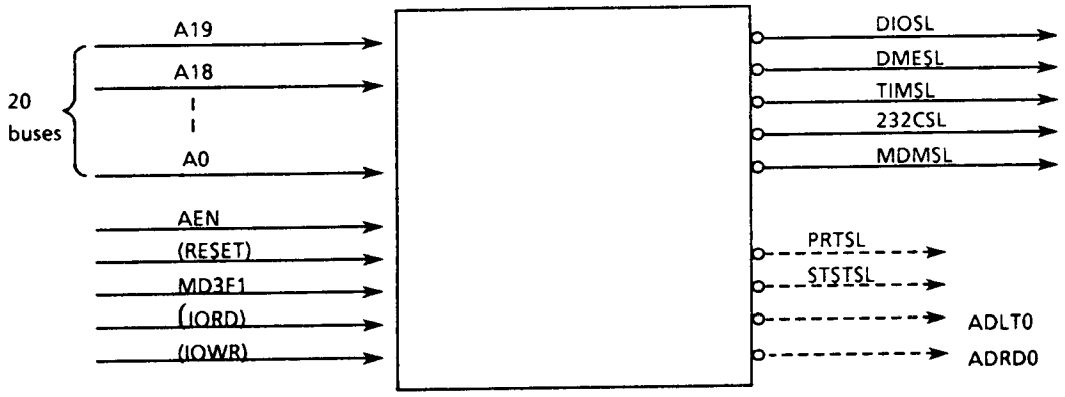


FIGURE B-3 I/O Address Decoder Block Diagram

a) DIOSL0 (Sisplay I/O register select)

$\overline{DIOSL0}$ = (3D0H-3DFH)·$\overline{AEN}$ (A9-A0 are decoded)

b) DMESL (Display memory select)

$\overline{DMESL0}$ = (B8000H-BFFFFH) (A19-A15 are decoded)

c) TIMSL (Real Time Select)

$\overline{TIMSL0}$ = (2C0H-2DFH)·$\overline{AEN}$ (A9-A0 are decoded)

d) 232SL0 (RS232C Register Select)

$\overline{232SL0}$ = (2F8H-2FFH)·$\overline{AEN}$·MD3F1+(3F8H-3FFH)·$\overline{AEN}$·$\overline{MD3F1}$
(A9-A0 are decoded)

e) MDMSL0 (Mode Register Select)

$\overline{MDMSL0}$ = (2F8H-2FFH) $\overline{AEN}$·$\overline{MD3F1}$+(3F8H-3FFH)·$\overline{AEN}$·MD3F1
(A9-A0 are decoded)

f) PRTSL0 (Printer Port Select)

$\overline{PRTSL0}$ = (378H-37FH)·$\overline{AEN}$ (A9-A0 are decoded)

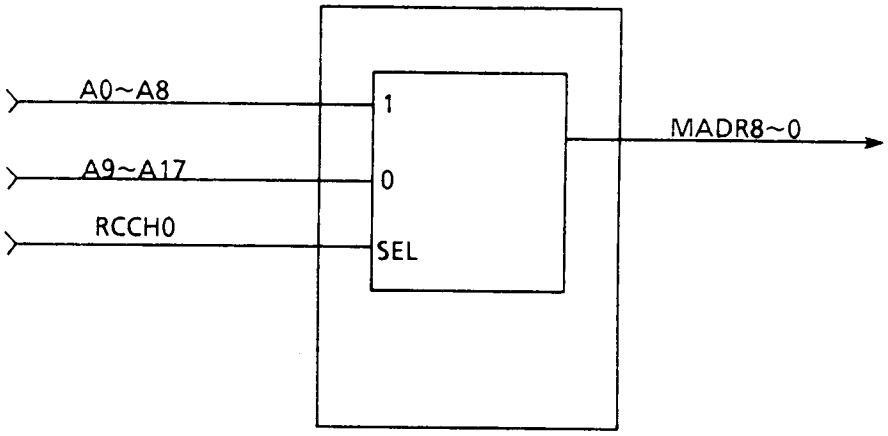
g) CTREG (Control Register Select)

$\overline{STSTSL0}$ = (2C0H-2DFH)·$\overline{AEN}$ (A9-A0 are decoded)

Note: f) and g) are used inside the G.A..

B.4.3 System RAM controller

This circuit is to change the address output to MADR8-0 by RCCH0 signal from the I/O driver GA.



$$\begin{cases} MADR\ (8\text{-}0) = \overline{RCCH0} \cdot A(8\text{-}0) \\ MADR\ (8\text{-}0) = RCCHO \cdot A(17\text{-}9) \end{cases}$$

FIGURE B-4 RAM Controller

B.4.4 DOS ROM controller

This circuit is provided to control address and selects signal of the DOS-ROM.

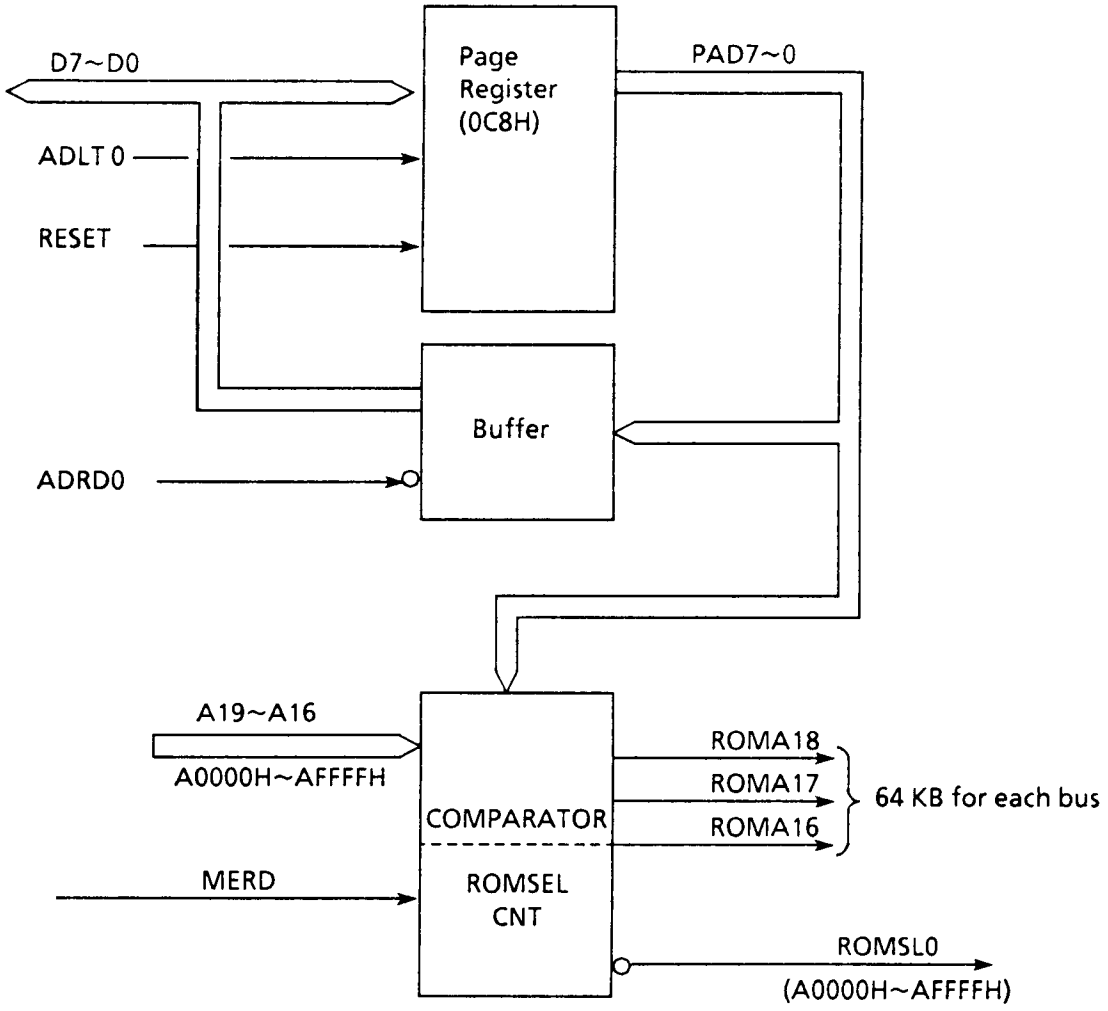


FIGURE B-5 DOS ROM Controller

LATCH DATA BIT (PAD7~0)							
7	6	5	4	3	2	1	0
ENABLE	-	-	-	-	OUT ROMA18	OUT ROMA17	OUT ROMA16

a) Page register

This register is reset by RESET signal.
The data buses D7-D0 are latched as PAD7-PAD0 by ADLT0 signal.

$$\overline{ADLT0} = (0C8H) \cdot \overline{IOWR} \cdot \overline{AEN}$$

By ADRD0 signal, PAD7-PAD0 are output on the buses D7-D0.

$$\overline{ADRD0} = (0C8H) \cdot \overline{IORD} \cdot \overline{AEN}$$

b) Comparator/ROM Select Control

When the address buses A19-A16 correspond to the address A0000H-AFFFFH and PAD is "1", ROMSL0 signal is output if MERD signal is then input.
Each of PAD2-PAD0 is output to the DOS ROM address lines RAD18-RAD16.

APPENDIX C

I/O DRIVER G.A.

C.1 GENERAL

I/O driver gate array indicates various gates which cannot be included in the I/O controller, and is composed of 48 pins.

Out of these 48 pins, 42 pins are for I/O signals, and 2 pins are for Vcc, and finally the rest 4 pins are used for GND.

Functions of the I/O drivers are as follows;

(1) FDD A/B Switching
(2) Reset Driver
(3) Clock Generation
(4) FDD Input Gate
(5) Speaker Driver Gate
(6) LCD Power Supply Controller
(7) External FDD Counter
(8) RAS/CAS Timing Generator
(9) COM1/COM2 Switching

The detailed explanations about each device is given in C.4.

C.2 **BLOCK DIAGRAM**

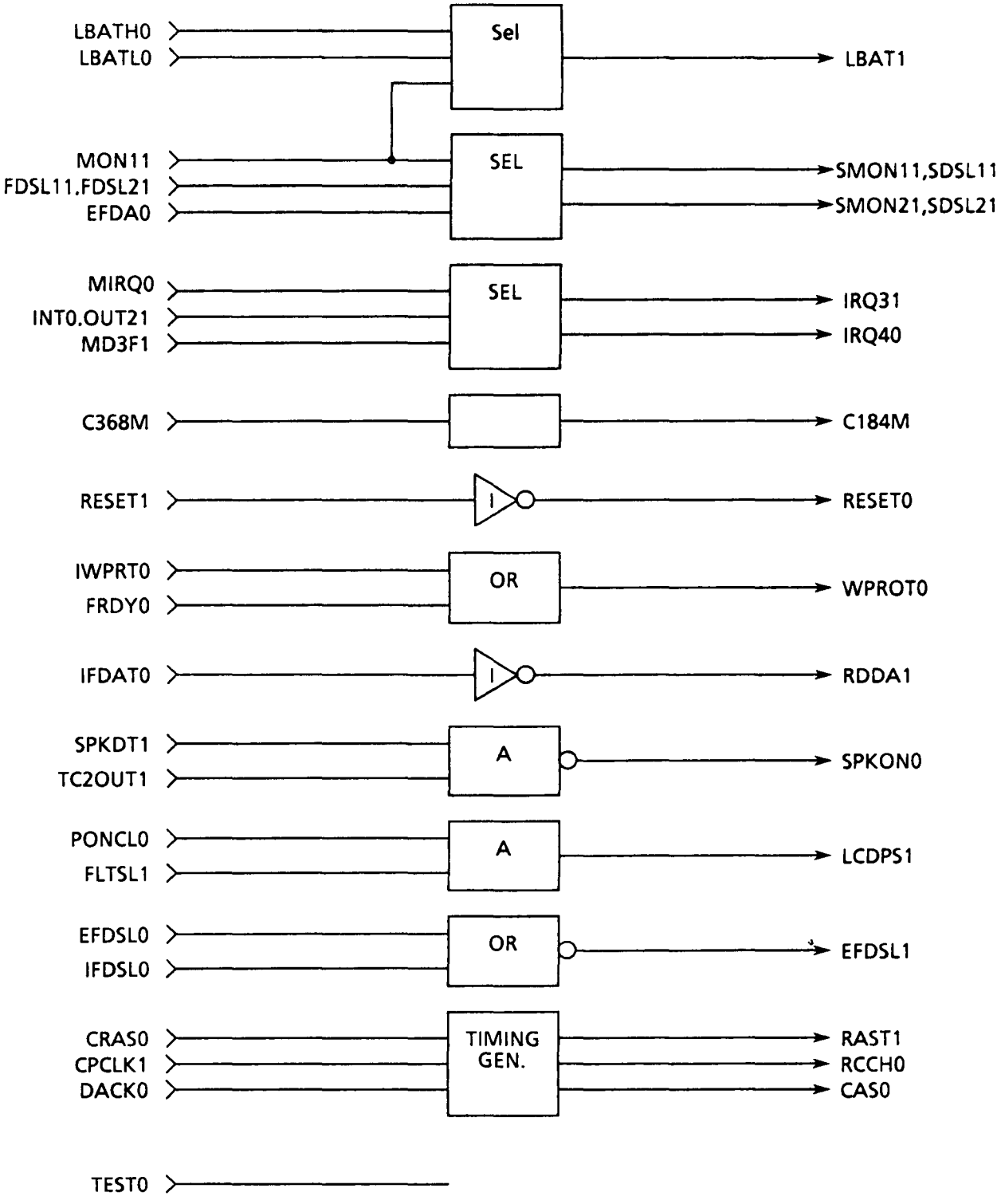


FIGURE C-1 Block Diagram

C.3 **PIN DESCRIPTION**

TABLE C-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
01 03	O	MON1 MON2	SMON11, SMON21 + : This is FDD motor ON signal, and when this signal is "1"; if SDSL11 is "1", SMON11 is also "1"., and if SDSL21 is "1", SMON21 is also "1".
02 04	O	SEL1 SEL2	SDSL11, SDSL21 + : FDD select output signal When this signal is "1", FDD is selected. The output contents vary depending on the polarity of EFDA0. Normally when FDSL11 is selected, SDSL11 is output, and when FDSL21is selected, SDSL21 is output.
05	O	IRQ40	IRQ40 - : This is an interrupt signal (level 4) to the 8259 (inside the SI).
07	I	WPROT	IWPRT0 - : This is a write protect input signal from the FDD.
08	I	FDAT	IFDAT0 - : This is the signal to indicate the read data from the FDD.
09	I	FRDY	FRDY0 - : This is READY signal from the FDD.
10	O	WPRT	WPROT0 - : This is the write protect signal from the FDC, and is activated with FRDY0 signal.
11	O	RDAT	RDDA1 + : This is the inverted IFDAT0 output signal, and is input to the 9420C.
12	I	FDSL1	EFDSL0 - : When the system is connected to the external FDD, this signal is "1".

Pin	I/O	SYMBOL	Signal name and Description
13	O	FDSL0	EFDSL1 + : When internal and external FDDs are connected at the same time, this signal is activated at "1".
14	I	PONCLR	PCLR0 - : This is the reset signal.
15	I	LSDSL	FLTSL1 + : This is the signal used to designate the LCD as the display for the system. This signal is activated when it is "1".
16	O	LCDPS1	LCDPS1 + : This is the signal used to designate the LCD and when it is active, it is "1". This is input to the + 5V P.S circuit of the LCD.
17	I	SYSCLK	CPCLK1 + : This is the CPU clock signal.
20	I	RAS1	CRAS0 - : This is the RAS timing signal for the system RAM.
21	I	REF	DACK0 - : This signal is activated when it is "0", during the refresh cycle.
22	O	RAST1	RAST1 + : This is RAS timing output signal, and is an inverted CRAS0 signal.
23	O	RCT	RCCH0 + : This is the timing signal for switching ROW and COLUMN.
24	O	CAS	CAS0 - : This is CAS timing signal for the system RAM.
25	O	CLRO	RESET0 + : This is the system reset signal, and is active when it is "0". This is the inverted RESET1 signal.

Pin	I/O	SYMBOL	Signal name and Description
26	I	CKIN	C368M1 + : This is 3,6864Mz clock signal input.
27	O	CKOUT	C184M1 + : This is an output clock signal which is half the frequency of the C368M1.
28	O	SPKD	SPKON0 - : This is the speaker drive signal, and is also a returned input signal to the SI.
29	I	SPKDR	SPKDT1 + : This is the speaker data signal from the SI.
30	I	TC20	TC2OUT1 + : This is a timer output signal for the speaker from the 82C53 inside the SI.
32	I	CLRI	RESET1 + : This is the system reset signal, and is activated when it is "1".
33	I	MON	MON11 + : Input signal from the SI When the motor of the FDD is ON, this signal is "1".
34 35	I	FSL1, FSL2	FDSL11, FDSL21 + : Input signals from the SI. These are FDD select signals, and when the selection is executed, each signal is set to "1".
36	I	EFDA	EFDA0 - : When this signal is "1', the external FDD is set to "B". When this is "0", the external FDD is set to "A".
37	I	MD3F	MD3F1 + : This is a signal to change IRQ31 and IRQ41.
38 39	I	OUT21, INT0	OUT21, INT0 + : This are the signal output from the SIO, and are used to generate IRQ signal.

Pin	I/O	SYMBOL	Signal name and Descritpion
40	I	IRQ30	IRQ30 - : This is the inverted IRQ signal input from the modem interface.
41	O	IRQ31	IRQ31 + : This is an interrupt signal (level 3) to the 82C59 (inside the SI).
44	I	TEST0	TEST0 - : This signal becomes "0", when Test mode.
45	I	IFDSL0	FDSL0 - : When the internal FDD is connected. this signal is "0".
46	I	LBATH	LBATH0 - : This signal is used to detect low battery.
47	I	LBATL0	LBATL0 - : This signal is used to detect low battery.
48	O	LBAT	LBAT1 + : When the FDD motor is off, the inverted LBATH0 is output, and when on, The inverted LBATL0 is output. This is used as the indicater lamp for low battery.

Notes: Pins 19,43 are used for Vcc, and 06, 18, 31, 42 are used for GND.

C.4 **FUNCTION OF EACH COMPONENT**

C.4.1 FDD drive A/B switching

This is the circuit that changes the mode between FDD-A and FDD-B.

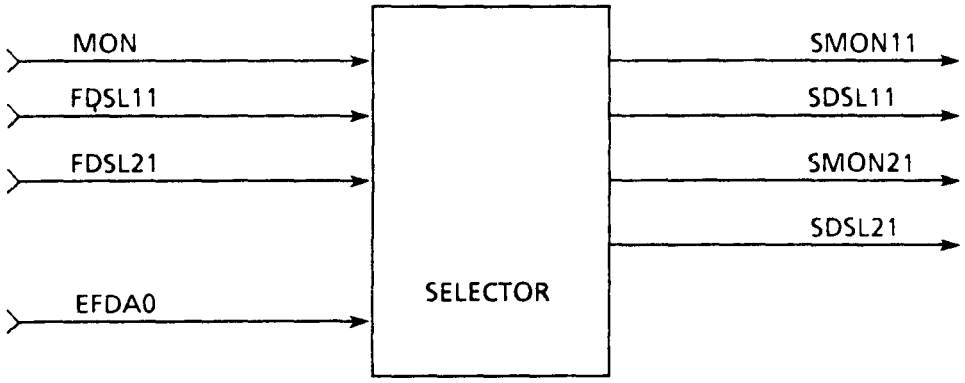


FIGURE C-2 FDD Switching

$$SMON11 = (MON \cdot FDSL11 \cdot EFDA0) + (MON \cdot \overline{FDSL21} \cdot \overline{EFDA0})$$
$$SDSL11 = (FDSL11\ EFDA0) + (FDSL21 \cdot \overline{EFDA0})$$
$$SMON21 = (MON \cdot FDSL21 \cdot EFDA0) + (MON \cdot \overline{FDSL11} \cdot \overline{EFDA0})$$
$$SDSL21 = (FDSL11 \cdot EFDA0) + (FDSL11 \cdot \overline{EFDA0})$$

C.4.2 Reset driver

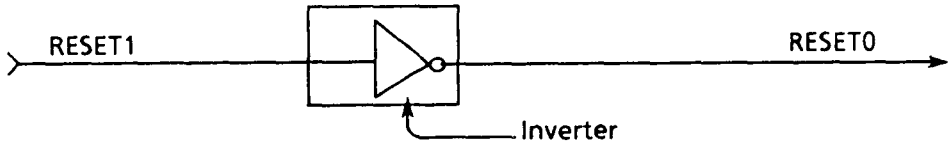


FIGURE C-3 Reset Driver

C.4.3 Clock generator

This driver outputs half of the frequency (3.68 MHz) that it acquires.

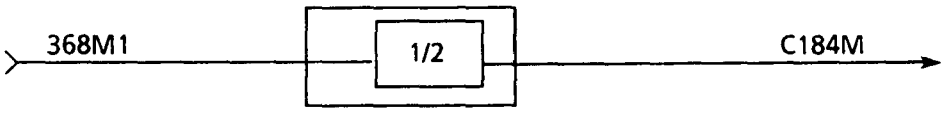
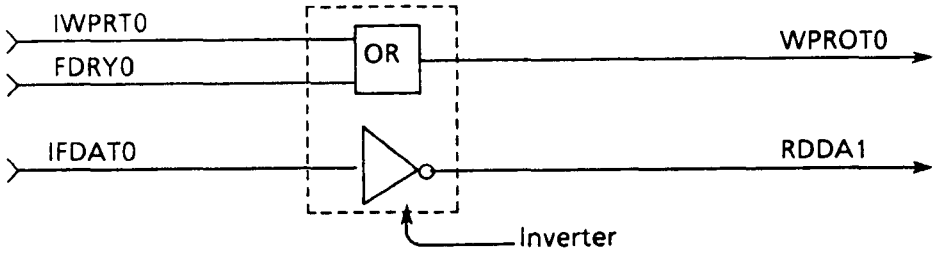


FIGURE C-4 Clock Generator

C.4.4 FDD input gate

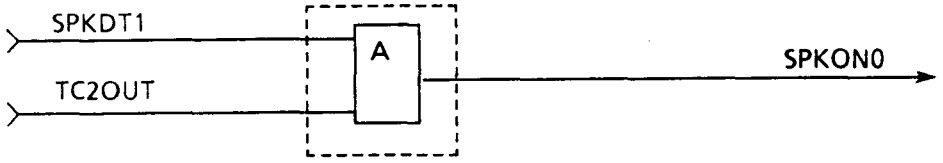
This gate acquires the following signals through the FDD input interface.



$$WPROT0 = \overline{IWPRT0}+FRDY0$$
$$RDDS1 = \overline{IFDAT0}$$

FIGURE C-5 FDD Input Gate

C.4.5 Speaker driver gate

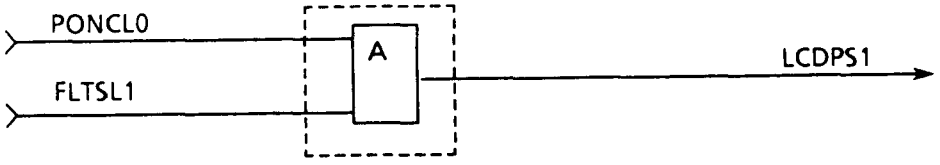


$$\overline{SPKON0} = SPKDT1 \cdot TC2OUT1$$

FIGURE C-6 Speaker Driver Gate

C.4.6 LCD PS controller

This is the circuit that controls the output 5Vdc for the LCD interface ICs.

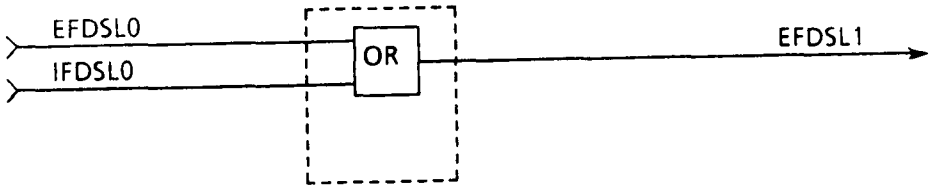


$$LCDPS1 = FTOFF0 \cdot PONCL0 \cdot FLTSL1$$

FIGURE C-7 LCP PS Controller

C.4.7 External FDD counter (option)

This is the circuit to output the signal that indicates the number of external FDDs. This circuit is provided optionally.

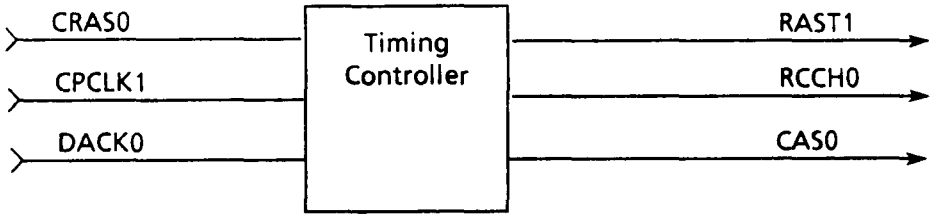


$$EFDSL1 = \overline{EFDSL0} \cdot \overline{IFDSL0}$$

FIGURE C-8 External FDD Counter

C.4.8 RAS/CAS timing controller

This is circuit that controls the timing of the RAS and CAS signals for the system RAM.

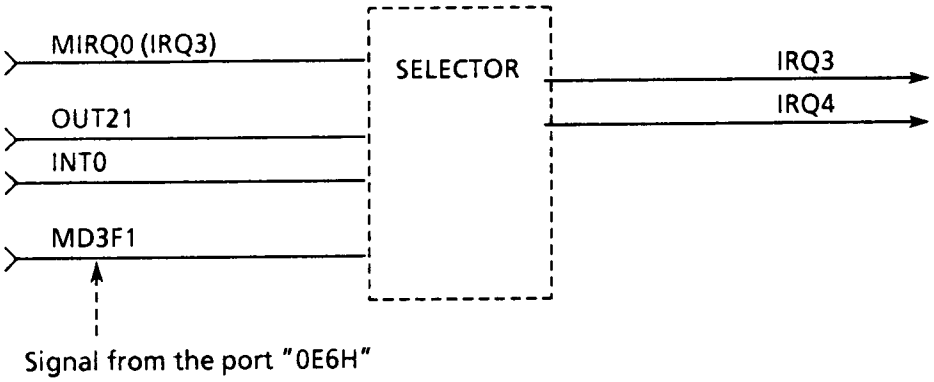


$$\overline{RAST1} = \overline{CRAS0}$$
$$\overline{RCCH0} = \overline{RAST1} \cdot CPCLK1 \ (\ )$$
$$\overline{CAS0} = \overline{RCCH0} \cdot CPCLK1 \ (\ )$$

FIGURE C-9 RAS/CAS Timing Controller

C.4.9 COM1/COM2 changing

This circuit is used to change the signals from RS232C connector and from Modem into the signals IRQ3 and IRQ4. This operation is executed with the MD3F1 signal.



When MD3F1 is at low level ("0"), then,

$\overline{IRQ4} = \overline{(OUT21+INT0)}$
$IRQ3 = \overline{MIRQ0}$

When MD3F1 is at high level ("1"), then,

$\overline{IRQ4} = \overline{\overline{MIRQ0}}$
$IRQ3 = (OUT21=INT0)$

FIGURE C-10 COM1/COM2 Changing

APPENDIX D

DISPLAY CONTROLLER G.A.

D.1 GENERAL

The Diaply Controller Gate Array is a CMOS type chip with 5,000-gate, 100-pin flat package, and it contains the color graphics adapter which can control both the external CRT display and the internal LCD display.

This gate array contains the following functions.

- LCD/CRT control function
- Attribute process function
- Interface with the CPU (I/O bus)
- Interface with the V-RAM and with the CG-ROM

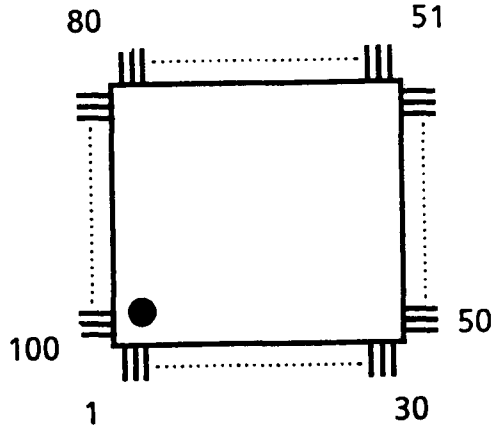


FIGURE D-1 Display Conroller Gate Array

The detailed description of each pin and signal is also given here.

The whole system including this gate array is called the Display Controller Subsystem, and it can control the following three types of displays.

A) 640x200 dot LCD (Liquid Cristal Display)
B) 640x200 dot CRT (Cathode Ray Tube) Display

Note that the external CRT display unit and the internal LCD can not be used at the same time, and its selection is performed by the keyboard operation.

Fn + Home ..... LCD is selected.
Fn + End ..... External CRT display is selected.

D.2 DISPLAY CONTROLLER SUBSYSTEM (DCS)

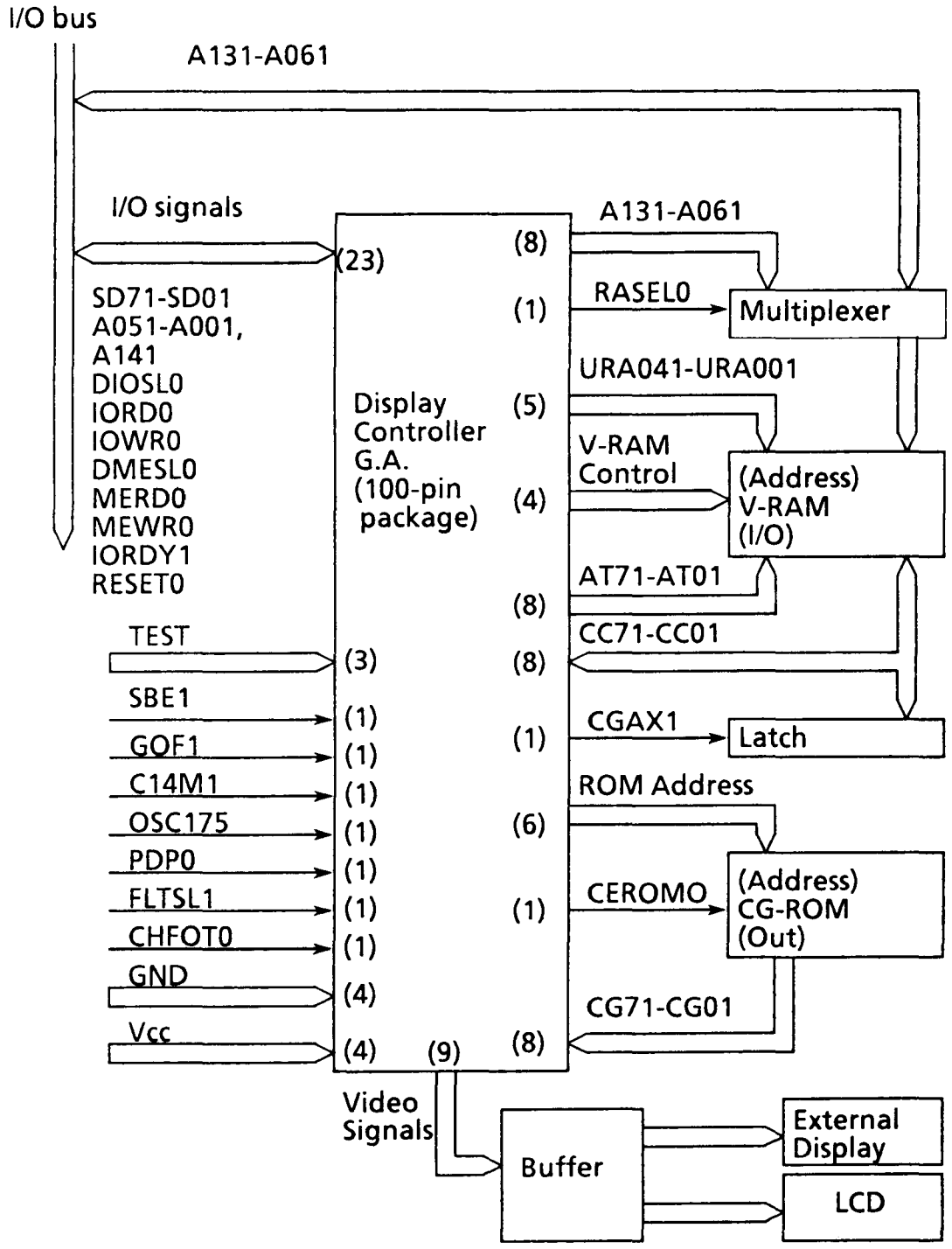


FIGURE D-2 Display Controller Subsystem

D.3 **DISPLAY CONTROLLER**

Table D-1 Pin Description

Pin	I/O	SYMBOL	Signal name and Description
1	I	CG03	CG31 Character generator output signal bit 3.
2	I	CG04	CG41 Character generator output signal bit 4.
3	I	Vcc	+ 5V
4	I	CG05	CG51 Character generator output signal bit 5.
5	I	CG06	CG61 Character generator output signal bit 6.
6	I	CG07	CG71Character generator output signal bit 7.
7	I	CRM0	CEROM0 Chip enable signal for CG-ROM (Character generater - ROM).
8	I	CG02	CG21 Character generator output signal bit 2.
9	I	CG01	CG11 Character generator output signal bit 1.
10	I	CG00	CG01 Character generator output signal bit 0.
11	O	RS01	RSA01 Raster scan address bit 0.
12	O	RS11	RSA11 Raster scan address bit 1.
13	O	RS21	RSA21 Raster scan address bit 2.
14	O	RS30	RSA31 Raster scan address bit 3. Not used.
15		GND	Ground
16	I	SBE1	Reserved for LCD. (Ground)
17	O	FNS0	INTEN1 Intensified font select signal.(single dot /double dots character)
18	O	FNP0	CGM01 8x8 / 8x16 font selection. Not used.

Pin	I/O	SYMBOL	Signal name and Description
19	O	CGA1	CGAX1 CG address latch.
20	O	RSL0	RASEL0 Refresh address selection.
21	O	RA12	RA121 Refresh address bit 12.
22	O	RA11	RA111 Refresh address bit 11.
23	O	RA10	RA101 Refresh address bit 10.
24	O	RA09	RA091 Refresh address bit 09.
25	O	RA08	RA081 Refresh address bit 08.
26	O	RA07	RA071 Refresh address bit 07.
27	O	RA06	RA061 Refresh address bit 06.
28	I	VCC	VCC + 5V
29	O	RA05	RA051 Refresh address bit 05.
30	I	OC14	C14M1 14. 31818 MHz for the video signal.
31	I	OISL0	DIOSL0 Display I/O selected. Access signal to the I/O port of the GA.
32	I	MSL0	DMESL0 V-RAM access signal for CPU or DMAC.
33	I/O	BD07	SD71 Data bus bit 7.
34	I/O	BD06	SD61 Data bus bit 6.
35	I/O	BD05	SD51 Data bus bit 5.
36	I/O	BD04	SD41 Data bus bit 4.

Pin	I/O	SYMBOL	Signal name and Description
37	I/O	BD03	SD31 Data bus bit 3.
38	I/O	BD02	SD21 Data bus bit 2.
39	I/O	BD01	SD11 Data bus bit 1.
40		GND	Ground.
41	I/O	BD00	SD01 Data bus signal bit 0.
42	O	RDY	IORDY1 I/O ready signal.
43	I	RST0	RESET0 GA reset signal.
44	I	UA05	A051 CPU address bit 5.
45	I	UA04	A041 CPU address bit 4.
46	I	UA03	A031 CPU address bit 3.
47	I	UA02	A021 CPU address bit 2.
48	I	UA01	A011 CPU address bit 1.
49	I	UA14	A141 CPU address bit 14.
50	I	MEW0	MWR0 Memory write signal.(for V-RAM write)
51	I	MER0	MRD0 Memory read signal. (for V-RAM read)
52	I	IOR0	IORD10 I/O read signal. It read out I/O port data to the data bus BD00-BD07.
53	I	VCC	+5V
54	I	IOW0	IOWR10 I/O write signal. It write data on the data bus to the I/O port.

Pin	I/O	SYMBOL	Signal name and Description
55	I	UA00	A001 CPU address bit 0.
56	I	PDP0	PDP0 Plasma display panel select. Not used.
57	I	GOF1	GOF1 GA off. If this signal is high, the GA becomes to be disable.
58		TEH1	Ground.
59		TFU1	Ground.
60		TCN1	Ground.
61	O	N.C.	BFR0 Video signal.
62	O	FRHV	FRHV1 Video signal. Vertical sync. signal for composite CRT display.
63	O	FVS1	FPVS1 Video signal. Vertical sync. signal for LCD/RGB CRT display.
64	O	SXV1	SXVD1 Video signal.
65	O	GND	Ground.
66	O	LHS1	LPHS1 Video signal. Horizontal sync. signal for LCD/RGB CRT display.
67	O	DOR1	D1R1 Video signal. Red signal for RGB CRT display.
68	O	DIG1	D2G1 Video signal. Green signal for RGB CRT display.
69	O	D2B1	D3B1 Video signal. Blue signal for cRGB CRT display.
70	O	D3I1	D4I1 Video signal. Intensity signal for all.
71	I	CHFOT	CHFONT0 Change character font signal
72	I	FDIS	FLTDSL1 Flat display selected. It changes internal / external display.

Pin	I/O	SYMBOL	Signal name and Description
73	I	OC18	OSC175 Clock 17.5 MHz
74	O	CEH0	Chip enable high. chip selected signal for the V-RAM. N.C.
75	O	WRC0	WRCC0 Write character code. it is used with chip enable signal to write them V-RAM. (even address)
76	O	WRA0	WRAT0 Write attribute data. It is used with chip enable signal to write them V-RAM. (odd address)
77	O	CEL0	CEL0 Chip enable low. It is V-RAM selection signal.
78		VCC	+ 5V
79	O	RA00	URA001 CPU / Refresh address bit 0.
80	O	RA01	URA011 CPU / Refresh address bit 1.
81	O	RA02	URA021 CPU / Refresh address bit 2.
82	O	RA03	URA031 CPU / Refresh address bit 3.
83	O	RA04	URA041 CPU / Refresh address bit 4.
84	I/O	AT00	AT01 Attribute data bit 0.
85	I/O	AT01	AT11 Attribute data bit 1.
86	I/O	AT02	AT21 Attribute data bit 2.
87	I/O	AT03	AT31 Attribute data bit 3.
88	I/O	AT04	AT41 Attribute data bit 4.

Pin	I/O	SYMBOL	Signal name and Description
89	I/O	AT05	AT51 Attribute data bit 5.
90	I/O	GND	Ground
91	I/O	AT06	AT61 Attribute data bit 6.
92	I/O	AT07	AT71 Attribute data bit 7.
93	I/O	CC00	CC01 Character code data bit 0.
94	I/O	CC01	CC11C Character code data bit 1.
95	I/O	CC02	CC21 Character code data bit 2.
96	I/O	CC03	CC31 Character code data bit 3.
97	I/O	CC04	CC41 Character code data bit 4.
98	I/O	CC05	CC51 Character code data bit 5.
99	I/O	CC06	CC61 Character code data bit 6.
100	I/O	CC07	CC71 Character code data bit 7.

D.4 FUNCTIONS OF THE DCS

Display controller subsystem (DCS) is composed of the following components.

TABLE D-2 Components of the Display Controller

Display ControllerG A		CMOS 5 KG 100-pin flat Package
Video- RAM		16 K bytes 64 K RAM x 2
CG-ROM		8 K bytes 64 K ROMx1
OSC	CPU-CLK	14.31818 MHz
Others	Multiplexer Latch Display Buffer	74 HC 157x2 74 HC 273x1

The following table shows the operation modes of the DCS of the internal LCD and external CRT display.

TABLE D-3 LCD/CRT Operation Mode

Operation Mode	LCD/CRT Resolution (Pixels)	LCD/CRT Character Box (Pixels)
40 x 25 TEXT	320 x 200	8 x 8
80 x 25 TEXT	640 x 200	8 x 8
320 x 200 GRAPH	320 x 200	8 x 8
640 x 200 GRAPH	640 x 200	8 x 8

D.5 VARIOUS SIGNALS

The DCS contains the following different groups of signals;

- I/O Interface signals (23 lines)
- V-RAM signals (34 lines)
- Character Generater (CG) signals (16 lines)
- Video signals (9 lines)
- Display mode selects signals (3 lines)
- Clock input (2 lines)
- Other signals (5 lines)

D.5.1 I/O Interface signals

DIOSL0 : Display I/O Select (Input)

When this signal is "0", the CPU is enabled to access the I/O port inside the gate array.
If this signal is "0", either IORD0 or IOWR0 becomes "1", and the CPU is enabled to read or write the I/O port inside the gate array.

IORD0 : I/O Read (Input)

When this signal is low and DIOSL0 is also low, the data of the I/O port is transferred to the CPU through the address BD00-BD07.

IOWR0 : I/O Write (Input)

When this signal is low and DIOSL0 is also low, the data from the CPU is written to the selected I/O port inside the gate array through the address BD00-BD07.

DMESL0 : Display Memory Selected (Input)

When this signal is low, the CPU or DMAC is enabled to access the video RAM. In the same condition, if either MERD0 or MEWR0 is low, read and write operation is enabled.

MERD0 : I/O Read (Input)

When this signal is low and DMESL0 is low, reading operation to V-RAM is executed, and the read data becomes effective in the address BD00-BD07.

MEWR0 : Memory Write (Input)

When this signal is low and DMESL0 is also low, the data on the address BD00-BD07 are written to the V-RAM.

UA00-UA05, UA14 (A001-A051,A141) : CPU Address (Input)

These are address data line from the CPU or DMAC, and when it is at high level, it shows logic true.
UA00-UA03 (A0-03) are used for selecting one of the I/O ports included in the gate array during read or write operation to the I/O port of the gate array. When memory read or write operation to the V-RAM is performed, memory location is selected by the address lines UA00-UA05 (A0-A5) and also by those of A06-A13 which are supplied directly to the V-RAM without passing the gate array.

BD00-BD07 (SD01-SD71) : 8-bit Data Bus (Input/Output)

These are 8-bit data lines and when those signals are at high level, it shows logic true. These lines are used for input or output of the data during read or write operation to the I/O port inside the gate array or to the V-RAM.

IORDY1 : I/O Ready (Output)

When access requirement to the V-RAM is generated from the CPU or DMAC, if DMESL0 becomes low, the gate array keeps this signal at low level, and puts the CPU and DMAC in the waiting position until the access is enabled.

RST0 (RESET0) : (Reset)

When this signal is at low, the gate array is reset.

D.5.2 V-RAM signals (34 lines)

UR00-UR04 : CPU/Refresh Address 00-04 (Input)

RA05-RA12 : Refresh Address 05-12 (Input)

These are address lines for the V-RAM.
The 5 address signals UR00-UR04 are directly connected to the address input pin of the V-RAM, while the upper 8 signals on the address lines RA05-RA12 are multiplexed with the address signals A061-A131 of the I/O bus and are connected to the address input pin of the V-RAM.
There are two modes in the accessing the V-RAM; one is the mode in which memory read or write operation from the CPU is executed through the I/O bus, and the other is the one in which the direct display fresh (read only) is performed from the gate array.

CELO, CEHO : Chip Enable Low/High (Output)

These are the chip enable signals for the V-RAM, and at low level the RAM is enabled. Only CEL0 is used in the system. 2 SRAMs (TC5565), configuration of which is 8k x 8, are used as the RAM.
The RAM connected to the data buses CC00-CC07 are assigned to the even byte, and the one connected to the data buses AT00-AT07 are assigned to the odd byte. 2-byte read operation of display refresh is executed to the V-RAM.
When he CPU or the DMAC reads the V-RAM, two bytes of the RAM is enabled, but only one of those two bytes is output to the I/O address BD00-BD07.
This is controlled by UA00 input signal.
When UA00 is at low level, one byte of the CC00-CC07 is output to the addresses BD00-BD07, and when UA00 is at high level, one byte of the AT00-AT07 is output to the affresses BD00-BD07.
When the CPU or the DMAC writes to the V-RAM, two bytes of the RAM is enabled, but only one of those two RAMs executes the write operation.

WRC0 : Write Character Code (Output)

WRA0 : Write Attribute Data (Output)

These are the write enable signals to the V-RAM.
When the chip enable signal is low and this signal is also low, write operation to the RAM is executed.
Write operation to the RAM is executed only when the request signal from the CPU or the DMAC is generated (when both MSL0 and MEW0 are low). In this case, either WRC0 or WRA0 becomes low depending on the status of UA00. When UA00 is low, WRC0 becomes also low, and write data appears on the addresses CC00-CC07 through the I/O buses BD00-BD07.
When UA00 is high, WRA becomes low, and the write data appears on the addresses AT00-AT07 through BD00-BD07.

Address Assignment of the V-RAM

TABLE D-4 V-RAM Address Assignment

V-RAM Pin Name	V-RAM Signal Name	CPU Address	Memory Refresh TEXT Mode	Memory Refresh GRAPH Mode
CE	CEL0	A14	MA13	RSA1
AD12	RA121	A13	MA12	RSA0
AD11	RA111	A12	MA11	MA11
AD10	RA101	A11	MA10	MA10
AD09	RA091	A10	MA09	MA09
AD08	RA081	A09	MA08	MA08
AD07	RA071	A08	MA07	MA07
AD06	RA061	A07	MA06	MA06
AD05	RA051	A06	MA05	MA05
AD04	RA041	A05	MA04	MA04
AD03	RA031	A04	MA03	MA03
AD02	RA021	A03	MA02	MA02
AD01	RA011	A02	MA01	MA01
AD00	RA001	A01	MA00	MA00
PG	WRCC0 / WRAT0	A00	—	—

Note:

* A00-A14 are address signals from the I/O bus of the CPU.

* MA00-MA13 are refresh memory address. They are generated by the 6845 circuit or its equivalent inside the gate array.

* RSA0-RSA1 are rester scan address. They are generated by the 6845 or its equivalent inside the gate array. There are 4 raster scans altogether, but only the lowest two bits are used in the graphics mode.

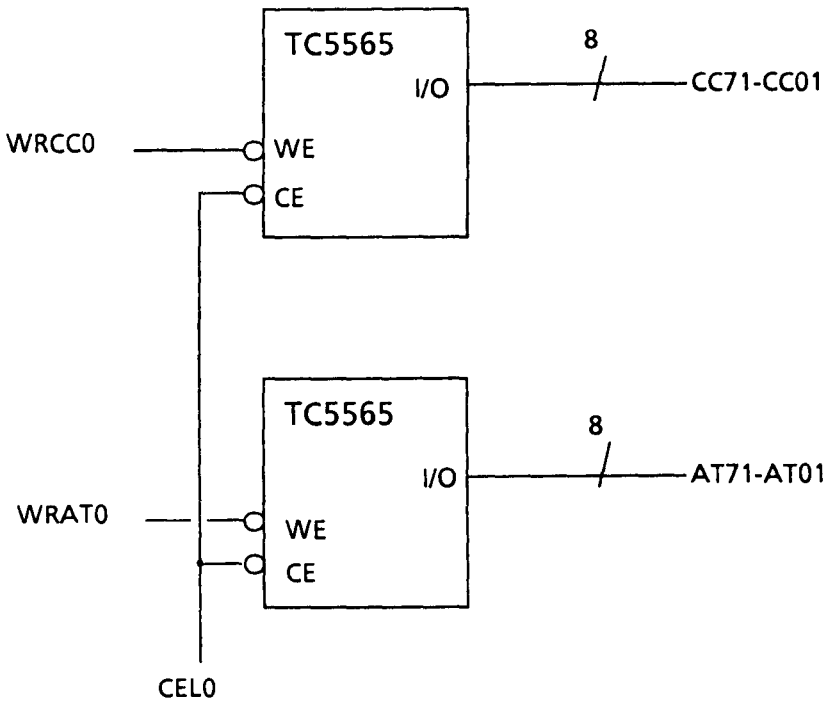


FIGURE D-3 V-RAM Control Signals

RSL0 : Refresh Address Selection (Output)

This signal is an input selection signal o the V-RAM address multiplexer.
If this is low, the display refresh address lines (RA05-RA12) are selected and supplied to the V-RAM. If it is high, the I/O bus address lines are selected and supplied to the V-RAM.

CC00-CC07 : Character Code Data Bus (Input/Output)

These lines are data bus from/to the even address V-RAM. The even address of the V-RAM is used to store the character codes in the TEXT mode.

AT00-AT07 : Attribute Data Bus (Input/Output)

These lines are data bus from/to the odd address V-RAM. The odd address of the V-RAM is used to store the attribute codes in the TEXT mode.

D.5.3 Character generator(CG) signals (16 lines)

CGA1 : CG Address Latch (Output)

This signal is used to set the character code read out from the V-RAM in the external latch. The set timing of the external latch circuit is at the raising edge of this signal. The output from the external latch circuit is used for the address of the CG-ROM. As the character code is of 8-bit, it can select one of the 256 characters.

ROM Address : (Output)

The following 6 signals are also used as CG-ROM address apart from the above mentioned character code which are latched in CGA1.

FNP0 ..... Plasma Font Slection (Not used)
FNS0 ..... Single Dot Font Selection
RS01, 11, 21, 30 ..... Raster Scan Address

The CG-ROM in this system has the capacity of 8 Kbytes, and it contains the fonts as floows;

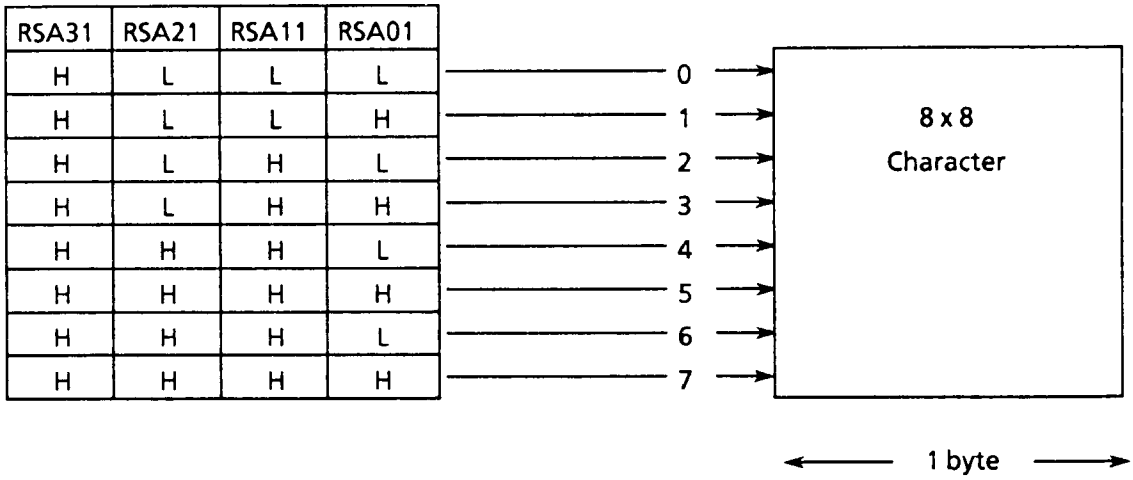
8x8 single dot character set
8x8 double dot character set

The LCD can not display intensified character like CRT display, thus double dot character is used for distinction between normal character and intensified character. FNS0 signal is used to select either single dot character or double dot character font.

FNS0 = Low ..... Single dot character
FNS0 = high ..... Double dot character

RS01-RS21, and RS30 are raster scan address. The RSA01 is the lowest bit (LSB).

TABLE D-5 ROM Address Assignment



D.5.4 Video signals (9 lines)

These are 9 video signals output from the gate array, and they are commonly used for the LCD, and for the CRT. Meaning of the signals for each display is as follows;

TABLE D-6 Video Signals

GA signal	LCD	CRT	
		RGB	Comp.
LHS1	LP1	CHSY1	
FVS1	FP1	CVSY1	
RHV1	FR131		CHVSY0
D0R1	LD11	CRV1	
D1G1	LD21	CGV1	
D2B1	LD31	CBV1	
D3I1	LD41	CIV1	CIV1
SXV1	LSCP1		CVD1
BFR0	FR1001		CBLNK0

D.5.5 Display mode select signals(3 lines)

CFN0 : Change Character Font (Input)

This signal is to change the font displayed on the screen. The function of this signal is shown on the Table C-7.

FLT1 : Flat Display Selected (Input)

This signal is to select one of internal and external display unit.
If this signal is at high level, the internal LCD is selected.
If this signal is at low level, the external CRT display (RGB, Composite) is selected.

PDP0 (Plasma Display Panel)

This signal is not used in this system.

The relation of these three signals and character fonts on the screen are as follows;

TABLE D-7 Signals and Character Fonts

	Bit 3 of attribute byte	GA Input			GA Input		Selected Display	Selected Display
		CHF0 NT0	CHF0 SL1	PDP0	INTE N1	CGM 01	Display	Display
80 x 25 or 40 x 25	0	H	H	H	H	H	LCD	8x8 double
	1	H	H	H	L	H	LCD	8x8 single
	0	L	H	H	L	H	LCD	8x8 single
	1	L	H	H	H	H	LCD	8x8 double
80 x 25 or 40 x 25	0	H	L	x	H	H	CRT	8x8 double
	1	H	L	x	H	H	CRT	8x8 double(High)
	0	L	L	x	L	H	CRT	8x8 single
	1	L	L	x	L	H	CRT	8x8 single (High)

D.5.6 Clock input (2 lines)

OSC14I : Oscillator 14 MHZ (Input)

This clock is the input signal to generate a video signal for the CRT display.
The frequency of the clock must be 14.31818MHZ.

OSC17I : Oscillator 18MHZ (Input)

This clock is the input signal to generate a video signal for the plasma display.
The frequency of the clock must be 17.5MHZ.

D.5.7 Other signals (15 lines)

GOFI : GA Off (Input)

If this signal is at high level, the gate array is disabled. This signal is used to disable the gate array in order to connect another display adapter to the I/O expansion box. In this system, this is fixed to "0".

SBEI : SBE -LCD (Input)

This signal is reserved for the LCD display.
In this system, this is fixed to "0".