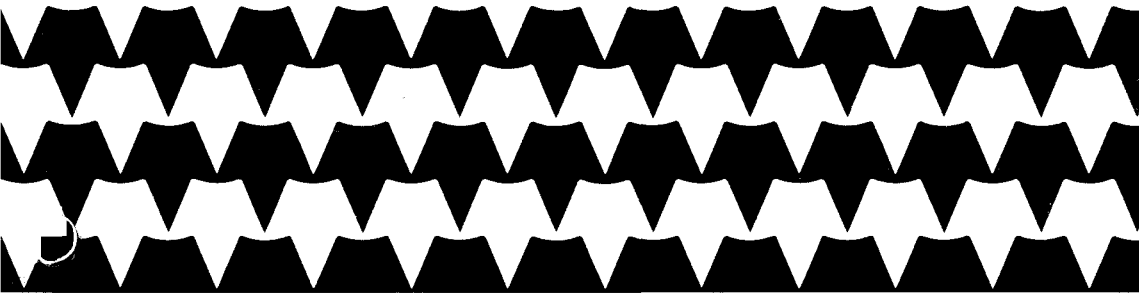
Cat. No. 25-1511

Tandy 1000 SX

Technical Reference Manual



TANDY®

TANDY 1000 SX
TECHNICAL REFERENCE MANUAL

Tandy 1000 SX Technical Reference Manual

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POWER SUPPLIES
KEYBOARD
8087 COPROCESSOR
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DEVICES

Note: Complete information for the Disk Drives for this unit is available through your local store. They will order the desired Service Manual from Radio Shack National Parts, Fort Worth, Texas.

Foldout Page Insertion Guide

To Be Inserted after Page 12 of the Main Logic Section

Light Blue to System Timing Diagram	Sheets 1 of 2 and 2 of 2
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To Be Inserted at the end of the Main Logic Section

PCB Art (Silkscreen, Component and Solder Sides)	1700337 Rev. A
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To Be Inserted at the end of the 67 Watt Dual Input Power Supply

Schematic	8790084 3P-M1-0165

To Be Inserted just before WD 8250 Asynchronous Communication Element Specification of RS-232 Section

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MAIN LOGIC BOARD

MAIN LOGIC BOARD
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INTRODUCTION TO THE TANDY 1000 SX COMPUTER

The Tandy 1000 SX Computer is modular in design to allow maximum flexibility in system configuration. The computer consists of a Main Unit, a detachable keyboard with coiled cable, and a monitor. The Main Unit is supplied with two internal floppy disk drives. The standard types of monitors used with the Tandy 1000 SX are the monochrome composite and the color RGB monitor. Since these units are modular, they may be placed on top of the Main Unit or at any convenient location.

The Tandy 1000 SX comes standard with 384K of system RAM. An optional 8 additional 256K RAM chips may be added on the system board to expand the memory to a full 640K bytes, the maximum RAM allowed by the system memory map.

Other features include a parallel printer port, two built-in joystick interfaces, a speaker for audio feedback, and a light pen interface.

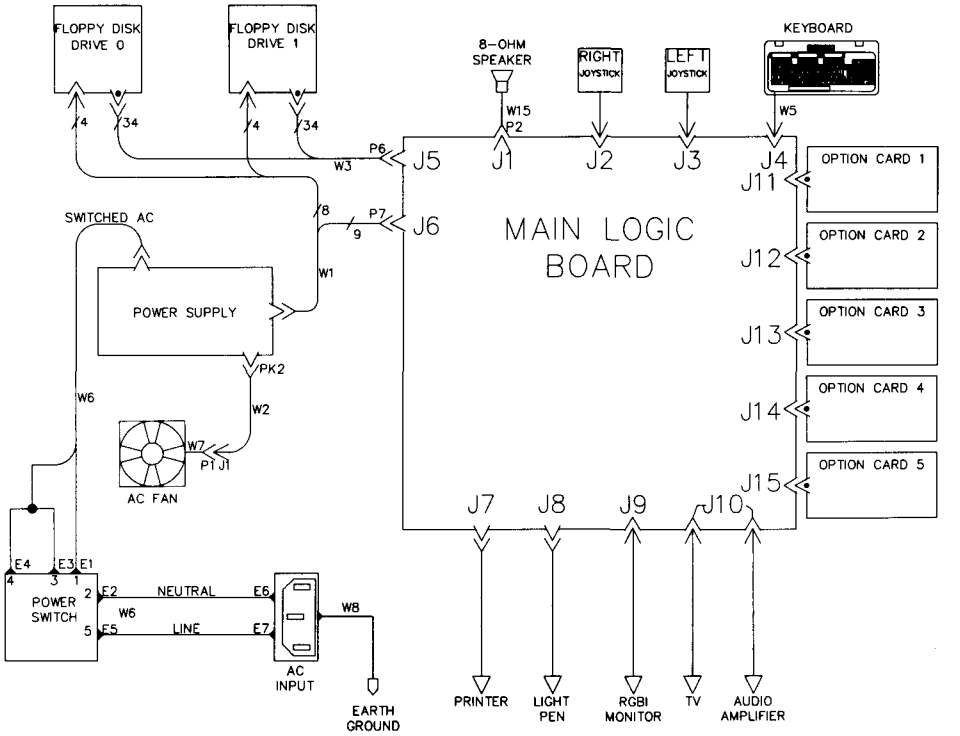
The Main Unit is the heart of the Tandy 1000 SX. It houses the Main Logic Assembly, system power supply, and floppy disk drives.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, and disk drives by a series of cables. The illustration in Figure 1 shows the major components of a Tandy 1000 SX system.

The Power Supply is a 67W switching regulator type, designed to provide adequate power capacity for a fully configured system using all the option slots.

The Floppy Disk Drive uses 5 1/4" double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The Disk Drive assembly is installed in the main unit. The floppy disk stores approximately 360K bytes (formatted) of data. All system programs, with the exception of the system startup sequence, are stored on disk.

Either a monochrome or a color display may be used with the Tandy 1000 SX. The monochrome monitor is a high-resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface. Each display is capable of 25 lines of 80 characters. The character matrix is 8 wide x 9 high.



REFERENCE

CABLE NO.	DESCRIPTION	DRAWING NO.	CABLE ASSY P/N
W1	DC POWER	C6009131	870-9886
W2	CABLE, PWR SPLY TO FAN	C6009141	870-9875
W3	SIGNAL, FLOPPY DISK	C6009057 Δ	870-9447
W5	CABLE, KEYBOARD	A6009129	870-9867
W6	AC POWER	C6009121	870-9863
W7	FAN	C2900009	
W8	EARTH GROUND	A6009125	870-9852
W15	SPEAKER	C6009070	870-9470

NOTE: Δ CABLE DWG C6009057 WILL BE USED IF CABLE TWIST IS REQUIRED TO CONNECT TO FLOPPY DISK DRIVES, OTHERWISE USE CABLE C6009118

CONNECTOR SYMBOLS

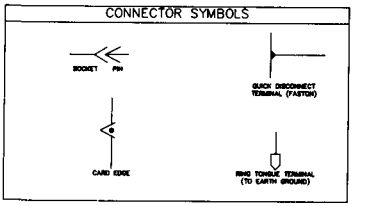


Figure 1. TANDY 1000 SX Interconnect Diagram

SPECIFICATIONS (Computer and Keyboard)

Processor: Intel 8088 - 2
Dimensions: Computer - 16 3/4" x 13 1/2" x 5 3/4"
Keyboard - 16 1/4" x 8" x 1.5"
Weight: Computer - 18 lbs (with 2 Floppy Disk Drives)
Keyboard - 3 lbs 4 oz.

Power Requirements:
Range: 105 VAC to 135 VAC
Nominal: 120 VAC, 60 Hz, 3 Amp maximum

With 2 Floppy Disk Drives, 640K Memory:
AC Current: 350 - 400 mA with Floppy doing R/W tests.
Leakage Current: 0.5 mA
Disk Drive:

	+5 VDC	+12 VDC
Idle	330 mA	160 mA
R/W	300 mA	330 mA
R/W	220 mA (Min.)	600 mA (Max.)
Main Logic Board:	1700 mA	360 mA
Option Cards:	-12VDC, 9 m,A	

Operating Environment:
Temperature: 55 to 85 degrees F (13 to 30 degrees C)
Humidity: 40% to 80% non-condensing

Non-Operating Environment:
Temperature: -40 to +160 degrees F (-40 to 71 degrees C)
Humidity: 20% to 90% non-condensing

Disk Drive Specifications
Power:

Supply Voltage	+5 VDC Input	+12 VDC Input
Ripple 0 to 50 kHz	100 mV	100 mV
Tolerance Including Ripple	+/-5%	+/-5%
Standby Current Nominal	190 mA	160 mA
Standby Current Worst Case	220 mA	190 mA
Operating Current Nominal	260 mA	600 mA
Operating Current Worst Case	300 mA	1000 mA

Environment:
Temperature
Operating 40 to 115 degrees F (4 to 46C)
Nonoperating -8 to 140 degrees F (-22 to 60C)
Relative Humidity
Operating 20% to 80% (noncondensing)
Nonoperating 5% to 95% (noncondensing)

Connector Pin Assignments

J1 -- Speaker Interface
(2-Pin Vertical Header)

1 -- Sound	2 -- Ground

J2 -- Right Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J3 -- Left Joystick
(6-Pin Rt. Angle Circular Din)

1 -- Y Axis	2 -- X Axis
3 -- Ground	4 -- Switch 1
5 -- +5 VDC	6 -- Switch 2

J4 -- Keyboard Interface
(8-pin Rt. Angle Circular Din)

1 -- KBDDATA	2 -- KBDBUSY*
3 -- Ground	4 -- KBDCLK
5 -- +5 VDC	6 -- KBDRST
4 -- MULTIDATA	8 -- MULTICLK

J5 -- Floppy Disk Interface
(Dual 17-Pin Vertical Header)

1 -- Ground	2 -- NC
3 -- Ground	4 -- NC
5 -- Ground	6 -- NC
7 -- Ground	8 -- INDEX*
9 -- Ground	10 -- DSO*
11 -- Ground	12 -- DS1*
13 -- Ground	14 -- NC
15 -- Ground	16 -- MTRON*
17 -- Ground	18 -- DIR*
19 -- Ground	20 -- STEP*
21 -- Ground	22 -- WRDATA*
23 -- Ground	24 -- WEN*
25 -- Ground	26 -- TRK0*
27 -- Ground	28 -- WRPRT*
29 -- Ground	30 -- RDDATA*
31 -- Ground	32 -- SIDESELECT*
33 -- Ground	34 -- DRVRDY*

J6 -- DC POWER
(9-PIN VERTICAL HEADER)

1 -- +5 VDC	2 -- +5 VDC
3 -- +5 VDC	4 -- Ground
5 -- Ground	6 -- Ground
7 -- +12 VDC	8 -- -12 VDC

J7 -- Parallel Interface
(34-Pin Card Edge)

1 -- PPSTROBE*	2 -- Ground
3 -- PPDATA0	4 -- Ground
5 -- PPDATA1	6 -- Ground
7 -- PPDATA2	8 -- Ground
9 -- PPDATA3	10 -- Ground
11 -- PPDATA4	12 -- Ground
13 -- PPDATA5	14 -- NC
15 -- PPDATA6	16 -- Ground
17 -- PPDATA7	18 -- Ground
19 -- PPACK*	20 -- Ground
21 -- PPBUSY	22 -- Ground
23 -- PPPAEM	24 -- Ground
25 -- PSEL*	26 -- NC
27 -- PPAUTOF*	28 -- PPFAULT
29 -- NC	30 -- PPINIT*
31 -- Ground	32 -- NC
33 -- Ground	34 -- +5V

J8 -- Light Pen
(9-Pin Connector Male Rt. Angle D-Subminiature)

1 -- +5 VDC	2 -- Ground
3 -- LPIN	4 -- LPSW*
5 -- NC	6 -- NC
7 -- NC	8 -- NC
9 -- NC	

J9 -- RGBI Video
(9-Pin Socket Rt. Angle D-Subminiature)

1 -- Ground	2 -- Ground
3 -- Red	4 -- Green
5 -- Blue	6 -- Intensity
7 -- Video	8 -- HSYNC
9 -- VSYNC	

J10 -- Composite Output
(Dual Rt. Angle RCA-Type Phone Jack)

A -- Video	B -- Audio

J11, J12, J13, J14, J15 -- Expansion Interface Connectors
(Dual 31-Pin Card Edge)

A01 -- NMI	B01 -- Ground
A02 -- D7	B02 -- BRESET
A03 -- D6	B03 -- +5 VDC
A04 -- D5	B04 -- IR2
A05 -- D4	B05 -- -5 VDC
A06 -- D3	B06 -- FDCDMARQ*
A07 -- D2	B07 -- -12 VDC
A08 -- D1	B08 -- AUDIOIN
A09 -- D1	B09 -- +12 VDC
A10 -- READY	B10 -- Ground
A11 -- AEN	B11 -- MEMW*
A12 -- A19	B12 -- MEMR*
A13 -- A18	B13 -- IOW*
A14 -- A17	B14 -- IOR*
A15 -- A16	B15 -- DACK3*
A16 -- A15	B16 -- DRQ3*
A17 -- A14	B17 -- DACK1*
A18 -- A13	B18 -- DRQ1*
A19 -- A12	B19 -- REFRESH*
A20 -- A11	B20 -- CLK
A21 -- A10	B21 -- IR7
A22 -- A09	B22 -- IR6*
A23 -- A08	B23 -- IR5
A24 -- A07	B24 -- IR4
A25 -- A06	B25 -- IR3
A26 -- A05	B26 -- FDCDACK*
A27 -- A04	B27 -- DMATC
A28 -- A03	B28 -- ALE
A29 -- A02	B29 -- +5 VDC
A30 -- A01	B30 -- OSC
A31 -- A00	B31 -- Ground

Tandy 1000 SX and IBM I/O Bus Cross Reference Chart

Pin No.	Description
B21	IBM - Interrupt Request 7. TANDY 1000 SX - Optional Interrupt Request 7.
B22	IBM - Interrupt Request 6. TANDY 1000 SX - Optional Interrupt Request 6.

Pin No.	Signal Name	Description
B08	AUDIOIN	IBM - Reserved TANDY 1000 SX - Audio input is supplied from an optional board on the I/O bus to a multiplexer on the main logic board for an output to the external speaker.

Note: All other pins are identical to the IBM PC. See Section 3 for the connector pin assignments.

BUS INTERFACE SPECIFICATIONS

This specification is for the primary bus on the Tandy 1000 SX main logic board, which also is available to the option board connectors. The specification describes the signals in the following manner. See Figures 2 - 4.

- The following signal nomenclature is used in the schematic and literature. Signals designated with the suffix "*" are logically "true low" (normal inactive state is high); if they are not so designated, the signal is logically "true high."
- Direction -- input or output -- is referenced to the CPU.
- Brief functional description of the signal.
- Description of the "drive" or "load" characteristics of the signal. This includes the specific source by IC type and reference designator, drive capability for "output" signals, and actual load for "input" signals. The drive/load is defined in "unit loads" and specified as "high/low." This specification is for the main logic board only. Some signals have an alternate source, an external bus master such as the DMA.
- 1 Unit Load (UL) is defined as: Ioh = .04mA @ 2.4V, Iol = 1.6mA @ 0.5V

Signal Listing

A00 - A19	O	ADDRESS	SOURCE: 43,42,U54 Drive - 65/15 UL Latch Strobe - ALE Output Enable - AEN Alternate external source
D0-D7	I/O	DATA	SOURCE: U52 Drive - 37/15 UL Direction Control - READ* (CPU read signal) Enable - DEN*
ALE	O	ADDRESS LATCH STROBE	SOURCE: U56
IOW*	O	I/O WRITE STROBE	Drive - 50/7.5 UL
IOR*	O	I/O READ STROBE	Output Enable - AEN
MEMW*	O	MEMORY WRITE STROBE	Pull-Up - 4.7K Ohms

MEMR*	O	MEMORY READ STROBE	Alternate external source
CLK	O	CPU CLOCK	4.77MHz, 33% duty cycle, 7.16MHz, 50% duty cycle. SOURCE: U54 Drive - 75/7.5 UL
OSC	O	OSCILLATOR	14.32MHz, 50% duty cycle SOURCE: U54 Drive - 75/7.5 UL
NMI	I	NON-MASKABLE INTERRUPT	To System NMI Load: 1/1 UL, U117
READY	I	SYSTEM WAIT	SOURCE: OPEN-COLLECTOR OR 3-STATE BUFFERS Load: 1 UL and 1.0K ohm pull-up. 10/0.9 UL Set LOW by Peripherals (I/O or Memory) to extend READ or WRITE cycles.
BRESET	O	SYSTEM RESET	Power On or Manual SOURCE: U54 Drive: 75/7.5 UL
AEN	O	BUS GRANT	To external masters SOURCE: U82 Drive - 75/7.5 UL
IR2	I	INTERRUPT REQUEST#2	To system interrupt controller
IR3	I	INTERRUPT REQUEST#3	Load: 1 UL and 2.2K pull-down
IR4	I	INTERRUPT REQUEST#4	
IR5	I	INTERRUPT REQUEST#5	
IR6	I	INTERRUPT REQUEST#6	
IR7	I	INTERRUPT REQUEST#7	
AUDIO IN	I		From External Sound Source Load: 10k ohms.

AUDIO	O		To External Source Drive: 1.25 Volts P-P into 10K
DRQ1	I	REQUEST DMA CHANNEL#1	Load: 8237A-5/9517A
FDCDMARQ	I	REQUEST DMA CHANNEL#2	1 MOS load 40/160 UL
DRQ3	I	REQUEST DMA CHANNEL#3	
REFRESH*	O	ACKNOWLEDGE DRQ0*	Dedicated output
DACK1*	O	ACKNOWLEDGE DRQ1*	acknowledges from DMA.
FDCDACK*	O	ACKNOWLEDGE DRQ2*	Drive: 8237A-5/9517A
DACK3*	O	ACKNOWLEDGE DRQ3*	2/2 UL
DMATC	O	TERMINAL COUNT	Used by DMA Controller to indicate Terminal Count reached. Drive: 2/2 UL

+5VDC	+5VDC 4% 0.6 Amps per slot available on the bus.
+12VDC	+12VDC 5% 0.1 Amps per slot available on the bus.
-12VDC	-12VDC +8.3% - 25% 0.06 Amps available on the bus.
GROUND	Power Return for +5, +12, -12 VDC.

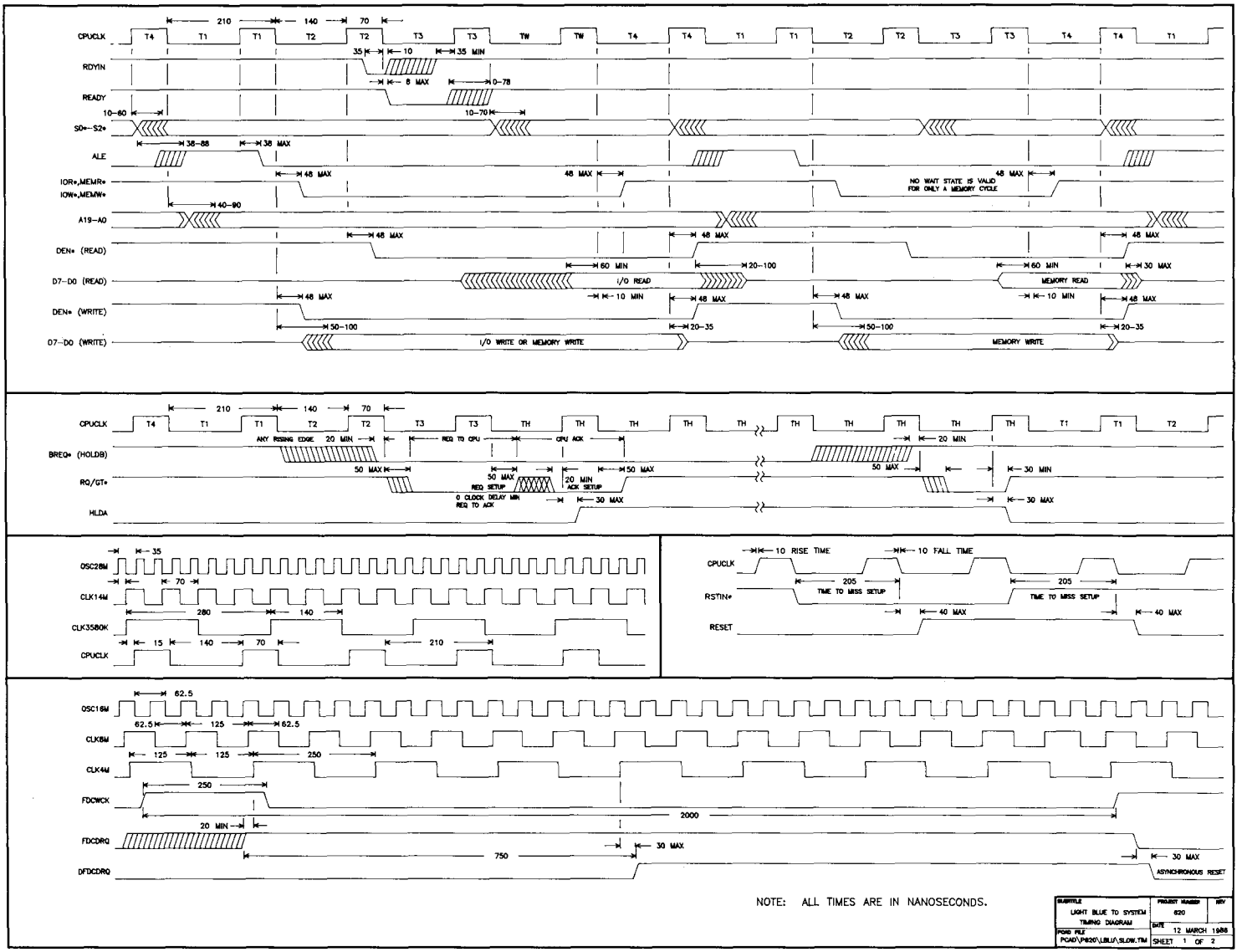


Figure 2. Light Blue to System Timing (1 of 2)

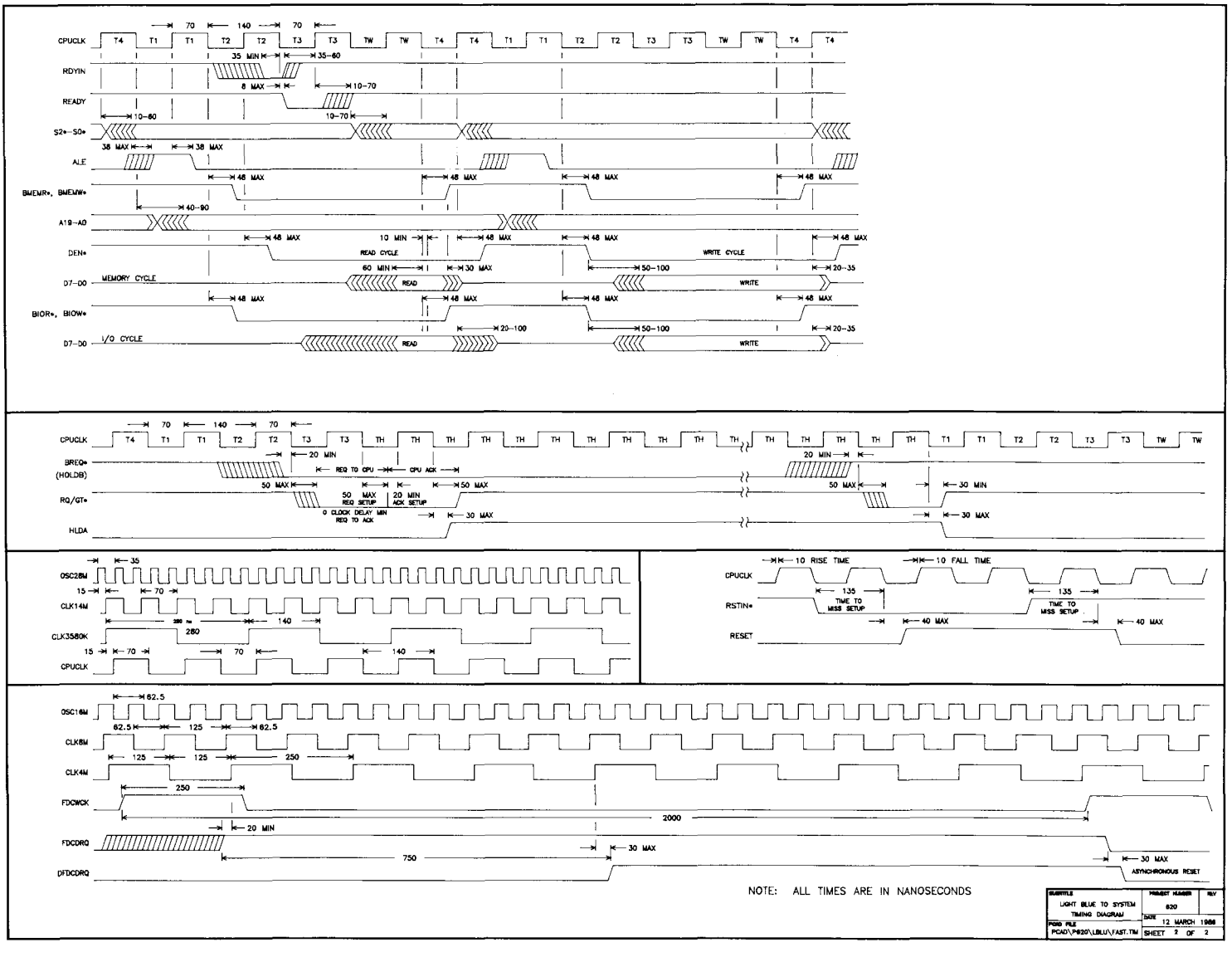


Figure 2. Light Blue to System Timing (2 of 2)

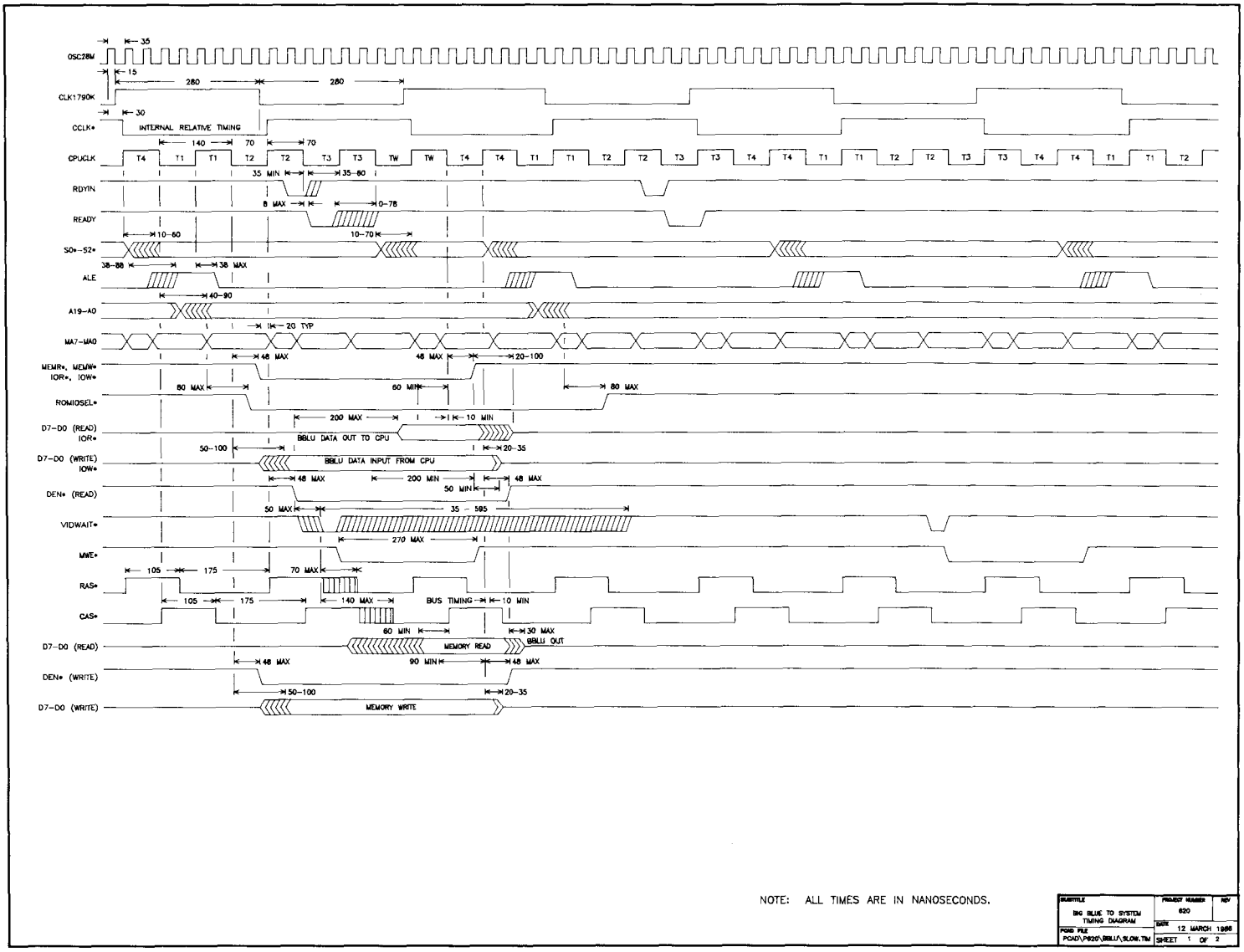


Figure 3. Big Blue to System Timing (1 of 2)

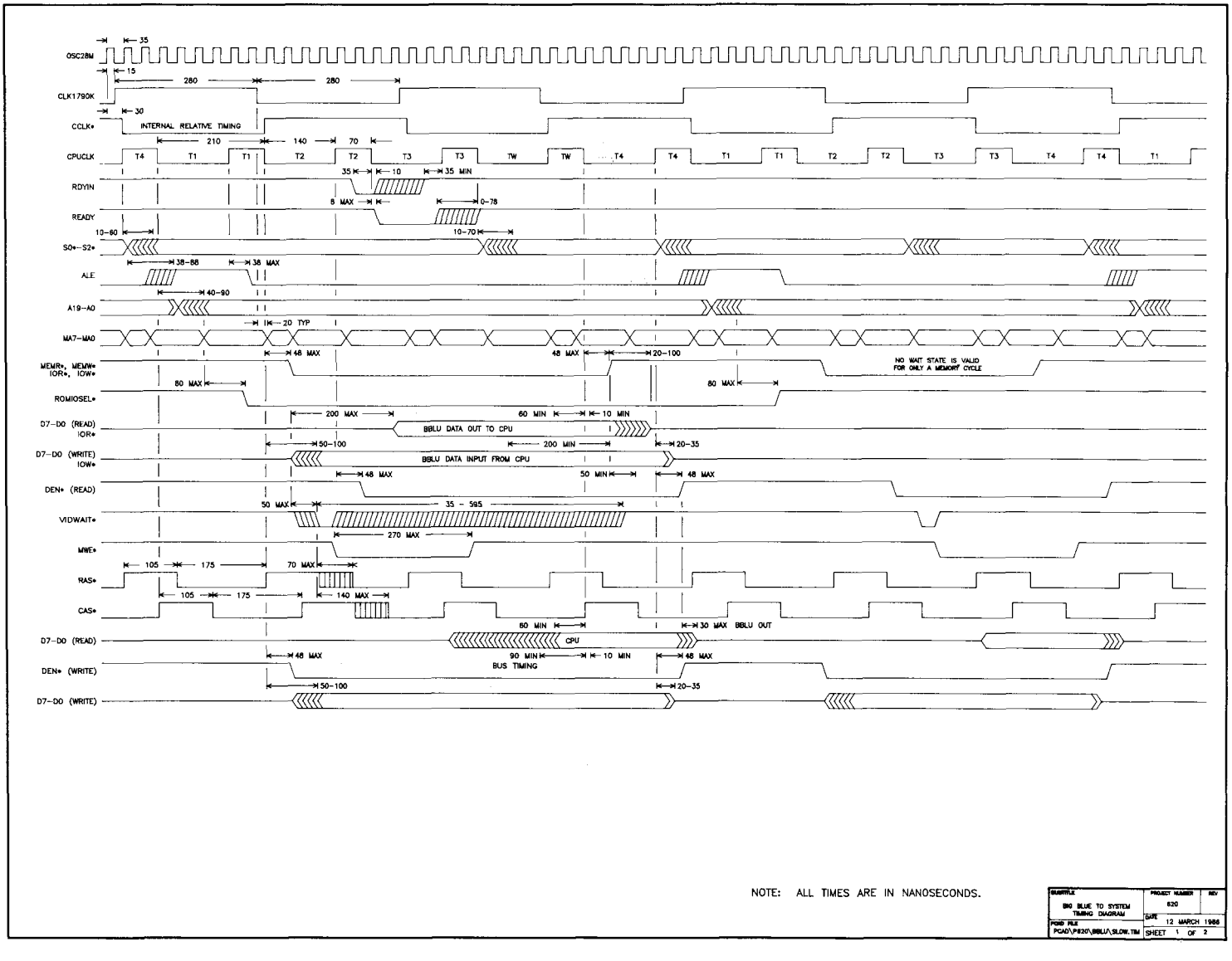


Figure 3. Big Blue to System Timing (2 of 2)

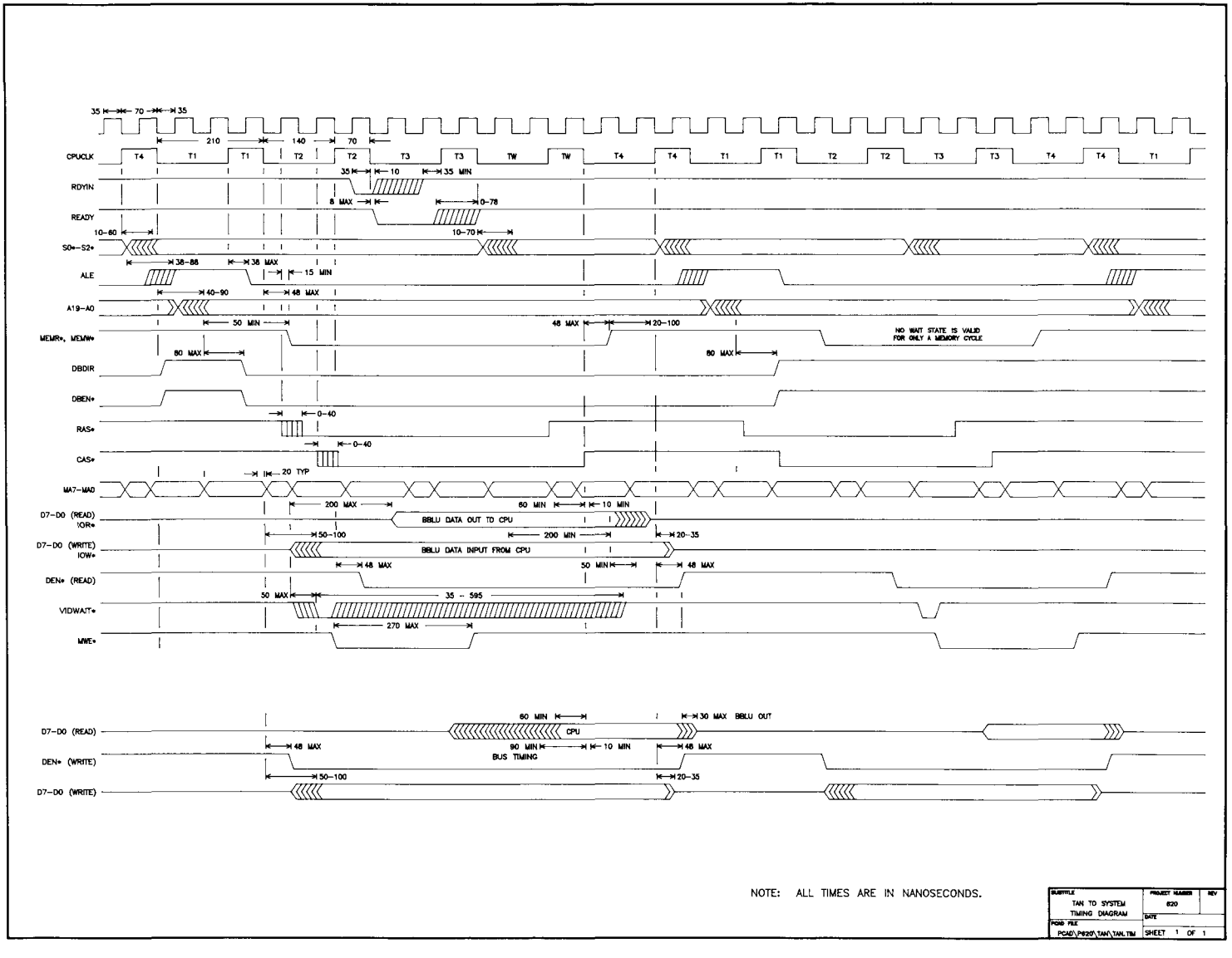
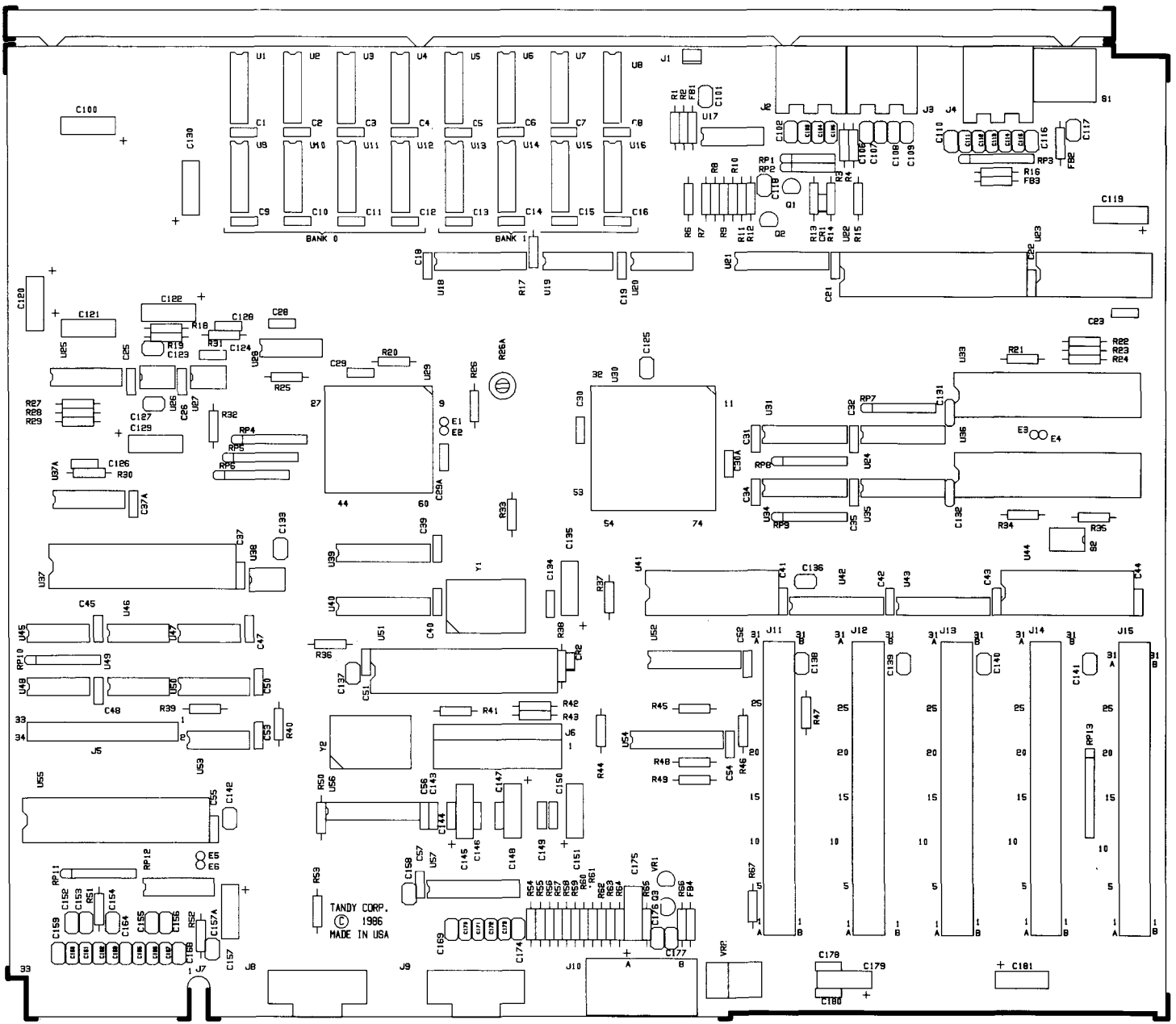


Figure 4. Tan to System Timing

TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD- 262-
PROJECT NO.: 682 DATE: 06/03/86	C/S SILKSCREEN
TITLE: MAIN LOGIC PCB	
DWG. NO.: 1700337 REV.A	
PART NO.: 8719699	
DESIGN GRID: x=.025 y=.025	
DESIGNER: DD	
INSP:	



Tandy 1000 SX Theory of Operation

The block diagram for the Tandy 1000 SX (sheet 1 of the schematic) shows the main elements of the computer system. The most important single element is the Central Processor Unit (CPU). The other major elements of the Tandy 1000 SX are the Timing and CPU Control chip, the video interface, the Direct Memory Access controller (DMA) and system memory, system Read Only Memory (ROM), system timer (8253), expansion bus, and five input/output (I/O) interfaces (keyboard, printer, floppy disk, joystick, and sound).

The CPU section of the Tandy 1000 SX consists of the 8088 CPU chip, the 8259A interrupt controller chip, and an optional 8087 numeric co-processor. These three devices share the CPU address/data bus, which is buffered before being supplied to the rest of the computer.

The CPU data bus is buffered by U52 (74LS245) before being supplied to the rest of the computer. The address bus is buffered as follows: 16 of 22 address bus lines are latched and buffered by U42 and U43 (74LS373). Four lines (A12-A15) are buffered by 1/2 of U54 (74LS244).

CPU Bus

The 8087 numeric data co-processor option provides up to 100 times the performance of the CPU alone on numeric applications. To install this option in your Tandy 1000 SX, simply remove the jumper connecting E3 to E4 and install the 8087-2 part in the socket for U33.

Also on the CPU bus, the 8259A interrupt controller chip supplies the maskable interrupt input to the CPU. The 8259A has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to generate the interrupt input to the CPU. The eight interrupts are assigned as follows:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Receiver
#2	Interrupt on the Bus	Hard Disk Controller
#3	Interrupt on the Bus	Modem
#4	Interrupt on the Bus	RS-232
#5	Vertical Sync	Optional Bus Interrupt
#6	Floppy Disk Controller	Optional Bus Interrupt
#7	Printer	Optional Bus Interrupt

Interrupts 0 and 1 are connected to system board functions as indicated in the chart. Interrupts 2 - 4 are connected directly to the expansion bus, with the normally assigned functions listed in the chart. Interrupts 5 - 7 are connected through a switch to the system board function listed, and are also connected to the expansion bus. To use interrupt 5, 6, or 7 on the bus, the system board function must be disconnected (set the appropriate switch to off). Please note that disconnecting the normal system board function may cause some application programs to fail or operate incorrectly.

After being buffered, the CPU address/data bus is connected directly to the 5 expansion bus connectors. Also, the address bus is directly connected to the rest of the system board. The data bus is separately buffered by (U40) before being supplied to system board.

U18 is a programmed logic device that is used to provide the ROM chip select signal, enable gating for the non-maskable interrupt, and chip select and direction signals for U40 (the system board data buffer). Table 1 lists the equations for U40.

The Tandy 1000 SX uses a 128K ROM to store the BIOS and diagnostic operating code. The ROM chip select enables the ROM for the top 64K of memory (F0000 - FFFFF).

The next major functional block of the Tandy 1000 SX is the CPU control and timing chip (light blue). A block diagram of this 40 pin custom part is shown in Figure 5. This chip accepts 16MHz and 28.6 MHz clock signals from the master oscillator circuits and generates clocks for all of the other circuitry on the board. This chip also generates the system reset signal and derives the CPU control signals based on status inputs from the CPU chip. The last major function of this part is to generate timing signals and a chip select signal for the FDC.

The next major block of the Tandy 1000 SX is the video interface circuitry. A block diagram of the video interface custom circuitry is shown in Figure 6. This custom part contains all of the logic necessary to generate an IBM compatible color video display. The video interface logic consists of the 84 pin custom video circuit, 4 - 64K X 4 RAMS, a 74LS244 buffer, and associated logic for generation of composite video.

System Control IFL

Inputs

```
PIN 1     =     !mio
PIN 2     =     !memr
PIN 3     =     a19
PIN 4     =     a18
PIN 5     =     a17
PIN 6     =     !memios
PIN 7     =     !fdcack
PIN 8     =     !ior
PIN 9     =     !refresh
PIN 11    =     nmien
PIN 12    =     nmi
PIN 13    =     a16
```

Outputs

```
PIN 14    =
PIN 15    =     enbnmi
PIN 16    =     !romcs
PIN 17    =     !bufenb
PIN 18    =     bufdir
PIN 19    =
```

Logic Equations

```
!bufdir =  memr & !mio & !fdcack
          #memr & !mio & memios
          #memr & !mio & ior
          #ior & mio
          #ior & fdack & !memios & ! memr;

!bufenb =  !memios & !romcs & !fdcack
          #memios & fdcack;

romcs = memr & !refresh & a19 & a18 & a17 & a16;

enbnmi - nmien & nmi;
```

Table 1

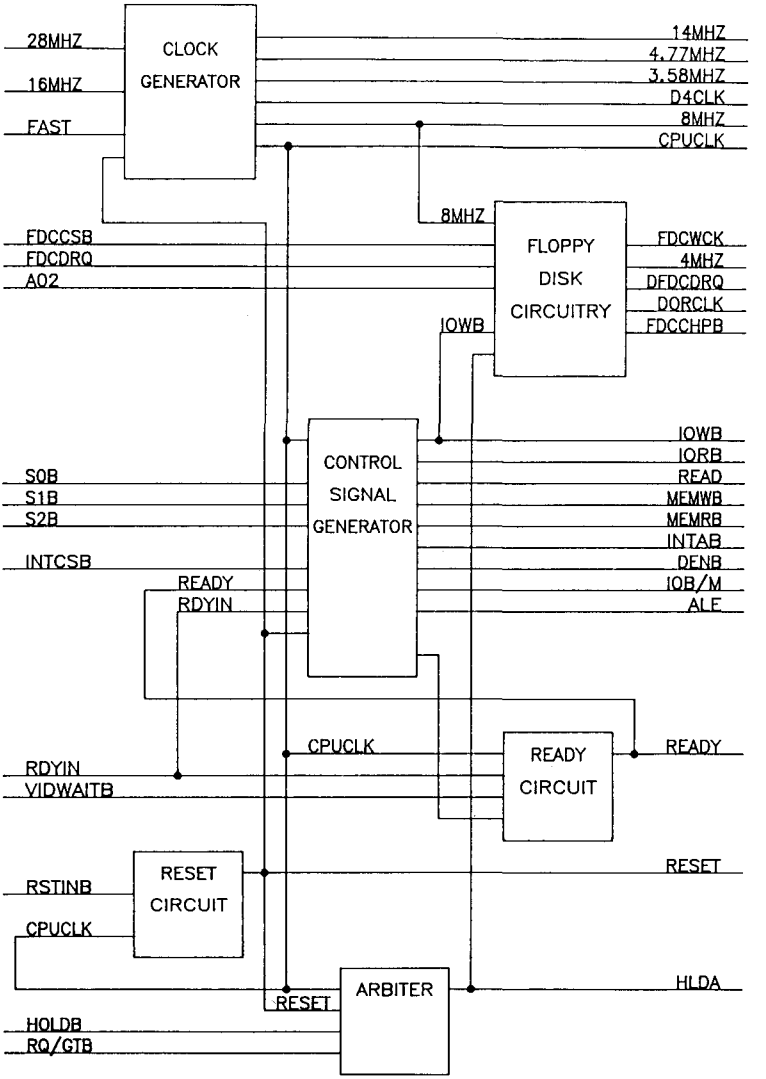


Figure 5. Timing Control Generator Block Diagram

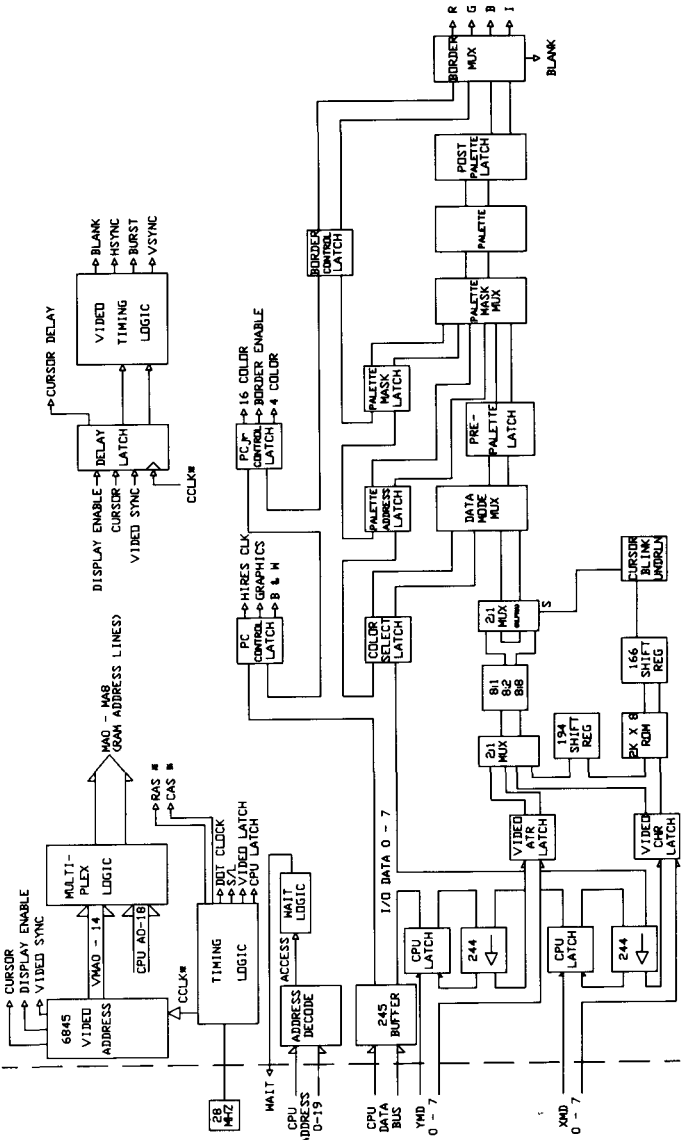


Figure 6. Video Controller Block Diagram

The Tandy 1000 SX video interface circuitry controls 128K of memory. This RAM is shared by the CPU and the video. Normally, the video only requires 16K or 32K for the video screen and the remainder of the 128K is available for system memory uses.

The Tandy 1000 SX video interface custom circuit is composed of a 6845 equivalent design, dynamic RAM address generation/timing, and video attribute controller logic.

Normal functioning of the video interface custom circuit is as follows. After the 6845 is programmed with a correct set of operating values (Table 2), the address inputs to the dynamic RAMs are generated by a 4:1 multiplexer. This Mux switches between video (6845) addresses and CPU address as well as between row and column address. Also, the video interface chip provides the RAM timing signals and generates a wait signal to CPU for proper synchronization with the video RAM access cycles.

The outputs from the RAM chips are only connected to the video interface custom circuit, so all CPU read/write operations are buffered by this part. During a normal display cycle, video data from the RAM chips is first latched in the Video Attribute latch and the Video Character latch. The video interface requires a memory organization of 64K X 16 and will latch 16 bits of memory during each access to RAM. From the output of the two latches, the data is supplied to the character ROM for the Alpha modes or to the shift registers for graphics modes. A final 2:1 Mux is used to switch between foreground or background in the alpha modes.

From the 2:1 Mux the RGBI data is combined with the PC color select data and latched in the Pre-Palette latch. This latch synchronizes the RGBI data before it is used to address the Palette. The palette mask Mux is used to switch between incoming RGBI data and the palette address register. During a CPU write to the palette, this address register selects one of the 16 palette locations. Also, the Palette mask Mux allows any of the input RGBI bits to be set to zero.

The palette allows the 16 colors to be remapped in any desired organization. Normally, the palette is set for a 1:1 mapping (red = red, blue = blue, etc.) for PC compatibility. However, instantly changing the on-screen colors is a very powerful tool for animation or graphics programs.

PROGRAMMING TABLE FOR THE 6845 All Values in Hex (Decimal)

Register Address	40 x 25 Alpha	80 x 25 Alpha	Low Res. Graphics	High Res. Graphics	40 x 25 Alpha	80 x 25 Alpha	Low Res Graphics	High Res Graphics
00 Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)	38 (56)	71 (113)
01 Horizontal Displayed	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)	28 (40)	50 (80)
02 Horizontal Sync Position	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)	2D (45)	59 (89)
03 Horizontal Sync Width	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)	08 (8)	10 (16)
04 Vertical Total	1C (28)	1C (28)	7F (127)	3F (63)	1F (31)	1F (31)	7F (127)	3F (63)
05 Vertical Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
06 Vertical Displayed	19 (25)	19 (25)	64 (100)	32 (50)	19 (25)	19 (25)	64 (100)	32 (50)
07 Vertical Sync Position	1A (26)	1A (26)	70 (112)	38 (56)	1C (28)	1C (28)	70 (112)	38 (56)
08 Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)	02 (2)
09 Max Scan Line Address	08 (8)	08 (8)	01 (1)	03 (3)	07 (7)	07 (7)	01 (1)	03 (3)
10 Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)	06 (6)
11 Cursor End	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)	07 (7)
12 Start Address (High)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
13 Start Address (Low)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)	00 (0)
Monitor Mode				**TV Mode**				

Table 2

After the Palette, the RGBI data is resynchronized in the Post Palette register. The final logic before the RGBI data is buffered off the chip is the Border Mux. This Mux allows the Border to be replaced with any color selected by the border color latch. This latch is normally disabled in PC modes, but it is used in all PC jr modes.

The next major functional block in the Tandy 1000 SX is the DMA/Memory controller chip. A block diagram for this part is shown in Figure 7. This custom part is composed of the equivalent of an 8237A-5 Direct Memory Access chip and a small amount of additional logic to complete the DMA function. Also, this chip provides timing and refresh addresses to the system memory. In the Tandy 1000 SX, this system memory is 256K and may be expanded to 512K of memory (with the video/system memory, this is a total of 640K on the main logic board). To expand the memory to 640K total, simply remove the jumper connecting E1 to E2 and add the 8 additional RAM chips in Bank 1.

The final system function other than I/O is the 8253 timer chip. This part is composed of three independent programmable counters. The clock for all three counters is 1.1925 MHz. Counter 0 and 1 are permanently enabled. Counter 2 is controlled by port Hex 0062, bit 0. Counter #0 is connected to system interrupt #0 and is used for software timing functions. Counter #1 is used for timing of the refresh function. Counter 2 is connected to the sound circuit and also to port Hex 0061, bit 5.

The sound circuit is one of the five I/O functions of the Tandy 1000 SX. The circuit provides sound output for the internal speaker and also for an external sound circuit. A functional block diagram of this circuit is shown in Figure 8.

The main source of sound in the Tandy 1000 SX is the 76496 complex sound generator. This device has 3 tone generators and 1 white noise generator. Each tone generator may be programmed for frequency and attenuation. Also, this device has an audio input pin which is connected to the gated output of timer channel 2. This audio input signal is mixed with the sound generator signal and supplied to the audio output pin.

From the output of the 76496, the sound signal is connected to a dual analog multiplexer. The multiplexer is switched by port 61, bits 5 and 6. One section of the multiplexer is used for the internal speaker, and the other section is used for the external audio signal. The section controlling the internal speaker may be disabled by port 61, bit 4.

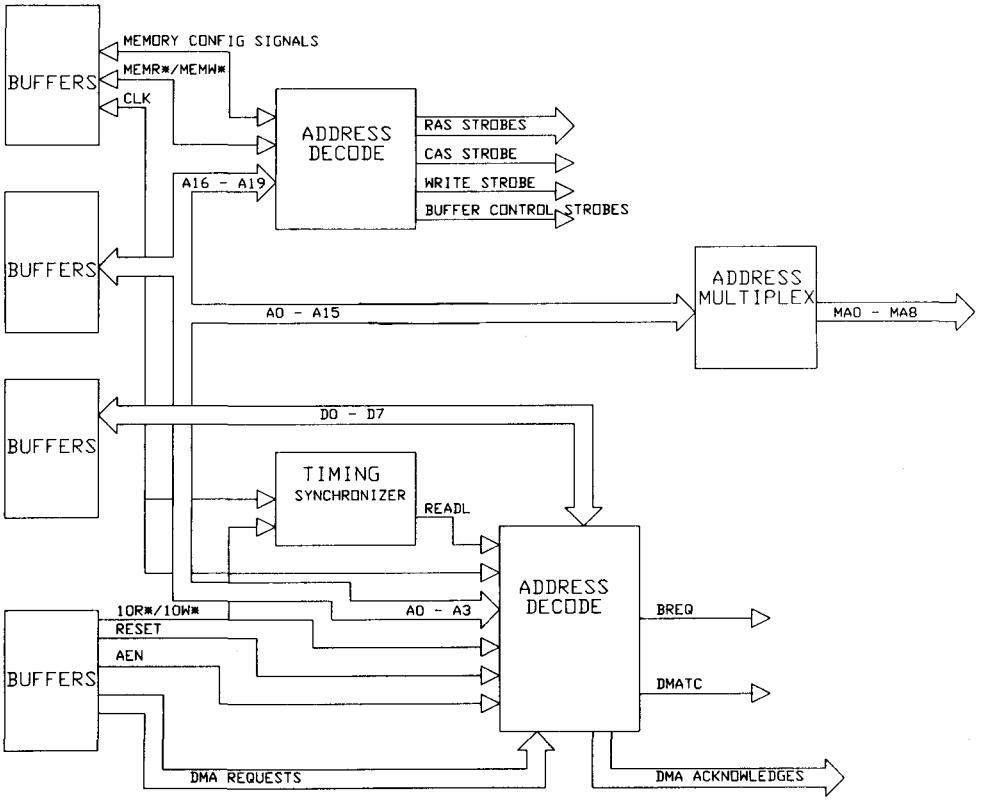


Figure 7. DMA/Memory Controller Chip Block Diagram

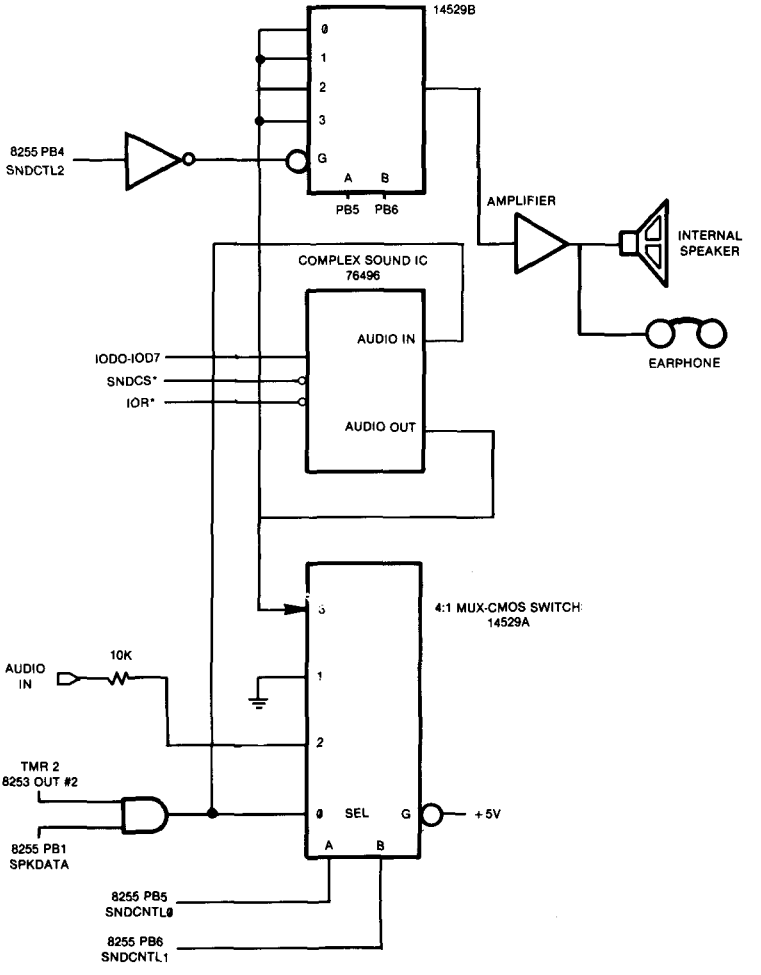


Figure 8. Sound Functional Block Diagram

The next I/O function of the Tandy 1000 SX is the Keyboard interface custom circuit. A block diagram of this part is shown in Figure 9. The heart of this custom part is several read-write registers that are used to control the keyboard interface logic, sound circuitry, and FDC circuitry. For the interface to the keyboard connector, a 164 type shift register is used to load the serial data and allow the CPU to read it as 8 parallel bits. The FDC circuitry consists of a write-only latch for the FDC control signal plus additional circuitry to allow the 2 drive select signals to be switched.

Joystick Interface

The joystick interface converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides 1 or 2 push-buttons and X,Y position for a total of 4 bits each. You can use 2 joysticks. The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator U17. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts.) When the position signal is equal or less than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever a "write" is made at Port 200/201 Hex. The IOW* signal turns on Q2, which drains C118 to 0.0 volts. When Q2 is turned off, Q1, R12, R13, R14, and CR1 create a constant-current source that linearly charges C118 to +5.0 VDC in 1.12 milliseconds. The joystick information is "read" by the CPU at Port 200/201 Hex through U21. See Figure 10.

One of the most important I/O functions of the Tandy 1000 SX is the floppy disk interface. This I/O function consists of the 765 controller and support circuitry. In the Tandy 1000 SX, the support circuitry is broken up and located in several of the other custom circuits. The clock and chip select signals for the rest of the FDC circuit are generated by Light Blue. The motor on and drive select signals are supplied from the keyboard interface custom circuit. Also, the logic to switch between the DMA terminal count and the CPU terminal count is located in the printer interface custom chip.

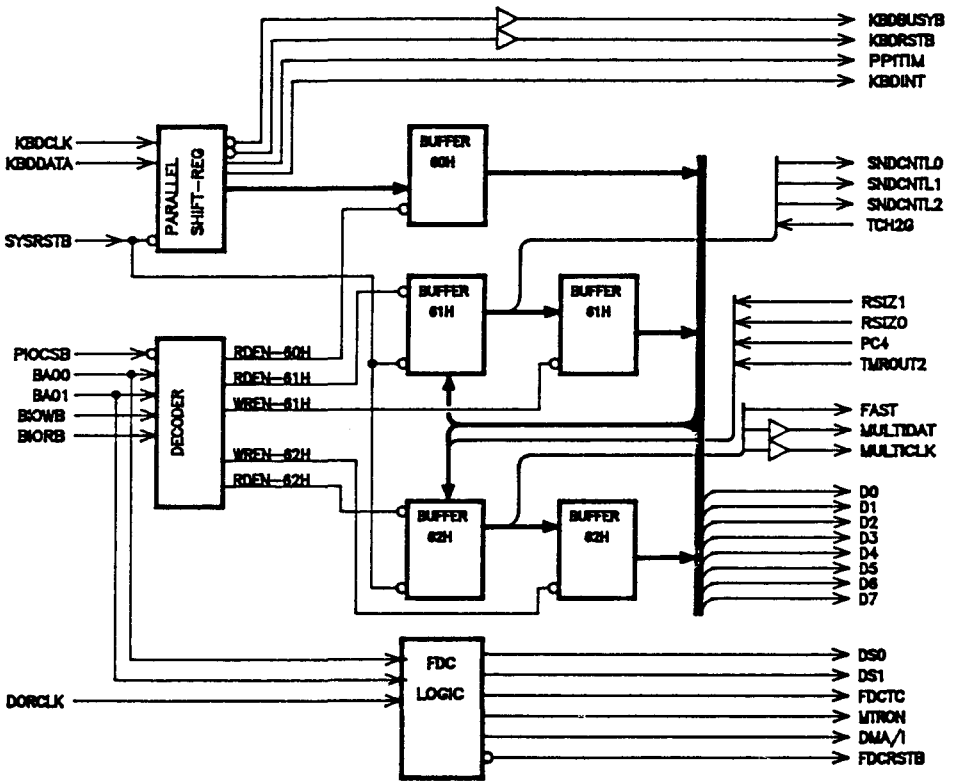
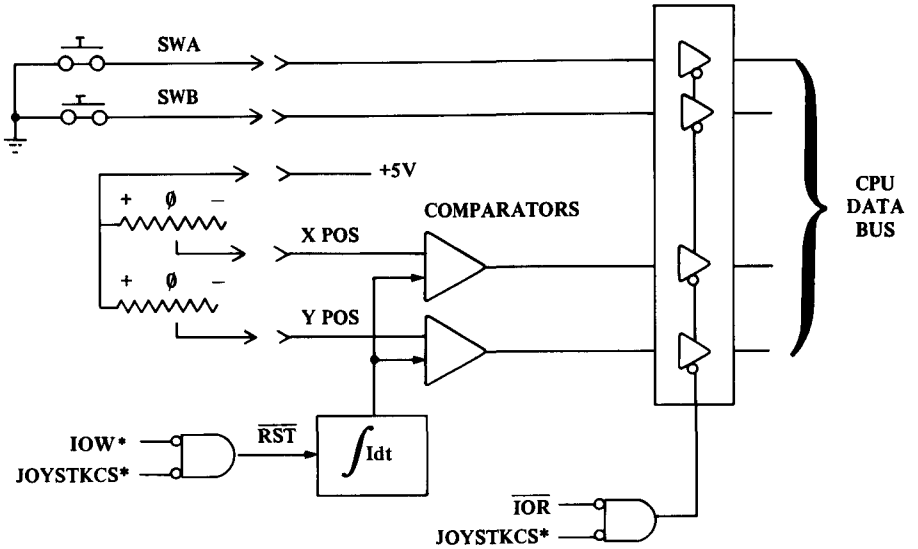
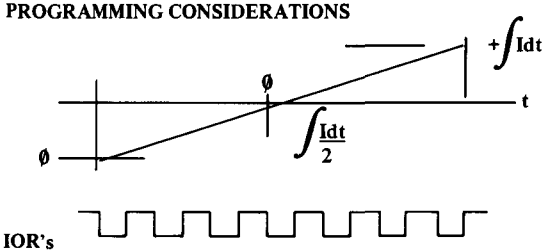


Figure 9. Keyboard Interface Block Diagram



PROGRAMMING CONSIDERATIONS



@ REGULAR INTERVALS

ONCE TRIGGERED BY SOFTWARE THE INTERGRATOR CIRCUIT PRODUCES A PULSE THE DURATION OF WHICH IS DEPENDENT ON JOYSK POSITION.

Figure 10. Joystick Interface Block Diagram

The bulk of the FDC interface is handled by the 765 controller chip and the 9216 digital data separator. The 765 generates write data which has pre-compensation added by U50. Read data from the floppy drive is separated into data and clock for the 765 by the 9216 data separator.

The final I/O interface of the Tandy 1000 SX is the Printer Interface, shown in block diagram form in Figure 11. This part supplies all of the signals required to interface to a typical parallel printer. These signals are 8 data out lines, plus various handshake control signals. Also, the printer interface will generate an interrupt to the CPU if enabled.

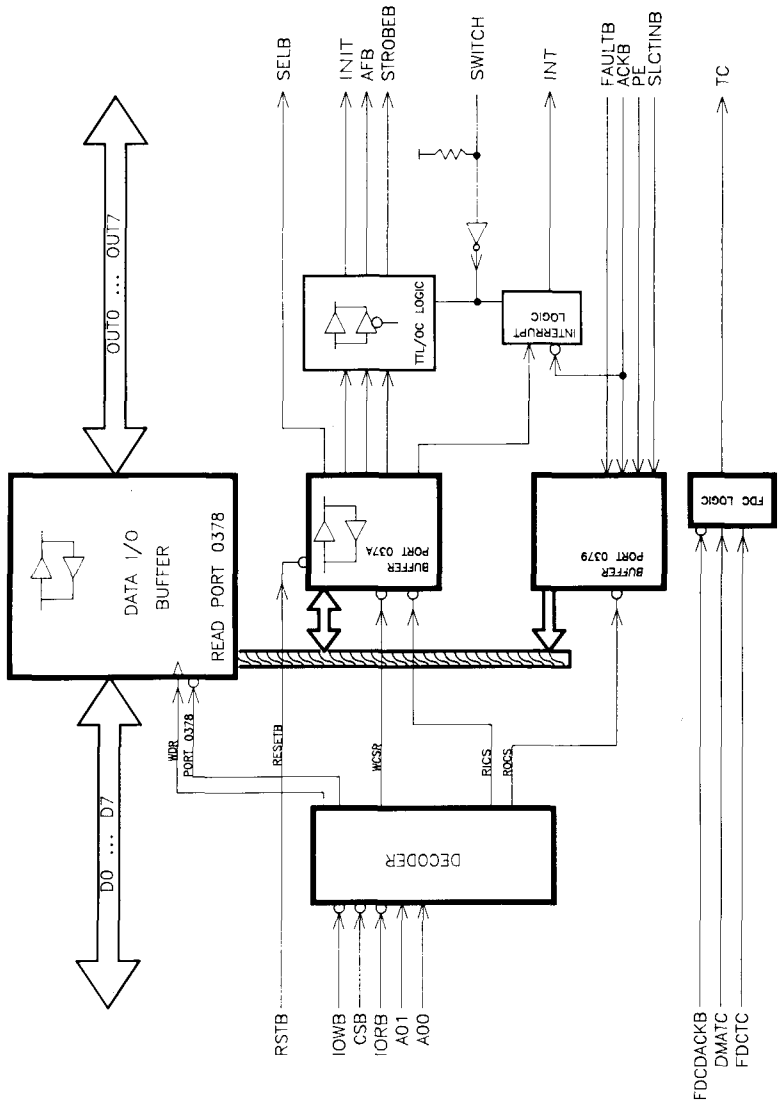


Figure 11. Printer Interface Block Diagram

I/O MAP SUMMARY

Block	Usage	Function
0000-001F	0000-000F	DMA Function
0020-003F	0020-0021	Interrupt Controller
0040-005F	0040-0043	Timer
0060-007F	0060-0063	PIO Function
0080-009F	0080-0083	DMA Page Register
00A0-00BF	00A0	NMI Mask Register
00C0-00DF	00C0-00C1	Sound Generator
00E0-01FF		Reserved
0200-020F	0200-0201	Joystick Interface
0210-031F		Reserved
0320-032F		Reserved Hard Disk
0330-036F		Not Assigned
0370-037F	0378-037B	Printer
0380-03CF		Not Used
03D0-03DF	All	System Video
03E0-03EF		Reserved
03F0-03FF	03F2,F4,F5	Floppy Disk Controller
0400-FFFF		Not Usable

Address **Description**

0000 DMA Controller
IOW* = 0: Channel 0 Base and Current Address
Internal Flip/Flop = 0: Write A0-A7
Internal Flip/Flop = 1: Write A8-A15
IOR* = 0: Channel 0 Current Address
Internal Flip/Flop = 0: Read A0-A7
Internal Flip/Flop = 1: Read A8-A15

0001 DMA Controller
IOW* = 0: Channel 0 Base and Current Word Count
Internal Flip/Flop = 0: Write W0-W7
Internal Flip/Flop = 1: Write W8-W15
IOR* = 0: Channel 0 Current Word Count
Internal Flip/Flop = 0: Read W0-W7
Internal Flip/Flop = 1: Read W8-W15

0002 DMA Controller
IOW* = 0: Channel 1 Base and Current Address
Internal Flip/Flop = 0: Write A0-A7
Internal Flip/Flop = 1: Write A8-A15
IOR* = 0: Channel 1 Current Address
Internal Flip/Flop = 0: Read A0-A7
Internal Flip/Flop = 1: Read A8-A15

Address	Description
0003	DMA Controller IOW* = 0: Channel 1 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 1 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0004	DMA Controller IOW* = 0: Channel 2 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 2 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0005	DMA Controller IOW* = 0: Channel 2 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 2 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0006	DMA Controller IOW* = 0: Channel 3 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR* = 0: Channel 3 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0007	DMA Controller IOW* = 0: Channel 3 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write W8-W15 IOR* = 0: Channel 3 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15

0008 DMA Controller
IOW* = 0, Write Command Register

Bit	Description
0	0 = Memory to Memory Disable 1 = Memory to Memory Enable
1	0 = Channel 0 Address Hold Disable 1 = Channel 0 Address Hold Enable X If bit 0 = 0
2	0 = Controller enable 1 = Controller disable
3	0 = Normal timing 1 = Compressed timing X If bit 0 = 1
4	0 = Fixed priority 1 = Rotating priority
5	0 = Late write selection 1 = Extended write selection X = If bit 3 = 1
6	0 = DREQ sense active high 1 = DREQ sense active low
7	0 = DACK sense active low 1 = DACK sense active high

IOR* = 0, Read Status Register

Bit	Description
0	1 = Channel 0 has reached TC
1	1 = Channel 1 has reached TC
2	1 = Channel 2 has reached TC
3	1 = Channel 3 has reached TC
4	1 = Channel 0 Request
5	1 = Channel 1 Request
6	1 = Channel 2 Request
7	1 = Channel 3 Request

0009 DMA Controller
IOW* = 0, Write Request Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Select channel 0
	0	1	Select channel 1
	1	0	Select channel 2
	1	1	Select channel 3
2	0	Reset request bit	
	1	Set request bit	
3-7	Don't Care		
	IOR* = 0, Illegal		

000A DMA Controller
IOW* = 0, Write Single Mask Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Select channel 0 mask bit
	0	1	Select channel 1 mask bit
	1	0	Select channel 2 mask bit
	1	1	Select channel 3 mask bit
2	0	Clear mask bit (Disable Channel)	
	1	Set mask bit (Disable Channel)	
3-7	Don't care		
	IOR* = 0, Illegal		

000B DMA Controller
IOW* = 0, Write Mode Register

Bit	Description		
0-1	Bit1	Bit0	
	0	0	Channel 0 select
	0	1	Channel 1 select
	1	0	Channel 2 select
	1	1	Channel 3 select
2-3	Bit3	Bit2	
	0	0	Verify transfer
	0	1	Write transfer to memory
	1	0	Read transfer to memory
	1	1	Illegal
	X	If bits 6 and 7 = 11	
4	0	Autoinitialization disable	
	1	Autoinitialization enable	
5	0	Address increment select	
	1	Address decrement select	
6-7	Bit7	Bit6	
	0	0	Demand mode select
	0	1	Single mode select
	1	0	Block mode select
	1	1	Cascade mode select
	IOR* = 0, Illegal		

000C DMA Controller
IOW* = 0, Clear Byte Pointer Flip/Flop
IOR* = 0, Illegal

000D	DMA Controller IOW* = 0, Master Clear IOR* = 0, Read Temporary Register
000E	DMA Controller IOW* = 0, Clear Mask Register IOR* = 0, Illegal
000F	DMA Controller IOW* = 0, Write all Mask Register Bits

Bit	Description
0	0 = Clear channel 0 mask bit (Enable) 1 = Set channel 0 mask bit (Disable)
1	0 = Clear channel 1 mask bit (Enable) 1 = Set channel 1 mask bit (Disable)
2	0 = Clear channel 2 mask bit (Enable) 1 = Set channel 2 mask bit (Disable)
3	0 = Clear channel 3 mask bit (Enable) 1 = Set channel 3 mask bit (Disable)
4-7	Don't care IOR* = Illegal

0010 - 001F	Not Used

Address	Description
0020	8259A Interrupt Controller

Note: Initialization Words are setup by the operating system and are generally not to be changed. Writing an initialization word may cancel pending interrupts.

Bit4 = 1: INITIALIZATION COMMAND WORD 1

```
Bit0 = 0:  ICW4 needed
     = 1:  ICW4 not needed
Bit1 = 0:  Cascade Mode
     = 1:  Single
Bit2 = Not used
Bit3 = 0:  Edge Triggered Mode
     = 1:  Level Triggered Mode
           when the SL bit is active
Bit5 - 7:  Not Used
```

Bit4 = 0 &
Bit3 = 0

OPERATION CONTROL WORD 2

Bit0 - 2: Determine the interrupt level acted on when the SL bit is active

Interrupt Level =	0	1	2	3	4	5	6	7
Bit0 (L0):	0	1	0	1	0	1	0	1
Bit1 (L1):	0	0	1	1	0	0	1	1
Bit2 (L2):	0	0	0	0	1	1	1	1

Bit5 - 7 Control Rotate and End of Interrupt modes

B7	B6	B5		
0	0	1	Non-specific EOI command	End of Interrupt
0	1	1	Specific EOI command	End of Interest
1	0	1	Rotate on non-specific EOI command	Automatic Rotation
1	0	0	Rotate in Automatic EOI Mode (set)	Automatic Rotation
0	0	0	Rotate in Automatic EOI Mode (clear)	Automatic Rotation
1	1	1	*Rotate on Specific EOI command	Specific Rotation
1	1	0	*Set priority command	Specific Rotation
0	1	0	No operation	

*L0 - L2 are used

Bit4 = 0 &
Bit3 = 1

OPERATION CONTROL WORD 3

Bit0 - 1:

Bit1 Bit0- Read Register Command
- 0 0 - No Action
- 0 1 - No Action
- 1 0 - Read IR Register on next IOR* Pulse
- 1 1 - Read IS Register on next IOR* Pulse

Bit2 = 0: No Poll Command
= 1: Poll Command

Bit5 - 6:

Bit6 Bit5- Special Mask Mode
- 0 0 - No Action
- 0 1 - No Action
- 1 0 - Reset Special Mask
- 1 1 - Set Special Mask

Bit7 = 0

0021 8259A Interrupt Controller

```
INITIALIZATION CONTROL WORD 2
Bit0 - 7:  Not Used
Bit3 - 7:  T3 - T7 of Interrupt Vector Address
           (8086/8088 Mode)

INITIALIZATION CONTROL WORD 3 (Master Device)
Bit0 - 7:  =1   Indicated IR input has a slave
           =0   Indicated IR input does not have
                a slave

INITIALIZATION CONTROL WORD 3 (Slave Device)
Bit0 - 2 = IDO - 2
       Bit0 Bit1 Bit2 - Slave ID #
         0    0    0  -     0
         0    0    1  -     1
         0    1    0  -     2
         0    1    1  -     3
         1    0    0  -     4
         1    0    1  -     5
         1    1    0  -     6
         1    1    1  -     7
Bit3 - 7 = 0 (Not Used)

INITIALIZATION CONTROL WORD 4
Bit0:  Type of Processor
  =0   MCS-80/85 Mode
  =1   8086/8088 Mode
Bit1:  Type of End Of Interrupt
  =0   Normal EOI
  =1   Auto EOI
Bit2 - 3:  Buffering Mode
       Bit3 Bit2
         0    X    Non-buffered Mode
         1    0    Buffered Mode/Slave
         1    1    Buffered Mode/Master
Bit4:  Nesting Mode
  =0   Not Special Fully Nested Mode
  =1   Special Fully Nested Mode
Bit5 - 7:  =0 (Not Used)

OPERATION CONTROL WORD 1 (IOR*/IOW*)
Bit0 - 7:  Interrupt Mask for IRQ0 - IRQ7
  =0   Mask Reset (Enable)
  =1   Mask Set (Disable)
```

NOTE: Peripherals Requesting an interrupt service must generate a low to high edge and then remain at a logic high level service, must generate a low to high edge and then remain at a high until service is acknowledged. Failure to do so will result in a Default Service for IRQ7

```
0022-003F          Not Used

Address            Description
0040/0044          8253-5 Timer
                   IOW* = 0:  Load Counter No. 0
                   IOR* = 0:  Read Counter No. 0
0041/0045          8253-5 Timer
                   IOW* = 0:  Load Counter No. 1
                   IOR* = 0:  Read Counter No. 1
Address            Description
0040/0044          8253-5 Timer
                   IOW* = 0:  Load Counter No. 0
                   IOR* = 0:  Read Counter No. 0
0041/0045          8253-5 Timer
                   IOW* = 0:  Load Counter No. 1
                   IOR* = 0:  Read Counter No. 1
0042/0046          8253-5 Timer
                   IOW* = 0:  Load Counter No. 2
                   IOR* = 0:  Read Counter No. 2
0043/0047          8253-5 Timer
                   IOW* = 0:  Write Mode Word
                        Control Word Format
                        Bit0:  BCD
                          = 0:  BCD Counter (4 Decades)
                          = 1:  Binary Counter 16 bits
                        BIT1 - 3:  Mode Selection
                         Bit3 Bit2 Bit1
                          0     0    0     Mode 0
                          0     0    0     Mode 1
                          X     1    0     Mode 2
                          X     1    1     Mode 3
                          1     0    0     Mode 4
                          1     0    1     Mode 5
                        BIT4 - 5:    Read/Load
                         Bit5 Bit4
                          0    0     Counter Latching Operation
                          0    1     Read/Load LSB only
                          1    0     Read/Load MSB only
                          1    1     Read/Load LSB first, then MSB
                        BIT6 - 7:  Select Counter
                         Bit7 Bit6
                          0    0     Select Counter 0
                          0    1     Select Counter 1
                          1    0     Select Counter 2
                          1    1     Illegal
                   IOR* = 0:  No-Operation 3-State
0048-005F          Not Used
```

0060 PORT A / KEYBOARD INTERFACE CONTROL PORTS (READ ONLY)

BIT	Description
0	Keyboard Bit 0-LSB
1	Keyboard Bit 1
2	Keyboard Bit 2
3	Keyboard Bit 3
4	Keyboard Bit 4
5	Keyboard Bit 5
6	Keyboard Bit 6
7	Keyboard Bit 7-MSB

0061 PORT B - READ or WRITE

BIT	Description
0	1 = 8253 Gate #2 Enable
1	1 = Speaker Data Out Enable
2	Not Used
3	Not Used
4	1 = Disable Internal Speaker (Sound Control 2)
5	0 = Sound Control 0
6	0 = Sound Control 1
7	1 = Keyboard Clear

0062 PORT C - READ/WRITE: Bits 0-3; READ ONLY: BITS 4-7

BIT	Description
0	(Output) Not Used
1	(Output) Multi-Data
2	(Output) Multi-Clock
3	(Output) CPU Clock Rate 0 = 4.77 MHz (PC Compatible Rate) 1 = 7.16 MHz (Default by Boot ROM)
4	Video Ram Size 0 = 128K Video 1 = 256K Video
5	8253 Out #2
6	Monochrome Mode 0 = Color Monitor 1 = 350 Line Monitor, Mono
7	0 = Reserved

0063-007F Not Used

Address	Description
0080	DMA Page Reg. (Not Used)

0081	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 2 Address A16
Bit 1	DMA Ch 2 Address A17
Bit 2	DMA Ch 2 Address A18
Bit 3	DMA Ch 2 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0082	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 3 Address A16
Bit 1	DMA Ch 3 Address A17
Bit 2	DMA Ch 3 Address A18
Bit 3	DMA Ch 3 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0083	WRITE ONLY
Address	**Description**
Bit 0	DMA Ch 0 - 1 Address A16
Bit 1	DMA Ch 0 - 1 Address A17
Bit 2	DMA Ch 0 - 1 Address A18
Bit 3	DMA Ch 0 - 1 Address A19
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

0084-008F	Not Used

00A0-00A7	NMI Mask Register, Write only
Bit	**Description**
0	External Video 0 = Normal Operation 1 = All Video Addresses and Ports are Disabled
1	MEMCONFIG 1 - A17 128K SW
2	MEMCONFIG 2 - A18 256K SW
3	MEMCONFIG 3 - A19 512K SW
4	"1" Enable 256K of Video RAM
5	Not Used
6	Not Used
7	1 = Enable NMI 0 = Disabled

BIT 4 256K Enable	BIT 3	BIT 2	BIT 1	MEMORY START	MEMORY LENGTH	MEMORY RANGE
0	0	0	0	0 0000	128K	0 0000-1 FFFF
0	0	0	1	2 0000	128K	2 0000-3 FFFF
0	0	1	0	4 0000	128K	4 0000-5 FFFF
0	0	1	1	6 0000	128K	6 0000-7 FFFF
0	1	0	0	8 0000	128K	8 0000-9 FFFF
1	0	0	1	0 0000	256K	0 0000-3 FFFF
1	0	1	0	2 0000	256K	2 0000-5 FFFF
1	0	1	0	4 0000	256K	4 0000-7 FFFF
1	1	0	0	6 0000	256K	6 0000-9 FFFF

NOTE: To turn off on-board video, be sure Port AOH, Data Bit 0 is a "1" AND Video Array Register 3 (Selected by writing 03 into 3DAH) Data Bit 0 (Write to Port 3DEH) must be = "0" to disable 3B8H and 3BAH.

00A8 - 00AF Not Used

Address	Description
00C0-00C7	Sound SN76496

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
= 1	0	0	0	F6	F7	F8	F9	Update Tone Frequency 1
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	0	1	A0	A1	A2	A3	Update Tone Attenuation 1
= 1	0	1	0	F6	F7	F8	F9	Update Tone Frequency 2
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	0	1	1	A0	A1	A2	A3	Update Tone Attenuation 2
= 1	1	0	0	F6	F7	F8	F9	Update Tone Frequency 3
= 0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
= 1	1	0	1	A0	A1	A2	A3	Update Tone Attenuation 3
= 1	1	1	0	X	FB	NFO	NFI	Update Noise Control
= 1	1	1	1	A0	A1	A2	A3	Update Noise Attenuation

00C8-00DF Not Used
00E0-01FF Reserved
WRITE (IOW*)
0200 - 0207 Joystick
Clear (Resets Integrator to Zero)
0208 - 020F Not Used

0201 READ R = Right Joystick, L = Left Joystick

Bit	Description
0	R - X Horizontal Position
1	R - Y Vertical Position
2	L - X Horizontal Position
3	L - Y Vertical Position
4	R Button #1 (Logic 0 = Button Depressed)
5	R Button #2 (Logic 0 = Button Depressed)
6	L Button #1 (Logic 0 = Button Depressed)
7	L Button #2 (Logic 0 = Button Depressed)

Addresses

0370 - 0377 Not Used

0378 Printer - Data Latch

Bit	Description
0	Data Bit 0 - LSB
1	Data Bit 1 -
2	Data Bit 2 -
3	Data Bit 3 -
4	Data Bit 4 -
5	Data Bit 5 -
6	Data Bit 6 -
7	Data Bit 7 - MSB

0379 Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	0 = Error
4	1 = Printer Select
5	0 = End of Form
6	0 = Acknowledge
7	0 = Busy

037A (037E) Printer - Control Latch

Bit	Description
0	0 = Strobe
1	0 = Auto FD XT
2	0 = Initialize
3	0 = Select Printer
4	1 = Enable Interrupt
5	0 = Enable Output Data
6	Not Used
7	Not Used

037B	Not Used
037C	Printer - Data Latch
037D	Printer - Read Status
037F - 03D3	Not Used
03D4	6845 Address Register
03D5	6845 Data Register
03D6	Not Used
03D7	Not Used
03D8	Mode Select Register
Bit 0	High Resolution Clock =0: Selects 40 by 25 Alphanumeric Mode =1: Selects 80 by 25 Alphanumeric Mode
Bit 1	Graphics Select =0: Selects Alphanumeric Mode =1: Selects 320 by 200 Graphics Mode
Bit 2	Black and White =0: Selects Color Mode =1: Selects Black and White Mode
Bit 3	Video Enable =0: Disables Video Signal =1: Enables Video Signal
Bit 4	640 Dot Graphics =0: Disables 640 by 200 B&W Graphics Mode =1: Enables 640 by 200 B&W Graphics Mode
Bit 5	Blink Enable =0: Disables Blinking =1: Enables Blinking
03D9	Color Select Register
Bit 0	Background Blue
Bit 1	Background Green
Bit 2	Background Red
Bit 3	Background Intensity
Bit 4	Foreground Intensity
Bit 5	Color Select
03DA, 03DE	Write Video Array Address & Read Status (3DA) Write Video Array Data (3DE)

READ (3DA)		WRITE (3DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
02 Bit 5		Reserved = 0
03 Bit 0		Mono Enable = "1"
03 Bit 1		Reserved = 0
03 Bit 2		Border Enable
03 Bit 3		4-Color High Resolution
03 Bit 4		16 Color Mode
03 Bit 5		Extra Video Mode
10-1F Bit 0		Palette Blue
10-1F Bit 1		Palette Green
10-1F Bit 2		Palette Red
10-1F Bit 3		Palette Intensity
Bits 4 - 7		Not Used

03DB Clear Light Pen Latch (Not Used on Tandy 1000 EX)
03DC Preset Light Pen Latch (Not Used on Tandy 1000 EX)

03DD Extended Ram Page Register - CPU Relative

Bit	Description
0	Extended Addressing Modes
1	Not Used
2	Not Used
3	CRT Video Page Address "17"
4	CRT Video Page Address "18"
5	CPU Page Address "17"
6	CPU Page Address "18"
7	Select 64K or 256K Ram

```
03DF                CRT Processor Page Register - Video Mem Relative
 Bit 0              A14                 CRT Page 0
 Bit 1              A15                 CRT Page 1
 Bit 2              A16                 CRT Page 2
 Bit 3              A14                 Processor Page 0
 Bit 4              A15                 Processor Page 1
 Bit 5              A16                 Processor Page 2
 Bit 6                                  Video Address Mode 0
 Bit 7                                  Video Address Mode 1

03F1                Drive Select Switch
                    "1" DSO = DSO
                    "0" DSO = DS1
03F2, 3F0, 3F3      DOR Register (Write Only)
                    Bit0 - 1:  Drive Select
                      Bit1 Bit0
                       0    0          Drive Select A*
                       0    1          Drive Select B*
                    Bit2:  0 = FDC Reset
                    Bit3:  1 = Enable DMA Req/Interrupt
                    Bit4:  1 = Drive A Motor On
                    Bit5:  1 = Drive B Motor On
                    Bit6:  1 = FDC Terminal Count
                    Bit7:  Not Used

03F4, 3F6           FDC - Status (Read Only) - See FDC Specification
03F5, 3F7           FDC - Data (R/W) - See FDC Specification
03F8 - 03FF         Not Used

For Ports 3F0 - 3F7, the following general conditions apply:
                    A1 = Don't Care
                    For DOR, A2 = 0
                    For FDC, A2 = 1
```

Main Logic T1000 SX Subassembly		8859003A
Main Logic T1000 SX PCB Rev. A		8709699A
C1-16,18,19,21-23, 25,26,28-32,29A, 30A,34,35,37,37A, 39-45,47,48,50-57,124,126,128, 134,143,144,146, 147,149,150,178, 180	Capacitor 0.1 MFD 50V Axial	8374104
C100,119,120,145, 148,151,157, 181	Capacitor 22 MFD 16V Elec Axial	8316221
C101,117,125,137-	Capacitor 1000 PFD C. Disk	8301474
C102-109	Capacitor 68 PFD 50V C. Disk	8300684
C110	Capacitor .01 MFD 50V. C. Disc El.	8303104
C111-116,152-154, 159-161,168	Capacitor 20 PFD 50V +80-20% Disk	8300204
C118	Capacitor .022 MFD 63V 10% Poly	8393225
C121,129,135,175, 179	Capacitor 10 MFD 16V Elec Axial	8316101
C122,130	Capacitor 100 MFD 16V Elec Axial	8317101
C123	Capacitor 330 PFD 50V C. Disk	8301332
C127	Capacitor 100 PF 50V C. Disk	8301104
C131,132,136,176	Capacitor .47 MFD 50V Mono. Rad.	8384475
C133	Capacitor 180 PF 50V C. Disk	8301184
C155,156,162-167	Capacitor 2200 PFD C. Disk U51 Between Pins 15 & 26	8302224
C157A	Capacitor .001 MFD C. Disk	8382104
C169-174,177	Capacitor 470 PFD 50V C. Disk	8301474
C176	Capacitor .47 MFD 50V Mono. Rad.	8384475
CR1	Diode 1N5235 6.8V	8150235
CR2	Diode 1N4148	8150148
E1-6	Staking Pins	8529014
FB1-4	Ferrite Bead	8419013
J1	Connector, 2-Pin Stra. Header	8519193
J2,3	Connector, 6-Pin Rt. Angle	8519289
J4	Connector, 8-Pin Rt. Angle	8519288
J5	Connector, Dual 17-Pin Str.Header	8519120
J6	Connector, 9-Pin St. Friction Lock	8519191

J8	Connector, 9-Pin Rt. Angle Male "D" Sub	8519235
J9	Connector, 9-Pin Rt. Angle Female Female "D" Sub	8519245
J10	Connector, Dual RCA Pho. Jack Rt. Angle	8519213
J11-15	Connector, Dual 31-Pin Str. Card Edge	8519236
Q1	Transistor 2N3906	8100906
Q2	Transistor VN0104N3	8190104
Q3	Transistor 2N3904	8110904
R1-4,22-24,27-29, 34,35,38,53	Resistor 10K Ohm 1/4 Watt 5%	8207310
R6,61	Resistor 680 Ohm 1/4 Watt 5%	8207168
R7	Resistor 2.7K Ohm 1/4 Watt 5%	8207227
R8-11	Resistor 1 Meg Ohm 1/4 Watt 5%	8207510
R12	Resistor 680K Ohm 1/4 Watt 5%	8207468
R13	Resistor 82.5K Ohm 1/4 Watt 1%	8200382
R14	Resistor 560 Ohm 1/4 Watt 5%	8207156
R15,17,25,26,39, 50-52	Resistor 4.7K Ohm 1/4 Watt 5%	8207247
R16	Resistor 330 Ohm 1/4 Watt 5%	8207133
R18,19	Resistor 100K Ohm 1/4 Watt 5%	8207410
R20,33,36,37,41-43, 48,54-56,63	Resistor 33 Ohm 1/4 Watt 5%	8207033
R21,45,47,49,57,67	Resistor 2.2K Ohm 1/4 Watt 5%	8207222
R26A	Resistor Variable 1K	8279411
R30,31	Resistor 10 Ohm 1/4 Watt 5%	8207010
R32	Resistor 3.9K Ohm 1/4 Watt 5%	8207239
R40	Resistor 1K Ohm 1/4 Watt 5%	8207210
R44,46	Resistor 47 Ohm 1/4 Watt 5%	8207047
R51	Resistor 470K Ohm 1/4 Watt 5%	8207447
R58	Resistor 750 Ohm 1/4 Watt 5%	8207175
R59	Resistor 1.1K Ohm 1/4 Watt 5%	8207211
R60	Resistor 1.2K Ohm 1/4 Watt 5%	8207212
R62	Resistor 3.3K Ohm 1/4 Watt 5%	8207233
R64	Resistor 620 Ohm 1/4 Watt 5%	8207162
R65	Resistor 270 Ohm 1/4 Watt 5%	8207127
R66	Resistor 75 Ohm 1/4 Watt 5%	8207075
RP1	Resistor Pak 1K Ohm 6-Pin SIP 5R	8290210
RP2	Resistor Pak 10K Ohm 6-Pin SIP 5R	8290032
RP3	Resistor Pak 10K Ohm 8-Pin SIP 7R	8292310
RP4-9	Resistor Pak 33 Ohm 8-Pin SIP 4R	8295033
RP10	Resistor Pak 150 Ohm 8-Pin SIP 7R	8290016
RP11	Resistor Pak 4.7K Ohm 8-Pin SIP 7R	8292246
RP12	Resistor Pak 33 Ohm 16-Pin DP 8R	8290044
RP13	Resistor Pak 10K Ohm 10-Pin SIP 9R	8290010

S1	Switch, reset	8489065
S2	Switch, 4-Pos. DIP	8489090
U1-4,9-12	IC 256K Dram	8049008
U1-16,37A	Socket 16-Pin DIP	8509003
U17	IC LM 339	8050339
U18	IC PLS153	8
U18,40,52	Socket 20-Pin DIP	8509009
U19	IC 74HCT138	8026138
U20	IC 74HCT32	8026032
U21,54,56,57	IC 74LS244	8020244
U22	IC Custom Keyoard I/F Array	8075069
U22,33,36,37,51,55	Socket 40-Pin DIP	8509002
U23	IC 8253-5 Timer	8040253
U23	Socket 24-Pin DIP	8509001
U24,31,34,35	IC 64K X 4 Dram	8040464
U24,31,34,35	Socket 18-Pin DIP	8509006
U25	IC 14529	8030529
U26	IC LM358	8050358
U27	IC LM386	8050386
U28,47	IC 74HCT04	8026004
U29	IC DMA Custom	8075711
U29	Socket 68-Pin, PLCC	8509020
U30	IC Big Blue (Video/Mem)	8040684
U30	Socket 84-Pin PLCC	8509031
U36	IC 8088 8 MHz	8041088
U37	IC UPD765A	8040272
U37A	IC SN76496 Tone Generator	8040496
U38	IC FDC9216	8040216
U38	Socket 8-Pin DIP	8509011
U39,*40,*52	IC 74LS245 (U52 Socketed)	8020245
U41	IC 128K ROM	8040328
U41,44	Socket 28-Pin DIP	8509007
U42,43	IC 74LS373	8020373
U44	IC 8259A	8040259
U45	Socket 14-Pin DIP	8509008
U45	IC 74HCT14 Socketed	8026014
U46	IC 74HCT08	8026008
U48	IC 7416	8000016
U49	IC 7417	8000017
U50	IC 74HCT195	8026195
U51	IC CPU Support (Lt. Blue)	8075306
U53	IC 74HCT02	8026002
U55	IC Parallel Port Array	8075068
VR1	Regulator 78L05	8052805
VR2	Regulator 79MO5CT	8190005

Y1	Oscillator 28.63636 MHz 50 PPM	8409039
Y2	Oscillator 16 MHz	8409034

*U40 & U52 Socketed

CHASSIS SUBASSEMBLY

QUANTITY	DESCRIPTION	NUMBER
11	Bi-Mount	8
1	Cable - Ground	8
1	Cable - Speaker 4.50" long	8709574
1	Chassis - Main	8729581
1	Clamp	8
1	Faston - Male .250"	8529018
4	Foot - Chassis (Adhesive Back)	8
3	Jumper Plug	8519098
2	Nut - Jack	8589070
5	Panel - Slot Cover	8729312
1	PC Board - Proj. 682	8709699
2	Rivit - 1/8" Dia.	8
5	Screw #4-40 X 1/4" Zinc	8569254
9	Screw #6-32 X 1/4"	8569258
2	Screw #6-32 X 1/4"	8
1	Screw #6-32 X 5/16" PPH	8569266
1	Shield - Main Logic Bd.	8
1	Shield - Side	8
1	Shield - Top	8
1	Speaker	8490010

DISK DRIVE SUBASSEMBLY

1	Cable - Signal Floppy	8709673
1	Clamp	8
2	Disk Drive - 5 1/4"	8790132
2	Rivit - 1/8" Dia.	8
5	Screw - #6-32 X 1/4"	8569258
6	Screw - M 3X5X6 MM PPH	8569293
4	Screw - #4-40 X 1/4", Nylon	8
1	Support - Disk Drive	8729582

KEYBOARD SUBASSEMBLY

1	Cable - Keyboard 11.5"	8709567
1	Case - Bottom	8719335
1	Case - top	8719334
2	Guide - center	8719371
1	Guide - left	8719373
1	Guide - right	8719372
1	Keyboard 640	8790056
2	Pad - Friction	8591004
9	Screw - #6 X 7/16"	8569229
4	Spring	8739015
2	Support - Legs	8719336

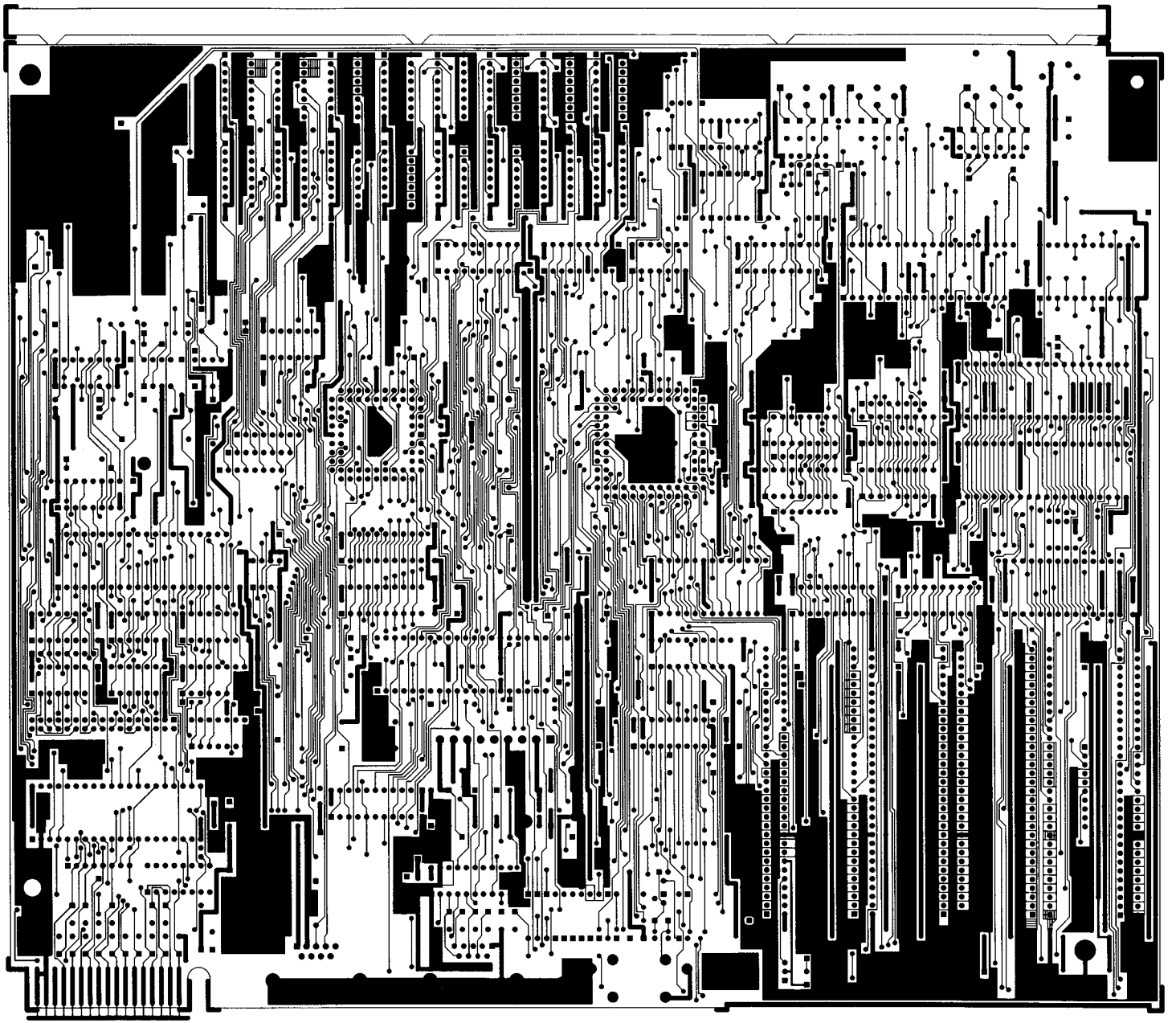
POWER SUPPLY ASSEMBLY

QUANTITY	DESCRIPTION	NUMBER
1	Assy - Switch, Voltage Select	8
1	Cable - DC Power	8709558
1	Cable - Ground Wire	8709674
1	Clip - Plastic W/AD	8559010
1	Enclosure - Power Supply	8729583
1	Fan - 80MM; 12VDC	8
1	Harness - AC Power	8790424
1	Nut - #6 KEPS	8579004
1	Plug - Receptical	8519246
1	Power - Supply 65 W/	8
4	Screw - #6-32 X 1/4" Zinc	8569258
4	Screw - "10 Tapit Thread Form. P. Washer Hex Head	8569303
1	Switch Plate	8729584
1	Switch - Power	8
1	Toroid Core	8419030
1	Tubing - Insulated 3/4"	8539065

FINAL ASSEMBLY

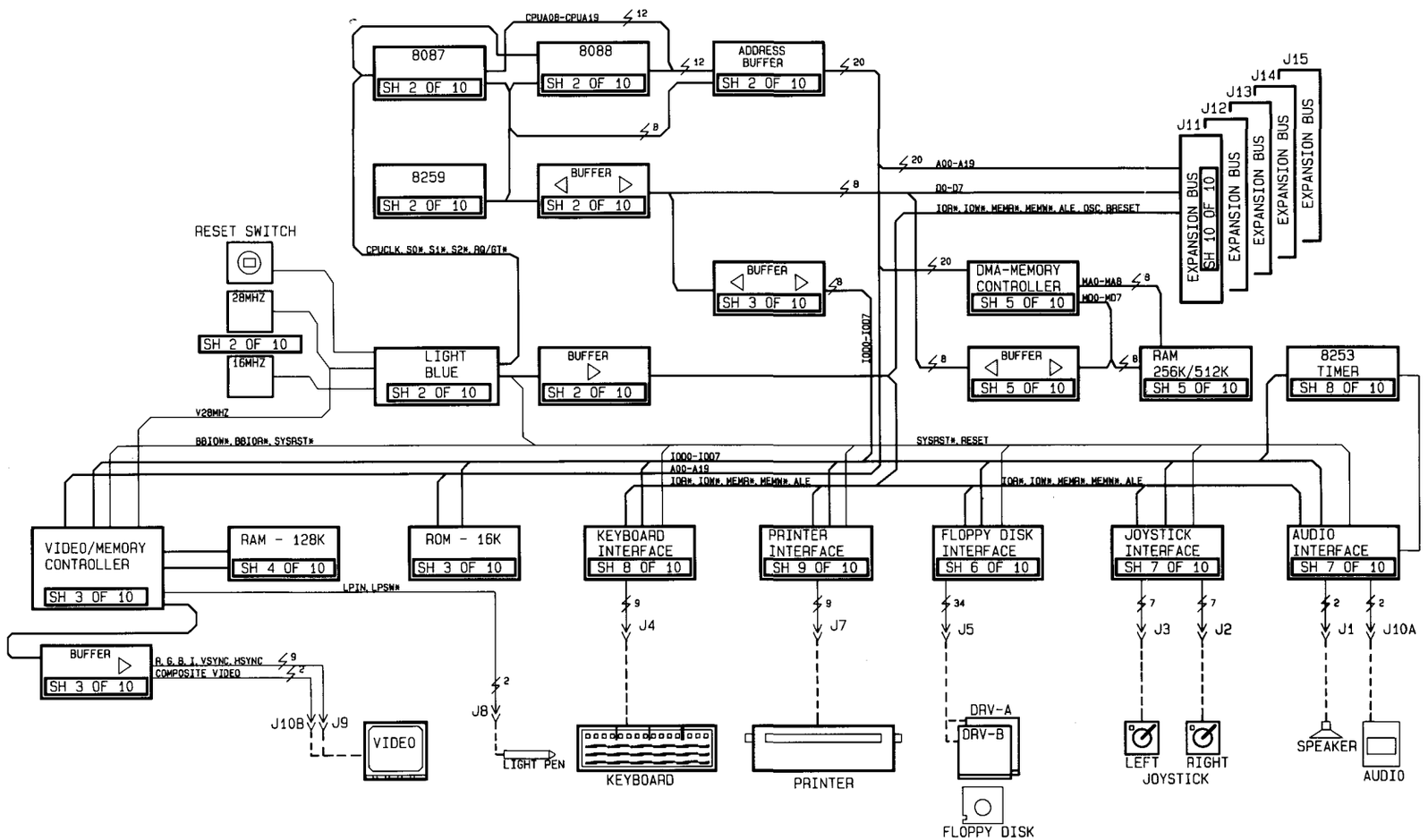
1	Button - Reset Front	8719440
1	Button - Reset Rear	8719441
1	Button - Spring Reset	8739018
1	Case - Top	8719527
3	Card - Function Key	87891012
1	Cord - Power 18/3 60/C	8709584
1	Insert - Accessory	8779227
1	Panel - Rear	8719526
4	Screw -#6-32 X 1/4"	8569258
2	Screw -#8-32 X 5/8" PPH	8569256

TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD- 262-
PROJECT NO.: 682 DATE: 06/03/86	
TITLE: MAIN LOGIC PCB	
DWG NO.: 1700937 REV. A	
PART NO.: 8709699	LAYER 1 COMPONENT SIDE
DESIGN GRID: x=.025 y=.025	
DESIGNER: DD	
INSP	



TANDY SYSTEMS DESIGN ELMWOOD	LAB. SPEC.: TSD- 585-
PROJECT NO.: 685 DATE: 06\03\89	
TITLE: MAIN LOGIC PCB	
DWG. NO.: I\D033\ REV.A	
PART NO.: 8\D8685	
DESIGNER GRID: *=.050 +=.050	LAYER 2 SOLDER SIDE
DESIGNER: DD	
1985	

REVISION				
ZONE	LETTER	DESCRIPTION	DATE	APPROVED
	A	RELEASED FOR PRODUCTION	7/1/86	



2. ALL RESISTORS ARE IN OHMS, 1/4 W, ± 5%.
1. CAPACITORS ARE 0.1uf.

NOTE: (UNLESS OTHERWISE SPECIFIED)

BLOCK DIAGRAM

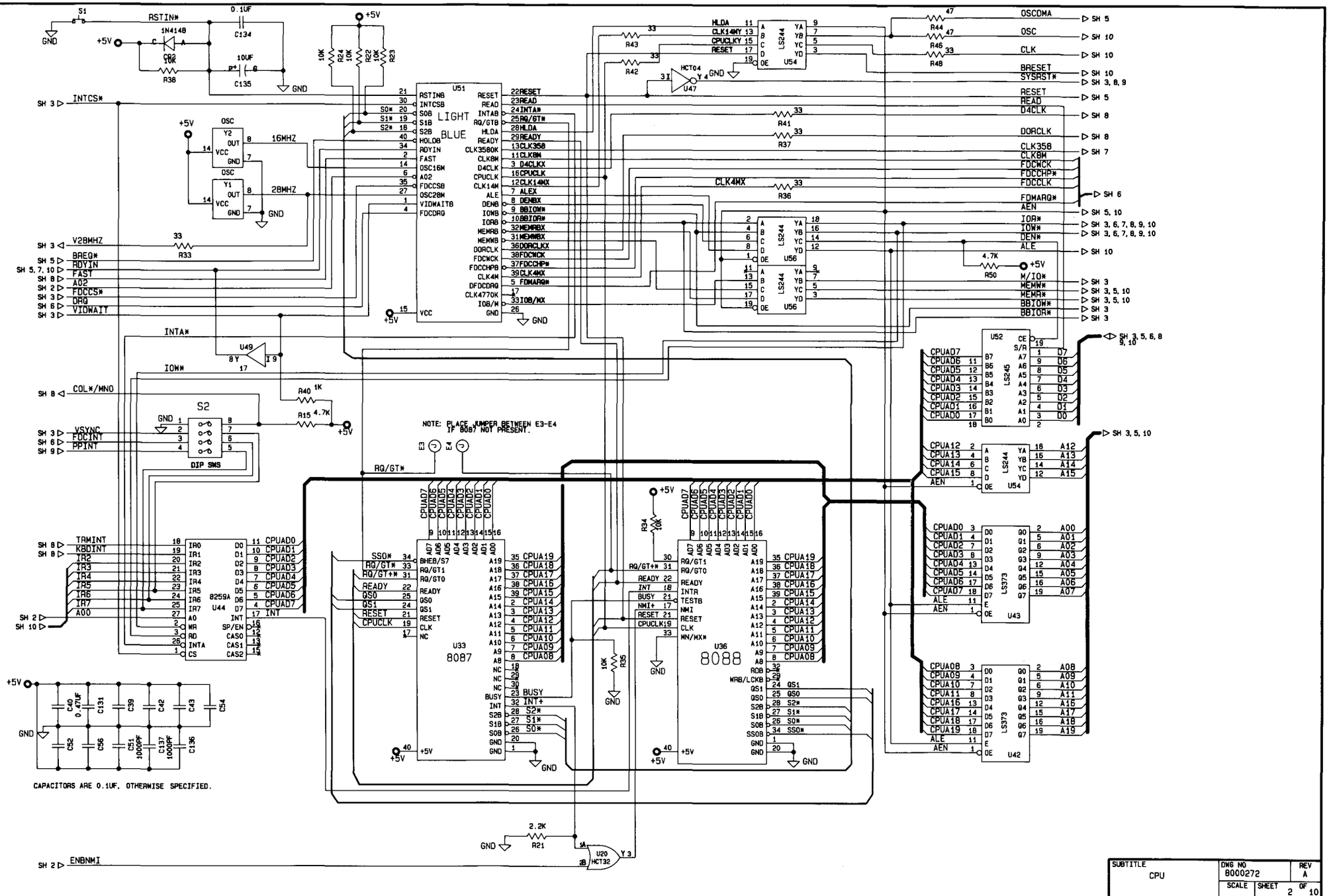
DRAFT	JOHANNES S.	DATE	06-23-86
CHECK		DATE	
DESIGN		DATE	
APPD		DATE	
APPD		DATE	7/2/86

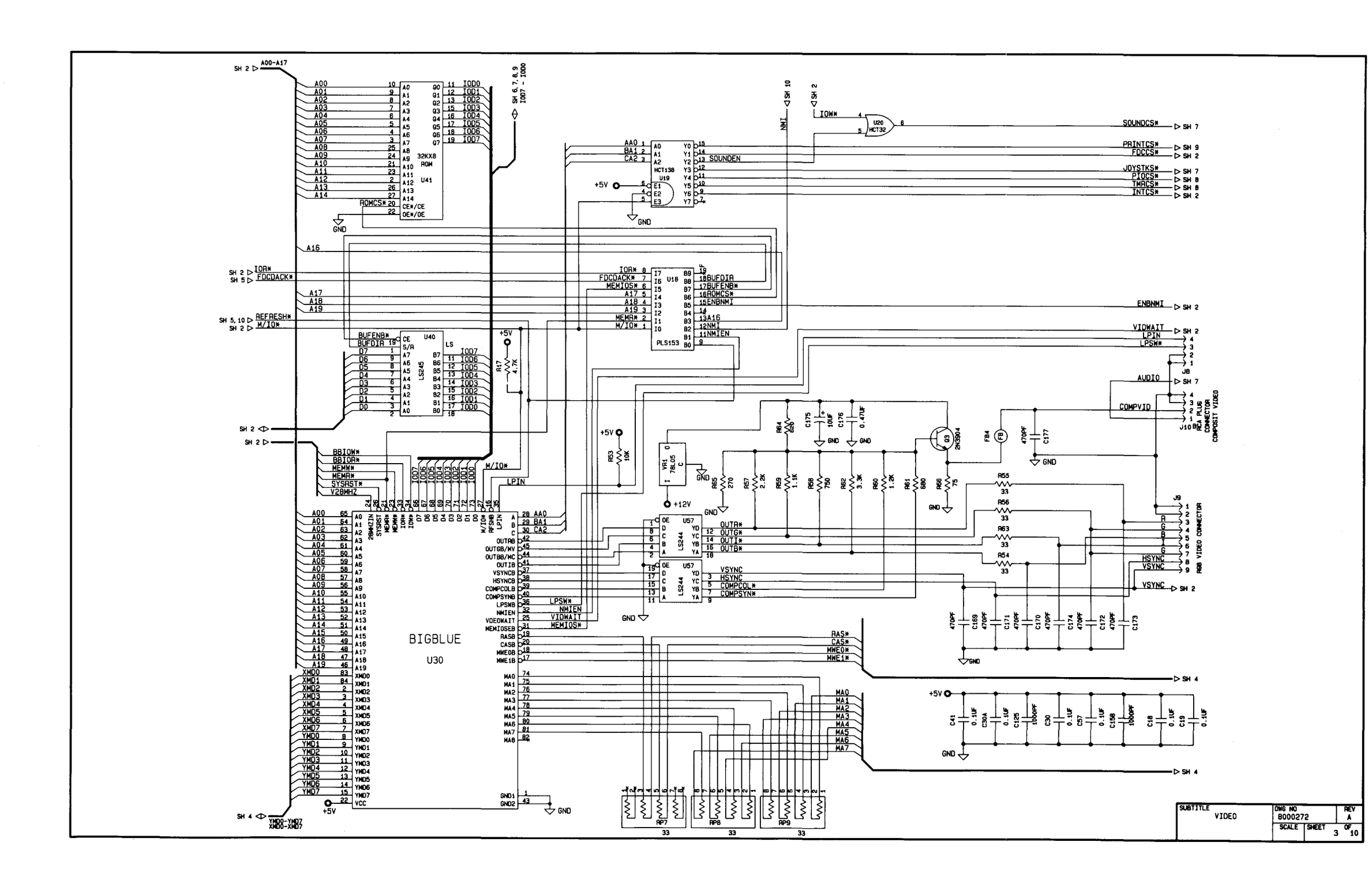
TITLE: SCHEMATIC- MAIN LOGIC BOARD TANDY 1000SX

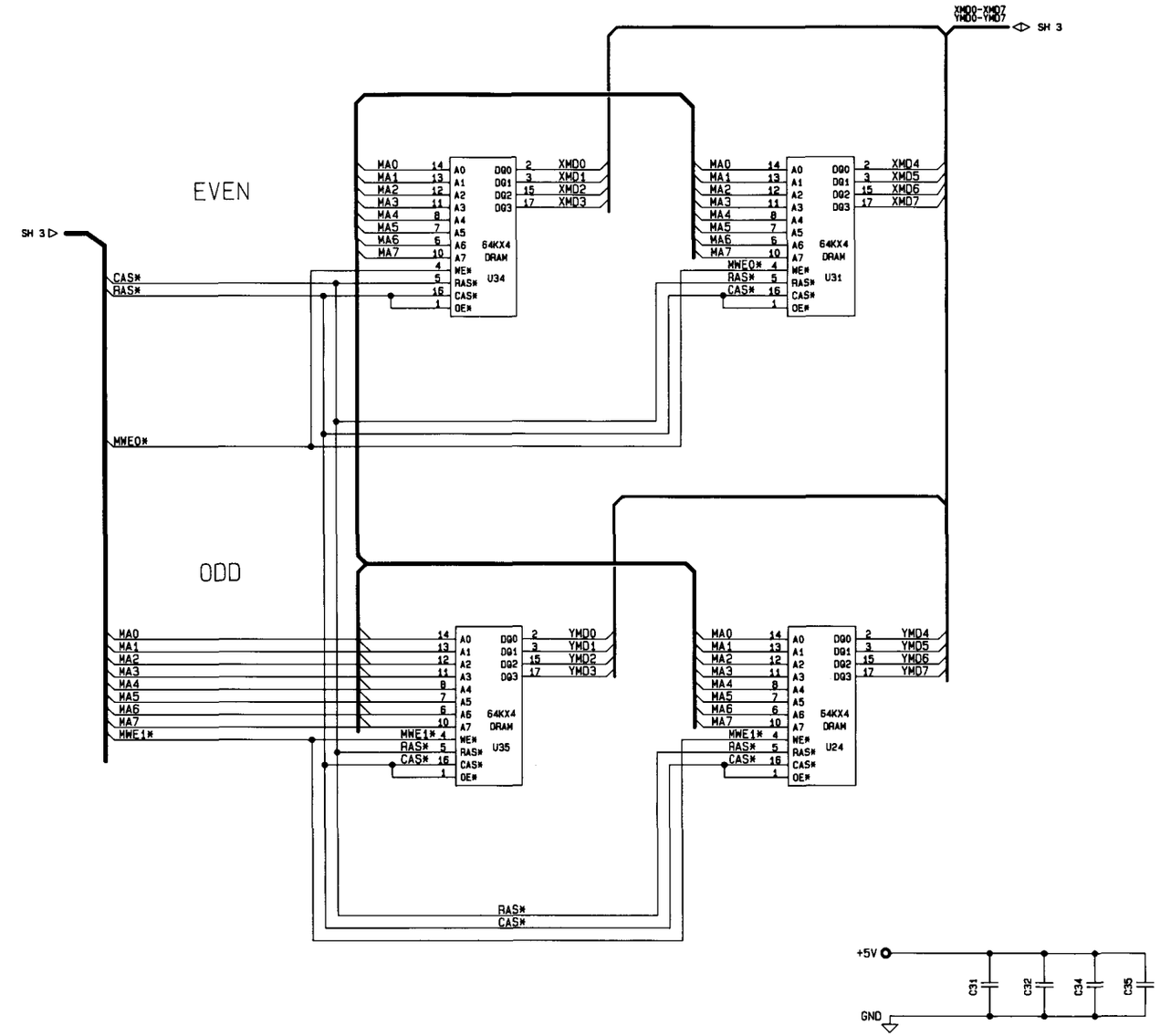
PROJ 682
USED ON

TANDY

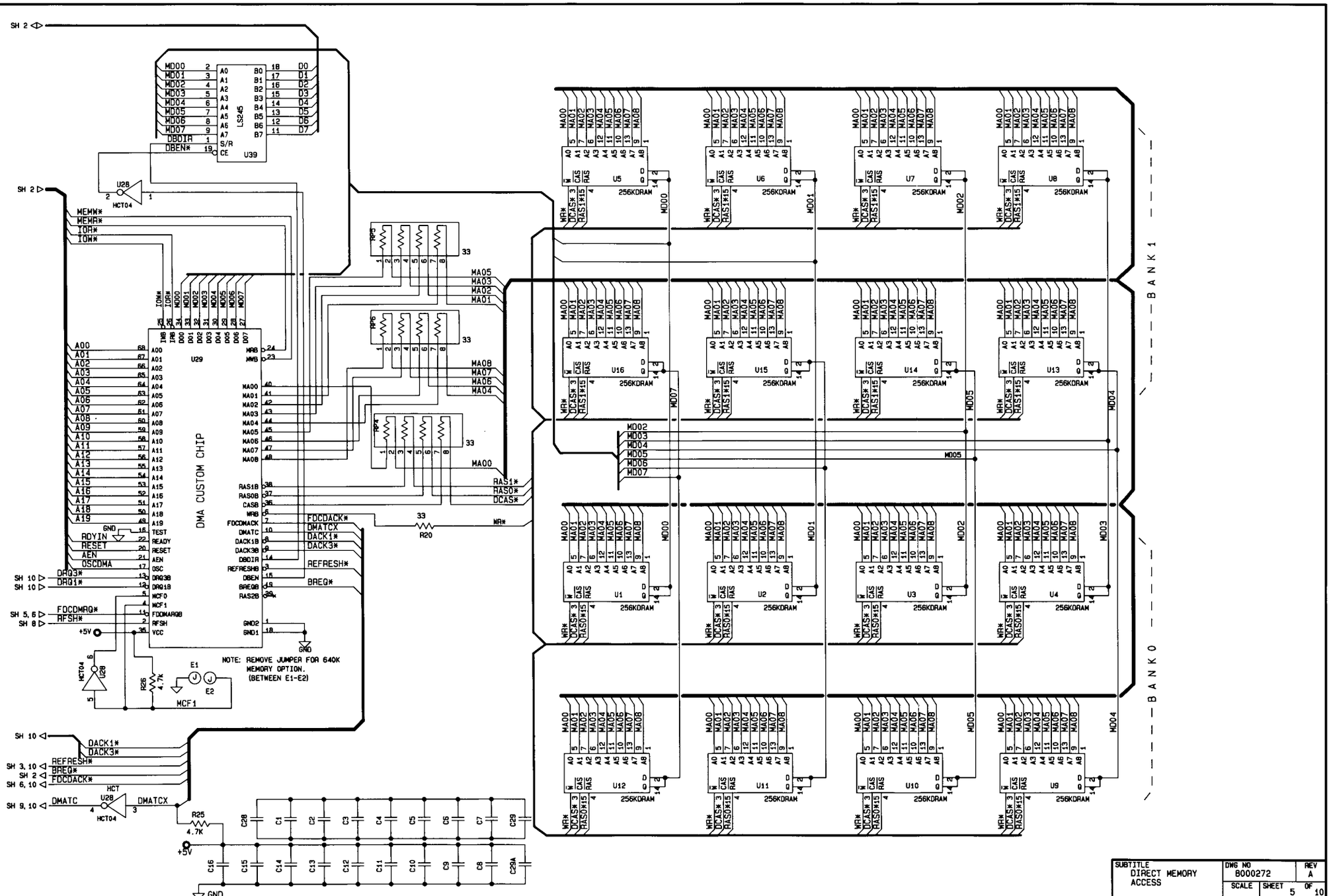
DWG NO: D- 8000272 REV: A
SCALE: SHEET 1 OF 10

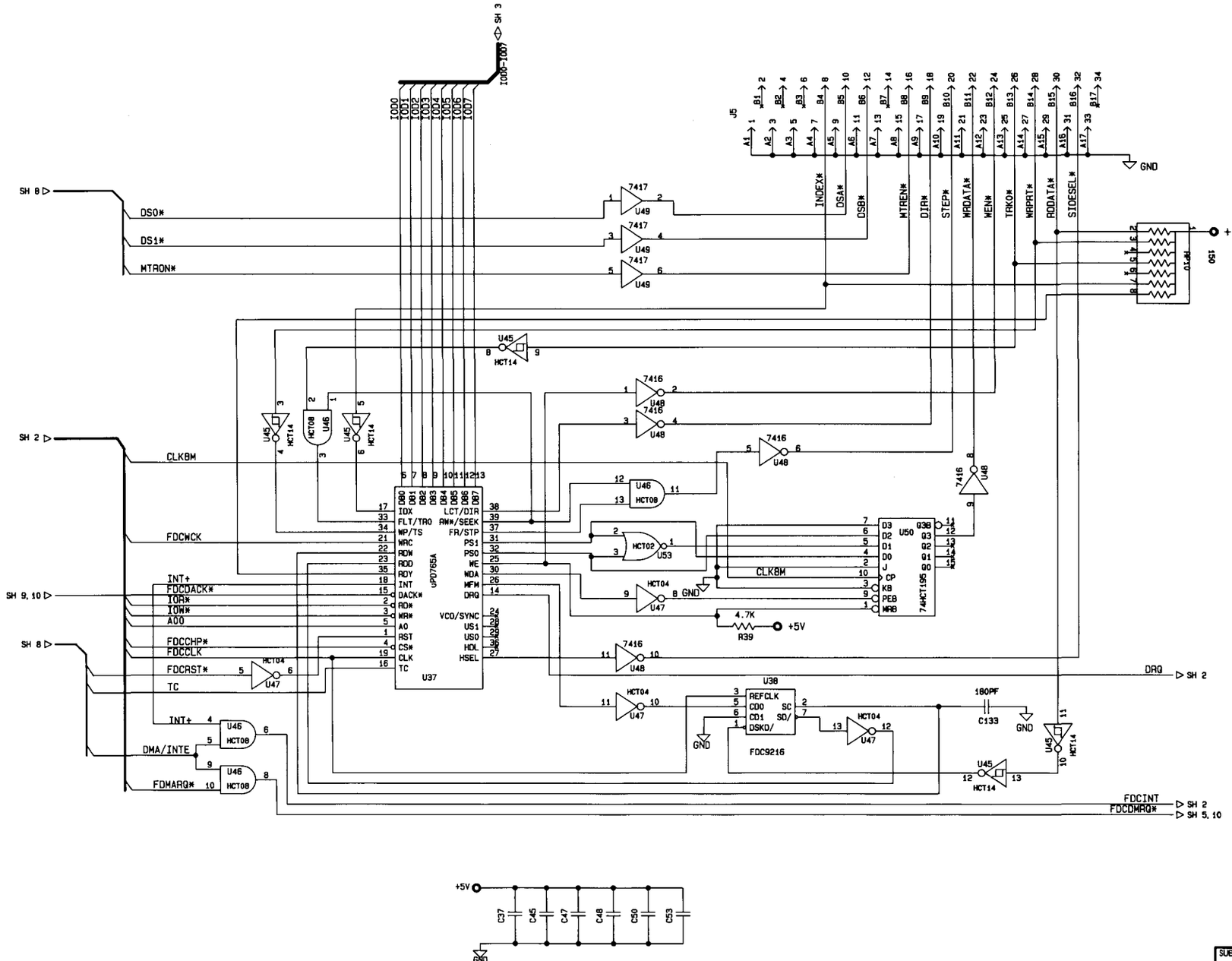

RSTIN*
0.1UF
C134
1N4148
10UF
C135
R38
10K
R24
R22
R23
U51
LIGHT BLUE
RESET
READ
INTA*
RQ/GT*
HLDA
READY
CLK3580K
CLK8M
D4CLK
CPUCLK
CLK14M
ALE
DEN*
IOB
IOR*
MEMR*
MEMW*
DORCLK
FDCWCK
FDCCHP*
CLK4M
FDMARQ*
CLK4770K
IO8/M
INTCS*
V28MHZ
BREQ*
RDYIN
FAST
A02
FDCCS*
DRQ
VIDWAIT
16MHZ
28MHZ
U49
U47
HCT04
U54
U56
LS244
LS245
CLK4MX
OSCDMA
OSC
CLK
BRESET
SYSRST*
RESET
READ
D4CLK
DORCLK
CLK358
CLK8M
FDCWCK
FDCCHP*
FDCCLK
FDMARQ*
AEN
IOR*
IOW*
DEN*
ALE
M/IO*
MEMW*
MEMR*
BBIOW*
BBIOR*
U52
U43
U42
LS373
S2
DIP SWS
TRMINT
KBDINT
IR2
IR3
IR4
IR5
IR6
IR7
A00
8259A
U44
U33
8087
U36
8088
NOTE: PLACE JUMPER BETWEEN E3-E4 IF 8087 NOT PRESENT.
E3
E4
CAPACITORS ARE 0.1UF, OTHERWISE SPECIFIED.
2.2K
R21
U20
HCT32
ENBNMI
SUBTITLE
CPU
DWG NO
8000272
REV
A
SCALE
SHEET
2
OF
10


BIGBLUE
U30
32KX8 ROM
U41
LS245
U40
PLS153
U18
HCT138
U19
HCT32
U20
LS244
U57
78L05
VR1
2N3904
Q3
SOUNDCS*
PRINTCS*
FDCCS*
JOYSTKS*
PIOCS*
TMRCS*
INTCS*
ENBNMI
VIDWAIT
LPIN
LPSW*
AUDIO
COMPVID
J8
J10
RCA PLUG
COMPOSIT VIDEO
J9
RGB VIDEO CONNECTOR
HSYNC
VSYNC
RAS*
CAS*
MWE0*
MWE1*
SUBTITLE
VIDEO
DWG NO
B000272
REV
A
SCALE
SHEET
3
OF
10

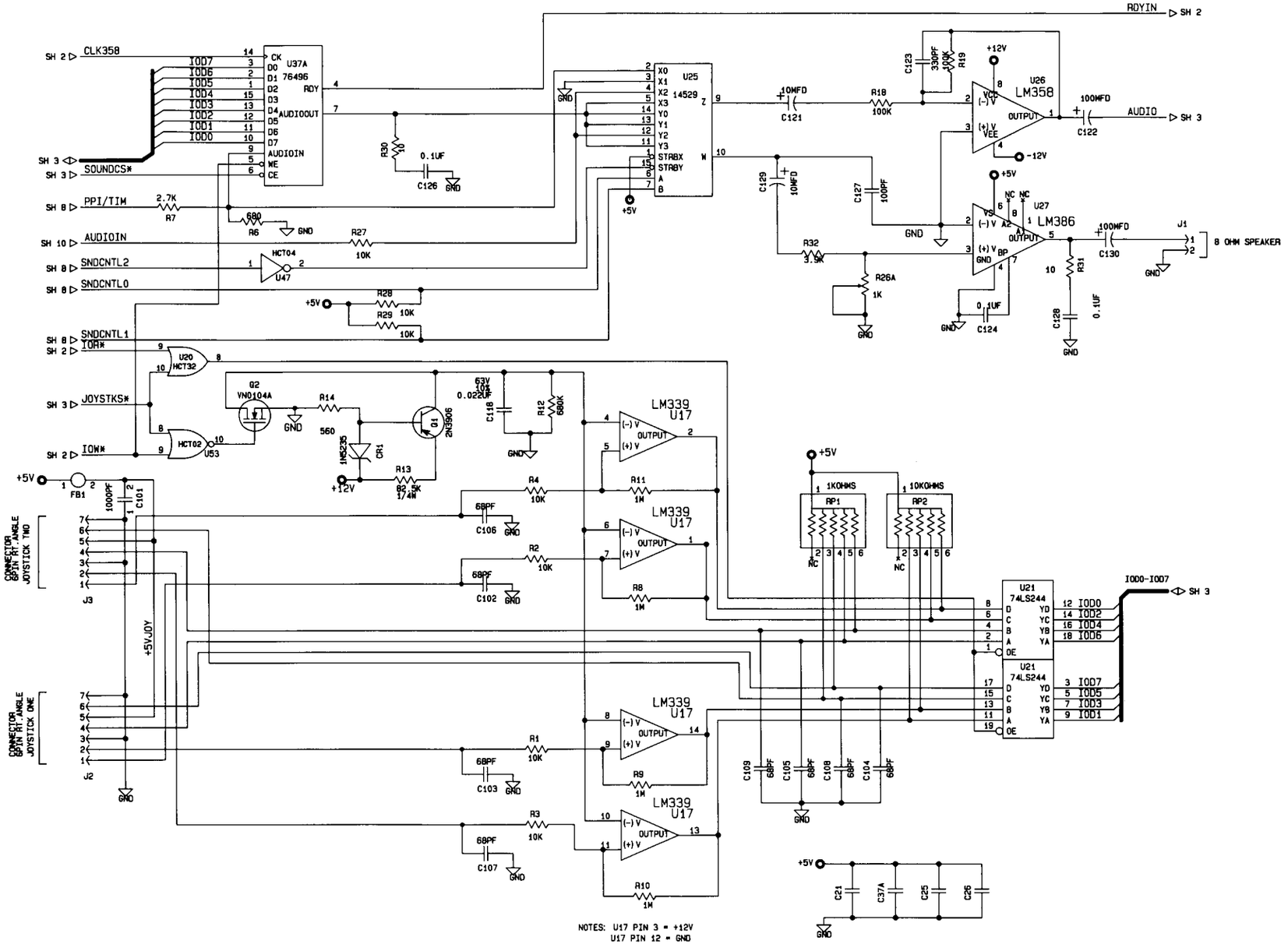


SUBTITLE: VIDEO MEMORY	DWG NO: 8000272	REV: A
	SCALE	SHEET: 4 OF 10

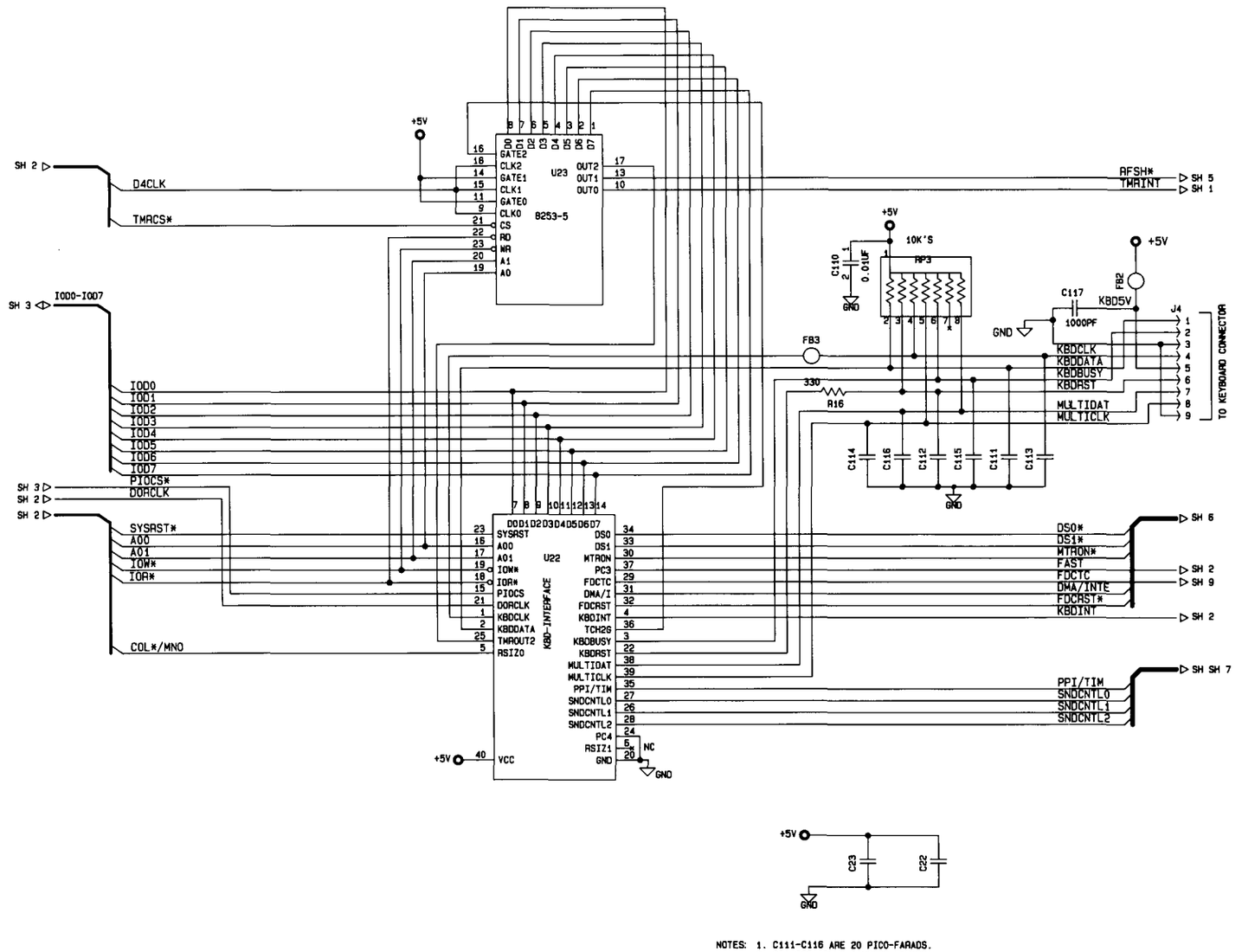

DMA CUSTOM CHIP
U29
LS245
U39
256KDRAM
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
HCT04
U26
U28
BANK 0
BANK 1
NOTE: REMOVE JUMPER FOR 640K MEMORY OPTION. (BETWEEN E1-E2)
MCF1
R20
R25
R26
4.7K
33
+5V
GND
SUBTITLE
DIRECT MEMORY ACCESS
DWG NO
B000272
REV
A
SCALE
SHEET
5
OF
10



SUBTITLE: FLOPPY DISK CONTROLLER	DWG NO: B000272		REV: A
	SCALE	SHEET: 6	OF: 10

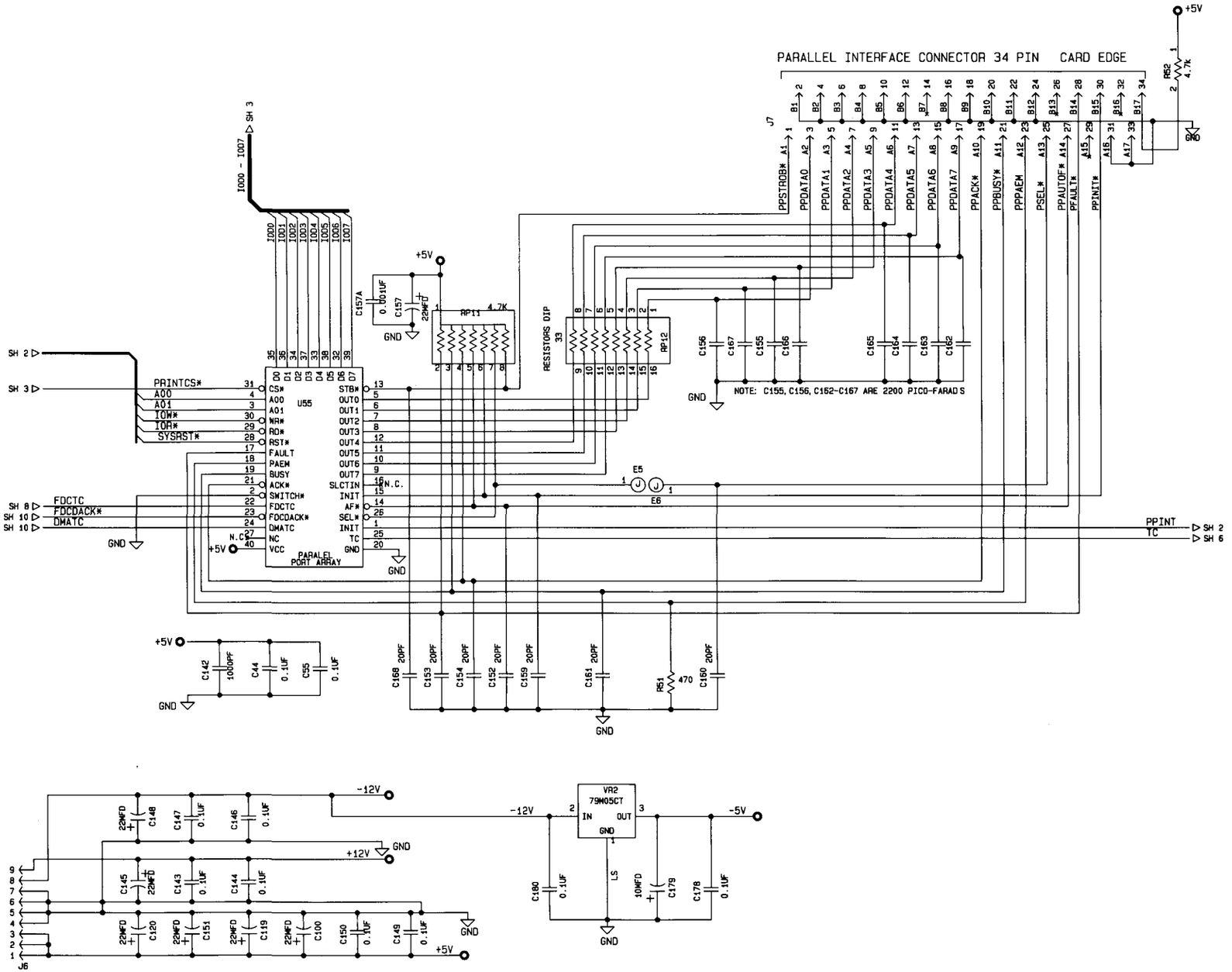


SUBTITLE AUDIO-JOYSTICK	DWG NO 8000272	REV A	
	SCALE	SHEET 7	OF 10

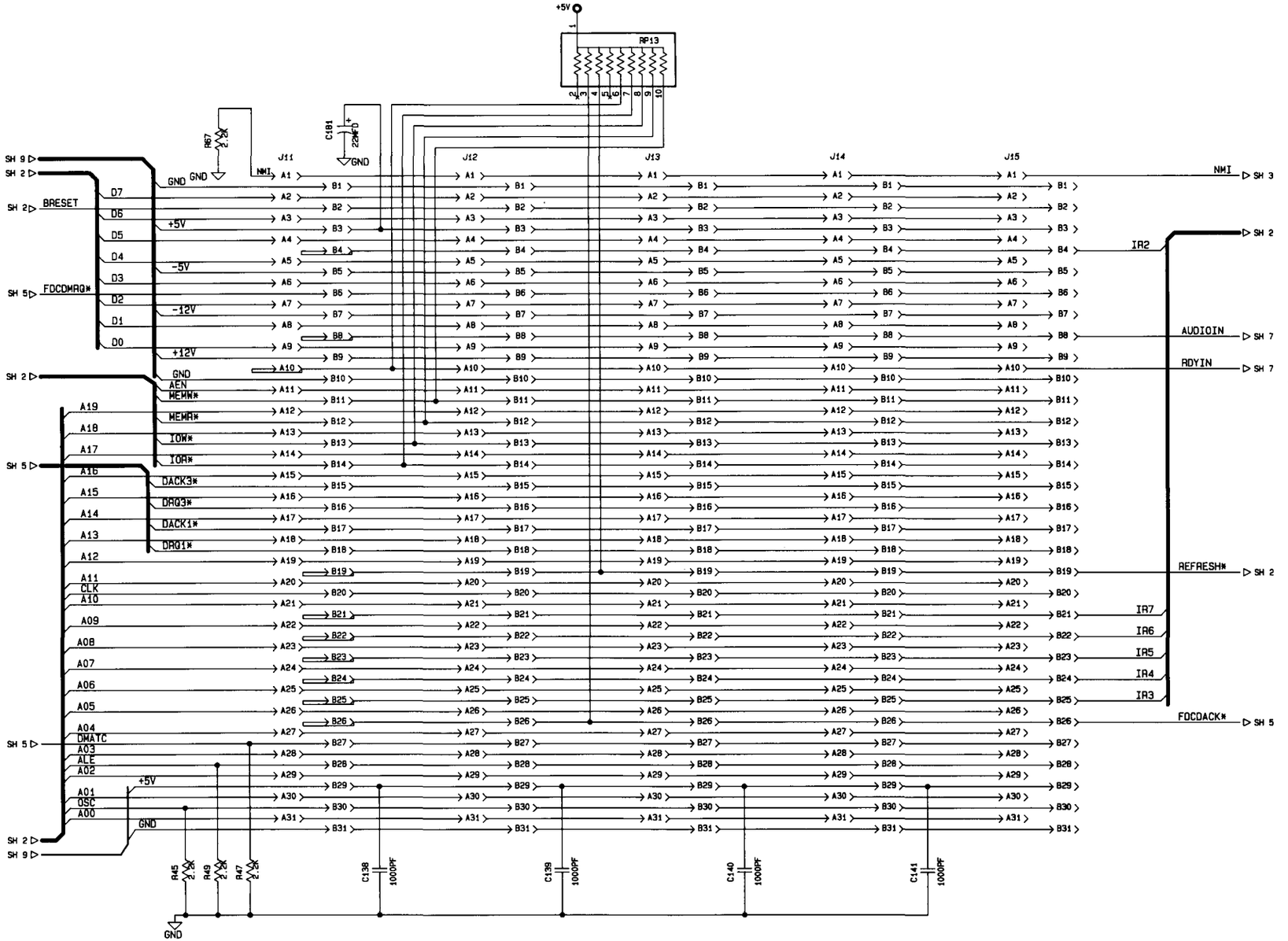


NOTES: 1. C111-C116 ARE 20 PICO-FARADS.
2. C21, C23 ARE 0.1 MICRO-FARADS.

SUBTITLE: KEYBOARD	DWG NO: B000272	REV: A
	SCALE	SHEET: 8 OF 10



SUBTITLE: PRINTER INTERFACE	DWG NO: 8000272	REV: A
	SCALE	SHEET 9 OF 10



SUBTITLE: EXPANSION BUS	DWG NO: B000272		REV: A
	SCALE	SHEET: 10 OF 10	

1000 SX POWER SUPPLIES (SINGLE AND DUAL INPUT)

1000 SX 67 Watt Single Input Power Supply

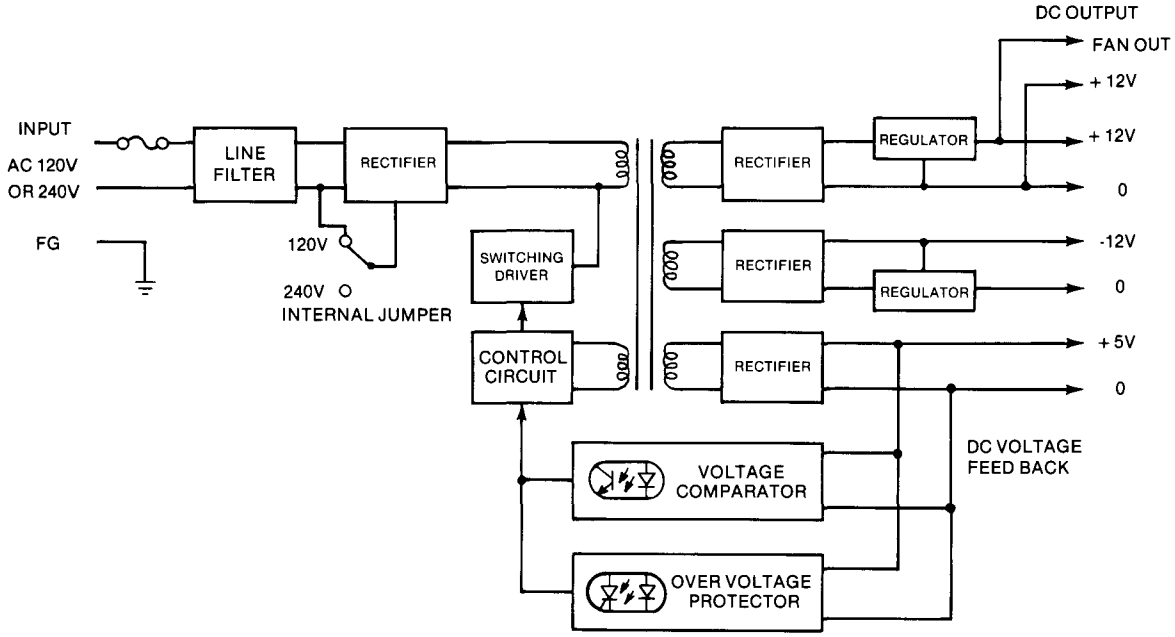
1000 SX 67 WATT SINGLE INPUT POWER SUPPLY
CONTENTS

OPERATING CHARACTERISTICS
BLOCK DIAGRAM
THEORY OF OPERATION
TROUBLESHOOTING
PARTS LIST
PCB ART
SCHEMATIC

OPERATING CHARACTERISTICS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90	120	135	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages				
Vol	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-12.00	-10.80	V
Output Loads				
Iol	1.25	-	7.0	A
Io2	0.15	-	2.4	A
Io3	0	-	0.25	A
Over Current Protection				
Current Limit ICL1	-	-	14.0	A
ICL2	-	-	4.8	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	63	65	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec.
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.7	-	-	KVDC

Power Supply Block Diagram



Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R2 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$$I_C = I_B .hfe$$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R12, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler PHC1 to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, a control signal turns on the photo coupler PHC2 (Photo Thyristor) with the current of zener diode (D11) and stops oscillation by turning on Q3, which turns off Q1 in the switching circuit.

In the case of stopped oscillation, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

The Photo Thyristor isolates the primary and secondary circuits.

Troubleshooting

Equipment for Test Set-Up

Isolation Transformer(minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

0-280V Variable Transformer (Variac)- Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

Voltmeter- Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

Oscilloscope- Need x 10 and x 100 probes.

Load board with connectors- See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

Ohmmeter

Set-Up Procedure

Set up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5 V	1.25 A	4 ohms	20 W	7.0 A	0.7 ohms	60 W
+12 V	0.15 A	80 ohms	5 W	2.4 A	5 ohms	50 W
-12 V	0	0	0	0.25 A	48 ohms	5 W

Table 1 Load Board Values (67 watt)

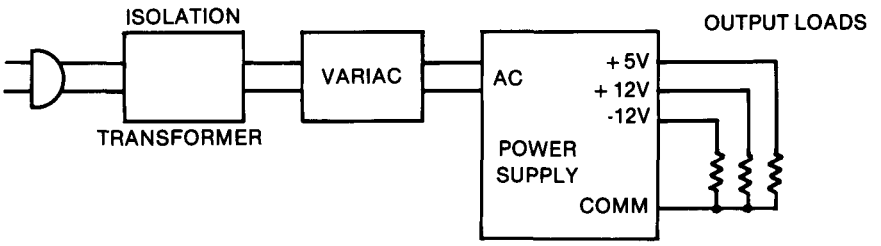


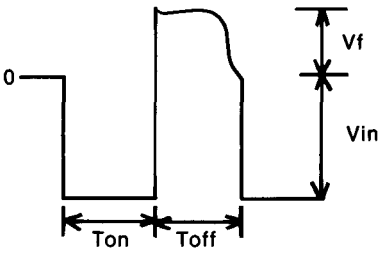
Figure 1 Test Setup

Start-Up

Load power supply with minimum load as specified in Table 1. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60 VAC applied, and should regulate when 90 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer Tl
Vf : Collector Voltage at turn-off time

Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistor (Q2,Q3) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from 0V. Output voltage will appear at some input voltage and then go down to 0V again. Check the Diode D11 or Photo Coupler (PHC2).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

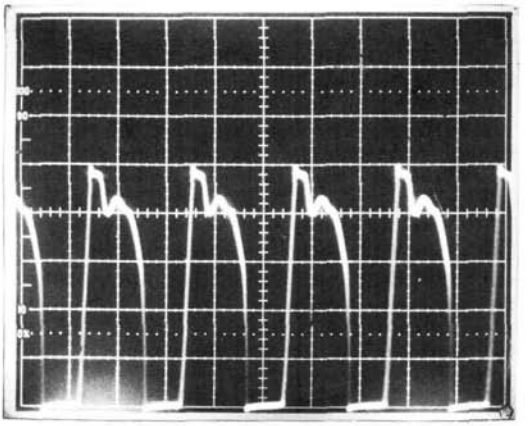
   Figure 2 is Q1 Collector normal waveform.

   Figure 3 is Q1 Base normal waveform.

   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

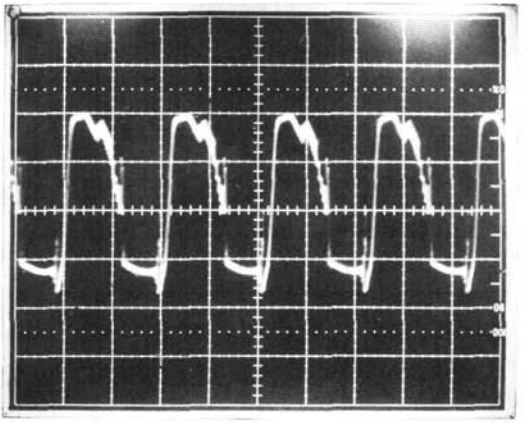
Collector Waveforms	Shorted Secondary Components
Figure 4	D8, D9, D10, C16, C17, C19, C20, C21, C22, C23

Table 2. List of Shorted Circuits



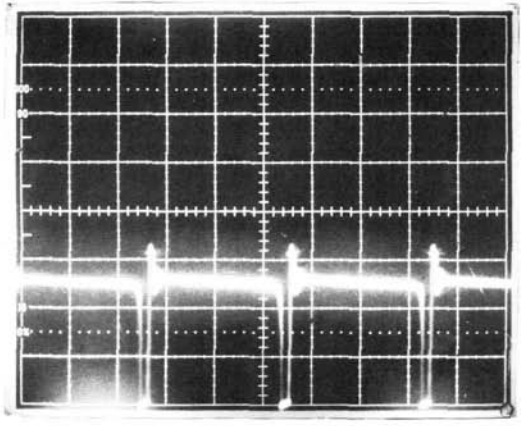
50V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)



50V/DIV
5µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

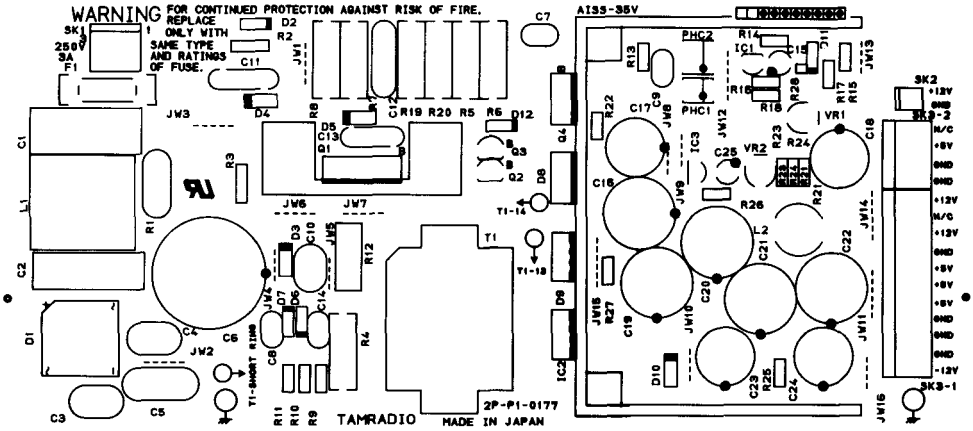
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790085

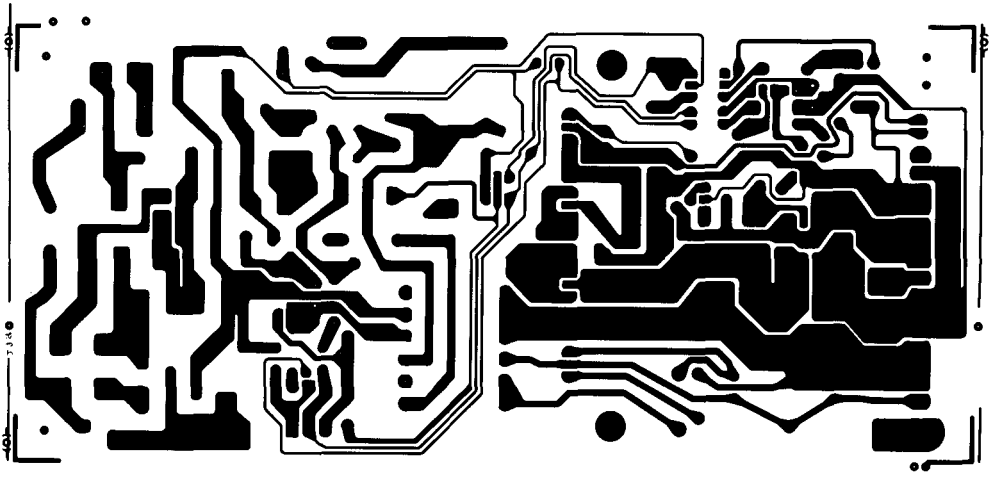
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C1	Film	0.1uF	250VAC	1		XE-104
C2	Film	0.22uF	250VAC	1		XE-224
C3/4/11	Ceramic	2200pF	400VAC	3		DE7100F222MVA1-KC or CS13-E2GA222MYAS
C5	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C6	Electrolytic	680uF	200WV	1		CETSW2D681 or 200LPSS680
C7/8/9	Film	0.047uF	50V	3		50F2D473K or AMZF473K50V
C10	Film	0.1uF (0.1-0.22uF)	50V	1		50F2D104K or AMZF104K50V (Adjust 104K-224K)
C12	Film	0.22uF	250V	1		250MW224K
C13	Ceramic	1500pF	2KV	1		DE1210R152K2K or CK45-B3DD152KYAR
C15/25	Electrolytic	1uF	50WV	2		CEUSM1H010
C16	Electrolytic	2200uF	25WV	1		CEUSM1E222
C17/23/24	Electrolytic	470uF	25WV	3		CEUSM1E471
C18	Electrolytic	1000uF	16WV	1		CEUSM1C102
C19/20/21	Electrolytic	4700uF	10WV	3		CEUSM1A472
C22	Electrolytic	2200uF	10WV	1		CEUSM1A222
CONNECTORS						
SK1	Connector, 2 conductors		Input	1		5277-02A
SK2	Connector, 2 conductors		Fan-out	1		5045-02F
SK3-1	Connector, 10 conductors		Output	1		5277-10A
SK3-2	Connector, 4 conductors		Output	1		5273-04A
DIODES						
D1	Silicon, Stack	400V	4A	1		S4VB40 or RB404 or DBA40E
D2/11	Silicon	5V	400mW	2		HZ5B3
D3/4/5	Silicon	600V	1A	3		FI-06 or V19G
D6/7	Silicon	100V	200mA	2		DS446 or 1S954
D8	Silicon, Stack	200V	5A	1		D5LCA20 or 5CH2SM

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
D9	Silicon, Stack	40V	10A	1		D10SC4M or 10CS04SM
FUSE						
F1	Fuse,	250V	3A	1		MT4 3A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		40-08440-01
HS2	Heatsink, for D8/D9/Q4/IC2			1		4P-D2-0180
INDUCTORS						
L1	Choke Coil	8mH		1		TO-9161-1 or TO-9161
L2	Choke Coil	4.3uH		1		PSC-156
INTEGRATED						
IC1	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
IC2	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC3	IC, Regulator	36V	30mA	1		M5236L
PHOTO COUPLERS						
PHC-1	Photo Coupler	35V	50mA	1		TLP521-1 or PC817
PHC-2	Photo Coupler	400V	150mA	1		TLP541G or S22MD1
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0177
RESISTORS						
R1	Thermistor	8	1.6A	1		117-080-45202 or 8D-11 or D4FFL8ROP
R2/3	Carbon	100K	1/2W	2		RD50P100KohmsJ or RD50S100KohmsJ
R4	Metal-oxide	27 (10-56)	2W	1		RSF2B27ohmsJ (Adjust 10-56ohms)
R5/6/19/20	Metal-oxide	27K	2W	4		RSF2B27KohmsJ

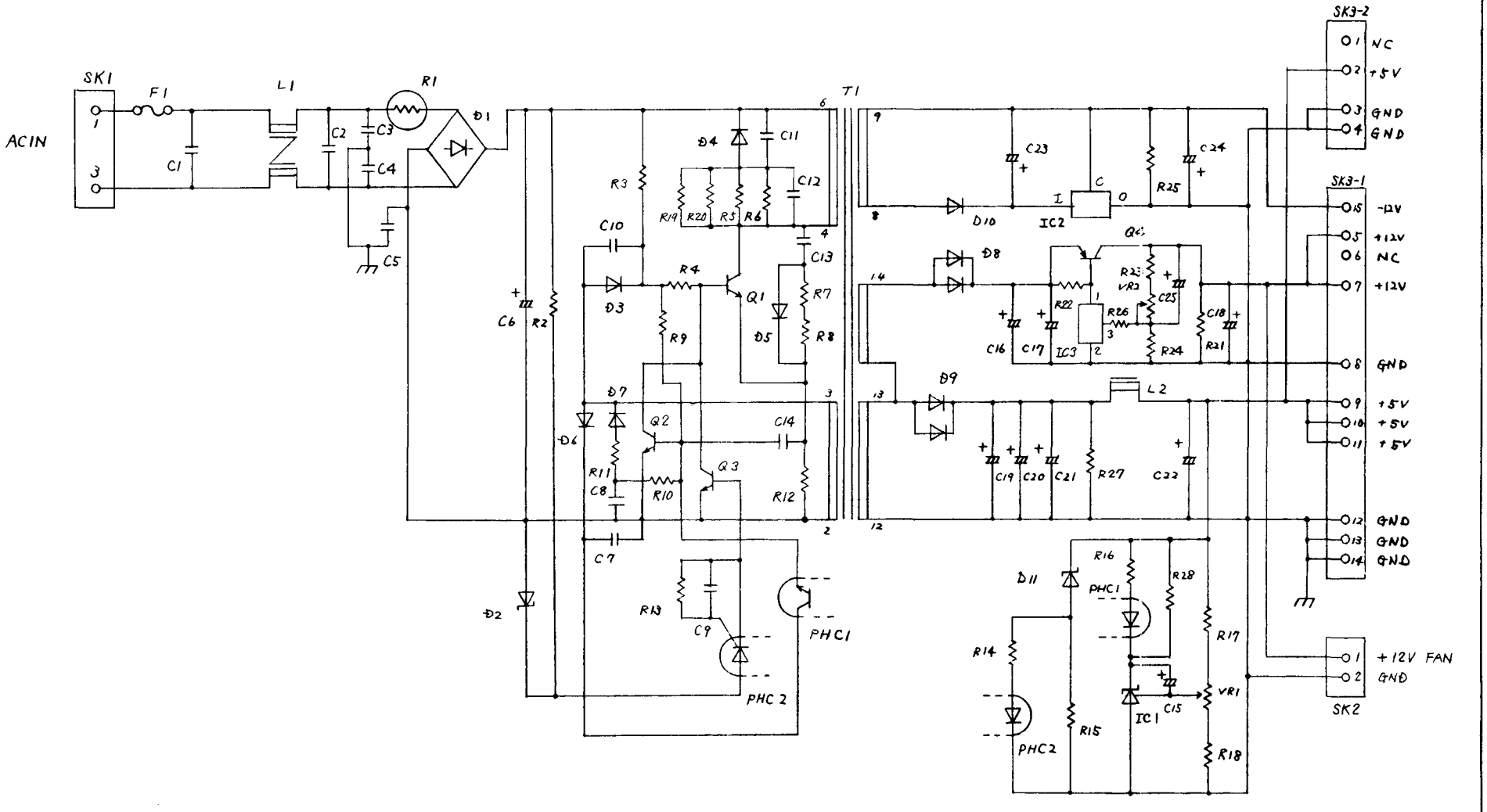
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
R7/8	Metal-oxide	470	2W	2		RSF2B470ohmsJ
R9	Carbon	560 (330-750)	1/4W	1		RD25P560ohmsJ or RD25S560ohmsJ (Adjust 330-750ohms)
R10	Carbon	270 (180-470)	1/4W	1		RD25P270ohmsJ or RD25S270ohmsJ (Adjust 180-470ohms)
R11	Carbon	47	1/4W	1		RD25P47ohmsJ or RD25S47ohmsJ
R12	Cement	0.27	5W	1		MPC71 0.27ohmsK
R13	Carbon	27K	1/4W	1		RD25P27KohmsJ or RD25S27KohmsJ
R14	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R15	Carbon	180	1/4W	1		RD25P180ohmsJ or RD25S180ohmsJ
R16	Carbon	100	1/4W	1		RD25P100ohmsJ or RD25S100ohmsJ
R17/18/21/24	Carbon	2.2K	1/4W	4		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R22/27	Carbon	220	1/4W	2		RD25P220ohmsJ or RD25S220ohmsJ
R23	Carbon	18K	1/4W	1		RD25P18KohmsJ or RD25S18KohmsJ
R25	Carbon	1K	1/4W	1		RD25P1KohmsJ or RD25S1KohmsJ
R26	Carbon	15K	1/4W	1		RD25P15KohmsJ or RD25S15KohmsJ
R28	Carbon	1K	1/6W	1		RD16P1KohmsJ or RD16S1KohmsJ
VR1/2	Variable	2K	0.5W	2		V6EK-PV(1S)202B or H0615-222B
TRANSFORMER						
T1	Transformer			1		TO-4342
TRANSISTORS						
Q1	Transistor	400V	12A	1		2SC2833 or 2SC2938
Q2/3	Transistor	50V	2A	2		2SD1207 or 2SC2655
Q4	Transistor	60V	5A	1		2SA1441 or 2SB1019



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



DWN	K.Miyajima	S790385	SP-MI-0164
CHKD	A.Miura		
APPD	T.Yokoyama		

TAMURA SEISAKUSHO CO., LTD.

1000 SX 67 Watt Dual Input Power Supply

1000 SX 67 WATT DUAL INPUT POWER SUPPLY
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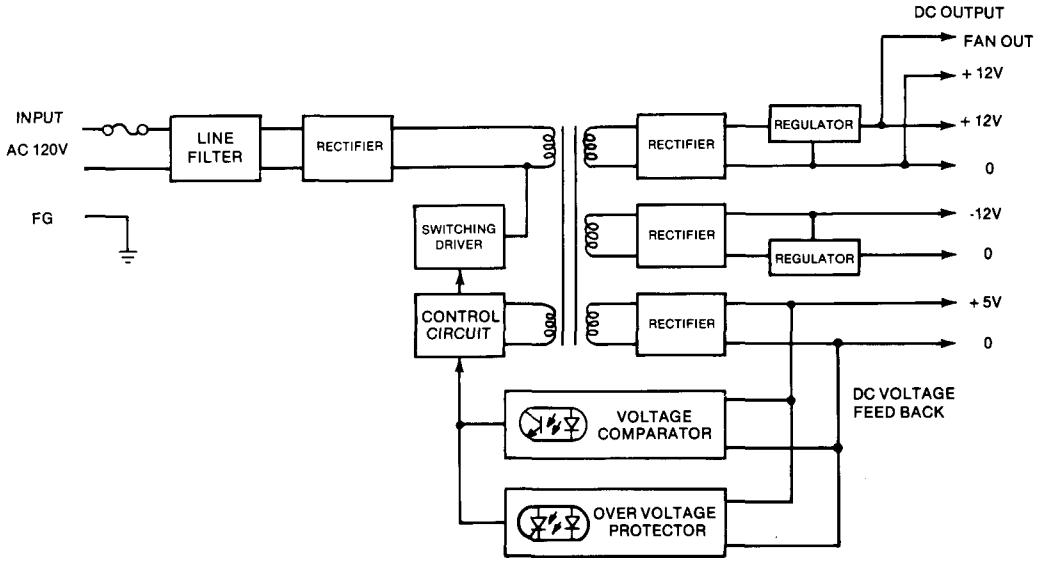
Vo3	-13.20	-120.00	-10.80	V
Output Loads				
Iol	1.25	-	7.0	A
Io2	0.15	-	2.4	A
Io3	0	-	0.25	A
Over Current Protection				
Current Limit ICL1	-	-	14.0	A
ICL2	-	-	4.8	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	63	65	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec.
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.25	-	-	KVAC
Input to Output	3.75	-	-	KVAC

Power Supply Block Diagram



Theory of Operation

AC Input Circuit

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This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R4 and R5 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(2-3) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (4-6). Increasing the collector current of transistor Q1 to the point of:

$$I_C > I_B .hfe$$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R13, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulators IC2, IC3 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler PHC1 to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, a control signal turns on the photo coupler PHC2 (Photo Thyristor) with the current of zener diode (D11) and stops oscillation by turning on Q3, which turns off Q1 in the switching circuit.

In the case of stopped oscillation, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

The Photo Thyristor isolates the primary and secondary circuits.

Troubleshooting

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CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

0-280V Variable Transformer (Variac)- Used to vary input voltage. Recommend 5 amp, 1.4 KVA rating, minimum.

Voltmeter- Need to measure DC voltages to 50 VDC and AC voltages to 300 VAC. Recommend two digital multimeters.

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NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

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Set up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

Start-Up

Load power supply with minimum load as specified in Table 1. Check up on the voltage selector jumper and don't apply over voltage. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60/80-120 VAC applied, and should regulate when 90/180 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+ 5 V	1.25 A	4 ohms	20 W	7.0 A	0.7 ohms	60 W
+ 12 V	0.15 A	80 ohms	5 W	2.4 A	5 ohms	50 W
-12 V	0	0	0	0.25 A	48 ohms	5 W

Table 1 Load Board Values (67 watt)

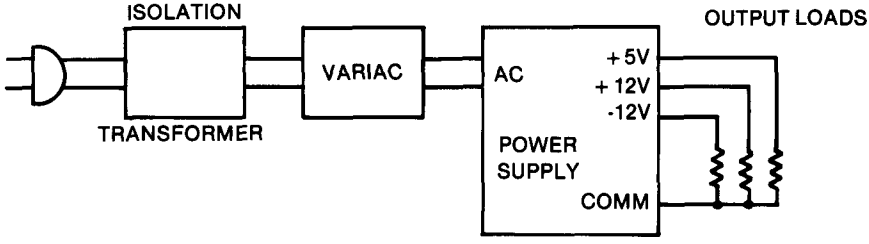


Figure 1 Test Setup

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistors (Q2,Q3) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from 0V. Output voltage will appear at some input voltage and then go down to 0V again. Check the Diode D11 or Photo Coupler (PHC2).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

   Figure 2 is Q1 Collector normal waveform.

   Figure 3 is Q1 Base normal waveform.

   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

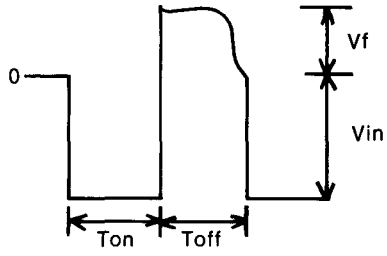
Collector Waveforms	Shorted Secondary Components
Figure 4	D8, D9, C17, C18, C20, C21, C22, C23,

Table 2. List of Shorted Circuits

6. Check Resistor (R26)
   If R26 is open, check D10, C24,and IC2.

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

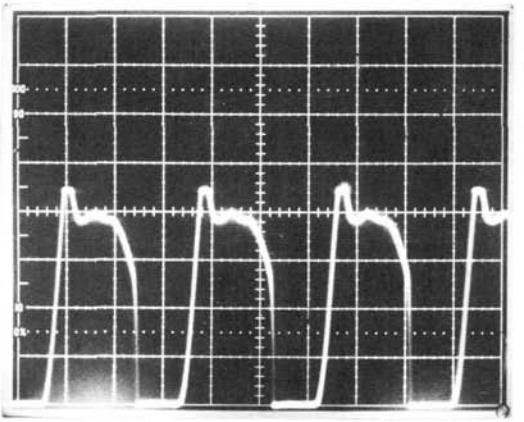
The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer Tl
Vf : Collector Voltage at turn-off time

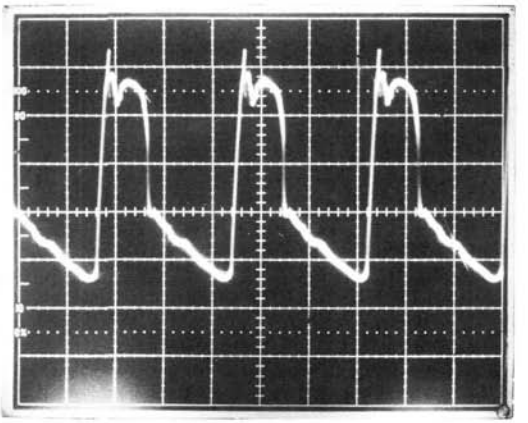
Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor



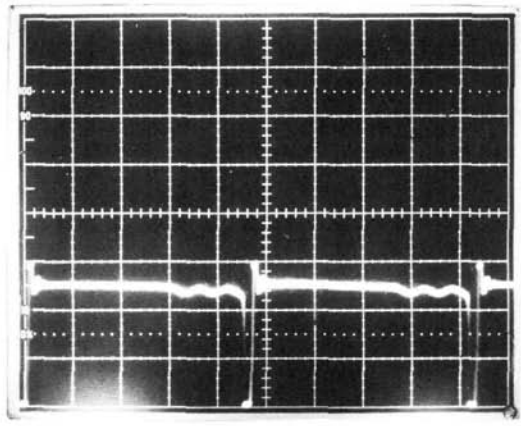
100V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)



100V/DIV
5µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

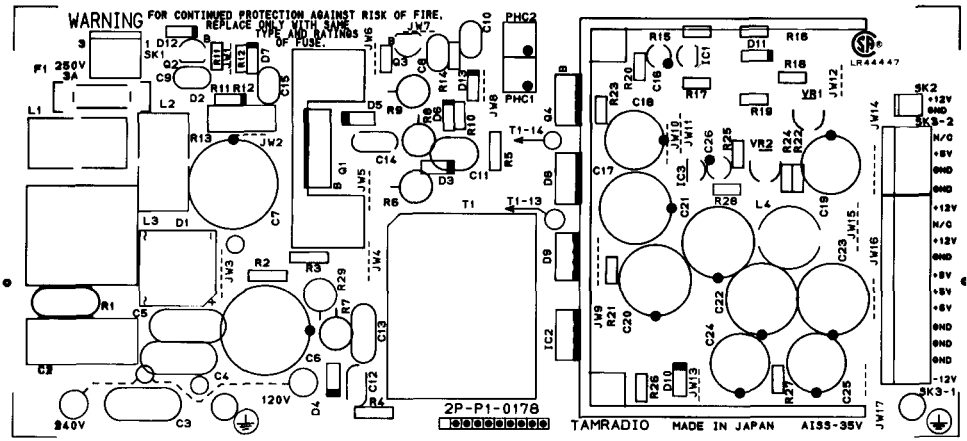
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790084

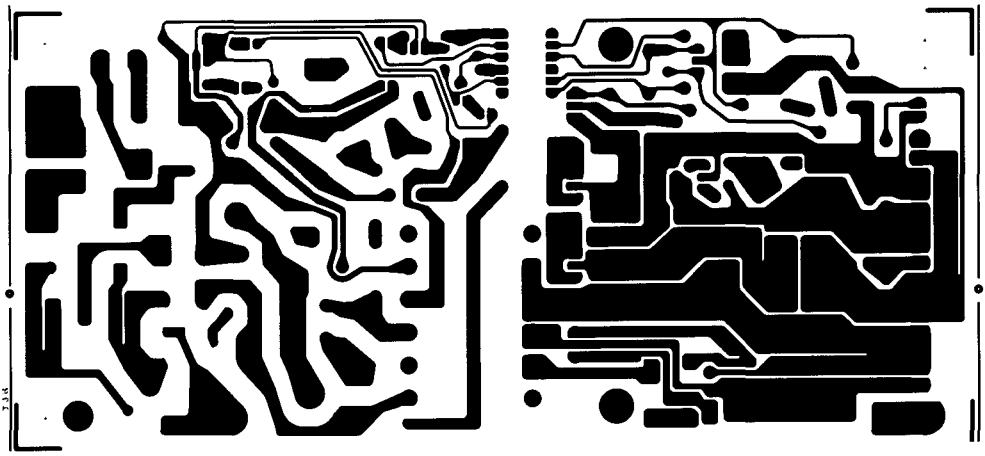
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C2	Film	0.22uF	400VAC	1		XE-224
C3/4	Ceramic	4700pF	400VAC	2		DE7150F472MVA1-KC or CS17-E2GA472MYAS
C5	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C6/7	Electrolytic	330uF	200WV	2		CETSW2D331 or 200LPSS330
C8/9/10/15	Film	0.047uF	50V	4		50F2D473K or AMZF473K50V
C11	Film	0.1uF (0.1-0.22uF)	50V	1		50F2D104K or AMZF104K50V
C12	Ceramic	470pF	2KV	1		DE0907R471K2K or CK45-B3DD471KYAR
C13	Film	0.01uF	630V	1		CF921L2J103K or MDDZ2J103K
C14	Ceramic	680pF	2KV	1		DE1010R681K2K or CK45-B3DD681KYAR
C16/26	Electrolytic	1uF	50WV	2		CEUSM1H010
C17	Electrolytic	2200uF	25WV	1		CEUSM1E222
C18/24/25	Electrolytic	470uF	25WV	3		CEUSM1E471
C19	Electrolytic	1000uF	16WV	1		CEUSM1C102
C20/21/22	Electrolytic	4700uF	10WV	3		CEUSM1A472
C23	Electrolytic	2200uF	10WV	1		CEUSM1A222
CONNECTORS						
SK1	Connector, 2 conductors Input			1		5277-02A
SK2	Connector, 2 conductors Fan-out			1		5045-02F
SK3-1	Connector, 10 conductors Output			1		5277-10A
SK3-2	Connector, 4 conductors Output			1		5273-04A
	Pin Terminal, Voltage Selector			2		RT-01N-2.3A
	Jumping Connector			1		4P-M3-0017
DIODES						
D1	Silicon, Stack	600V	3A	1		S3WB60
D2/11	Silicon, Zener	5V	400mW	2		HZ5B3
D3/10	Silicon	600V	1A	2		FI-06 or V19G
D4/5	Silicon	800V	1A	2		FI-08 or RU2B
D6/7/13	Silicon	100V	200mA	3		DS446 or 1S954

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
D8	Silicon, Stack	200V	5A	1		D5LCA20 or 5CH2SM
D9	Silicon, Stack	40V	10A	1		D10SC4M or 10CS04SM
FUSE						
F1	Fuse	250V	3A	1		MT4 3A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		40-08440-01
HS2	Heatsink, for D8/D9/Q4/IC2			1		4P-D2-0180
INDUCTORS						
L1/2	Choke Coil	0.5mH		2		TO-9175
L3	Choke Coil	8mH		1		TO-9161
L4	Choke Coil	4.3uH		1		PSC-156
INTEGRATED CIRCUITS						
IC1	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
IC2	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC3	IC, Regulator	36V	30mA	1		M5236L
PHOTO COUPLER						
PHC1	Photo Coupler	55V	60mA	1		TLP732 or PC111
PHC2	Photo Coupler	600V	150mA	1		TLP741J
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0178
RESISTORS						
R1	Thermister	16	1.2A	1		117-160-45201 or 16D-13 or D4FFL160P
R2/3/4/5	Carbon	100K	1/2W	4		RD50P100KohmsJ or RD50S100KohmsJ
R6	Metal-oxide	47 (15-68)	2W	1		RSF2B47ohmsJ (Adjust 15-68ohms)

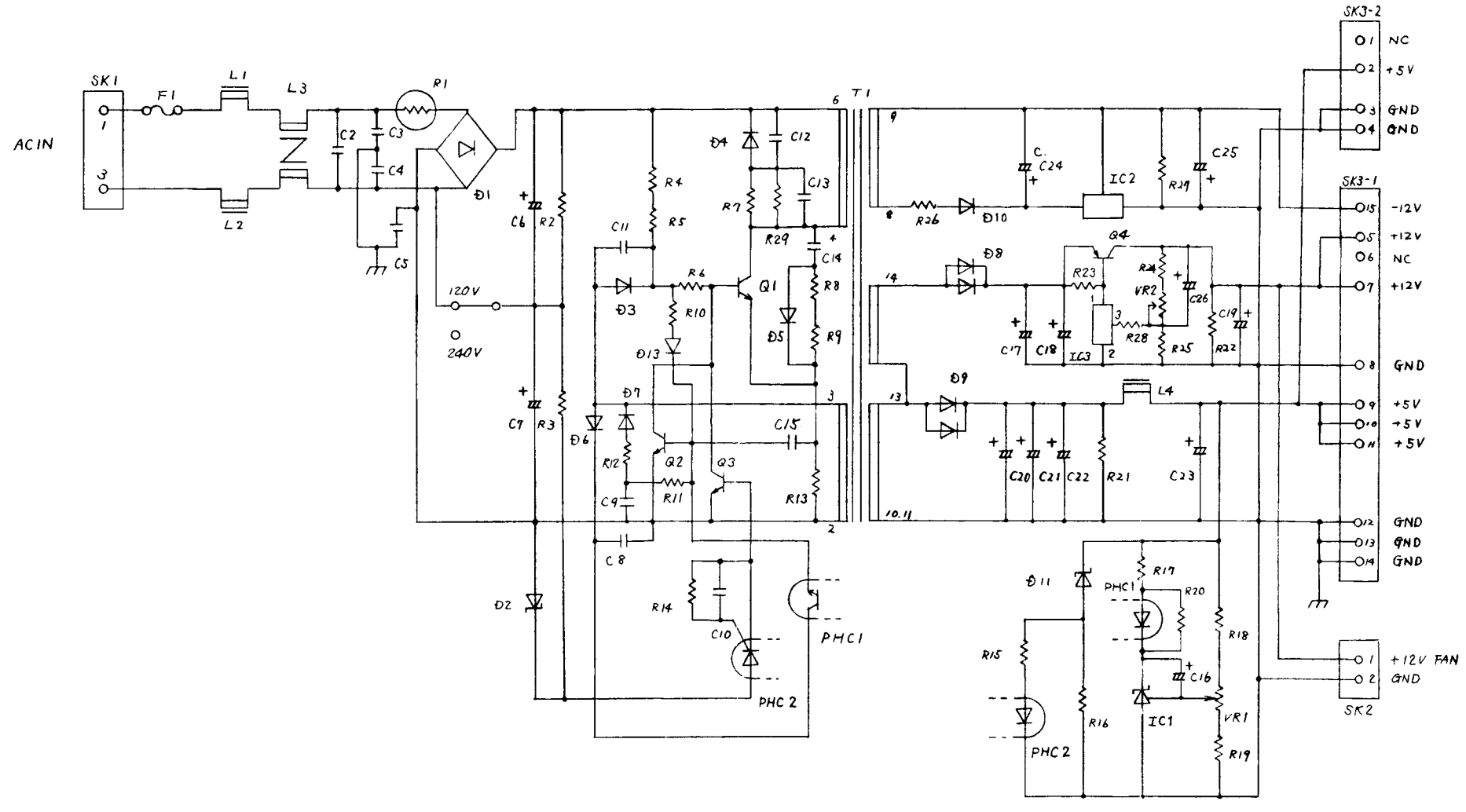
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
R7/29	Metal-oxide	100K	2W	2		RSF2B100KohmsJ
R8/9	Metal-oxide	100	2W	2		RSF2B100ohmsJ
R10	Carbon	560 (330-680)	1/4W	1		RD25P560ohmsJ or RD25S560ohmsJ (Adjust 330-680ohms)
R11	Carbon	330 (220-560)	1/4W	1		RD25P330ohmsJ or RD25S330ohmsJ (Adjust 220-560ohms)
R12	Carbon	47	1/4W	1		RD25P47ohmsJ or RD25S47ohmsJ
R13	Cement	0.56	5W	1		MPC71 0.56ohmsK
R14	Carbon	27K	1/4W	1		RD25P27Kohms or RD25S27KohmsJ
R15	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R16	Carbon	180	1/4W	1		RD25P180ohmsJ or RD25S180ohmsJ
R17	Carbon	100	1/4W	1		RD25P100ohmsJ or RD25S100ohmsJ
R18/19/22	Carbon	2.2K	1/4W	3		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R20/27	Carbon	1K	1/4W	2		RD25P1KohmsJ or RD25S1KohmsJ
R21/23	Carbon	220	1/4W	2		RD25P220ohmsJ or RD25S220ohmsJ
R24	Carbon	18K	1/4W	1		RD25P18KohmsJ or RD25S18KohmsJ
R26	Fusing	1	1/4W	1		RF25S1ohmsJ
R28	Carbon	15K	1/4W	1		RD25P15KohmsJ or RD25S15KohmsJ
VR1/2	Variable	2K	0.5W	2		V6EK-PV(1S)202B or H0615-222B
TRANSFORMER						
T1	Transformer			1		TO-4341
TRANSISTORS						
Q1	Transistor	800V	6A	1		2SC3460 or 2SC3680
Q2/3	Transistor	50V	2A	2		2SD1207 or 2SC2655
Q4	Transistor	60V	5A	1		2SA1441 or 2SB1019



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



DWN	K.Miyajima	8790084	3P-M1-0165
CHKD	A Miura		
APPD	T.Yokoyama		

TAMURA SEISAKUSHO CO., LTD.

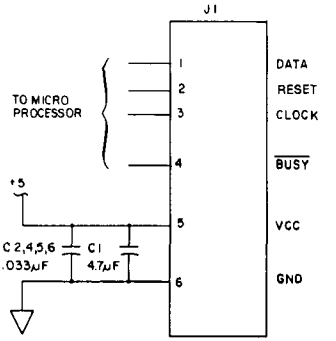
1000 SX KEYBOARD

KEYBOARD
CONTENTS

SPECIFICATION
KEYBOARD TIMING
KEYBOARD LAYOUT

KEYBOARD ASSEMBLY

The Tandy 1000 has a 90-key keyboard that includes 12 function keys, a numeric keypad, and special purpose keys for paging. The keyboard is connected to the Main Unit by a coiled cable and operated at a maximum distance of 4 feet from the main unit. Figure shows the interconnecting cable connector to the keyboard assembly. The cable assembly can be disconnected from the keyboard assembly during repair.



Keyboard Assembly Connector

Figure 1

Keyboard Specifications

The keyboard is fully encoded with microprocessor control, and requires +5 VDC supplied from the Main Unit.

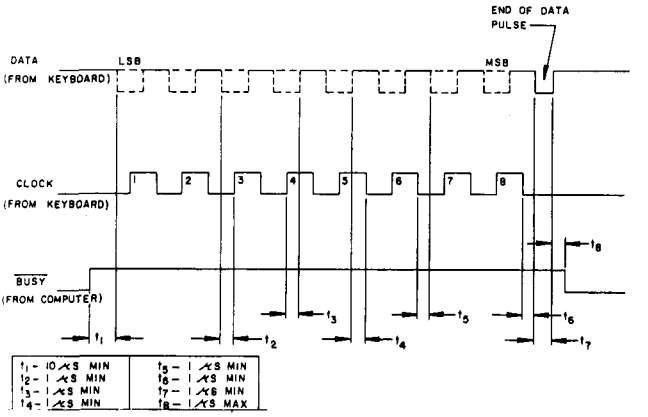
1. Key Type — all keys generate "make" and "break" codes. See the Key Code Chart. Break codes are formed by adding 80H to the make code. Keys 49 and 71 have alternate action that "makes" on one actuation of the key and "breaks" on succeeding actuation. No code is generated for these two keys when the key is released.

2. Number of Keys — 90

3. Repeat Strobe — there is a repeat strobe of 66 to 111 mSec when any key is depressed for more than 1 second, with the exception of SHIFT, CTRL, CAPS, ENTER, and NUMBER LOCK.

Keyboard Timing

Figure 2 is the timing chart for the Tandy 1000 Keyboard Assembly.



Keyboard Assembly Timing Chart

Figure 2

Key Code Chart

Key Number	Legend	Scan Code
1	F1	3B
2	F2	3C
3	F3	3D
4	F4	3E
5	F5	3F
6	F6	40
7	F7	41
8	F8	42
9	F9	43
10	F10	44
11	F11	59
12	F12	5A
13	INSERT +	55
14	DELETE -	53
15	BREAK	54
16	ESC	01
17	1 !	02
18	2 @	03
19	3 #	04
20	4 $	05
21	5 %	06
22	6 ^	07
23	7 &	08
24	8 *	09
25	9 (	0A
26	0)	0B
27	- _	0C
28	= +	0D
29	BACKSPACE	0E
30	ALT	38
31	PRINT	37
32	7 (backslash)	47
33	8 (Tilde)	48
34	9 PG UP	49
35	TAB	0F
36	Q	10
37	W	11
38	E	12
39	R	13
40	T	14
41	Y	15
42	U	16
43	I	17
45	P	19

Key Number	Legend	Scan Code
46	{ [	1A
47	}]	1B
48	HOLD	46
49	NUM LOCK	45
50	4 :	4B
51	5	4C
52	6	4D
53	CTRL	1D
54	A	1E
55	S	1F
56	D	20
57	F	21
58	G	22
59	H	23
60	J	24
61	K	25
62	L	26
63	; :	27
64	' "	28
65	ENTER	1C
66		29
67	HOME	58
68	1 END	4F
69	2 (Grave)	50
70	3 PG DN	51
71	CAPS	3A
72	SHIFT	2A
73	Z	2C
74	X	2D
75	C	2E
76	V	2F
77	B	30
78	N	31
79	M	32
80	, <	33
81	. ‡	34
82	/ ?	35
83	SHIFT	36
84		2B
85		4A
86		4E
87	0	52
88		56
89	ENTER	57

90 (Space Key)

91 thru 95 — reserved for International

Keyboard Layout

Shown below is the keyboard layout and number designation of the keys on the Tandy 1000 keyboard. They should be used with the Key Code Chart for determining data value transmitted by the keyboard.

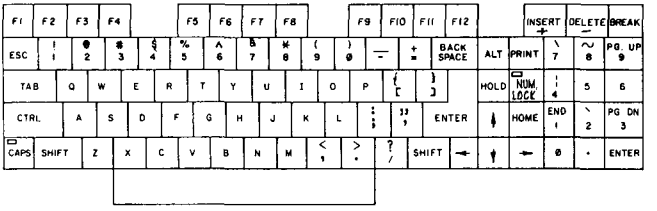
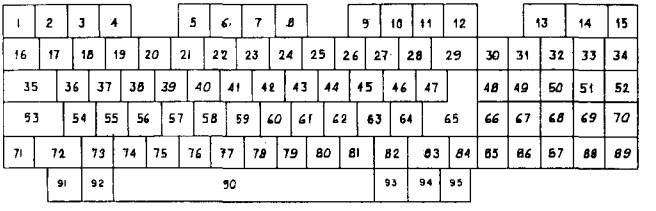


Figure 3 Keyboard Identification



NOTE: KEYS 91 THRU 95 NOT USED ON U.S. VERSION, USED ON INTERNATIONAL VERSION ONLY

Figure 4 Key Number Identification

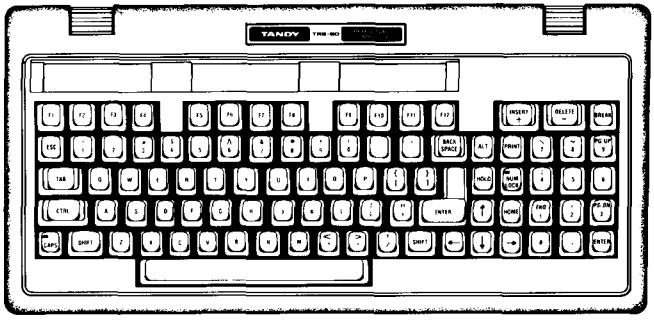

TANDY
INSERT
DELETE
BREAK
ESC
BACK SPACE
ALT
PRINT
TAB
HOLD
CTRL
ENTER
HOME
END
CAPS
SHIFT
SHIFT
ENTER

Figure 5

8087 NUMERIC DATA COPROCESSOR

8087 Coprocessor Operation

The 8087 executes instructions as a coprocessor to the 8086 processor while in the maximum mode (MN/MX pin is connected to ground). The processors status (S0-S1) and queue status lines (QS0-QS1) enable the coprocessor to monitor and decode instructions in synchronization with the microprocessor. An instruction Opcode is sent to the coprocessor and the processor. The processor calculates the memory addresss and the co-processor checks the instruction simultaneously. The coprocessor then accesses the memory location through the local bus from the processor when the processor finishes its current instruction. After the coprocessor is finished with a memory transaction, it returns local bus to the processor. The BUSY signal is used to inform the processor that the coprocessor is performing an operation. The processor WAIT instruction tests this signal to ensure that the coprocessor is ready to excute subsequent instructions.

The control unit (CU) keeps the coprocessor operation synchronized with the processor. The processor and the coprocessor fetch all instructions at the same time from a single stream of mixed instructions. The processor's status lines (S0-S1, S6) are used by the control unit to determine when an instruction is being fetched.

The coprocessor sends an error signal which generates an interrupt through the NMI interrupt logic when the correct execution mask for the coprocessor is not set. The following two conditions will disable the coprocessor interrupt to the processor:

1. Interrupt Enable bits and the exception of the control word are set to 1's.

2. NMI Mask Register is set to zero. During Power On the NMI Mask Reg. is cleared to disable the NMI. This condition (NMI mask Reg. is set to zero) causes the processor to wait indefinitely for a BUSY* signal from the coprocessor, while the coprocessor expects an interrupt signal from the processor.

For additional information on the the 8087 coprocessor see the 8087 Numeric Data Coprocessor information sheet in this manual.

Tandy® 1000 PLUS RS-232 Interface Board

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International.....4

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8/ WD8250 Asynchronous Communications Element

1/ Introduction to RS-232 Interface Board

The RS-232 board is a single-channel asynchronous serial communications board. The heart of the board is the WD8250 Asynchronous Communications Element (ACE), that functions as a serial data input/output interface. It performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the CPU.

Status information reported includes the type and condition of the ACE's transfer operations as well as any error conditions. The WD8250 includes a programmable baud rate generator that allows operation from 50 to 9600 baud. The WD8250 can be software tailored to the user's requirements. It can add and remove start bits, stop bits, and parity bits. It supports 5-,6-,7- or 8-bit characters with 1, 1 1/2, or 2 stop bits. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

This manual covers both domestic and international RS-232 boards. The main difference between the domestic and international boards is the jumper configuration and the programming of the receiving baud rate. This information is covered in section 2. An international parts list is also included in section 5.

Other features include:

- Full double buffering which eliminates the need for precise synchronization.
- Independent receiver clock input.
- False start bit detection.
- Line break generation and detection.
- Modem control functions: Clear To Send (CTS), Request To Send (RTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect (CD).

2/ Jumper Configuration

Most commercially available terminal or communications programs use the primary addresses. Points E2 and E3 should be jumpered for primary operation. Points E1 and E2 should be jumpered for secondary operation.

International RS-232 Board

The RS-232 serial communications board for the Tandy 1000 has two versions. One board is a domestic version which cannot be altered and is used for domestic operations only. Domestic operations means that the board transmits and receives at the same baud rate. The other board is an international version which can be used as either a domestic board or easily modified to accommodate international operations. International operations means that the board can be programmed to transmit at one baud rate while receiving at another baud rate. This is known to be a common mode of operation in Europe. In order for the board to operate in the international mode, some jumpers on the board will have to be changed. The jumper arrangements for domestic and international operation as well as operation in the primary and secondary address spaces are as follows:

Domestic operation in the primary address (3F8-3FF) -
- Jumper E2 to E3
- Jumper E4 to E6
- Jumper E7 to E9, E8 and E10 empty

Domestic operation in the secondary address (2F8-2FF) -
- Jumper E1 to E2
- Jumper E4 to E6
- Jumper E7 to E9, E8 and E10 empty

International operation in the primary address -
- Jumper E2 to E3
- Jumper E4 to E5
- Jumper E7 to E8
- Jumper E9 to E10

International operation in the secondary address -
- Jumper E1 to E2
- Jumper E4 to E5
- Jumper E7 to E8
- Jumper E9 to E10

While the board is jumpered to the international mode of operation, the user can select between domestic and international operation. This can be done as follows:

Primary address - 3FC, or secondary address - 2FC, Bit 2. Set low for domestic operation, set high for international operation.

NOTE: This bit is low on power up and reset.

Programming the Baud Rates for International Operation

While the Board is setup for international operation, two baud rate generators will have to be programmed. One for the transmit baud rate and the other for the receive baud rate. The transmit baud rate is supplied from the internal baud rate generator on the 8250 UART and is programmed the same as before with the domestic board. The receive baud rate is supplied from an external baud rate generator and is totally independent from the programming for the internal transmit baud rate generator. This external receive baud rate generator is enabled through address 3FF (primary) or 2FF (secondary). The baud rate generator is then programmed by sending the appropriate bits via the data bus (D0-D3). Refer to the following table for selecting the various baud rates.

Frequency Options

Transmit/Receive Address				Baud Rate	Theortical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	--	50/50	6336
0	0	0	1	75	1.2	1.2	--	50/50	4224
0	0	1	0	110	1.76	1.76	--	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	--	50/50	2112
0	1	0	1	300	4.8	4.8	--	50/50	1056
0	1	1	0	600	9.6	9.6	--	50/50	528
0	1	1	1	1200	19.2	19.2	--	50/50	264
1	0	0	0	1800	28.8	28.8	--	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	--	50/50	132
1	0	1	1	3600	57.6	57.6	--	50/50	88
1	1	0	0	4800	76.8	76.8	--	50/50	66
1	1	0	1	7200	115.2	115.2	--	50/50	44
1	1	1	0	9600	153.6	153.6	--	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

Crystal Frequency = 5.0688 MHZ

3/ Theory Of Operation

The user's manual for the TRS-80 RS-232-C Interface (Cat. No. 26-1145) has a general discussion of the EIA RS-232-C Standard. The RS-232 asynchronous communications board has various modes of operation that can be selected by programming the WD8250 ACE. The WD8250 is programmed by selecting the I/O address (3F8 to 3FE primary, and 2FB to 2FE secondary), and writing data out to the board. Address bits A0, A1, and A2 are used to define the modes of operation by selecting the different registers to be programmed or read.

One interrupt is provided to the system from IRQ4 for primary operation, and IRQ3 for secondary operation. This interrupt is active high. Bit 3 of the modem control register must be set high in order to send interrupts to the system. When this bit is high, any interrupts allowed by the interrupt enable register will cause an interrupt.

Refer to Section 8 for the Functional Pin Definitions and Timing Diagrams for the WD8250.

Figure 1 shows the Block Diagram for the RS-232 Adapter.

Figure 2 shows the Functional Pin Definitions for the 82S153 IFL.

Figure 3 shows the IFL equations for the 82S153 IFL.

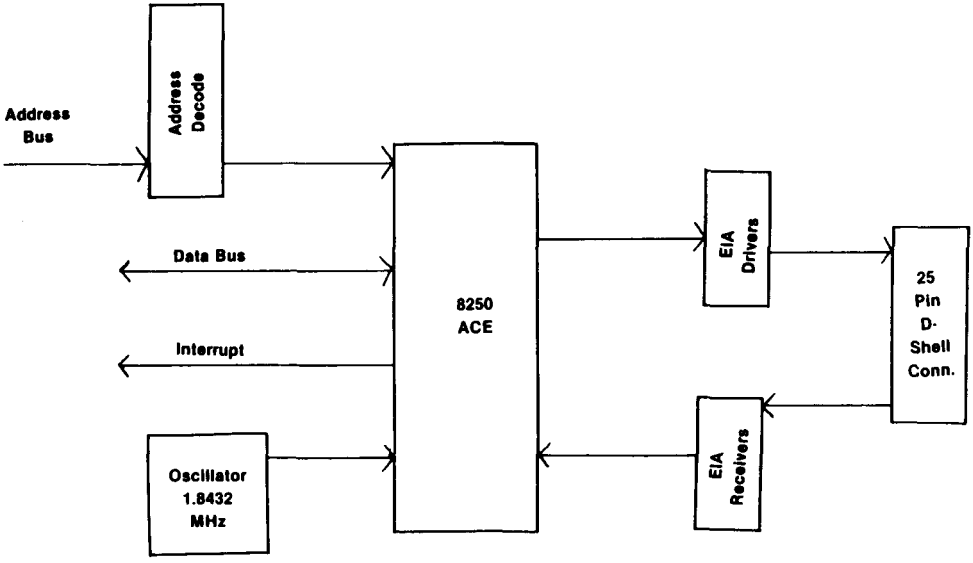


Figure 1. Block Diagram for the RS-232 Adapter.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	ADDRESS ENABLE	$\overline{AEN}$	DMA cycle when high, CPU cycle when low.
2-8	ADDRESS LINES	A3-A9	These address lines are used for decoding the address space 2F8-2FF (secondary) or 3F8-3FF (primary).
9	SECONDARY INTERRUPT REQUEST	IORQ3	Sends interrupts to the CPU while operating in the secondary address space.
10	GROUND		
11	PRIMARY INTERRUPT REQUEST	IORQ4	Sends interrupts to the CPU while operating in the primary address space.
12	PRIMARY OR SECONDARY UARTS	P or S	An input that determines which address space will be used. Primary (3F8-3FF) when high or secondary (2F8-2FF) when low.
13	UART INTERRUPT	INT	Receives interrupt signal from the 8250.
14	UART CHIP SELECT	$\overline{UCS}$	Enables the 8250 ACE when low.
15	NOT USED		
16	NOT USED		
17	DATA CHIP SELECT	$\overline{DCS}$	Enables the data bus buffers when low.
18	NOT USED		
19	NOT USED		
20	VCC		

Figure 2. Functional Pin Definitions for the 82S153 IFL.

INPUTS

PRI_PORT = IOADDRESS 3F8-3FF
SEC_PORT = IOADDRESS 2F8-2FF

OUTPUTS

$\overline{DCS}$ = PRI_PORT $\overline{AEN}$ P_OR_S + SEC_PORT AEN $\overline{P\_OR\_S}$

IORQ4 = MODEM_INT P_OR_S M_OR_U + UART_INT P_OR_S $\overline{M\_OR\_U}$

IORQ3 = UART_INT $\overline{P\_OR\_S}$ $\overline{M\_OR\_U}$ + MODEM_INT $\overline{P\_OR\_S}$ M_OR_U

UART_CS = PRI_PORT AEN P_OR_S + SEC_PORT AEN $\overline{P\_OR\_S}$

Figure 3. IFL Equations for the 82S153 IFL.

4/ Troubleshooting

The RS-232 board can be tested by using the IOTEST program included with the Tandy 1000 diagnostics diskette. The following is an excerpt from the IOTEST reference quide.

Equipment Needed

1. Computer: Tandy 1000 or 1200 HD

2. RS-232 card

3. Loopback connector test fixture in the following configuration:

DB-25	Signal
2-3	TX-RX
4-5	RTS-CTS
6-8-20-22	DTR-DSR-CD-RI

4. Tandy 1000 Diagnostic Diskette

Troubleshooting Hints

. If some of the control functions are bad:

  Check the loopback connector.
  Check the line drivers/receivers for activity.
  Check the 8250 UART (U2) for any bent pins.

. The BRG fails:

  Check for correct configuration of the jumpers.
  The 8250 UART may be malfunctioning.

. The RX test fails:

  Check for interrupts on the bus.
  Check the 8250 and jumper configurations.

- Break detect fails:

  The 8250 UART may be malfunctioning.

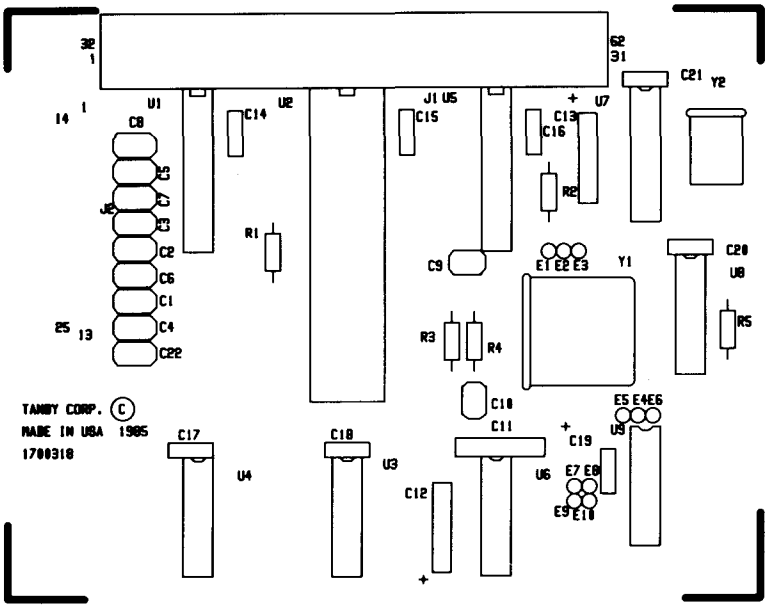
- RX and Break detect fails:

  Check the data path through the loopback connector and the line drivers/receivers.
  Check the 8250 and jumper configurations.

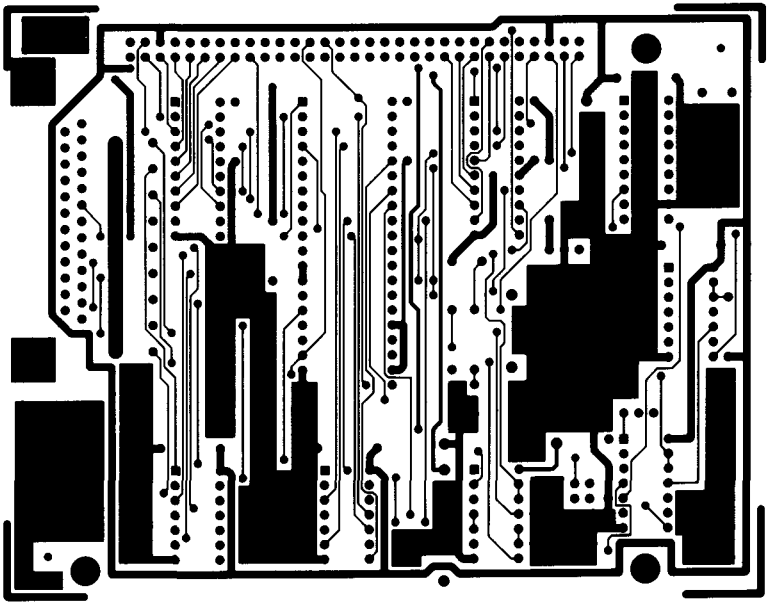
- If the above tests are negative:

  Check the 82S153 (U5).
  Check the 8250 UART and jumper configurations.
  Check the 74LS245 (U1).

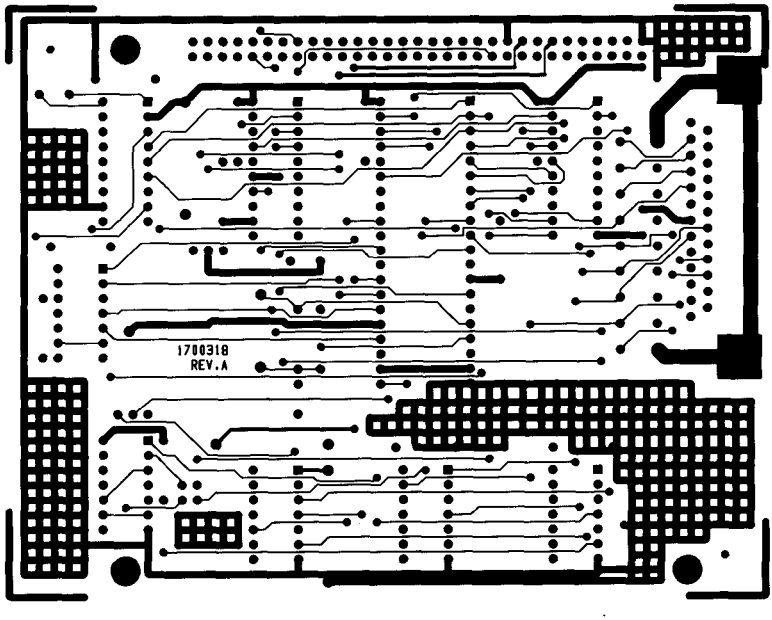
5/ Component Layout



Silkscreen



Component Side



Solder Side

6/ Parts List
RS-232 Board
Catalog Number 25-1014

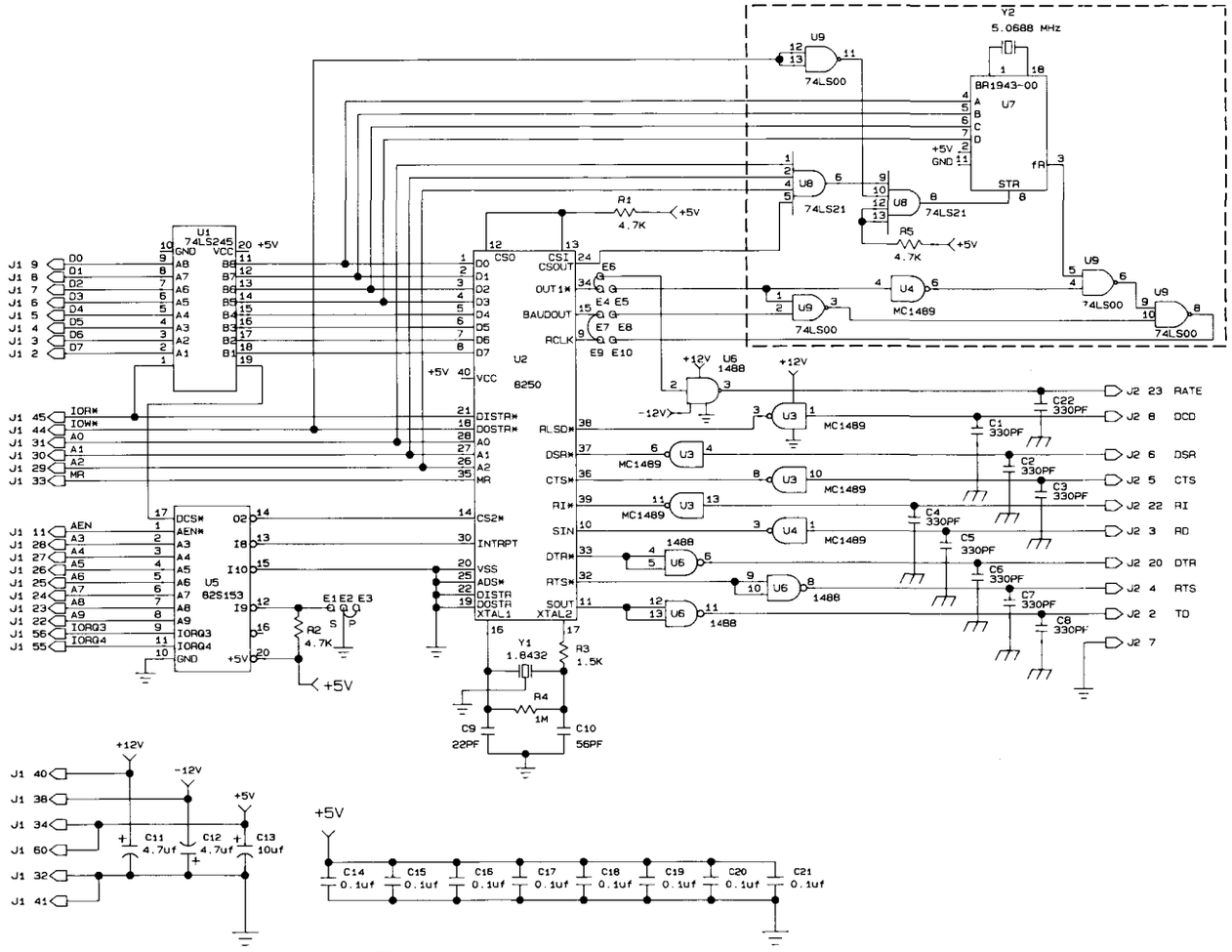
SYMBOL	QTY	DESCRIPTION	PART NO.
	1	RS-232 COMBO/ T1000 REV. A	
	3	JUMPER PLUG	AJ-6908
	3	STANDOFF	AHC-2429
	4	SCREW - 4-40 X 1/4 PAN H, MACHINE	AHD-2991
	2	NUTS - 4-40	AHD-7143
	1	PANEL BRACKET, RS-232	AHC-3192
C1-8,22	9	CAPACITOR 330 PF 5/50V C. DISK	CF-7412
C9	1	CAPACITOR 22 PF/+.5PF/50V	CC-220DJCP
C10	1	CAPACITOR 56 PF 80% 50V C. DISK	CC-560QJCP
C11-12	2	CAPACITOR 4.7 MFD 20% 50V ELEC. AXIAL	CC-475MJAA
C13	1	CAPACITOR 10 MFD +20/25V ELEC. AXIAL	CC-106MFAA
C14-18	5	CAPACITOR 0.1 MFD 50V AXIAL	CC-104JJLA
E1-10	10	STAKING PINS	AHB-9682
J1	1	RECEPTICAL	AJ-4052
J2	1	CONNECTOR, DB25 FEMALE RT. ANGLE METAL SHELL, GROUND STRAP 4-40 THREADED INSERTS	AJ-6983
R1-2	2	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R3	1	RESISTOR 1.5K OHM 1/4 WATT 5%	N-0206EEC
R4	1	RESISTOR 1 MEG OHM 1/4 WATT 5%	N-0445EEC
U1	1	IC 74LS245 OCTAL BUS TRANSCEIVER	AMX-4470
U2	1	IC 8250 SINGLE CHIP UART	MX-6859
U2	1	SOCKET 40-PIN DIP	AJ-6580
U3-4	2	IC MC1489 RECEIVER	MX-2143
U5	1	IC 82S153 IFL, MOD UART	MX-6858
U5	1	SOCKET 20-PIN DIP	AJ-6760
U6	1	IC 1488 DRIVER	AMX-3867
Y1	1	CRYSTAL 1.8432 MHZ	MX-0097

RS-232 Board--International
Catalog Number 25-1014X

SYMBOL	QTY	DESCRIPTION	PART NO.
	1	RS-232 COMBO/ T1000 REV. A	
	4	JUMPER PLUG	AJ-6908
	3	STANDOFF	AHC-2429
	4	SCREW - 4-40 X 1/4 PAN H, MACHINE	AHD-2991
	2	NUTS - 4-40	AHD-7143
	1	PANEL BRACKET, RS-232	AHC-3192
C1-8,22	9	CAPACITOR 330 PF 5/50V C. DISK	CF-7412
C9	1	CAPACITOR 22 PF/±.5PF/ 50V	CC-220DJCP
C10	1	CAPACITOR 56 PF 80% 50V C. DISK	CC-560QJCP
C11-12	2	CAPACITOR 4.7 MFD 20% 50V ELEC. AXIAL	CC-475MJAA
C13	1	CAPACITOR 10 MFD ±20/25V ELEC. AXIAL	CC-106MFAA
C14-21	8	CAPACITOR 0.1 MFD 50V AXIAL	CC-104JJLA
E1-10	10	STAKING PINS	AHB-9682
J1	1	RECEPTICAL	AJ-4052
J2	1	CONNECTOR, DB25 FEMALE RT. ANGLE METAL SHELL, GROUND STRAP 4-40 THREADED INSERTS	AJ-6983
R1,2,5	3	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R3	1	RESISTOR 1.5K OHM 1/4 WATT 5%	N-0206EEC
R4	1	RESISTOR 1 MEG OHM 1/4 WATT 5%	N-0445EEC
U1	1	IC 74LS245 OCTAL BUS TRANSCEIVER	AMX-4470
U2	1	IC 8250 SINGLE CHIP UART	MX-6859
U2	1	SOCKET 40-PIN DIP	AJ-6580
U3-4	2	IC MC1489 RECEIVER	MX-6859
U5	1	IC 82S153 IFL, MOD UART	MX-6858
U5	1	SOCKET 20-PIN DIP	AJ-6760
U6	1	IC 1488 DRIVER	AMX-3867
U7	1	IC BR1943-00	AMX-3921
U8	1	IC 74LS21 DUAL 4-IN AND	MX-6502
U9	1	IC 74LS00 QUAD 2-IN NAND	MX-3495
Y1	1	CRYSTAL 1.8432 MHZ	MX-0097
Y2	1	CRYSTAL 5.0688	AMX-2395

8/ WD8250 Asynchronous Communications Element

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		RELEASE FOR PRODUCTION	5/22/85	

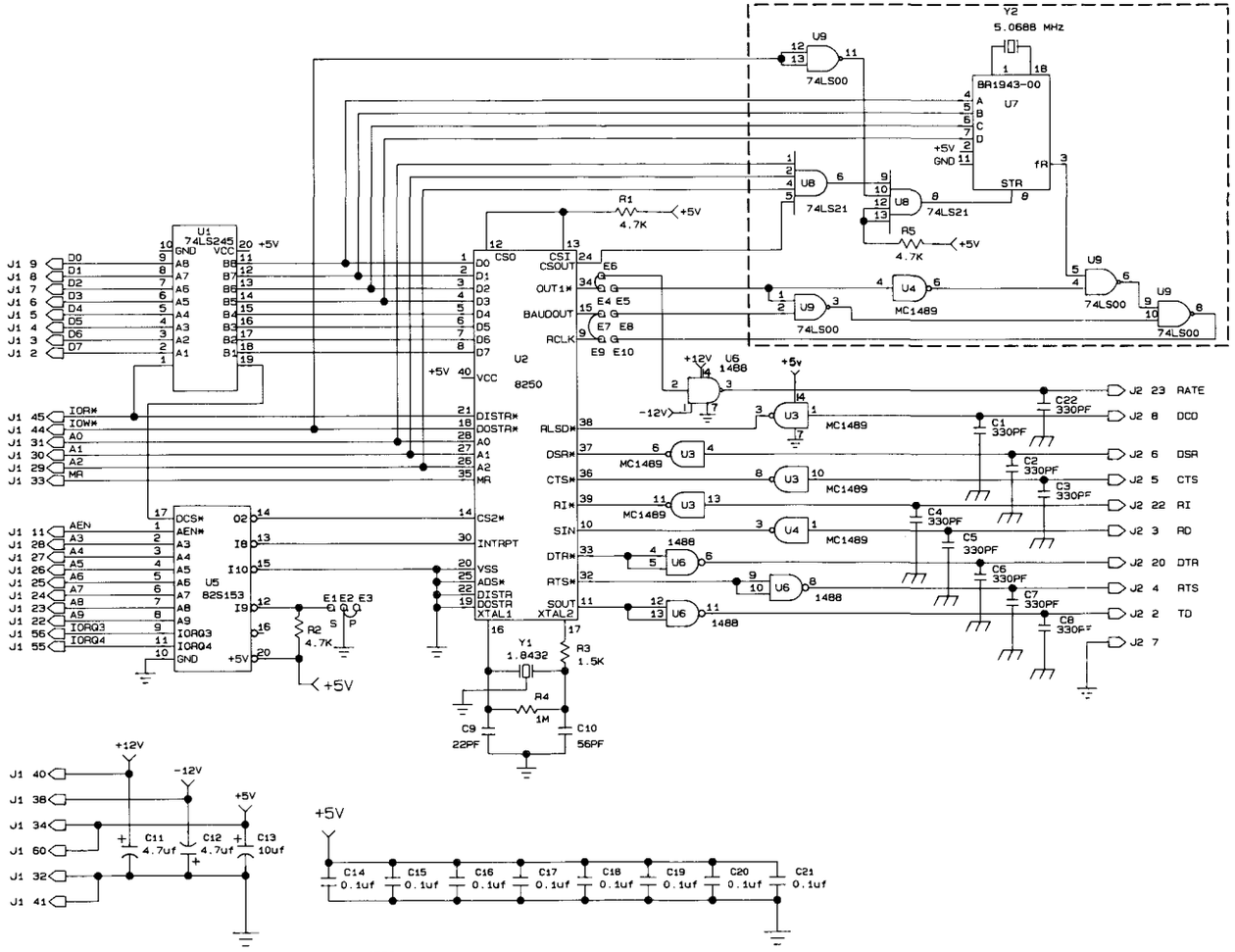


NOTES:
1. COMPONENTS WITHIN DASHED BOX USED ONLY FOR INTERNATIONAL VERSION.
2. JUMPERS SHOWN IN PRIMARY, DOMESTIC CONFIGURATION.

652

DRAFT	DATE	TITLE	SCHEMATIC– RS-232 COMBO TANDY 1000
CHECK	DATE		PROJECT NO. 652
DESIGN	DATE		
APPR.	DATE		
A	DATE 5/22/85		
tandy		DWG NO 8000253	SIZE D
		SCALE —	SHEET 1 OF 1

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	——	RELEASE FOR PRODUCTION	5/22/85	
	A	U3- +5v WAS +12v; ADDED PIN NO'S. PER TCO SI2776 kn	5/20/86	



NOTES:
1. COMPONENTS WITHIN DASHED BOX USED ONLY FOR INTERNATIONAL VERSION.
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DRAFT	DATE	TITLE	SCHEMATIC— RS-232 COMBO TANDY 1000
CHECK	DATE		PROJECT NO. 652
DESIGN	DATE		
APPD	DATE		
APPD	DATE		
tandy		DWG NO 8000253	SIZE D
		SCALE ——	SHEET 1 OF 1

652

WESTERN DIGITAL
C O R P O R A T I O N

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

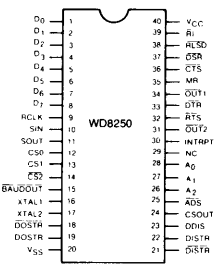
The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

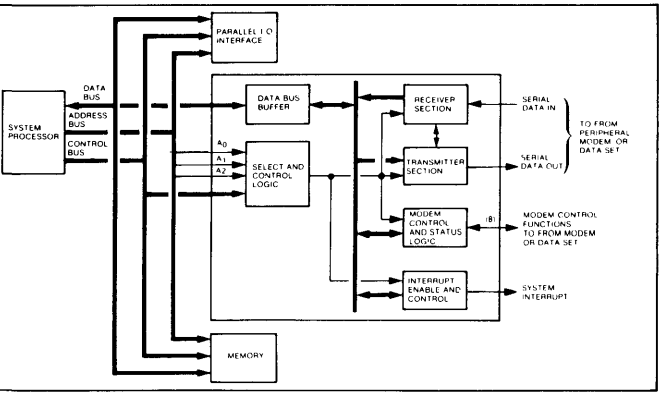
Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.



PIN DESIGNATION



WD8250 GENERAL SYSTEM CONFIGURATION

PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for register. Select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$) NOTE: An active $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	V_{CC}	+5 Volt Supply.

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe (ADS pin 25): When low provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: An active $\overline{ADS}$ input is required when register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, tie this input permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is CS0, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

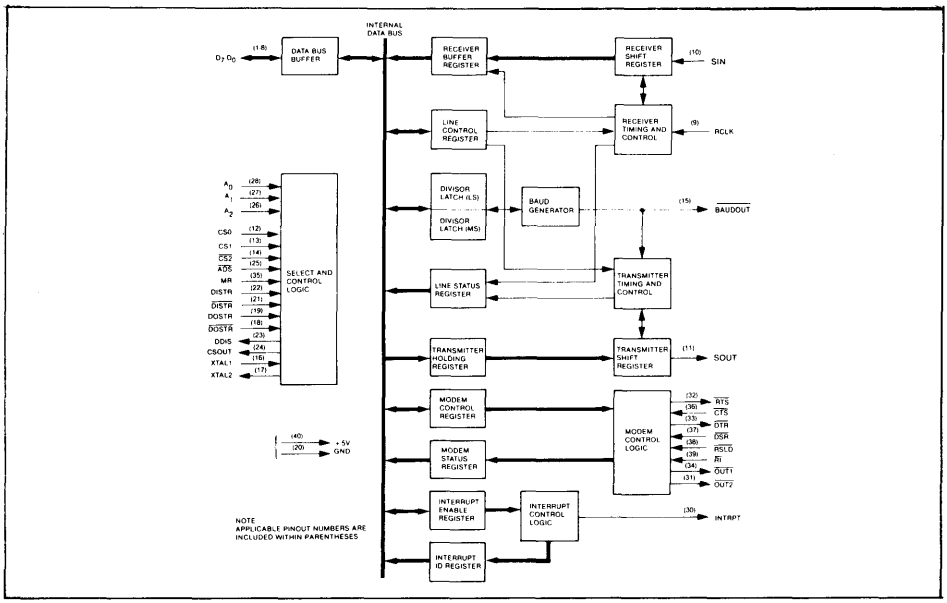
WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.



WD8250 BLOCK DIAGRAM

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT}} \cdot \text{RCLK} \cdot \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode. Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 2. Summary of WD8250 Accessible Registers

	Register Address									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB 1	1DLAB=1
Bit No	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	**Data Bit 0***	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interurpt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of a read of the Receiver Buffer Register.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1. Bit 1 is reset to logic 0 upon a write to the Transmitter Holding Register.

Table 5. Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the HIGH IMPEDANCE state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

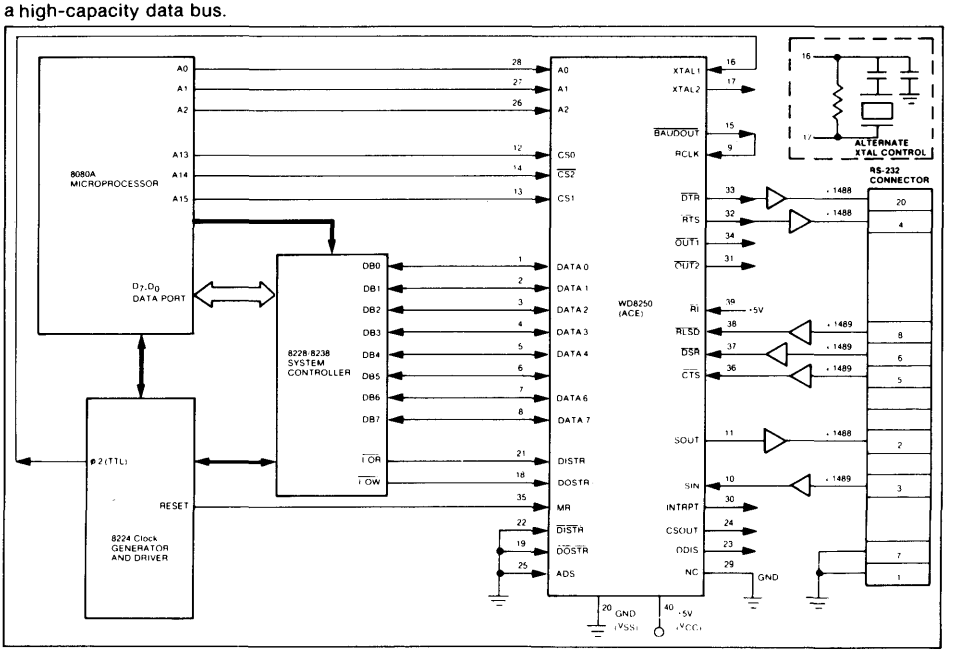


FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

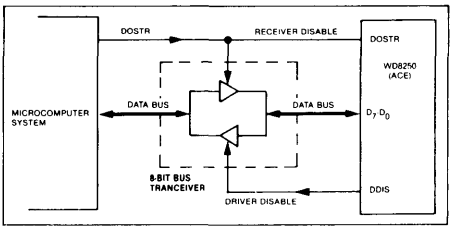


FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

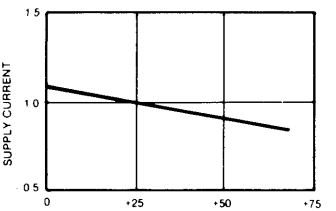
Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

Typical Supply Current vs. Temperature, Normalized

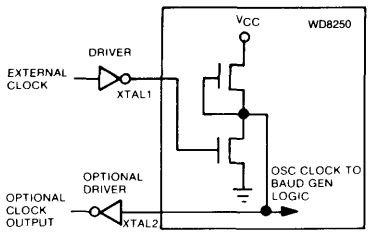


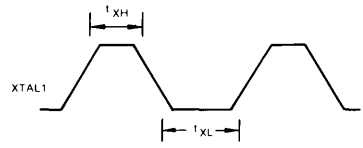
AC Electrical Characteristic T_A = 0°C to +70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	Units	Test Conditions Min	Max	
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{AH}	Address Hold Time	ns	0		1TTL Load
t_{CSS}	Chip Select Output Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = t_{ACS} + t_{DID} + t_{DIW} + t_{RC} + 20 ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = t_{ACS} + t_{DOD} + t_{DOW} + t_{WC} + 20 ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}	Chip Select Output Delay from Select	ns		260	1TTL Load
t_{DIC}	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load

Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100pF Load
t_{LW}	Baud Output Down Time	425 Typ		ns	100pF Load
t_{HW}	Baud Output Up Time	330 Typ		ns	100pF Load
Receiver					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	µs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	µs	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt	.250	1 typ	µs	100pF Load
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1 typ	µs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1 typ	µs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
T_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1 typ	µs	100pF Load
Modem Control					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output	.250	1 typ	µs	100pF Load

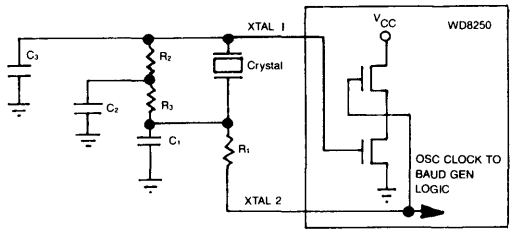
t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1 typ	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)	.250	1 typ	μs	100pF Load





Timing	Min	Units
tXH	100	ns
tXL	115	ns

FIGURE 3. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	O.SM	O.SM	40-60pF	O.OuF	10-30pF

FIGURE 4. TYPICAL CRYSTAL OSCILLATOR NETWORK

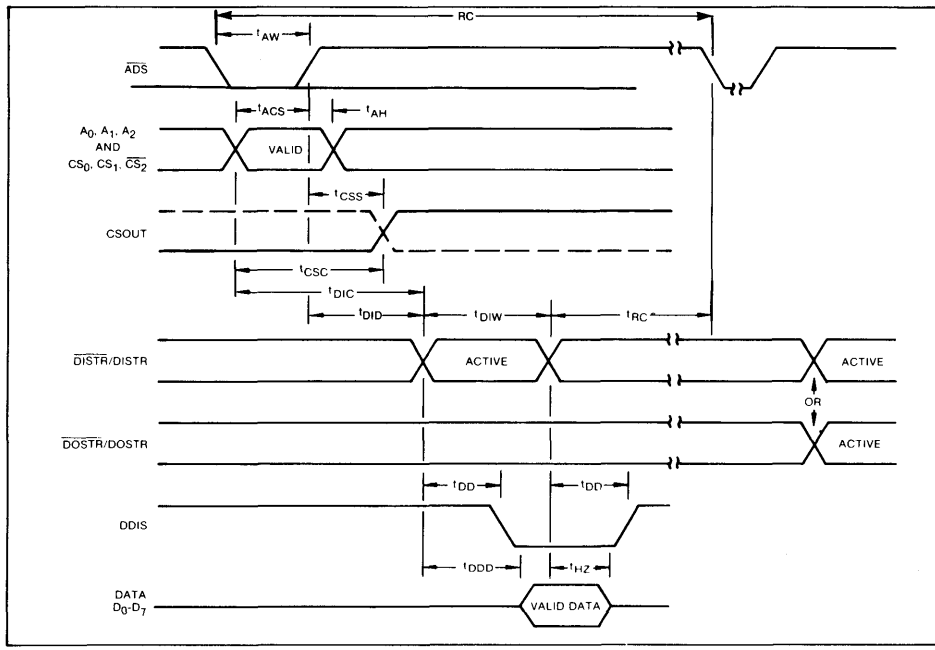


FIGURE 5. READ CYCLE TIMING

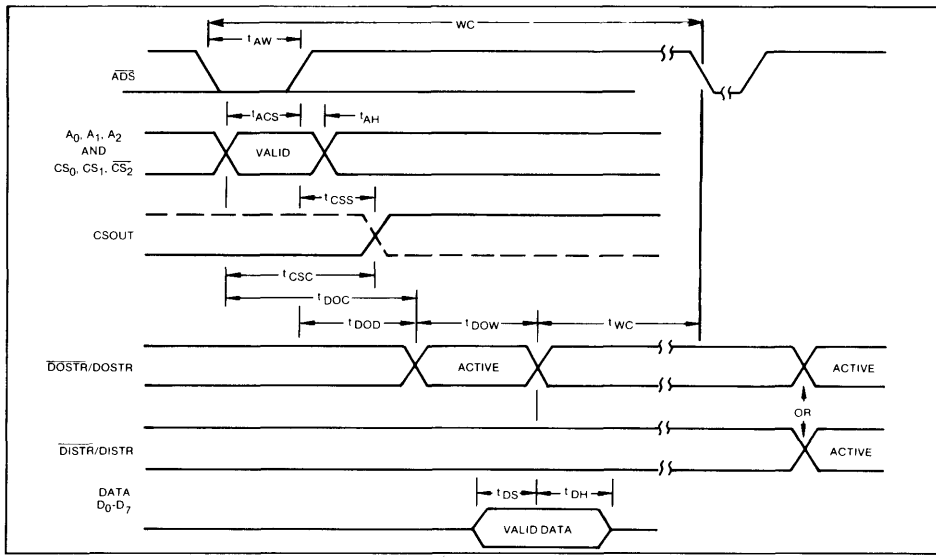


FIGURE 6. WRITE CYCLE TIMING

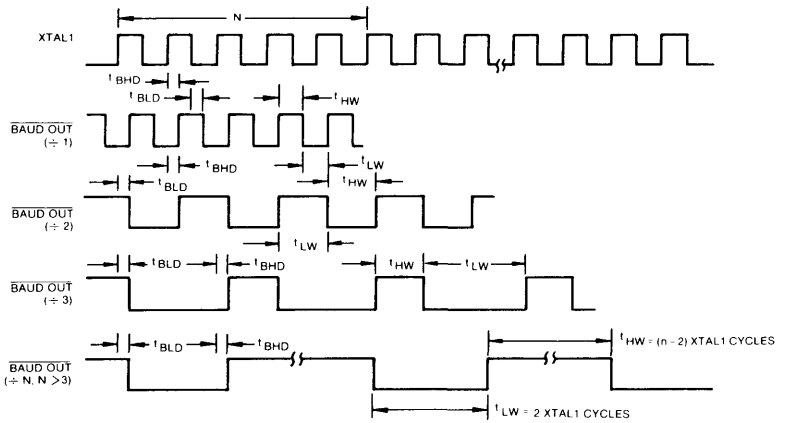
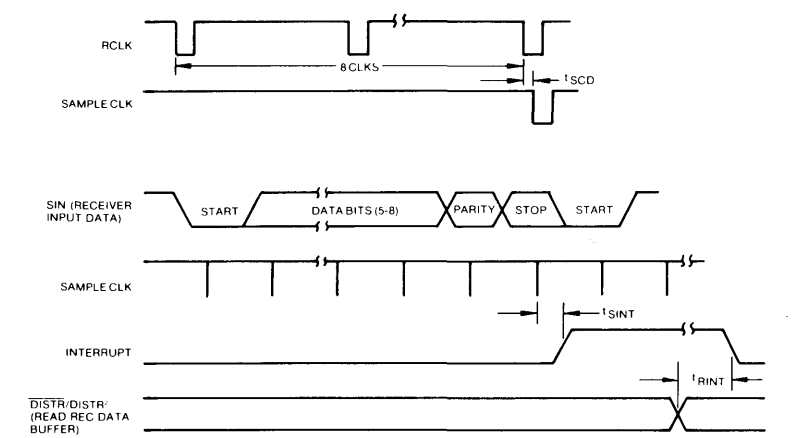
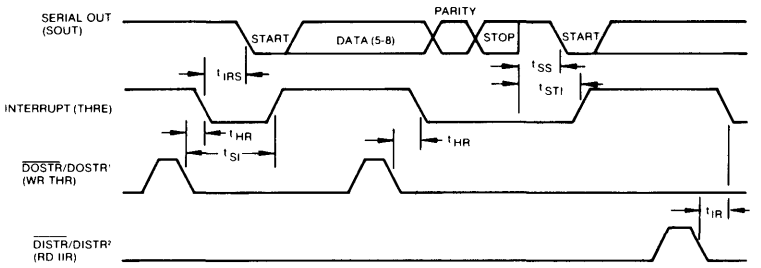


FIGURE 7. BAUDOUT TIMING



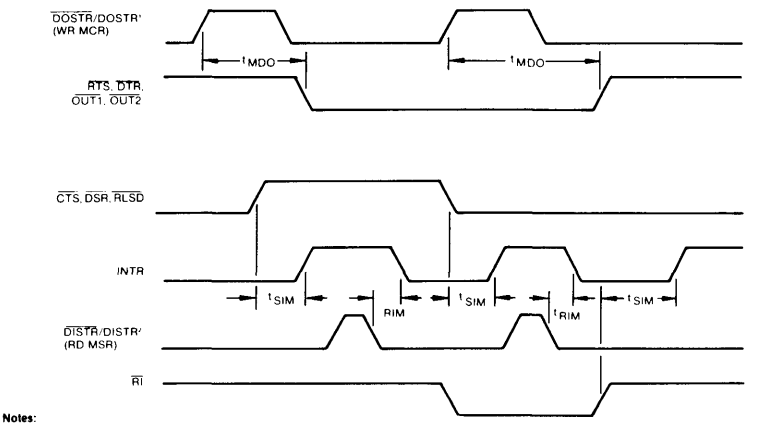
Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 8. RECEIVER TIMING



Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

FIGURE 9. TRANSMITTER TIMING



Notes:
¹See Write Cycle Timing
²See Read Cycle Timing

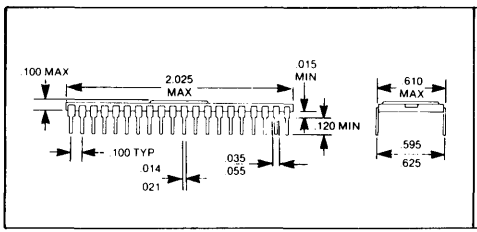
FIGURE 10. MODEM CONTROLS TIMING

ORDERING INFORMATION

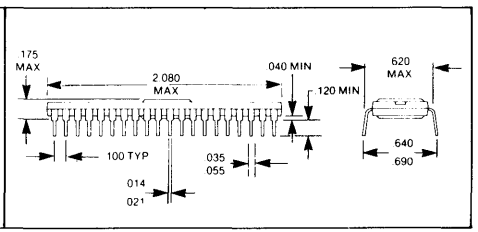
Part Number	Max Clock Rate[1]	Bits/Character
WD8250*-00	3.1 MHz	5, 6, 7, 8
WD8250*-20	3.1 MHz	6, 7, 8
WD8250*-30	500 kHz	5, 6, 7, 8

NOTES:

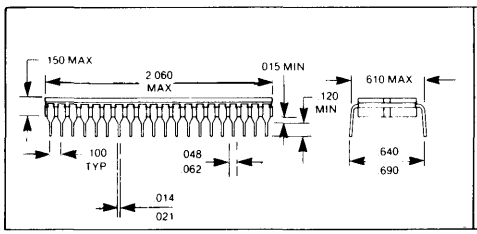
1. This is the maximum clock rate that can be applied to pins 16 or 17.
   * Consult your local Western Digital Sales Representative for information regarding package availability, price, and delivery.



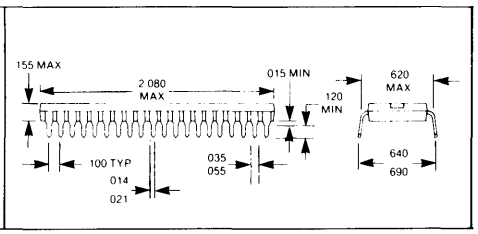
40 LEAD CERAMIC "A" or "AL"



40 LEAD RELPACK "B" or "BL"



40 LEAD CERDIP "CL"



40 LEAD PLASTIC "P" or "PL"

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Tandy® 1000 Mouse Controller/Calendar

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1/ Introduction

The Mouse Controller/Calender Board interfaces the DIGI-Mouse pointing device (Cat. No. 26-1197) to the Tandy 1000. The application programs that require the DIGI-Mouse pointing device can be used on the Tandy 1000. Also the battery backed clock/calendar allows the user to run the software provided on the diskette that comes with the owner's manual.

2/ Specifications

Dimensions: Standard half size board (5 x 4.2 inches).

Battery: 3.0-Volt Lithium coin cell, type CR2320 (Cat. No. 23-163). The battery life is one year.

Processor: 8042 8-bit single chip processor.

Clock Speed: 7.16 MHz

Ambient Temperature Range:
55° to 95° F (12° to 35° C)

Storage Temperature Range:
-40° to +160° F (-40° to 71° C)

3/ Theory of Operation (Hardware)

Look at the block diagram (Figure 1) and the clock/calendar schematic while reading the information below.

Bus I/F

Data, address, and control signals of the 1000 interface bus are buffered by U9 (an octal bus transceiver) and U7 (an octal buffer/line driver with 3-state outputs).

Chip Select and Reset Logic

The address lines are decoded by U2, U5, and U6. When the 1000 writes or reads to Ports 2FC or 2FE, a chip select signal is generated at Pin 6 of U2. The chip select controls U9 (the data buffer) and U3 (the 8042 processor).

During DMA cycles, the AEN signal from the 1000 bus, disables the chip select signal at Pin 1 of U7. An active AEN signal disables the 1Y outputs of U7, causing the A08 signal from Pin 12 of U7 to float and be pulled high by R20. U5 then inverts the A08 signal, ensuring that the chip select is disabled during DMA.

One half of U1 (a dual D-type flip-flop) is used in a "divide by 2" configuration. The 14.32 MHz oscillator signal from the 1000 interface bus is divided in half for a clock speed of 7.14 MHz, to be used by the 8042 processor. The 7.14 MHz clock is at Pin 5 of U1.

The other half of U1 is used as a reset latch. A reset signal is provided for the 8042 processor by ORing together the System Reset signal from the computer interface bus and the signal from the reset latch at Pin 11 of U2. The 8042 processor can be reset by a system reset or a write to I/O port 2FF. A write to I/O port 2FD clears the reset signal.

8042 Processor

In the heart of the option board is the 8042 processor (U3). This processor acts as an input port for serial information from the DIGI-Mouse and the Clock/Calendar chip (U8). It then translates this information to a parallel format and controls its transfer to the computer interface bus. The Clock/Calendar option board uses interrupt request IRQ3 to inform the 1000 when it is ready to transfer data.

DIGI-Mouse Buffers and Filters

A 9-Pin DB jack at J2 connects the DIGI-Mouse to the clock/ calendar board. RC filtering is used to reduce noise in the inputs. U4 (a CMOS hex schmitt trigger) provides further buffering and waveshaping of the DIGI-Mouse inputs, which are interfaced to the processor chip through its peripheral port bits P10 to P16.

Clock Chip

The Phillips-Signetics Clock/Calendar Chip (U8) interfaces directly to U3 at its peripheral port bits P17, P20-P23, and P27. The time base for the clock chip is a 32.768 KHz crystal, which is similar to that found in watches. The battery **MUST** be installed for the clock function to work. When a power failure occurs, the chip indicates this by sending a low-battery signal (POWF) to the 8042 processor.

4/ Theory of Operation (Software)

User specifications:

- The motion sensor is oriented with the connecting cable and buttons pointing away from the user, the positive x axis extends to the right and the positive y axis extends toward the user.
- Minimum motion allowed before it is detected is 1/79 of an inch along either axis. This distance is called a tick.
- The minimum unit of time for the Clock/Calendar chip is 1 minute. Maximum accuracy is ± 1/2 minute. The units of time accepted by the chip are minutes, (24) hours, day of month, and month.
- There are 3 modes for the mouse's motion data and button data that can be transfered to the host: the full interrupt mode, the initial interrupt and poll mode, and the poll only mode.
- To communicate with the clock/calendar chip, the user employs the set time command and a read time command.

I/O Ports used by the Clock/Calendar Board:

8042 Data Port	2FC
8042 Command/Status Port	2FE
8042 Set RESET 8042 Port	2FF
8042 Clear RESET 8042 Port	2FD

Layout of the 8042's status port (2FE):

Read by the 8088:

Bit #0 = Output register full flag (OBF)	1=full
Bit #1 = Input register full flag (IBF)	1=full
Bit #2 = F0 flag - not used	
Bit #3 = F1 flag - command flag	1=input to port 2FE
Bit #4 = Primary button status	1=button up
Bit #5 = Secondary button status	1=button up
Bit #6 = Tertiary button status	1=button up
Bit #7 = Calendar power status	1=power has failed

Written to by the 8088:

This is the same as for the data written to Data Port 2FC, except the F1 (command) flag in 8042's status port is set.

Output:

When sending data or commands from the 8088 to the 8042, the following procedure must be used:

1. Check the status port (2FE) of the 8042 to see if the input port full flag is set (Bit 1).

2. If the flag is set, wait until the 8042 clears it. If it is not cleared within 1 millisecond, reset the 8042 chip because it is locked up.

3. If the flag is clear, proceed.

4. Check the length of the command. If it is equal to 1, then send the data to 2FE, and stop here.

5. If the length equals 2 or more, then send the data to 2FC, and proceed.

6. Wait until the input port full flag is cleared by the 8042 before sending the next byte of data to 2FC.

7. When the length equals 1, send it to 2FE, and stop here.

Formats of Commands to the 8042:

Command	Header	Data
Set Time	01h	All data must be in BCD format. 1st byte = minutes. 2nd byte = hours (24 hour clock). 3rd byte = day of the month. 4th byte = month.
Read Time	02h	None Returns data packet "R".
Set Mouse Motion Interrupt and	08h	Output is 2 bytes. 0 = disable function. 1 - 255 = net number of "ticks" to be moved before interrupt is triggered. Returns data packet "M".

Button Interrupt		0 = disable function. 1 - 255 = enable function Returns data packet "B".
Set Timer Interrupt	20h	Outputs 1 byte of data 0 = disable function. 1 - 255 = enable function Returns data packet "A".

(Timer is set to interrupt approximately 40 times per second if the data is available to send.)

What is happening:

The 8042 is interrupted every time data is written to the input port 2FC (or 2FE, which set the command flag). The 8042 moves the data from the input register into the input buffer and increments a counter. It then returns to the point in the mouse data sampling and processing cycle at the point of interruption.

During each cycle, the 8042 checks the command flag to see if a command has been received. If the command flag is set, the 8042 checks the header byte to determine which command is in its input buffer. It then compares the counter to the number of bytes in that command. If any of these tests fails, the 8042 resets the pointer to the input buffer, clears the counter and the command flag, and continues with its normal cycle. If all the tests succeed, the 8042 jumps to the routine that handles that command. Each command has the requirement to reset the buffer pointer, the counter, and the command flag, and then return control to the normal process.

Input:

Data transfer between the 8042 and the main processor (8088) uses the interrupt mode, the poll mode, or both. The 8042 interrupts the 8088 by toggling Port 21h, Bit 3, which is connected through a buffer to the 8259A interrupt controller chip. The clock/calendar board uses IRQ3 as an interrupt. Internally, the 8042 knows if the 8088 has read/written a byte from/to it by checking the status of the OBF/IBF flags. Three procedures are available to transfer the data from the 8042 to the 8088. They are discussed below.

Mode 1: Full interrupt mode

This mode uses the interrupt line to signal each byte to be transmitted. As each byte is transmitted, the common procedure below is executed except Mode 3 must have the latched interrupt cleared after each byte is processed. This mode may be the fastest mode when only the clock interrupt is actively being triggered.

Mode 2: Initial interrupt and poll mode

This mode uses the interrupt line to signal the start of a data packet, and polls the rest of the packet. It clears the latched interrupt only after all the data packet is transmitted. It uses the common procedure outlined below.

Mode 3: Poll only mode

This mode does not use the interrupt signal at all. It uses only the output register full flag in the 8042's status register (Port 2FE).

Common procedure:

The 8088 must have the following initialized before any interrupt mode is used:

- A hardware interrupt vector at 002C.
- An interrupt controller at port 21 (ANDed with a F7).

The 8042 has a data packet set up in its output buffer and begins transmitting by placing the "header" into the output register (Port 2FC). Placing the header byte into the ouput register sets the output register full flag in the status register (Port 2FE, Bit 0) and sends a signal on the interrupt line to the 8088 (via the 8259A). The 8042 begins its normal processing cycle, testing the output register full flag on each cycle.

If the flag is set, the 8042 sends another signal on the interrupt line. If the flag is cleared and the packet still contains data to send, the 8042 places the next data byte into the output register and sends a signal on the interrupt line to the 8088. If the flag is cleared and the data packet is empty, the 8042 does NOT send an interrupt signal, but continues with its normal processing.

On the 8088 side, the "mouse" interrupt has a priority behind the 8253 timer, keyboard, and hard disk. This means that when the interrupt enters its routine, the higher-level interrupts can be enabled. The interrupt handler routine should do all the following:

- Ensure that the 8042 generated the interrupt by checking the status of its output register full flag.
- Identify the type of data packet by its "header" byte and switch to the appropriate routine when the entire data packet is received.
- After the data packet has been processed, clear or reset the buffer pointers, counters, and the latched interrupt.

Format of Data Packets from the 8042:

Data Packet	Header	Data
Mouse data		4 bytes of data
All data	"A"	1st byte = MSB of Delta x
Motion data only	"M"	2nd byte = LSB of Delta x
		3rd byte = MSB of Delta y
		4th byte = LSB of Delta y

(The button data is found in the status register (Port 2FE.)

Mouse data		none
Button data only	"B"	data found in status register (Port 2FE bits # 4, 5, 6)
Read time data	"R"	4 bytes of data in BCD format 1st byte = minutes 2nd byte = hours (24-hour clock) 3rd byte = day of month 4th byte = month

Initialization Procedures of 8088:

The following hardware and software interrupts should be initialized:

Description	Address	Type
Hardware interrupt vector (INT 0B)	002C	Doubleword Pointer
Application interrupt vector (INT 33)	00CC	Doubleword Pointer
Hardware interrupt controller (IRQ3)	Port 21	(reset Bit 3)
Video display interrupt (INT 10)	0040	Doubleword Pointer

Operation of the Clock/Calendar:

When the 8042 receives either the Set Time or Read Time command, it shuts off all other operations until it is finished with the command. All the resources of the 8042 are required to communicate with the clock/calendar chip.

In the Set Time command, the 8042 breaks up the 4 bytes of time data into 4 packets and sends them serially a bit at a time. Upon completion, the 8042 resumes normal operation.

In the Read Time command, the 8042 sets up bit serial communications with the clock/calendar chip and builds 4 time data packets. The 4 packets are converted to bytes and placed in the output buffer behind the "R" header byte. The 8042 sets up a Read Time data packet to be sent to the 8088 and returns to normal operation.

If the power fails, the calendar power status bit in the status register (Port 2FE Bit 7) is set. First, check to see if the power failure is temporary. (Perhaps the battery lost contact with the clock circuit because of a bump or jarring of the equipment.) To check for temporary failure, issue a Set Time command. If the power failure bit goes to zero everything is normal. If the power failure bit is not reset, then the battery either is dead or is dislodged from its holder clip. After replacing or resetting the battery, issue the Set Time command to ensure proper operation.

Operation of the 8042:

Upon power up/RESET, the 8042 initializes the system by zeroing all RAM and clearing all flags, ports, and registers. It then sets up the default conditions and enters the normal mouse data processing cycle, which follows:

1. The 8042 takes a copy of the Mouse/Clock/Calendar data port (P1) and saves a copy.

2. It then checks to see if there is any change in the status of the buttons. If there is, the 8042 sends a copy to the status register.

3. Next, the 8042 determines the Delta x changes or Delta y changes. Both Deltas use the same process.

4. The 8042 retrieves the copy of Port P1 and compares the bit pattern of xA and xB to the old copy to see if any changes have occured. If a change has occured, then the 8042 determines whether the change is +1, -1, or null. (Null occurs when the 8042 misses 2 state changes of xA and xB.)

5. The Delta x (or y) working accumulator (+-32735 units) is then either incremented or decremented respectively. A null result does not affect the accumulators.

6. At this point, the 8042 checks the event-triggered data polls for motion and button data. If either occurred, then the 8042 transfers the values in the working accumulators to the output buffer behind the appropriate header byte and clears the working accumulators to zero. If not, then the 8042 checks to see if any input from the 8088 has been received by checking the F1 command flag. If there is input in the input buffer, the 8042 tests the header to see which bit is "on" and jumps to the routine that handles that command.

7. After checking for input, the 8042 then checks the internal timer to see if anything has timed out. Two items are connected to the timer flag, the 8042 and the timed data transfer interrupt. All outputs to the 8088 are tied to the timer. Each time the timer times out, the 8042 checks the output register full flag to see if it is set. If the flag is set, the 8042 sends off a signal on the interrupt line to the 8088, resets the timer, and returns to normal operation. The 8042 checks to see if it needs to send any more data. If it does, it moves the next data byte to the output register, sends a signal on the interrupt line, and returns to normal operations. If the output buffer is empty, the 8042 simply returns to normal operation. Connected to the timer is the timed data transfer interrupt. When the timer interrupt is enabled, the 8042 also checks to see if the timer has timed out. If it has, then the 8042 transfers the mouse data from the working accumulators to the output buffer behind the header byte and ships it to the 8088. It then clears the working accumulators and returns to the start of the cycle.

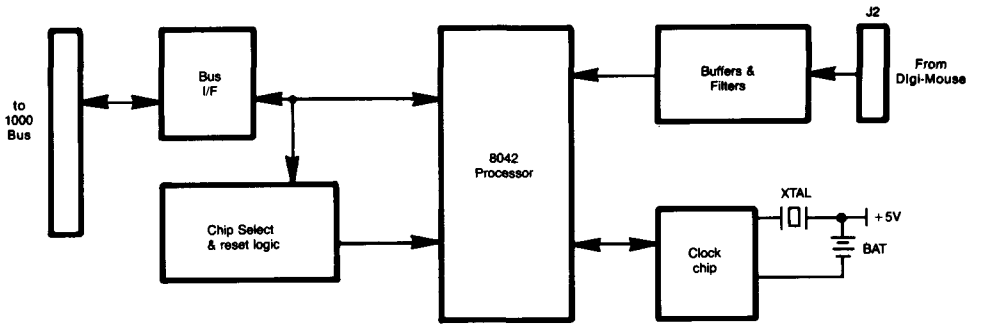


Figure 1

DIGI-Mouse/Clock Controller Board
Block Diagram I/F

5/ Alignments

A Frequency Counter with a timer function is necessary for a correct alignment. To ensure an accurate time base, the trim capacitor (C19) is set at the factory. If you need to replace Y1, U8, or C19, adjust C19 for an average waveform period of 7.8125 milliseconds at Pin 11 of U8.

The oscillator will not be loaded by the test instrument because the Signetics SAB3019 Clock/Calendar chip provides a buffered oscillator output at Pin 11 that is divided by 256. The frequency at Pin 11 should be 128 Hz. Since this is a low frequency, most frequency counters are more accurate if their timer fuction is used.

No other alignments need be made. When installing the board, however, take normal precautions against static electricity discharge.

6/ Troubleshooting

If the board is malfunctioning, check to see that the clocks are present at both the 7.16MHz signal at Pin 3 of U3 and the 128Hz at Pin 11 of U8. Note: For correct operation of the clock function, the battery must have a minimum charge of 2.75 volts and make complete contact with the battery socket clip. The chip select signal at Pin 6 of U2 can be tested by using a short Basic program to access Ports 2FCh or 2FEh. Access to Ports 2FF or 2FD should generate a pulse at Pin 11 of U1. Although the inputs to CMOS (U4) are well protected, a large discharge could damage the CMOS. Swapping the processor or clock chip with known good devices can help you isolate the problem.

7/Clock/Calendar Component Side

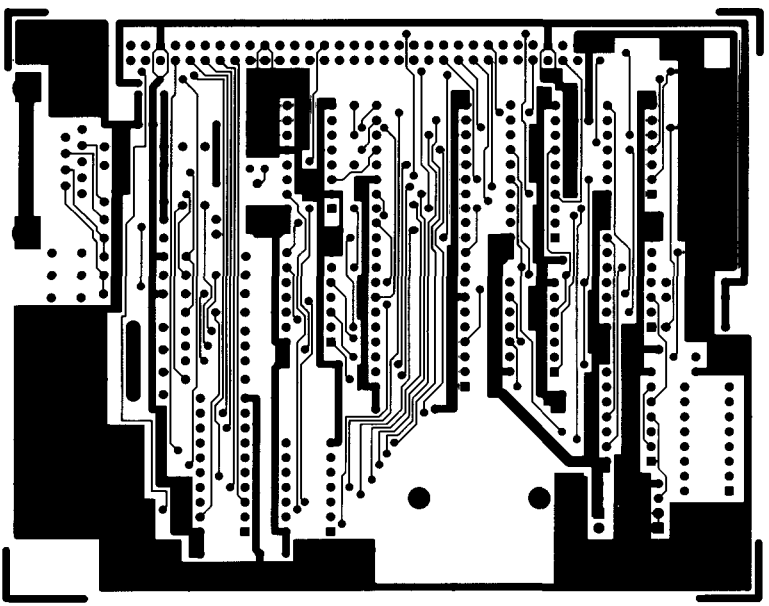


Figure 2

Clock/Calendar Solder Side

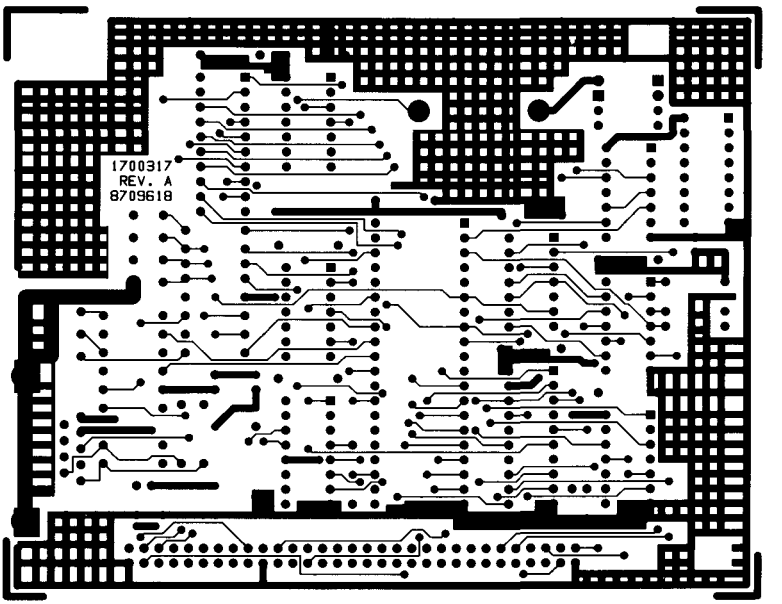


Figure 3

Clock/Calendar Silkscreen

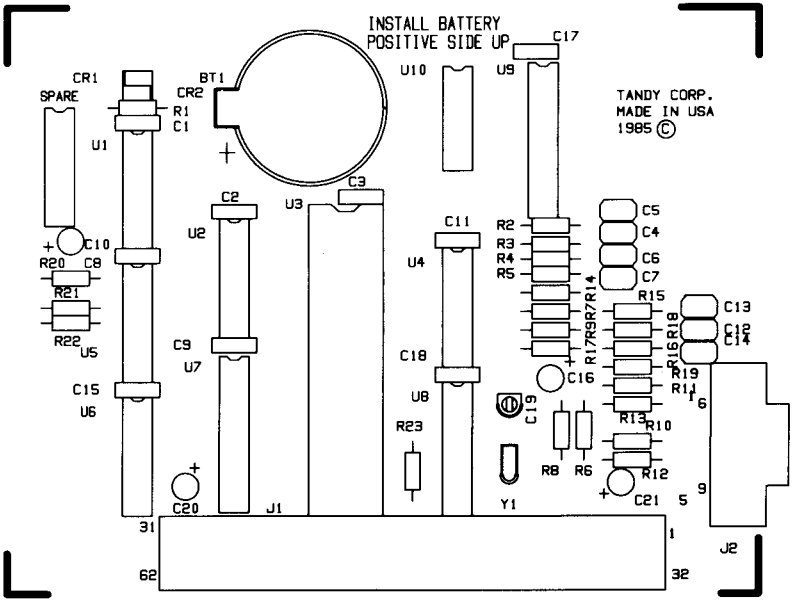
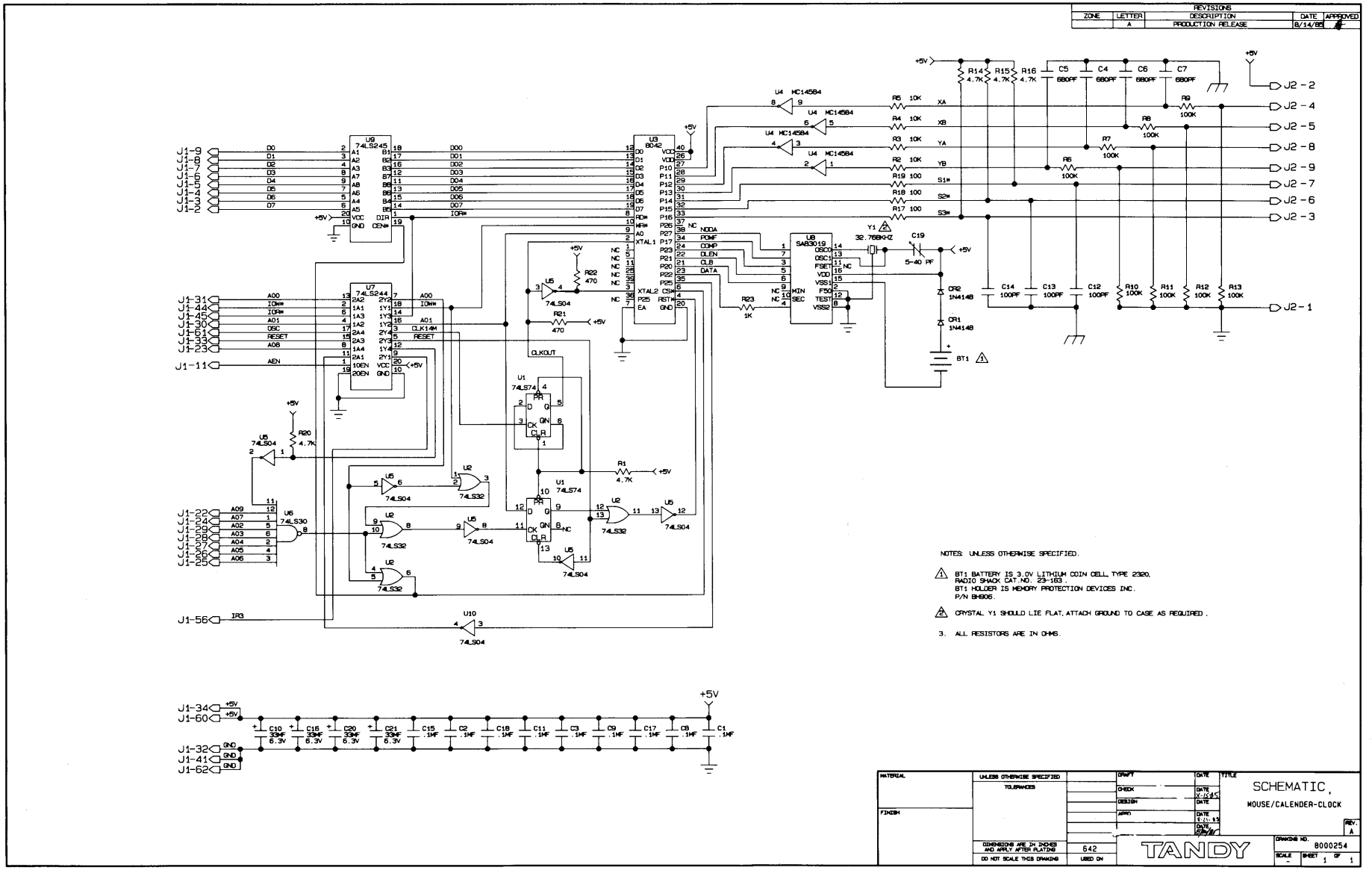


Figure 4

Clock/Calendar Schematic



8/ Parts List

Tandy 1000 Mouse/Clock/Calendar
Catalog Number 25-1015

SYMBOL	QTY	DESCRIPTION	PART NO.
		DIGI MOUSE CONT./COMBO BD. REV. A	
		SCREW #4-40 X 1/4" ZINC	AHD-2991
	2	SCREWS (PANEL) #4-40 X 3/8	AHD-2222
	2	NUTS, 4-40	AHD-7166
	3	STANDOFF, NYLON PCB	AHC-2429
		STANDOFF, #4-40 HEX	AHC-2259
BT1	1	BATTERY 3.0V #23-16	ACS-0103
BT1	1	SOCKET, PCB MOUNT	AJ-7056
C1-3,8,9, 11,15,17, 18	9	CAPACITOR 0.1 MFD 50V MONO AXIAL	CC-104JJLA
C4-7	4	CAPACITOR 680 PFD 50V 20%	CC-681MJCP
C10,16, 20,21	4	CAPACITOR 33 MFD 6.3V TANTALUM RAD.	CC-336KBTP
C12-14	3	CAPACITOR 100 PFD 5% 50V	CC-101JJCP
C19	1	CAPACITOR 5-40 PFD TRIM	ACF-7370
CR1-2	2	DIODE 1N4148	DX-0022
J1	1	RECEPTACLE	AJ-4052
J2	1	CONNECTOR DB9 MALE RT. ANGLE (9-PIN) METAL SHELL, GROUNDING DETENTS AND STRAP, 4-40 THREADED INSERTS	AJ-5062
R1,14-16, 20	5	RESISTOR 4.7K OHM 1/4 WATT 5%	N-0247EEC
R2-5	4	RESISTOR 10K OHM 1/4 WATT 5%	N-0281EEC
R6-13	8	RESISTOR 100K OHM 1/4 WATT 5%	N-0371EEC
R17-19	3	RESISTOR 100 OHM 1/4 WATT 5%	N-0132EEC
R21-22	2	RESISTOR 470 OHM 1/4 WATT 5%	N-0169EEC
R23	1	RESISTOR 1K OHM 1/4 WATT 5%	N-0196EEC

SYMBOL	QTY.	DESCRIPTION	PART NO.
U1	1	IC 74LS74 FLIP FLOP	MX-3808
U2	1	IC 74LS32 QUAD 2-IN OR	MX-6183
U3	1	IC 8042 PROCESSOR	MX-6884
U3	1	SOCKET 40-PIN DIP	AJ-6580
U4	1	IC MC14584 CMOS HEX INVERTER	MX-6207
U5,10	1	IC M74LS04P HEX INVERTER	AMX-3552
U6	1	IC 74LS30 8-IN NAND	AMX-3556
U7	1	IC 74LS244 OCTAL BUS TRANSCEIVER	AMX-3864
U8	1	IC SAB3019 CAL/CLK	MX-6178
U8	1	SOCKET 16-PIN DIP	AJ-6581
U9	1	IC 74LS245 OCTAL BUFFER	AMX-4470
Y1	1	CRYSTAL 32.768 KHz.	MX-1113
Y1	1	STAKING PIN (GROUND FOR CRYSTAL)	AHB-9682

PLUS Network 4 Interface

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Theory of Operation 2

Installation Instructions 5

Parts List 11

P.C. Board 13

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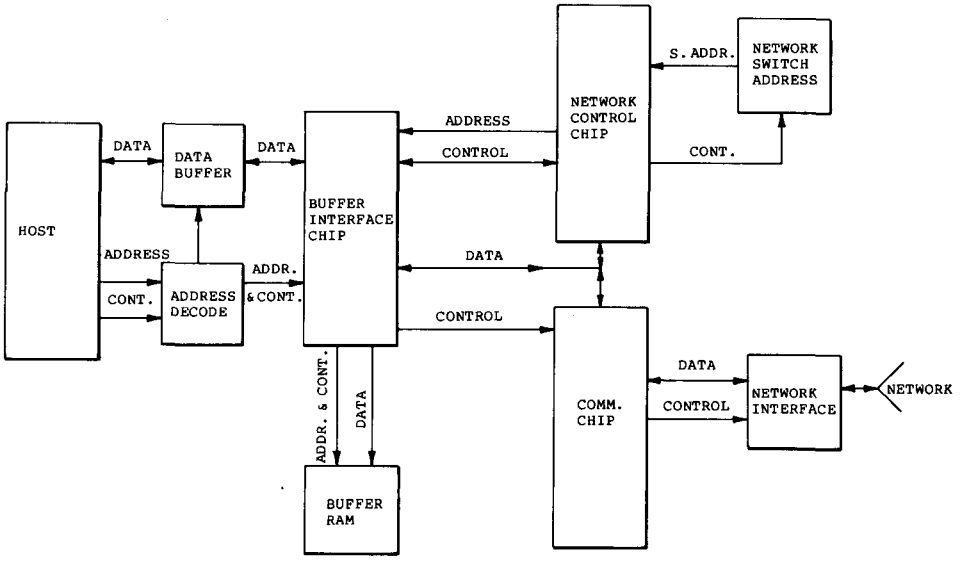
INTRODUCTION

PLUS Network 4 is Local Area Network (LAN) system for communication between as many as 64 units, all operating asynchronously at a clock rate of 1 MHz. The 64 units are tied together by twisted pairs of wires. This network is interconnected through the Tandy 1000's 62-pin option slot. This interconnection is hardwired at the I/O addresses 0248-024F, and ties the Tandy 1000 to the CORVUS chip set which does most of the data formatting and recognizes the network protocol.

Insert block diagram.



THEORY OF OPERATION

Address Decode

Address decoding uses ICs U15, U16, and U17 to decode I/O port addresses. The outputs are then gated with *IOW and *IOR signals. Read and write operations are as follows:

I/O Port	Read & Write Operation
248	Read Transporter Status Byte
249	Read RAM
24A	Read the Counter Saver Byte
24B	Read RAM, Increment the Counter by 1.
248	Write the Counter High Byte
249	Write to the CAR
24A	Write the Counter Low Byte
24B	Write to RAM, Increment the Counter by 1.

Interrupt Operation

The PLUS Network 4 Interface board supports the following interrupts.

I/O Port	Interrupt Operation
24C	Disable interrupts
24D	Clear current interrupt request
24E	Enable interrupts (All three operations can be done by reading or writing with meaningless data.)
24F	Interrupt status Bit 4 set => interrupt pending Bit 5 set => interrupts disabled

Boot ROM /Buffer RAM

The PLUS Network 4 Interface board has a 2K-byte boot ROM (U11) and 4K-bytes of buffer RAM (U1, U2). ROM extends from host CPU address DF000 to address DFFFF and uses the first 1024 bytes of the 4K buffer RAM.

PLUS Network 4 Interface

The PLUS Network 4 Interface uses two components, (U10) which is a differential driver and receiver, and a transformer (T1), which acts as a filter. Note that since the input is a differential (as is the output) and the data is NRZI, which depends solely on transmission, the connector pins may be reversed on a unit without any effect to data transmission. The network interface is the lowest level of the network architecture.

Communications

The Comm. Chip, a CORVUS 68A54 Advanced Data Link Controller Chip, (U5) mainly encodes and decodes network data and monitors the network status for CRC errors, etc. This device constitutes the second level of the network architecture.

Network Control

The Network Control Chip, a CORVUS 6801 Chip, (U4) forms the network interface intelligence by monitoring the output of the Comm. chip (U5) and handling the header information. It handles the header information by communicating with the host side by a "command vector" in the buffered RAM and a message as to where to find the vector (sent via the C.A.R.). This device constitutes the third level of the network architecture.

Buffer Interface

The Buffer Interface Chip, a CORVUS 3131 Gate Array Chip, (U3) controls the timing and bus control for interfacing the users of the buffer RAM. It may be thought of as a two port memory controller, interfacing the host and the CORVUS 6801 chip with memory. In addition, the buffer interface chip also gates, times, and controls signals to each to facilitate their part of the interface.

Installation Instructions

Introduction

Adding the PLUS Network 4 Interface to your computer allows you to communicate with up to 64 units, all operating asynchronously at 1 MHz., via the Network 4 LAN (local area network).

The PLUS Network 4 Interface is readily installable by you. However, you can have the kit installed by the service technicians at your Radio Shack Service Center. Having service technicians install the kit not only ensures expert installation, but also enables them to quickly check that all the equipment is functioning properly.

Installation

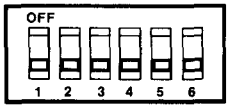
Caution should be exercised in low humidity environments to prevent damage to electronic parts by static electricity being discharged through them. Discharge any built-up static electricity by touching a grounded metal object before proceeding further.

Warning: Turn off all equipment. Turn the power off and disconnect the power cord from the wall socket. If the computer is on, you could damage the central processing unit, as well as your PLUS Network 4 Interface board.

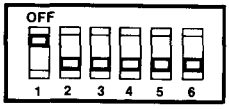
Before proceeding with the installation of the PLUS Network 4 Interface, be sure the kit contains the PLUS Network 4 Interface board, a terminal block and 2 star washers, 2 wing nuts, an alternate mounting bracket and 2 mounting screws, and 3 plastic standoffs (for the Tandy 1000 SX).

On the PLUS Network 4 Interface board locate the jumper at J1 which selects the interrupt that is to be used. Be sure the jumper is set to interrupt 3 (IR3) as this interrupt is recognized by the software.

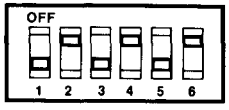
Also on the PLUS Network 4 Interface board, find DIP Switch SW1 (in the mounting bracket) which selects the station number. The settings on the DIP switches are a binary encoding of the numbers 0 to 63 (decimal). Each dip switch represents a digit in the 6 bit binary number. A switch set to down or "OFF" equals bit on or binary "1". Switch SW1-1 is the least significant bit. See the switch setting examples in Figure 1.



Station 0



Station 1



Station 42

Figure 1.

Note: On each PLUS Network 4 Interface board set these SW1 switches to a **unique number** of 0-63. **Be sure to record the switch settings for each computer.** The software currently selects station 63 as the disk server, therefore, we recommend that the stations be set at 0-62.

When installing the PLUS Network 4 Interface board in the Tandy 1000 SX:

1. Remove the 2 screws on the front of the computer. Then remove the computer's cover by tilting it away from you and lifting it clear of the slot. See Figure 2.

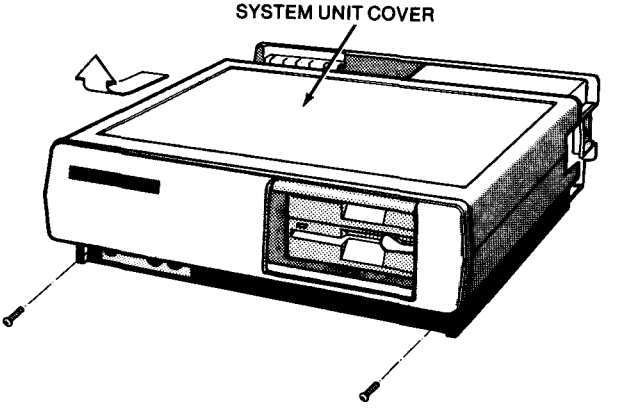


Figure 2.

2. If you are going to use an installed Memory PLUS Expansion board (Cat. No. 25-1011) as the carrier board for the PLUS Network 4 Interface board remove the Memory PLUS Expansion board from its slot.

3. Remove the mounting bracket from this Memory PLUS Expansion board.

4. Disconnect the small harness assembly from the pins of J2 on the PLUS Network 4 Interface board.

5. Remove the mounting bracket from the PLUS Network 4 Interface board.

6. Remove the nuts, plastic washers (plain and shouldered), small harness assembly and screws from the mounting bracket.

7. Install these screws, plastic washers, nuts and the small harness assembly on the supplied alternate mounting bracket as shown in Figure 3. The polarity on the wire harness does not matter, therefore, either ring terminal on the wire harness can be used with either screw. Be sure the shouldered plastic washers are seated in the bracket holes so that the screws are insulated from (that is, do not touch) the mounting bracket. Also be sure that the harness wires do not show through the switch setting opening in the mounting bracket.

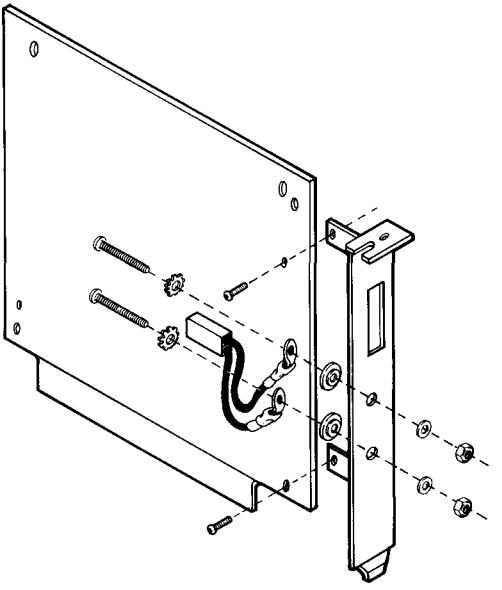


Figure 3.

8. Install the alternate mounting bracket on the carrier board, either the:

   PLUS Upgrade Adapter board, Cat. No. 25-1016, or

   the Memory PLUS Expansion board, Cat. No. 25-1011, (if you have one)

   using the 2 screws that mounted the old bracket.

9. Plug the small harness into the PLUS Network 4 Interface board.

10. Install the 3 standoffs in the PLUS Network 4 Board. Then carefully install the PLUS Network 4 Interface board on the carrier board by aligning the pins and the connector and pressing the PLUS Network 4 Interface board down firmly but gently to seat it.

11. If necessary remove the option slot cover of an unused expansion slot. Carefully insert the carrier board in the empty slot. Secure the mounting bracket of the carrier board to the chassis with the screw that held the slot cover on. See Figure 4.

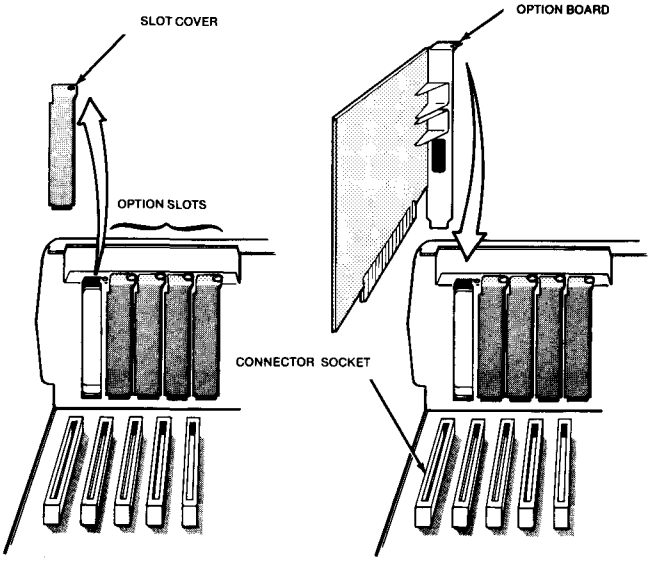


Figure 4.

12. Slide the terminal block over the 2 screws that protrude from the back of the computer, with the flat side of the block with 2 round indentations facing to the outside. See Figure 5.

13. Slip the 2 star washers over the protruding screws, with the teeth facing toward the terminal block. Also install the 2 wing nuts on the ends of the screws.

14. Install a strand of the network cable between the terminal block and the star washer on one of the protruding screws and tighten the wing nut. Do likewise for the other cable strand, protruding screw and wing nut.

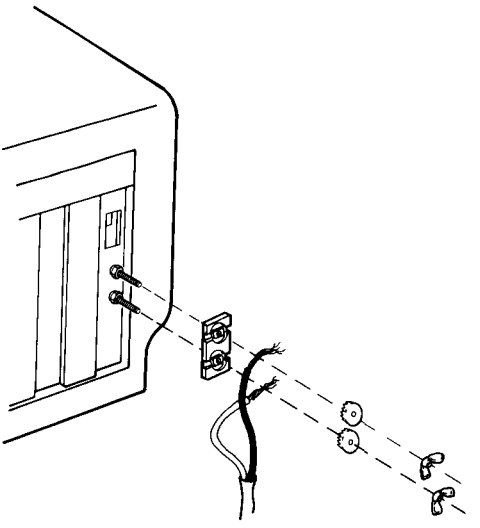


Figure 5.

15. Reinstall the computer's cover, securing it with the screws previously removed.

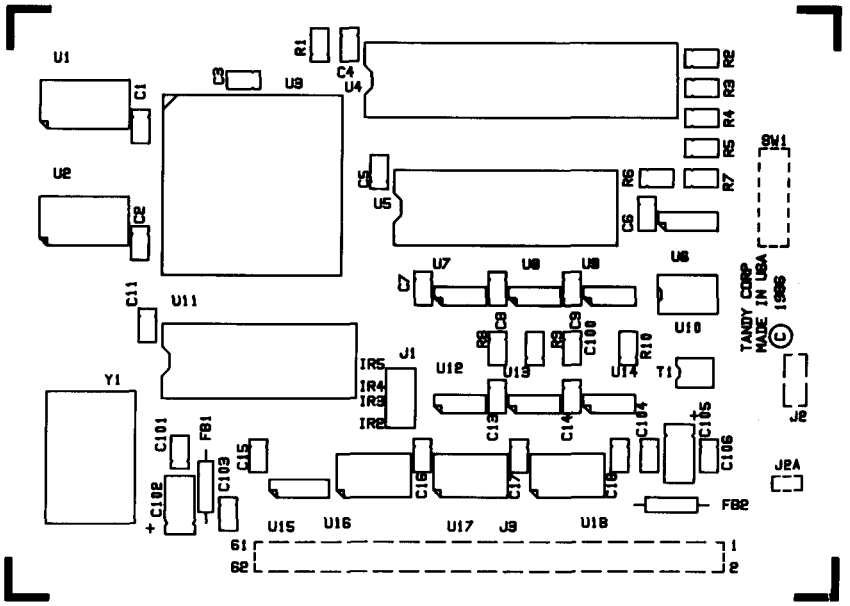
The PLUS Network 4 board is now ready for use. See the PLUS Network 4 Interface Owner's Manual.

TANDY 1000 Network SMT Parts List

Symbol	Description	Part No.
	PC Board, T1000 Network SMT	8859002A
C1-9,11,13-18, 101,103,104,106	Capacitor 0.1 MFD 50V Axial	X37410341
C102,105	Capacitor 33 MFD 10V Tant.Rad.	X33633310
C100	Capacitor 220 PFD	X30122241
FB1,2	Ferrite Bead	8419013
J1	Staking Pin	8529014
J2	Connector 2-Pos. Rt. Angle	8519308
J3	Connector, Recepticle 2 X 31	8519257
R1	Resistor 3K Ohm 1/8W 5%	X20323030
R2-7	Resistor 22K Ohm 1/8W 5%	X20332230
R8,10	Resistor 2.2K Ohm 1/8W 5%	X20322230
R9	Resistor 1K Ohm 1/8W 5%	X20321030
SW1	Switch, 12-Pin 6 POS DIP Rt. Angle	8489087
T1	Transformer	8417001
U1,2	SOWIC, 4016 2KX8 Static RAM	X04016020
U3	IC, Corvus Chip Set #2 (3131)	8
U3	Socket 68-Pin	8509020
U4	IC, Corvus Chip Set #3 (MC6801)	8
U4	Socket 40-Pin	8509002
U5	IC Corvus Chip Set #1 (MC6854)	8
U5	Socket 28-Pin	8509007
U6	SOIC, 74LS367	X02367000
U8	SOIC, 74LS125	X02125000
U7	SOIC, 74LS08	X02008000
U9	SOIC, 74LS04	X02004000
U10	IC, SN75176	8050176
U11	IC, TMS2732A 300NS	8
U11	Socket 24-Pin	8509001
U12	SOIC, 74LS21	X02021000
U13	SOIC, 74LS32	X02032000
U14	SOIC, 74LS74	X02074000
U15	SOIC, 74LS138	X02138000
U15	Socket 8-Pin	8509011
U16,17	SOWIC, 74LS688	X02688000
U18	SOWIC, 74LS245	X02245000
Y1	Oscillator, 10 MHz	8409041

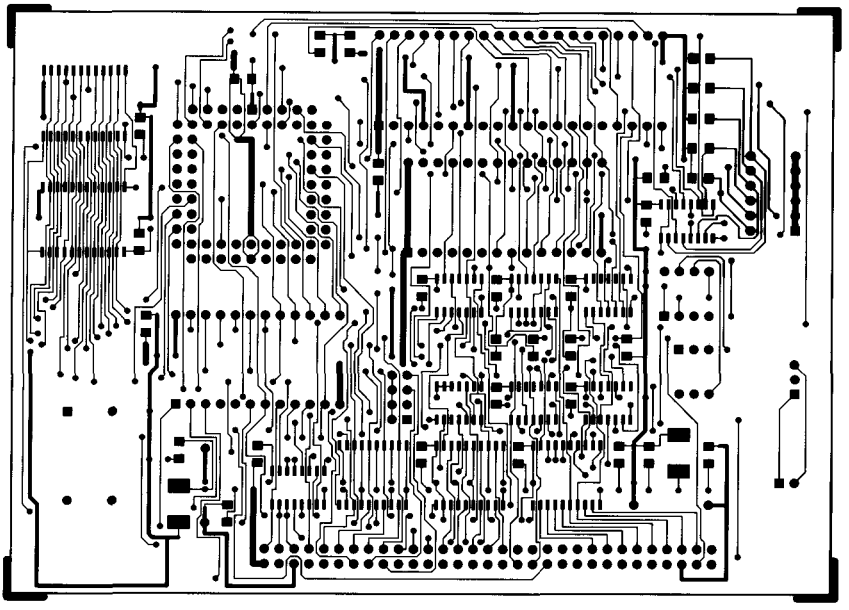
TANDY 1000 Network SMT Parts List

Symbol	Description	Part No.
	Bracket,	8729601
	Bracket,	8729572
	Standoff, Pastic	8590164



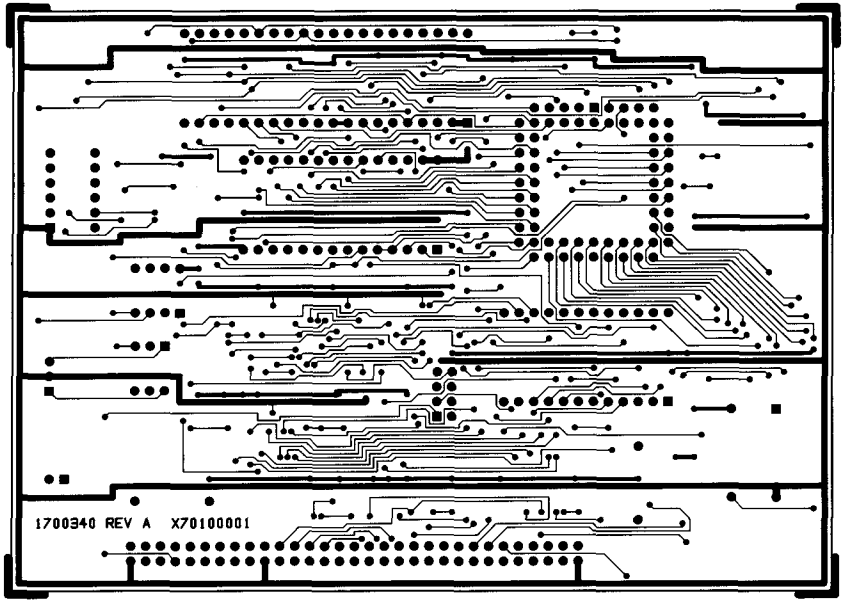
TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804 DATE: 06/17/86	C/S SILKSCREEN
TITLE: NETWORK	
DWG. NO.: 1700340 REV.A	
PART NO.: X70100001	
DESIGN GRID: x=.025 y=.025	
DESIGNER: GM DD	
INSP	

PLUS Network 4 Interface Board - Silkscreen



TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804 DATE: 06/17/86	LAYER 1 COMPONENT SIDE
TITLE: NETWORK	
DWG. NO.: 1700340 REV. A	
PART NO.: X70100001	
DESIGN GRID: x=.025 y=.025	
DESIGNER: GM DD	
INSP	

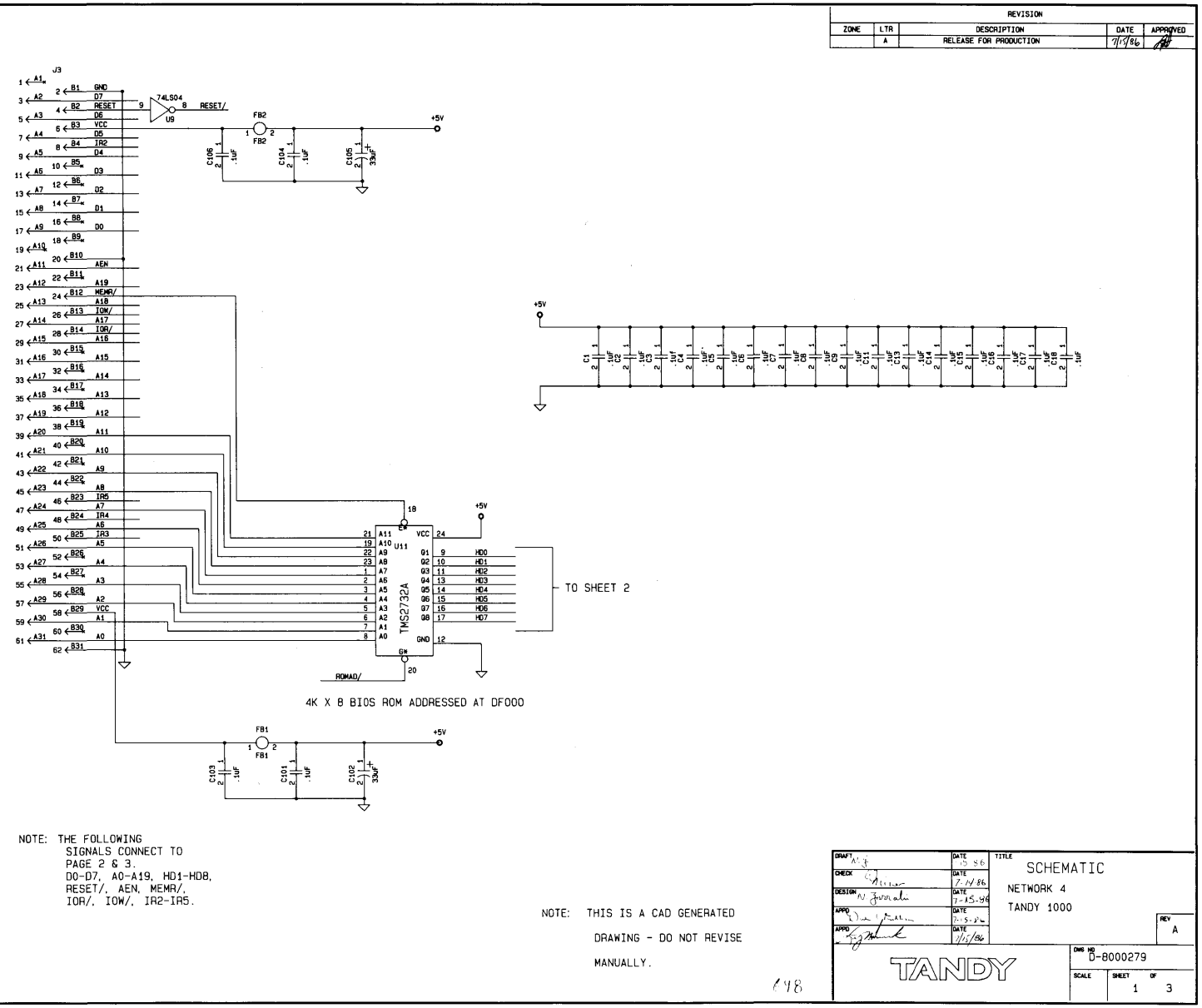
PLUS Network 4 Interface Board - Component Side

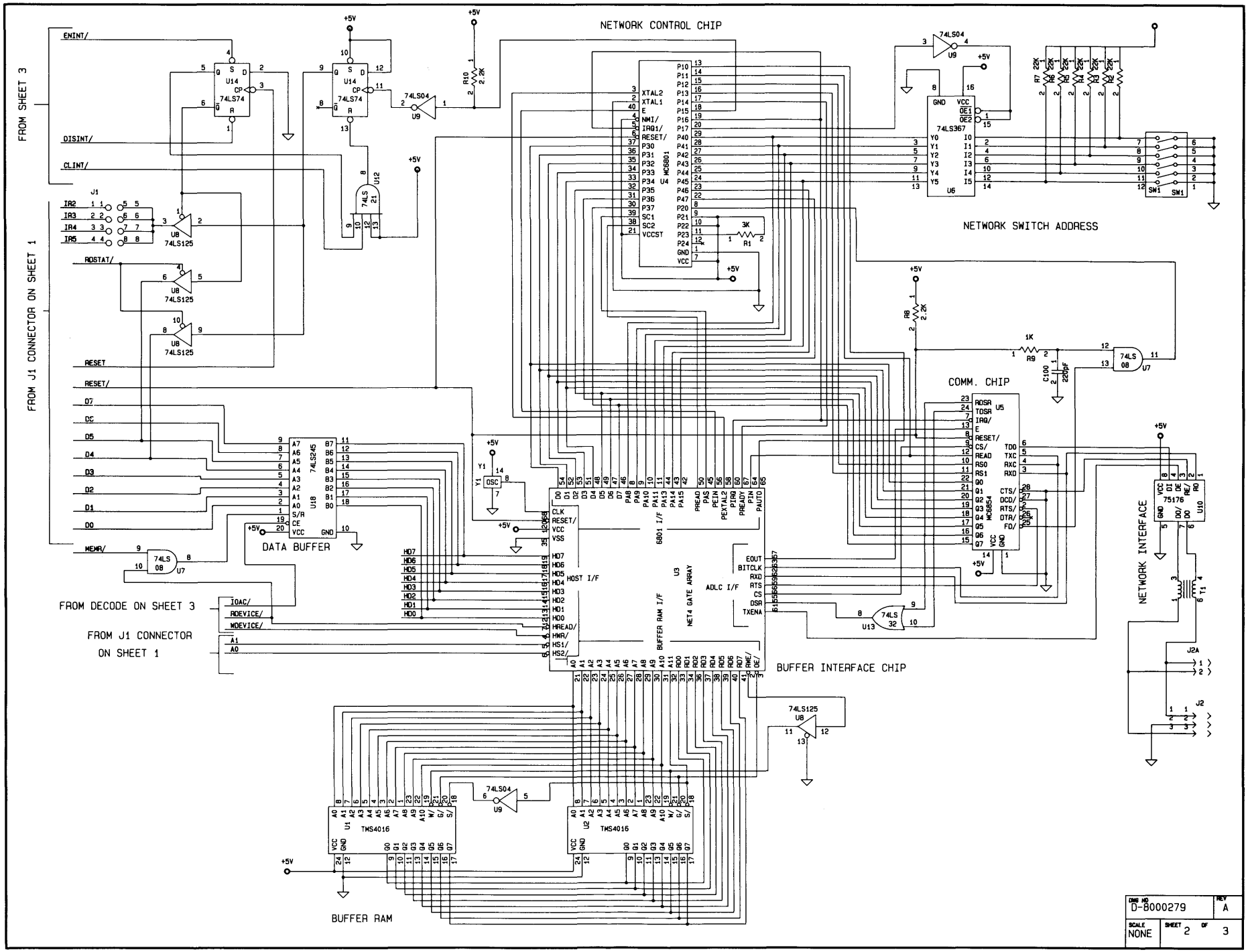


TANDY SYSTEMS DESIGN FILMWORK	FAB. SPEC.: TSD-C262-2
PROJECT NO.: 804 DATE: 06/17/86	
TITLE: NETWORK	
DWG. NO.: 1700340 REV. A	
PART NO.: X70100001	
DESIGN GRID: x=.025 y=.025	LAYER 2 SOLDER SIDE
DESIGNER: GM DD	
INSP	

PLUS Network 4 Interface Board - Solder Side

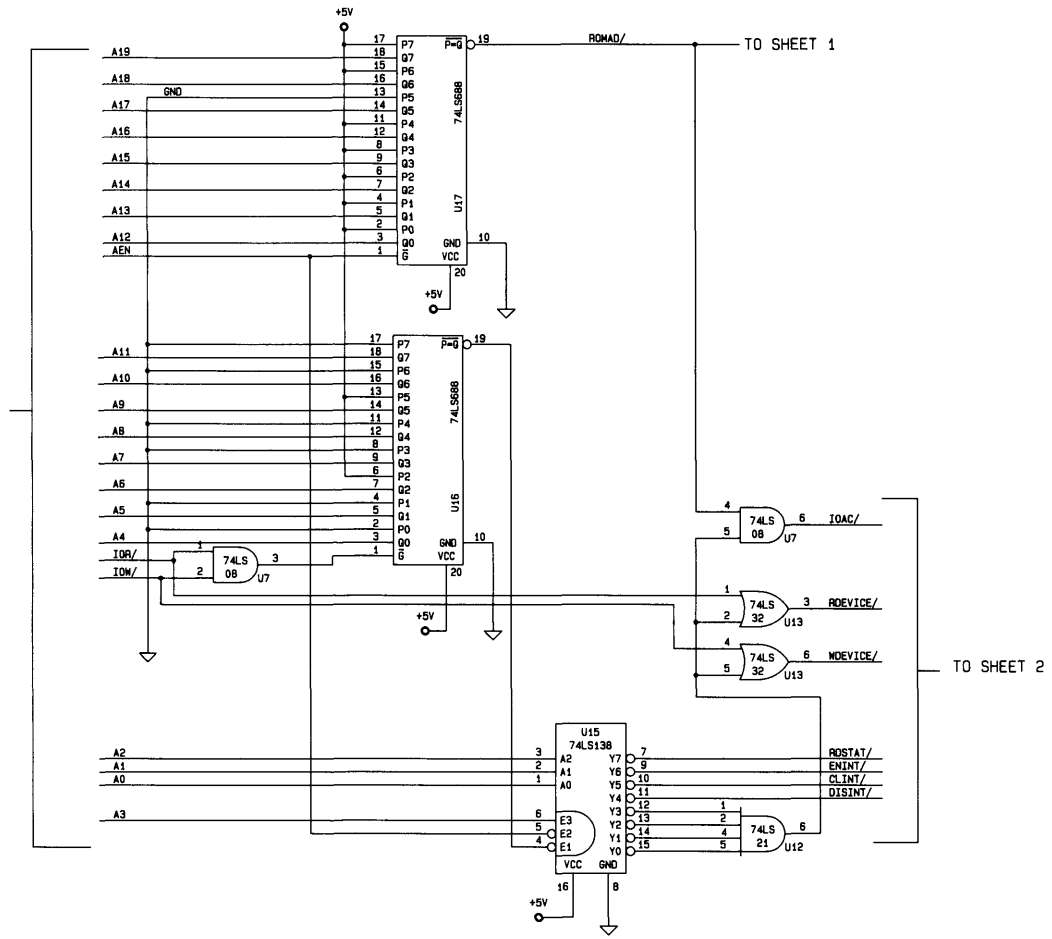
Schematic


REVISION
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | RELEASE FOR PRODUCTION | 7/1/86
J3
74LS04
U9
RESET/
FB2
+5V
C106 1uF
C104 .1uF
C105 33uF
C1 .1uF
C2 .1uF
C3 .1uF
C4 .1uF
C5 .1uF
C6 .1uF
C7 .1uF
C8 .1uF
C9 .1uF
C10 .1uF
C11 .1uF
C12 .1uF
C13 .1uF
C14 .1uF
C15 .1uF
C16 .1uF
C17 .1uF
C18 .1uF
TMS2732A
U11
ROMAD/
TO SHEET 2
4K X 8 BIOS ROM ADDRESSED AT DF000
FB1
C103 .1uF
C101 .1uF
C102 33uF
NOTE: THE FOLLOWING SIGNALS CONNECT TO PAGE 2 & 3. D0-D7, A0-A19, HD1-HD8, RESET/, AEN, MEMR/, IOR/, IOW/, IR2-IR5.
NOTE: THIS IS A CAD GENERATED DRAWING - DO NOT REVISE MANUALLY.
TITLE SCHEMATIC
NETWORK 4
TANDY 1000
REV A
DWG NO D-8000279
SCALE
SHEET 1 OF 3
TANDY


NETWORK CONTROL CHIP
NETWORK SWITCH ADDRESS
COMM. CHIP
NETWORK INTERFACE
DATA BUFFER
BUFFER INTERFACE CHIP
BUFFER RAM
HOST I/F
ADLC I/F
BUFFER RAM I/F
NET4 GATE ARRAY
6801 I/F
FROM SHEET 3
FROM J1 CONNECTOR ON SHEET 1
FROM DECODE ON SHEET 3
FROM J1 CONNECTOR ON SHEET 1
ENINT/
DISINT/
CLINT/
RESET
RESET/
RDSTAT/
MEMR/
IOAC/
RDEVICE/
WDEVICE/
HREAD/
HWR/
HS1/
HS2/
74LS125
74LS04
74LS367
74LS08
74LS32
74LS245
74LS74
TMS4016
MC6801
MC6854
75176
SW1
J1
J2
J2A
U1
U2
U3
U5
U6
U7
U8
U9
U10
U12
U13
U14
U18
Y1
R1
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
C100
3K
1K
2.2K
22K
220pF
+5V
DMG NO
D-8000279
REV
A
SCALE
NONE
SHEET
2
OF
3

	A19	A16	A15	A12	A11	A8	A7	A4	A3	A0	
ROM	1101	1111	XXXX	XXXX	XXXX						(DF000)
	1100	0000	XXXX	XXXX	XXXX						(C0000)
I/O	XXXX	XXXX	0010	0100	0XXX						(240)
	XXXX	XXXX	0010	0100	1XXX						(248)
	XXXX	XXXX	0011	0110	0XXX						(360)
	XXXX	XXXX	0011	0110	1XXX						(368)
	110R	RRRR	XXXX	XXXX	XXXX						TWO ADDRESSES
	XXXX	XXXX	001I	01IO	SDDD						FOUR ADDRESSES

X = DON'T CARE
R = ROM CHANGES 1 TO 0
I = I/O CHANGES 0 TO 1
S = STEP UP B
D = DECODE ADDRESS



DWG NO	REV
D-8000279	A
SCALE	SHEET 3 OF 3

DEVICES

DEVICES
CONTENTS

VIDEO CONTROLLER CHIP SPECIFICATION
DMA CHIP SPECIFICATION
PRINTER INTERFACE
KEYBOARD INTERFACE SPECIFICATION
TIMING CONTROL GENERATOR
8087 NUMERIC DATA COPROCESSOR

VIDEO CONTROLLER CHIP SPECIFICATION

VIDEO CONTROLLER CHIP SPECIFICATION
CONTENTS

GENERAL DESCRIPTION.....1
BLOCK DIAGRAM.....2
OPERATING MODES 3
PIN LIST.....24
LOGIC BLOCK DIAGRAM.....27
ELECTRICAL SPECIFICATIONS.....29
TIMING.....30

VIDEO CONTROLLER CHIP SPECIFICATION

GENERAL DESCRIPTION

The Tandy 1000 video controller chip is designed to operate with three types of display devices: A standard TV using an RF modulator, a composite monitor, and an RGBI 200 line Color monitor. This custom controller chip implements all of the video logic for the Tandy 1000 plus most of the system decode logic. Figure 1 shows a block diagram of the controller chip.

The video display system is very flexible and can be programmed for a number of video modes. These modes use varying numbers of colors (2,4 or 16). These 16 colors are defined by combinations of the RGBI as shown in the color chart below and can be used for the foreground color or background color. If you are using a black and white monitor, these colors will appear as shades of gray. In addition, any 1 of the 16 colors or shades of gray can be used for the screen border.

I	R	G	B	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Pink
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

TABLE 1 AVAILABLE COLORS TABLE

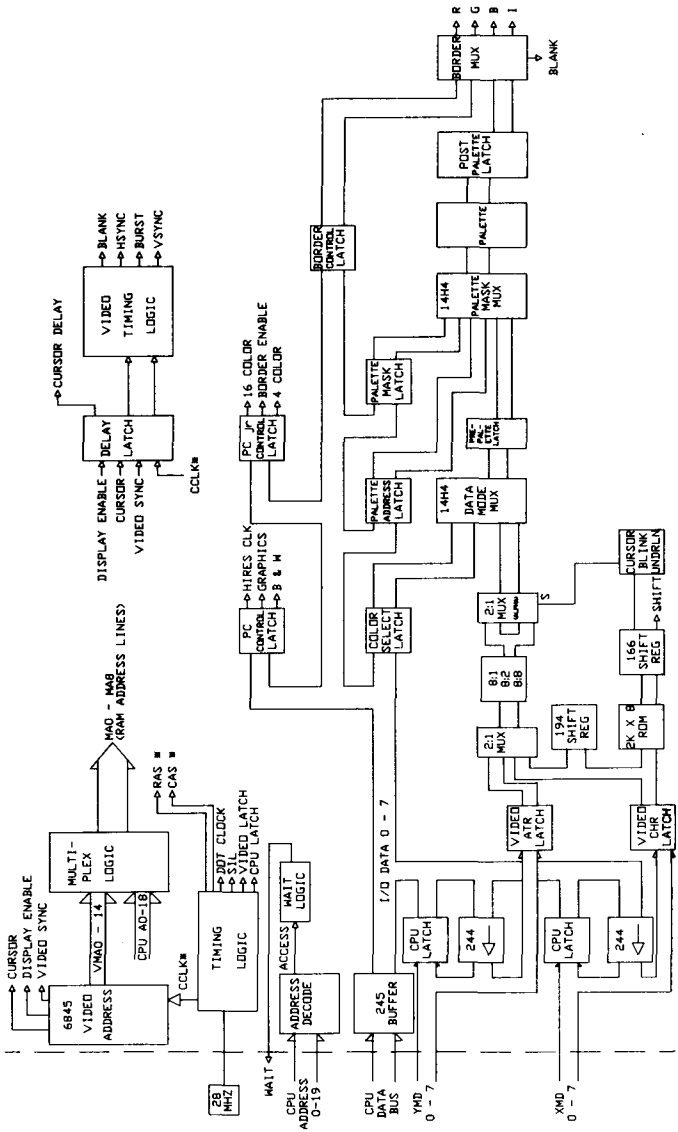


Figure 1. VIDEO CONTROLLER CHIP BLOCK DIAGRAM

OPERATING MODES

The operating modes supported by the Tandy 1000 video controller may be grouped in two categories: Alphanumeric and Graphic.

ALPHANUMERIC MODE

The Alphanumeric mode has two basic types of operation: 80 character by 25 rows, and 40 character by 25 rows. In both modes the characters are generated by a 256 character ROM. The character ROM is divided into the following groups:

* 96 Standard ASCII characters
* 48 Block Graphics characters
* 64 Foreign Language/Greek characters
* 16 Special Graphics characters.
* 32 Word Processing/Scientific Notation characters

In both modes all characters are 7 dots wide by 7 dots high and are placed in an 8 dot wide by 8 or 9 dot high matrix. In both the 40x25 and the 80x25 modes, two bytes of data are used to define each character on the screen. The even address (0,2,4 etc.) is the character code and is used in addressing the character generating ROM. The odd address (1,3,5 etc.) is the attribute byte, that defines the foreground and the background color of the character. The following chart shows how the attribute byte controls colors.

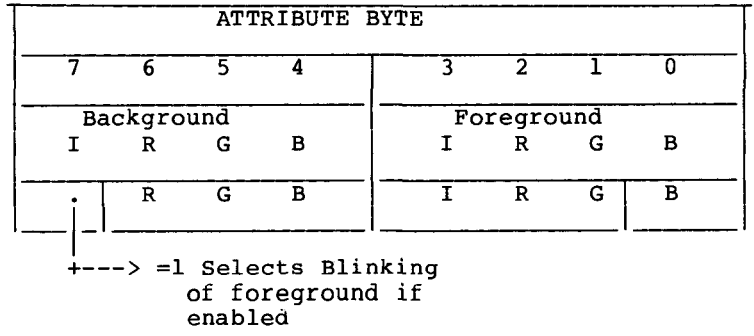


Table 2 ALPHANUMERIC MODE ATTRIBUTE BYTE DEFINITION

* Writing a 1 in bit 5 of register 'H3D8 enables Blinking

GRAPHICS MODE

The Tandy 1000 Video Controller chip can be programmed for a variety of modes.
The Tandy 1000 Computer family supports the following Graphics Modes:

MODE		IBM PCJR	IBM PC
4 Color Medium Resolution	320 x 200	X	X
16 Color Medium Resolution	320 x 200	X	
16 Color Low Resolution	160 x 200	X	
2 Color High Resolution	640 x 200	X	X
4 Color High Resolution	640 x 200	X	

GRAPHICS MEMORY USAGE

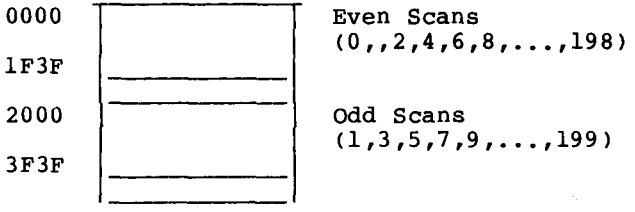
* 200 line Graphics Memory uses either 2 or 4 banks of 8000 bytes. In either case, pixel information for the display's upper left corner is found at address 0000.

```
####   The  4 Color High Resolution 640 X 200 and
####   The 16 Color Medium Resolution 640 X 200
####   use 4 banks of 8000 bytes as follows

(Hex) | <------160 Bytes------>

0000  ┌──────────────────────┐   00 Scans
      │                      │   (0,4,8,...,196)
1F3F  │______________________│
      │______________________│
2000  │                      │   01 Scans
      │                      │   (1,5,9,...,197)
3F3F  │______________________│
      │______________________│
4000  │                      │   10 Scans
      │                      │   (2,6,10,...,198)
5F3F  │______________________│
      │______________________│
6000  │                      │   11 Scans
      │                      │   (3,7,11,...,199)
7F3F  │______________________│
      │______________________│
```

```
####   The  2 Color High Resolution 640 X 200 and
####   The  4 Color Medium Resolution 640 X 200 and
####   The 16 Color Low Resolution 640 X 200
####   use only 2 banks of 8000 bytes as follows
```



2 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 2 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Available in the IBMPC and IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 2 of 16 possible colors
Requires 16K bytes of read/write memory
Formats 8 PELs per byte for each byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL

4 COLOR HIGH RESOLUTION 640 X 200 GRAPHICS MODE

The 4 Color High Resolution 640 X 200 Graphics mode may require a high resolution monitor for proper operation. Only supported on the IBM PCjr, this mode has the following characteristics:

Contains a maximum of 200 rows of 640 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 32K bytes of read/write memory
Formats 8 PELs per two bytes (1 even byte and 1 odd byte) in the following manner:

EVEN BYTES

7	6	5	4	3	2	1	0
PA0	PA0	PA0	PA0	PA0	PA0	PA0	PA0

First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL	Fifth Display PEL	Sixth Display PEL	Seventh Display PEL	Eighth Display PEL
PA1 7	PA1 6	PA1 5	PA1 4	PA1 3	PA1 2	PA1 1	PA1 0

ODD BYTES

16 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 16 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only and has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 32K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

16 COLOR LOW RESOLUTION 160 X 200 GRAPHICS MODE

The 16 Color Low Resolution 160 X 200 Graphics mode works with all types of display devices. This mode is available in the IBM PCjr only, with the following characteristics:

Contains a maximum of 200 rows of 160 PELs
Can display 16 of 16 possible colors
Each pixel selects 1 of 16 colors
Requires 16K bytes of read/write memory
Formats 2 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA3	PA2	PA1	PA0	PA3	PA2	PA1	PA0
First Display PEL				Second Display PEL			

4 COLOR MEDIUM RESOLUTION 320 X 200 GRAPHICS MODE

The 4 Color Medium Resolution 320 X 200 Graphics mode works with all types of display devices. It is available in the IBM PC and PCjr. This mode has the following characteristics:

Contains a maximum of 200 rows of 320 PELs
Can display 4 of 16 possible colors
Each pixel selects 1 of 4 colors
Requires 16K bytes of read/write memory
Formats 4 PELs per byte in the following manner:

7	6	5	4	3	2	1	0
PA1	PA0	PA1	PA0	PA1	PA0	PA1	PA0

First Display PEL	Second Display PEL	Third Display PEL	Fourth Display PEL

VIDEO MEMORY MAP AND GRAPHICS USAGE

Hex Address	Register
3D0	Not Used
3D1	Not Used
3D2	Not Used
3D3	Not Used
3D4	G845 Address Register
3D5	G845 Data Register
3D6	Not Used
3D7	Not Used
3D8	Mode Select Register
3D9	Color Select Register
3DA	Video Array Address & Status
3DB	Clear Light Pen Latch
3DC	Set Light Pen Latch
3DD	Extended RAM Page Register
3DE	Video Array Data
3DF	CRT Processor Page Register

VIDEO ARRAY REGISTERS

The following registers can be accessed by writing their Hex Address to 3DA and their Data to 3DE

Hex Address	Video Array Register
01	Palette Mask
02	Border Color
03	Mode Control
10-1F	Palette Registers

ARRAY PALETTE MASK REGISTER

Bit Programming

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
01	Palette Mask	X	X	X	X					Write Only
MSK[3]	Palette Mask 3									
MSK[2]	Palette Mask 2									
MSK[1]	Palette Mask 1									
MSK[0]	Palette Mask 0									

When bits 0-3 are 0, they force the appropriate palette address to be 0 regardless of the incoming color information. This can be used to make some information in memory a 'don't care' condition until it is requested.

ARRAY BORDER COLOR

Hex Address	Array Register	7	6	5	4	3	2	1	0	Notes
02	Border Color	X	X	0	X					Write Only
	Reserved = 0									
BORI	I (Intensity) Border Color Select									
BORR	R (Red) Border Color Select									
BORG	G (Green) Border Color Select									
BORB	B (Blue) Border Color Select									
	A combination of bits 0-3 selects the screen border as one of 16 colors, as listed in Table 1 "Available Colors Table" at the beginning of this section.									

ARRAY MODE CONTROL REGISTER

Hex Address	Array Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
03	Mode Control	X	X					0	X	Write Only
NVDM	Set to 1 for 640x200 secondary pixel organization									
C16COL	Set to 1 for 16 Color Modes									
C4COLHR	Set to 1 for 4 Color 640x200 Mode									
BORENB	Enables the border color register For PC compatibility, this bit should be 0. For PCjr compatibility, this bit should be 1.									
	Reserved for future implementations. Must always be set to zero.									

ARRAY PALETTE REGISTERS

There are sixteen 4 bit wide palette registers implemented by a 16x4 bit RAM. These registers are 'write' only; they cannot be 'read'. Their address in the Video Array are from hex 10 to 1F. They can be used to redefine any color.

To load the palette, write the hex address to the Video Array register at 3DA. Then, the new palette color is written to 3DE.

Palette address hex 10 is accessed whenever the color code from memory is a hex 0, address hex 11 is accessed whenever the color code from memory is a hex 1, and so forth. A description of the color codes is in Table 1 "Available Colors Table" at the beginning of this section.

Note: The palette address can be 'masked' by using the palette mask register.

The following is a description of the register's bit functions:

Bit Number	Function
0	Blue
1	Green
2	Red
3	Intensity

When loading the palette, the video is 'disabled' and the color viewed on the screen is the data contained in the register being addressed by the processor.

When the program has completed loading the palette, it must change the hex address to some address less than hex 10 for video to be 'enabled' again.

If a programmer does not wish a user to see the adverse effects of loading the palette, the palette should be loaded during the vertical retrace time. The program must modify the palette and change the address to less than hex 10 within the vertical retrace time. A vertical retrace interrupt and a status bit are provided to facilitate this procedure.

In two color modes, the palette is defined by using one bit (PA0), with the following logic:

PALETTE ADDRESS BIT

PA0	Function
0	Palette Register 0
1	Palette Register 1

In four color modes, the palette is defined by using two bits (PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA1	PA0	Function
0	0	Palette Register 0
0	1	Palette Register 1
1	0	Palette Register 2
1	1	Palette Register 3

In sixteen color modes, the palette is defined by using four bits (PA3,PA2,PA1 and PA0), with the following logic:

PALETTE ADDRESS BITS

PA3 (I)	PA2 (R)	PA1 (G)	PA0 (B)	Function
0	0	0	0	Palette Register 0
0	0	0	1	Palette Register 1
0	0	1	0	Palette Register 2
0	0	1	1	Palette Register 3
0	1	0	0	Palette Register 4
0	1	0	1	Palette Register 5
0	1	1	0	Palette Register 6
0	1	1	1	Palette Register 7
1	0	0	0	Palette Register 8
1	0	0	1	Palette Register 9
1	0	1	0	Palette Register 10
1	0	1	1	Palette Register 11
1	1	0	0	Palette Register 12
1	1	0	1	Palette Register 13
1	1	1	0	Palette Register 14
1	1	1	1	Palette Register 15

DETAILED I/O REGISTER INFORMATION

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D4	6845 Address Register	X	X	X						Write Only Addresses 1 of 18 6845 Registers
					<- 5 bit address ->					
Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D5	6845 Data Register									Write Only Data placed in 1 of 18 6845 Registers
		<------ 8 bit Data ---->								

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3D8	Mode Register	X	X							Write Only
ENABLINKCR	Alpha Blink Enable.A 1 selects blink if attribute bit 7 is set. A 0 selects 16 background colors. A 1 selects 8 background colors.									
HRESAD	640 Dot Graphics. A 1 selects 640 X 200 (2 or 4 Color)									
VIDENBCR	Video Enable. A 1 enables the Video display.									
BW	Black & White Select. Selects B&W or color mode for TV or composite monitors. In RGB monitors, a different color palette is selected by this bit in 320 x 200 4 Col Mode. This bit will have no other effect on RGB operation									
GRPH	Graphics Select. A 0 selects Alpha-numeric Mode. A 1 selects Graphics Mode.									
HRESCK	High Resolution Dot Clock. A 0 selects the lower speed for 40 character text or low resolution graphics mode. A 1 selects the higher speed for 80 character text or high resolution graphics mode.									

Hex Address	Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
3D9	Color Select Register	X	X							Write Only
COLSEL	320 X 200 4 Color Blue Control									
BACKGROUNDI	Alpha Background/320 Graphics Foreground Intensity. When Blink is enabled in alpha mode, this bit is used to select intensity. In the 320 X 200 4 color mode, it selects the intensity of the foreground									
OVERSCANI	In Alpha mode screen Border intensity In 320x200 4 Col Background intensity if PA0=PA1=0 In 640x200 2 Col Foreground intensity									
OVERSCANR	In Alpha mode screen Border Red In 320x200 4 Col Background Red if PA0=PA1=0 In 640x200 2 Col Foreground Red									
OVERSCANG	In Alpha mode screen Border Green In 320x200 4 Col Background Green if PA0=PA1=0 In 640x200 2 Col Foreground Green									
OVERSCANB	In Alpha mode screen Border Blue In 320x200 4 Col Background Blue if PA0=PA1=0 In 640x200 2 Col Foreground Blue									

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DA	Video/Light Pen Status	X	X	X	X					Read Only

CVSYNC — When 1 Vertical retrace is active

LPSWB — Light Pen Switch Status
When 0 Light Pen Switch is on.
Switch not latched or debounced.

LPSTRB — When 1 Light Pen input has positive going edge and has set Light Pen trigger. When this trigger is low during a system power on, it may be cleared by performing an I/O command to address 3DB. No specific data is required.

DISPENB — When 0 Display is active
When 1 Video is not displayed

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DC	Set Light Pen Latch	X	X	X	X	X	X	X	X	Write Only
3DB	Clear Light Pen Latch	X	X	X	X	X	X	X	X	Write Only

Data Byte has no effect. Before the 6845 can read the light pen again, the latch at 3DB must be cleared

Hex Address	Register	Bit Programming 7	6	5	4	3	2	1	0	Notes
3DD	Extended Ram Page Reg	X					X	X		Write Only
PG18 (#)	CPU Page Address 18									
PG17	CPU Page Address 17									All bits cleared by a System Reset
VPG18 (#)	Video Page Address 18									
VPG17	Video Page Address 17									
EXTADR	Extended Addressing Mode for 256K systems									

Note (#) Not implemented in current design but reserved for future implementations

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
3DF	CRT/Processor Page Reg									Write Only
ADRM1(**)	Video Address Mode 1 with Reg 3DD bit0 selects Video Address supplied to RAM									
ADRM0(**)	Video Address Mode 0 with Reg 3DD bit0 selects Video Address supplied to RAM									
	Processor Page 2									
	Processor Page 1									
	Processor Page 0									
CRTPG2	CRT Page 2									
CRTPG1	CRT Page 1									
CRTPG0	CRT Page 0									

The processor page bits are combined with the CPU address to select the 32K segment of memory accessed at B8000. If an odd page number is selected, the window is reduced to 16K.

The CRT Page bits select the 16K Page used by the Video. In 32K modes bit 0 is ignored.

Note (**) :
These bits are used in conjunction with Reg 3DD bit 0 to select the Video addresses to the RAM. See the Video Memory Addressing Modes Table. Also the Graphics control bit 3D8 bit 1 (GRPH) will force the same condition as setting ADRM0.

Bit Programming

Hex Address	Register	7	6	5	4	3	2	1	0	Notes
00A0-00A7	NMI Mask Register		X	X						Write Only
NMIEN	Enable Non Maskable Interrupt									
PORTMD	Enable 256K Video RAM									All bits
MC3	Memory Configuration 3									cleared
MC2	Memory Configuration 2									by a
MC1	Memory Configuration 1									System
XTERNVID	Disables all video Accesses to Video Memory at B8000-BFFFF and video I/O locations 3D0-3D7									Reset

6845 PROGRAMMING TABLE FOR ALL MODES

*	REGISTER	40X25 ALPHANUM	80X25 ALPHANUM	160X200 16 Col 320X200 4 Col 640X200 2 Col	640X200 4 Col 320X200 16 Col
0	Horizontal Total	38 (56)	71 (113)	38 (56)	71 (113)
1	Horiz. Displayed	28 (40)	50 (80)	28 (40)	50 (80)
2	Horiz. Sync. Pos	2D (45)	5A (90)	2D (45)	5A (90)
3	Horiz. Sync. Width	08 (8)	0E (14)	08 (8)	0E (14)
4	Vertical Total-1	1C (28)	1C (28)	7F (127)	3F (63)
5	Vert. Total Adjust	01 (1)	01 (1)	06 (6)	06 (6)
6	Vertic. Displayed	19 (25)	19 (25)	64 (100)	32 (50)
7	Vert. Sync Pos.	1A (26)	1A (26)	70 (112)	38 (56)
8	Interlace Mode	02 (2)	02 (2)	02 (2)	02 (2)
9	MaxScanLineAdd -1	08 (8)	08 (8)	01 (1)	03 (3)
10	Cursor Start	06 (6)	06 (6)	06 (6)	06 (6)
11	Cursor End	07 (7)	07 (7)	07 (7)	07 (7)
12	StartAddresss High	00 (0)	00 (0)	00 (0)	00 (0)
13	StartAddress Low	00 (0)	00 (0)	00 (0)	00 (0)

MODE SELECTION SUMMARY

MODE	'H3D8 BIT 0 HRESCK	'H3D8 BIT 4 HRESAD	'H3DE REG3 BIT 3 C4COLHR	'H3DE REG3 BIT 4 C16COL	'H3DE REG3 BIT 5 NVDM	'H3D8 BIT 1 GRPH	'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0
40X25 ALPHA	0	0	0	0	0	0	0	0	0
80X25 ALPHA	1	0	0	0	0	0	0	0	0
160X200 16 COL	0	0	0	1	0	1	0	0	1
320X200 4 COL	0	0	0	0	0	1	0	0	1
320X200 16 COL	1	0	0	1	0	1	0	1	1
640X200 2 COL	0	1	0	0	0	1	0	0	1
640X200 4 COL	1	1	1	0	0	1	0	1	1

VIDEO/SYSTEM MEMORY ADDRESS MAP

'H0A0 BITS 4 3 2 1	VIDEO/SYSTEM MEMORY START ADDRESS	VIDEO/SYSTEM MEMORY LENGTH	VIDEO/SYSTEM MEMORY ADDRESS RANGE
0 0 0 0	0 0 0 0 0	128K	0 0 0 0 0 - 1 F F F F
0 0 0 1	2 0 0 0 0	128K	2 0 0 0 0 - 3 F F F F
0 0 1 0	4 0 0 0 0	128K	4 0 0 0 0 - 5 F F F F
0 0 1 1	6 0 0 0 0	128K	6 0 0 0 0 - 7 F F F F
0 1 0 0	8 0 0 0 0	128K	8 0 0 0 0 - 9 F F F F
1 0 0 1	0 0 0 0 0	256K	0 0 0 0 0 - 3 F F F F
1 0 1 0	2 0 0 0 0	256K	2 0 0 0 0 - 5 F F F F
1 0 1 1	4 0 0 0 0	256K	4 0 0 0 0 - 7 F F F F
1 1 0 0	6 0 0 0 0	256K	6 0 0 0 0 - 9 F F F F

VIDEO MEMORY ADDRESSING MODES

'H3DD BIT 0 EXTADR	'H3DF BIT 7 ADRM1	'H3DF BIT 6 ADRM0	VIDEO MEMORY ORGANIZATION (128)
0	0	0	1 16K Segment of Memory (8 Pages)
0	0	1	2 8K Segments of Memory (8 Pages) Switched on RA[0]
0	1	0	2 16K Segments of Memory (4 Pages) Switched on RA[0]
0	1	1	4 8K Segments of Memory (4 Pages) Switched on RA[0],RA[1]
1	0	0	1 32K Segment of Memory (4 Pages)
1	0	1	2 32K Segments of Memory (2 Pages) Switched on RA[0]

For 8 Page Modes CRTPG[2:0] select the Video Page
For 4 Page Modes CRTPG[2:1] select the Video Page
For 2 Page Modes CRTPG[2] select the Video Page

OTHER CHIP FUNCTIONS

In addition to the video controller functions, the Tandy 1000 video controller chip also provides most of the system address decode functions. These decode and chip select functions are described as follows:
A, B, C outputs are encoded device select lines and are connected to an external LS138.

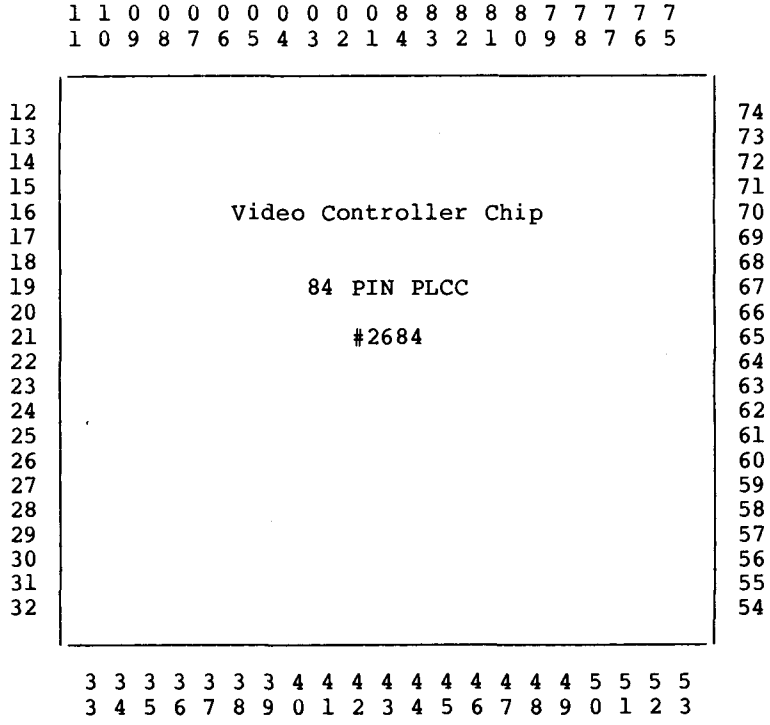
C	B	A	IOMB	BA0-15(HEX)	DESCRIPTION
1	1	1		NONE OF BELOW	
1	1	0	1	0020-0027	INTCSB
1	0	1	1	0040-0047	TMRCSB
1	0	0	1	0060-0067	PIOCSB
0	1	1	1	0200-0207	JOYSTKCSB
0	1	0	1	00C0-00C7	SNDCSB
0	0	1	1	03F0-03F7	FDCCSB
0	0	0	1	0378-037F	PRINTCSB

The output signal ROMIOSELB is the enable signal for an LS245 that controls all of the data flow to devices on the main logic board. This signal is active low and will be activated for any of the following conditions:

1. Video/System Memory Read or Write
2. Video Access at B8000-BFFFF
3. Rom Access at F0000-FFFFF
4. Video I/O access at 03D0-03DF
5. I/O access to any of the following addresses:

   0040-0047
   0060-0067
   00A0-00A7
   00C0-00C7
   0200-0207
   0378-037F
   03F0-03F7

PIN LIST


1 1 0 0 0 0 0 0 0 0 0 8 8 8 8 8 7 7 7 7 7
1 0 9 8 7 6 5 4 3 2 1 4 3 2 1 0 9 8 7 6 5
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
Video Controller Chip
84 PIN PLCC
#2684
74
73
72
71
70
69
68
67
66
65
64
63
62
61
60
59
58
57
56
55
54
3 3 3 3 3 3 3 4 4 4 4 4 4 4 4 4 5 5 5 5
3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3

DESCRIPTION OF EACH PIN FUNCTION

PIN#	PIN NAME	TYPE	DESCRIPTION
1	VSS	Ground	Ground
2	XMD[2]	Input/Output	External Memory Data I/O Bank 0
3	XMD[3]	Input/Output	External Memory Data I/O Bank 0
4	XMD[4]	Input/Output	External Memory Data I/O Bank 0
5	XMD[5]	Input/Output	External Memory Data I/O Bank 0
6	XMD[6]	Input/Output	External Memory Data I/O Bank 0
7	XMD[7]	Input/Output	External Memory Data I/O Bank 0
8	YMD[0]	Input/Output	External Memory Data I/O Bank 1
9	YMD[1]	Input/Output	External Memory Data I/O Bank 1
10	YMD[2]	Input/Output	External Memory Data I/O Bank 1
11	YMD[3]	Input/Output	External Memory Data I/O Bank 1
12	YMD[4]	Input/Output	External Memory Data I/O Bank 1
13	YMD[5]	Input/Output	External Memory Data I/O Bank 1
14	YMD[6]	Input/Output	External Memory Data I/O Bank 1
15	YMD[7]	Input/Output	External Memory Data I/O Bank 1
16	RFSHB	Input	Memory Refresh Strobe Input
17	MWE1B	Output	Ram Bank 1 Write Enable Signal
18	MWE0B	Output	Ram Bank 0 Write Enable Signal
19	RASB	Output	Ram Row Address Strobe
20	CASB	Output	Ram Column Address Strobe
21	BMEMRB	Input	CPU Memory Read Strobe
22	VDD	Power	5 Volts Supply
23	BMEMWB	Input	CPU Memory Write Strobe
24	CK28M	Clock	28.63636 Mhz Clock Input
25	VIDEOWAIT	Output(OpenDrain)	Video Wait Signal
26	SYSRSTB	Input	System Reset
27	IOMB	Input	CPU I/O-Memory Signal (Memory ->1, I/O -> 0)
28	A	Output	Encoded Peripheral Select Line
29	B	Output	Encoded Peripheral Select Line
30	C	Output	Encoded Peripheral Select Line
31	IOMEMSELB	Output	External Buffer Enable
32	NMIEN	Output	Nonmaskable Interrupt Enable
33	BIORB	Input	CPU I/O Read Strobe
34	BIOWB	Input	CPU I/O Write Strobe
35	LPIN	Input	Light Pen Signal Input
36	LPSWB	Input	Light Pen Switch Input
37	OUTVSYNC	Output	Vertical Sync Output
38	OUTHSYNC	Output	Horizontal Sync Output
39	COMPCOLOR	Output	Composite Color Signal
40	COMPSYNC	Output	Composite Sync Signal
41	OUTI	Output	Intensity Out
42	OUTR	Output	Red Video Out
43	VSS1	Ground	Ground
44	OUTB	Output	Blue Video Out/Monochrome Dotclock

45	OUTG	Output	Green Video Out/Monochrome Video
46	BA[19]	Input	CPU Address Line
47	BA[18]	Input	CPU Address Line
48	BA[17]	Input	CPU Address Line
49	BA[16]	Input	CPU Address Line
50	BA[157	Input	CPU Address Line
51	BA[14]	Input	CPU Address Line
52	BA[13]	Input	CPU Address Line
53	BA[12]	Input	CPU Address Line
54	BA[11]	Input	CPU Address Line
55	BA[10]	Input	CPU Address Line
56	BA[9]	Input	CPU Address Line
57	BA[8]	Input	CPU Address Line
58	BA[7]	Input	CPU Address Line
59	BA[6]	Input	CPU Address Line
60	BA[5]	Input	CPU Address Line
61	BA[4]	Input	CPU Address Line
62	BA[3]	Input	CPU Address Line
63	BA[2]	Input	CPU Address Line
64	BA[1]	Input	CPU Address Line
65	BA[0]	Input	CPU Address Line
66	DB[7]	Input/Output	CPU Data I/O
67	DB[6]	Input/Output	CPU Data I/O
68	DB[5]	Input/Output	CPU Data I/O
69	DB[4]	Input/Output	CPU Data I/O
70	DB[3]	Input/Output	CPU Data I/O
71	DB[2]	Input/Output	CPU Data I/O
72	DB[1]	Input/Output	CPU Data I/O
73	DB[0]	Input/Output	CPU Data I/O
74	MA[0]	Output	Memory Address Line
75	MA[1]	Output	Memory Address Line
76	MA[2]	Output	Memory Address Line
77	MA[3]	Output	Memory Address Line
78	MA[4]	Output	Memory Address Line
79	MA[5]	Output	Memory Address Line
80	MA[6]	Output	Memory Address Line
81	MA[7]	Output	Memory Address Line
82	BANKSL	Output	Memory Address Line
83	XMD[0]	Input/Output	External Memory Data I/O Bank 0
84	XMD[1]	Input/Output	External Memory Data I/O Bank 0

LOGIC BLOCK DIAGRAM

TEST MODES AND THEIR OPERATIONS

There are four Test Modes that the chip can be placed into to make the part easily and efficiently testable. All these Test Modes use conditions that can never occur in a System environment, therefore avoiding accidental entry in Test Mode. All the test modes are entered when both MEMRB and MEMWB are active. The selection of the different tests is done by an additional decode on some bits of the BA lines according to the following chart:

TEST MODE	ENABLED WHEN						OPERATION PERFORMED
	BMEMRB	BMEMWB	BA15	BA14	BA13	BA12	
1	0	0	1	X	X	X	Pinout the 6845 Megacell on external pins and/or Start Self Test Rom. While the testing of the Megacell is in progress, the Rom is performing a signature analysis. At the end of 4500 clocks, a PASS/FAIL bit is set, if the Self Test was successful.
2	0	0	0	1	X	X	Enable a Software Reset on the 6845.
3	0	0	0	X	1	X	Clear the Clock generators & blink counter to start from a known condition.
4	0	0	0	X	X	0/1	A 1 writes a bit that forces Display Enable constantly. A 0 removes forced Display Enable. Cleared by SYSRSTB.

TEST MODE 1 PINOUT THAT EMULATES THE 6845 STANDARD PRODUCT

The following signals of the Megacell are available on the following pins in Test Mode 1:

6845 SIGNAL	VIDEO CONTROLLER SIGNAL
RESETB	SYSRSTB
LPSTB	LPIN
MA[7:0]	MA[7:0]
MA[8]	BANKSL
MA[9]	MWE1B
MA[10]	ROMIOSELB
MA[11]	A
MA[12]	B
MA[13]	C
DE	COMPSYNC
CURSOR	COMPCOLOR
CLK	IOMB (See Note ***)
RNW	BIOWB
E	RFSHB
RS	BA[0]
CSB	LPSWB
DB[7:0]	DB[7:0]
RA[0]	RASB
RA[1]	CASB
RA[2]	OUTR
RA[3]	OUTI
RA[4]	MWE0B
HS	OUTHSYNC
VS	OUTVSYNC

Also the Pass/Fail bit for the Self Test Rom can be tested on the OUTG output pin during TEST MODE 1. Note that at least 4,500 clocks must be given in Test Mode 1 before checking the Pass/Fail bit. These clock times could be used to exercise the 6845 as a standard part according to the previous pinout.

Note*: IOMB is in fact CLK Bar so in order to test it using the standard part's test program, there is a need to invert the clock coming in the Test program.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0v)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS

OPERATING AMBIENT AIR TEMP. RANGE	MIN	TYP	MAX	UNITS
	0	25	70	DEGREES C.

POWER SUPPLIES				
VCC SUPPLY VOLTAGE	4.5	5.0	5.5	VOLTS
VSS SUPPLY VOLTAGE	0	0	0	VOLTS
ICC SUPPLY CURRENT		20	35	MILLIAMPS
TOTAL POWER DISSIPATION (INCLUDE LOADING ON OUTPUTS)		100	175	MILLIWATTS

LEAKAGE CURRENT ALL INPUTS AND TRISTATE OUTPUTS	MIN	TYP	MAX	
	-10		10	MICROAMPS

INPUT VOLTAGES LOGIC "0" (Vil) ALL INPUTS	0.8	VOLTS
LOGIC "1" (Vih) ALL INPUTS	2.0	VOLTS

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC"0" (Vol) ALL OUTPUTS	2.0 MA			0.4	VOLTS
LOGIC"1" (Voh) ALL OUTPUTS	0.4 MA	2.4			VOLTS

INPUT CAPACITANCE	MIN	TYP	MAX	
ALL INPUTS			10	PICOFARADS

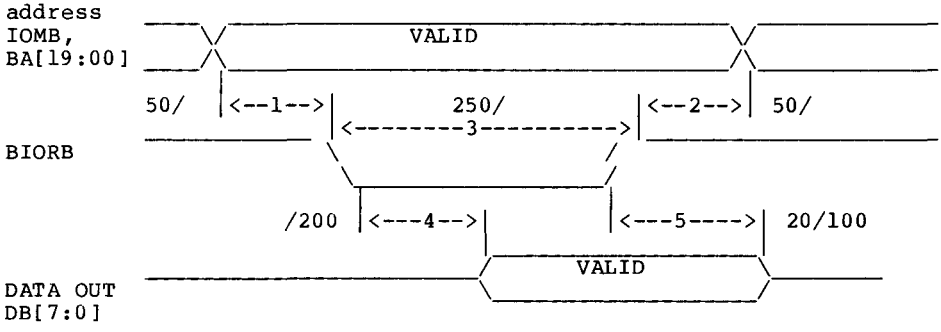
TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

MA[8]-MA[0]	100 pF
ALL OTHER OUTPUTS	20 pF

CHARACTERISTICS

READ Operation

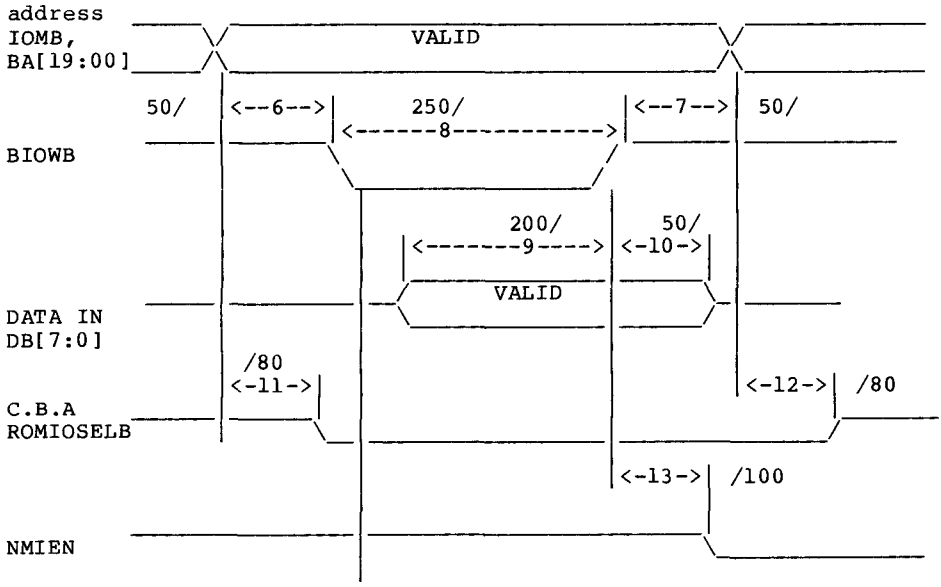


I/O TIMING

#	DESCRIPTION	MIN	MAX	UNITS	NOTE
1	ADDRESS VALID TO BIORB ACTIVE SETUP	50		NS	
2	ADDRESS VALID HOLD AFTER BIORB INACTIVE	50		NS	
3	BIORB PULSE WIDTH LOW	250		NS	
4	BIORB ACTIVE TO DATA OUT VALID		200	NS	
5	BIORB INACTIVE TO DATA OUT TRISTATE	20	100	NS	

READ OPERATION

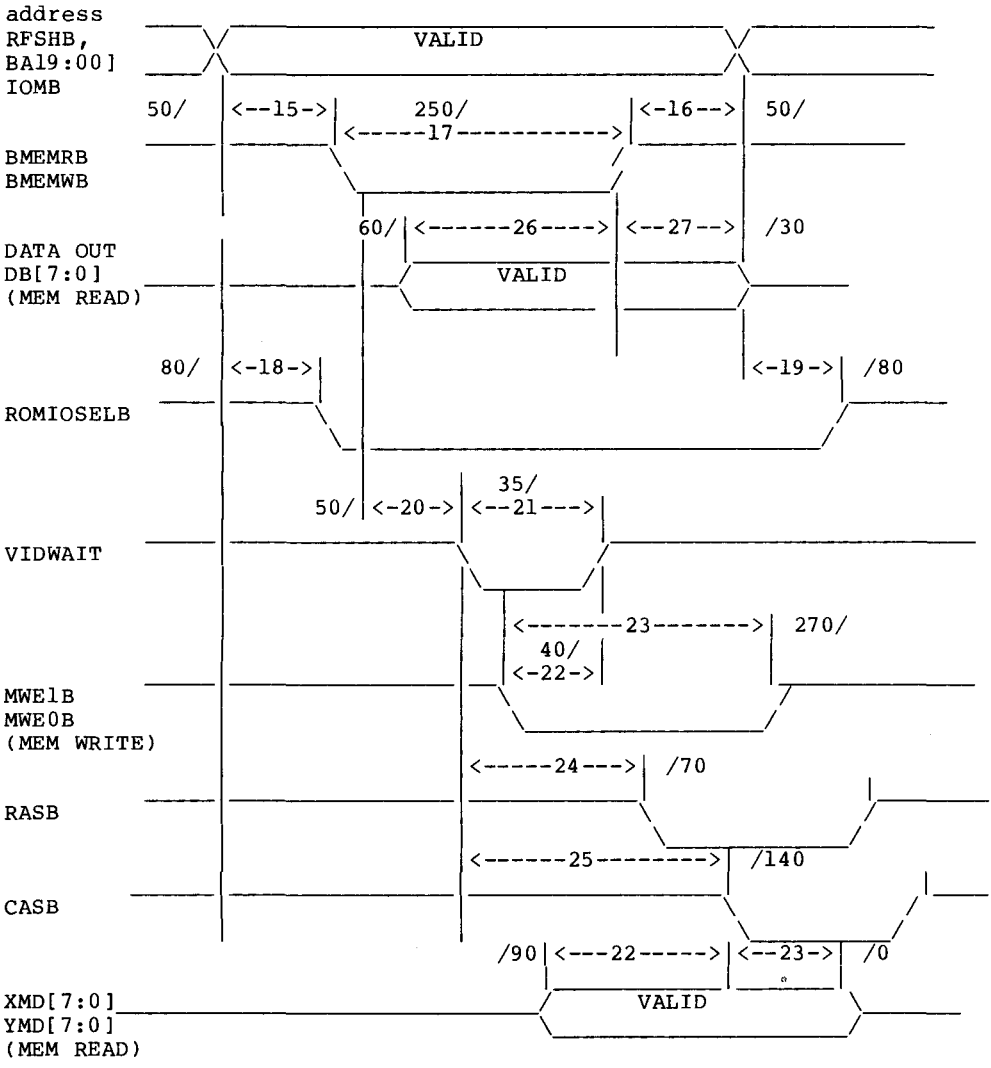
WRITE OPERATION AND I/O OUTPUT TIMING



#	DESCRIPTION	MIN	MAX	UNITS	NOTE
6	ADDRESS VALID TO BIOWB ACTIVE SETUP	50		NS	
7	ADDRESS VALID HOLD AFTER BIOWB INACTIVE	50		NS	
8	BIOWB PULSE WIDTH LOW	250		NS	
9	DATA IN VALID TO BIOWB INACTIVE SETUP	200		NS	
10	BIOWB INACTIVE TO DATA IN VALID HOLD	50		NS	
11	ADDRESS VALID TO C,B,A,ROMIOSELB OUTPUT DELAY		80	NS	
12	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY	80		NS	
13	BIOWB INACTIVE TO NMIEN LATCHED OUTPUT DELAY		100	NS	

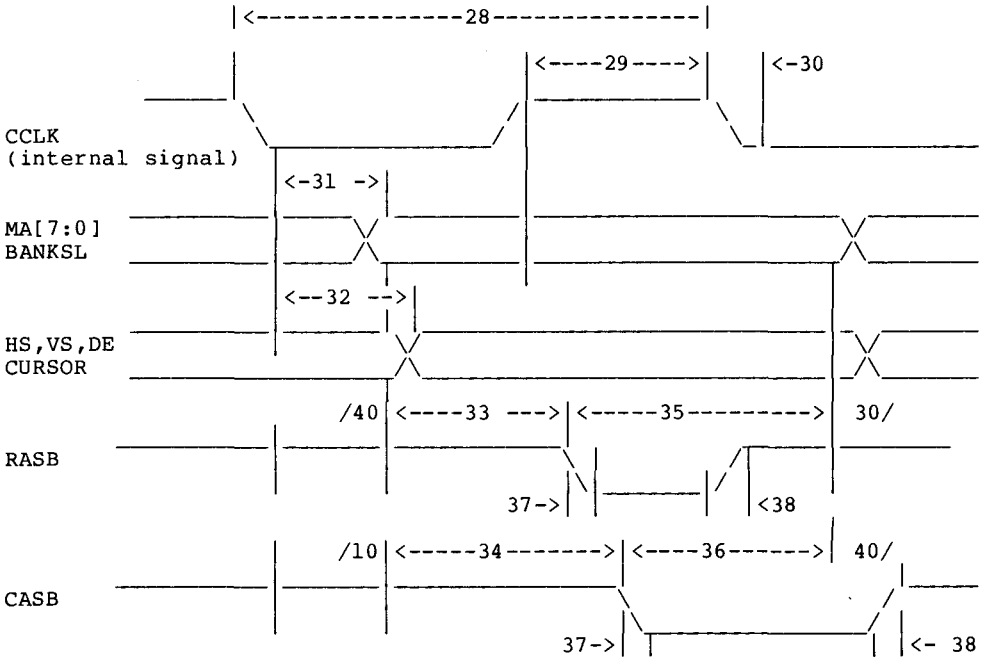
MEMORY DECODE TIMING

MEMORY READ OR WRITE OPERATION



*	DESCRIPTION	MIN	MAX	UNITS	NOTE
15	ADDRESS VALID TO BMEMRB ACTIVE SETUP	50		NS	
16	ADDRESS VALID HOLD AFTER BMEMRB INACTIVE	50		NS	
17	BMEMRB PULSE WIDTH LOW	250		NS	
18	ADDRESS VALID TO ROMIOSELB OUTPUT DELAY		80	NS	
19	ADDRESS NOT VALID TO ROMIOSELB INACTIVE OUT DELAY		80	NS	
20	VIDWAIT DELAY FROM BMEMRB READ LOW		50	NS	
21	VIDWAIT PULSE WIDTH	35	600	NS	
22	XMD, YMD SETUP TO CASB LOW (MEM READ)	90		NS	
23	XMD, YMD HOLD TO CASB LOW (MEM READ)	0		NS	
24	VIDWAIT LOW DELAY TO RASB LOW		70	NS	
25	VIDWAIT LOW DELAY TO CASB LOW	0	140	NS	
26	I/O DATA BUS OUT SETUP TO BMEMRB HIGH	60		NS	
27	I/O DATA BUS OUT HOLD TO BMEMRB HIGH	0	30	NS	

CRTC TIMING


28
29
30
CCLK
(internal signal)
31
MA[7:0]
BANKSL
32
HS,VS,DE
CURSOR
/40
33
35
30/
RASB
37
38
/10
34
36
40/
CASB
37
38

CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
28	CCLK frequency	Fcyc			2	MHz
29	CCLK width	PWcl	100			nS
30	CCLK rise and fall time	Tcr,Tcf			5	nS
31	CLK fall to MA[7:0]RA0-4 delay time	Tmad,Trad			50	nS
32	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS
33	MA[7:0],BANKSL setup to RASB low		40			nS
34	MA[7:0],BANKSL setup to CASB low		10			nS
35	MA[7:0],BANKSL hold from RASB low		30			nS
36	MA[7:0],BANKSL hold from CASB low		40			nS
37	RASB,CASB fall				20	nS
38	RASB,CASB rise				5	nS

OTHER TIMING SPECS

	Characteristics	Symbol	Min	Nom	Max	Units
39	Relative Skew of R,G,B,I				10	nS
40	Relative Skew of R,G,B,I With respect to Compcol				20	nS
41	Relative Skew of R,G,B,I With respect to CompSync OutHsync,OutVsync				35	nS
42	Relative Skew of R,G,B,I With respect to CompSync				35	nS

MEGACELL 6845R1 SPECIFICATION DATASHEET FOR 6845 MEGACELL

VE 68C45 MEGACELL DESIGN KIT
CRT CONTROLLER MEGACELL

FEATURES

- Completely integrated with VTI's extensive IC design tools and libraries
- CMOS (2-micron) M68C45 Megacell configurable as:
  - -- 68C45R - CMOS equivalent of Motorola 6845R CRTC
  - -- 68C45R1 - CMOS equivalent of Motorola 6845R1 Enhanced CRTC
  - -- 68C45S - CMOS equivalent of Hitachi 6845S CRTC
  - -- 68C45SY - CMOS CRTC similar to Synertek 6545 CRTC
- 4.5 MHz video memory interface
- 3 MHz system processor interface
- Compatible with the VTI bus architecture
- Programmable Display Enable and Cursor delays (standard for S and SY versions -- optional for R and R1 versions)
- Programmable Vertical Sync pulse width (standard for S version -- optional for R, R1 and SY versions)
- Row/Column display memory addressing (SY version)
- Double Width character control

OPTIONAL FEATURES

- 16K, 32K, or 64K display Memory Address range (14, 15, or 16 bits)
- 7, 8, or 9-bit Vertical Row counter

VTI MEGACELLS

Megacells are building block equivalents of standard LSI functions that can be combined with other megacells, standard cells or compiled cells to create custom User-Specific ICs (USICs). Megacells are fully compatible with VTI's other cell technologies and design tools.

The VTI bus (TM) architecture allows multiple megacells to be combined on a single IC, along with additional cells from VTI's extensive libraries -- decreasing the design time, design cost, and size of complex systems. A detailed Functional Model provided with each megacell further reduces design verification time.

SIGNAL DESCRIPTIONS

The following signals function the same on the M68C45 Megacells and on the standard VL6845 family of CRT Controller ICs.

Signal	I/O	Description
RS	IP	Register Select
E	IP	Enable
RNW	IP	Specify READ (high) or WRITE (low) operation
CSB	IP	Chip (6845 megacell) select, low true
CCLK	IP	Character Clock
LPSTB	IP	Light Pen Strobe
D0-D7	I/O	Data Bus
RA0-RA4	OP	Raster Address
HS	OP	Horizontal Sync
RESETB	IP	Reset, low true

The following signals are unique to the VE68C45 Megacells, or are functionally different on the VE68C45 Megacells and the VL6845 ICs.

Signal	I/O	Description
DE	OP	Display Enable output - active (DE = "1") when the VE68C45 is generating active display information. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
CURSOR	OP	Cursor output - this signal is high when the raster scan coincides with the programmed cursor position. The S version can be programmed with a 0, 1, or 2 character delay. The SY version can be programmed for a 0 or 1 character delay.
VS	OP	Vertical Sync output - active high pulse which determines the vertical placement of the video data. An optional feature permits programming the Vertical Sync pulse width.

MA0-MA13, 14,15	OP	14, 15, or 16- bit Video Memory Address bus. These tri-state outputs provide the binary address to the external video RAM. If row/column addressing is selected (SY version only) this bus will provide row/column addressing to the external RAM instead of binary addressing. The AENB input signal can be used to place the MA bus in the high impedance state.
AENB	IP	Address Enable input - when asserted low (AENB = "0") the MA outputs are enabled. AENB = "1" forces the MA outputs into a high impedance state.
LD0-LD13, 14,15	I/O	14, 15, or 16-bit Advanced Memory Address bus - separate video memory address information on this bus precedes the information on the MA bus by one character clock. This bus is provided to interface with a separate strip of logic for split display capability.
LOAD	IP	When asserted (high) a new value is loaded into the RA counter. Tie to VSS when not used.
BREAK	IP	To be used for splitted screen format. Tie to VSS when not used.
READB	OP	This signal goes LOW during a legitimate read operation.
VDRA (reserved)	n/c	Reserved for future expansion. To be left unconnected.
DW	IP	Double Width input - this input puts the VE68C45 in a double-width display mode. Tie to VSS when not used.

6845R, 6845S, 6545SY	IP	One of these three inputs is tied high to select the version of the VE68C45 used in your application. The remaining two inputs must be grounded. NOTE: the VE68C45SY does not provide 6545 transparent addressing or the 6545 status register.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

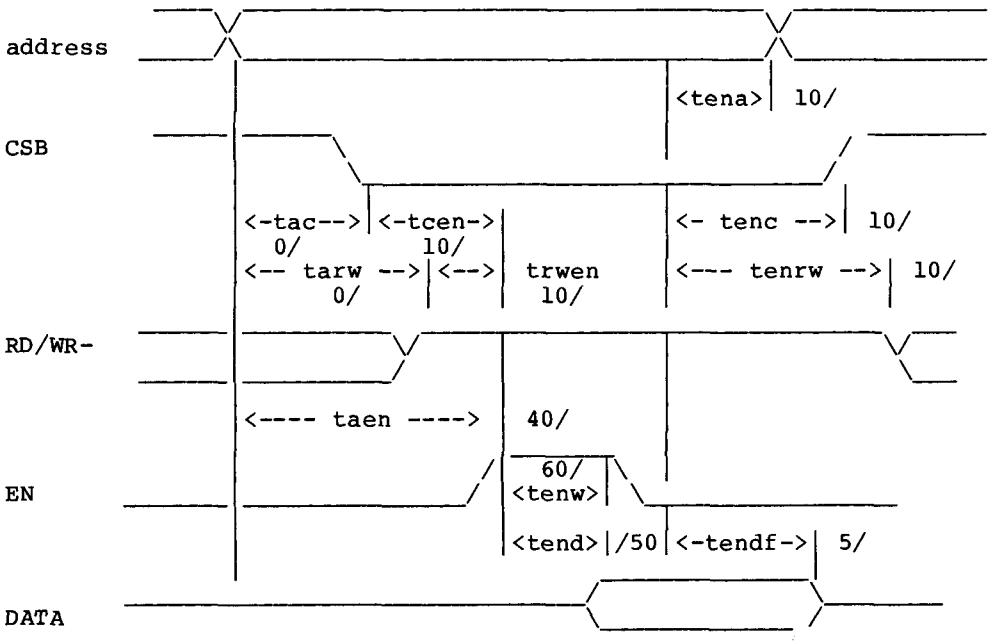
Ambient temperature under bias	0 C to 70 C
Storage temperature	-65 C to +150 C
Voltage on any signal with respect to Gnd	-0.5V to +7V
Power dissipation	750mW

DC characteristics (Ta = 0 - 70 degree C, Vss=0v, Vcc=+5 +/- 10%)

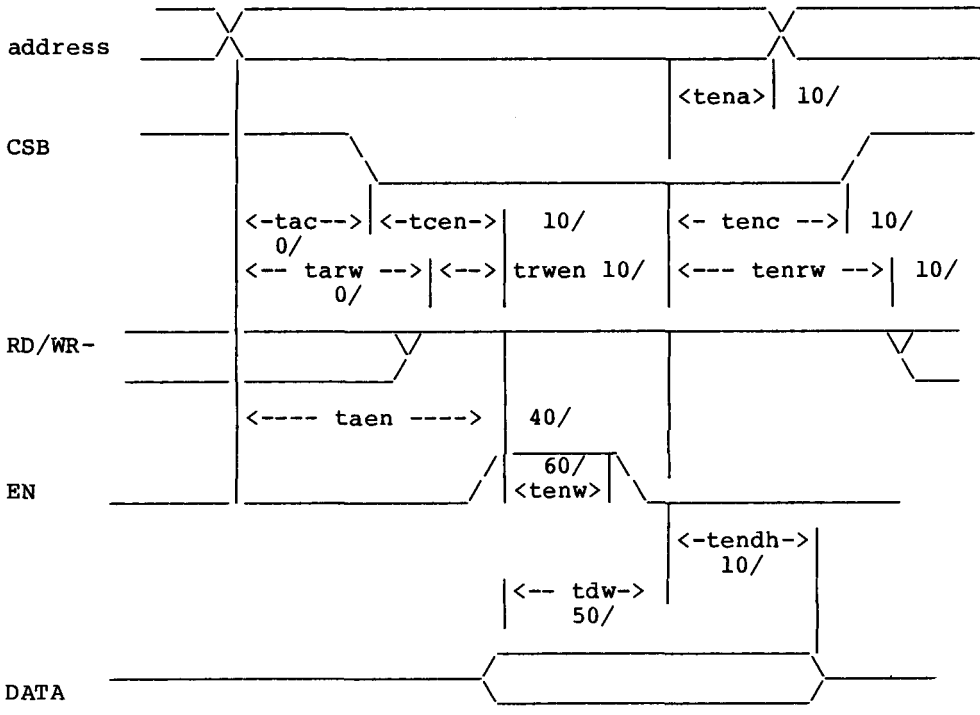
Characteristics	Symbol	Min	Typ	Max	Units
Input High Voltage					
Inputs,I/O	Vih	3.0		Vcc	Volts
Input Low Voltage					
Inputs,I/O	Vil	Vss		0.8	Volts
Output High Voltage					
Outputs,I/O	Voh	3.0		Vcc	Volts
Output Low Voltage					
Outputs,I/O	Vol			0.4	Volts
Capacitance					
Input Capacitance					
CLK input	Cin			6	pF
remaining inputs	Cin			.7	pF
Output Loading					
MA0-13,D0-7	Cout			9	pF
RA0-4,HS,VS,DE, Cursor	Cout			3	pF

AC CHARACTERISTICS (Vcc=+5v +/- 10%, Vss=0v, Ta=0 C to 70 C)

VTI BUS TIMING



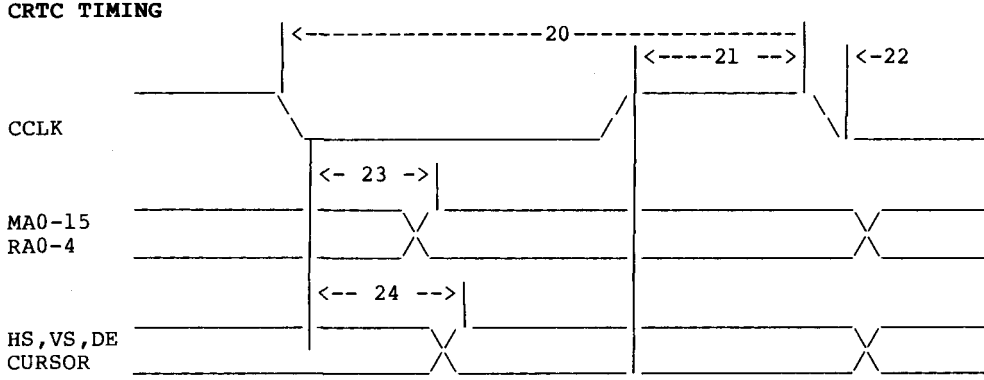
WRITE


address
CSB
RD/WR-
EN
DATA
<tena> 10/
<-tac--> 0/
<-tcen-> 10/
<- tenc --> 10/
<-- tarw --> 0/
<--> trwen 10/
<--- tenrw --> 10/
<---- taen ----> 40/
60/
<tenw>
<-tendh-> 10/
<-- tdw-> 50/

VTI BUS TIMING

	MIN(ns)	MAX(ns)
TAC address to CS delay	0	
TARW address to read/write delay	0	
TAEN address to enable set up	40	
TCEN CS to enable delay	10	
TRWEN read/write to enable set up	10	
TENW enable pulse width	100	
TENA enable to address hold time	10	
TENC enable to cs hold time	10	
TENRW enable to read/write hold time	10	
read:		
TEND enable to read data delay		50
TENDF enable to data bus float	5	30
write:		
TDEN write data to enable setup time	50	
TENDH enable to write data hold time	10	

CRTC TIMING



CRTC TIMING

	Characteristics	Symbol	Min	Nom	Max	Units
20	CLK frequency	Fcyc			4.5	MHz
21	CLK width	PWcl	100			nS
22	CLK rise and fall time	Tcr,Tcf			5	nS
23	CLK fall to MA0-15,RA0-4 delay time	Tmad,Trad			50	nS
24	CLK fall to HS, VS, DE,CURSOR delay time	Thsd,Tvsd Tdtd,Tcdd			50	nS

DMA CHIP SPECIFICATION

DMA CHIP SPECIFICATION
CONTENTS

GENERAL DESCRIPTION.....1
ADDRESS DECODE.....1
PIN LIST.....5
PIN FUNCTIONS.....6
LOGIC BLOCK DIAGRAM.....10
ELECTRICAL SPECIFICATIONS.....11
TIMING.....18

DMA CHIP SPECIFICATION

GENERAL DESCRIPTION

The DMA Chip is an Intel 8237A-5 (AMD 9517) DMA Controller plus associated support circuity to integrate the TANDY 1000 External Memory function into a single ASIC part. The support circuity is divided into the five functional sections. The ADDRESS DECODE-MEMORY and ADDRESS DECODE-IO are independent of the DMA function and interface directly into the bus. The TIMING and DMA RDY sections are DMA support functions. The BUFFERS support the in/out pins.

The functional configuration of the 8237 for the DMA Chip is a fixed subset of its total capability. It is configured via the BIOS ROM for: normal timing, fixed priority, late write, high DREQ sense, low DACK sense.

ADDRESS DECODE - MEMORY

Provides RAM Memory access decode and address generation. Bus addresses A19-A15 determine which segment(bank) of memory is being accessed based on one of four possible memory configurations. (see memory map Figure 1). This is combined with Bus strobes MEMWB or MEMRB and CLK to create one of the three RAS strobes (RAS0B, RAS1B or RAS2B), MUX, CAS, data directional controls DBDIR, DBENB and the multiplexed RAM addresses MA0-MA8. The signals CAS and MUX will occur for all access's except REFRESH. The address lines MA0-MA8 are Bus addresses A0-A8 and A9-A17 multiplexed together by the signal MUX. These will occur for all access's including REFRESH (since MUX does not occur during REFRESH, MA0-MA8 will be only A0-A8). The selection of MA8 will be made externally since Bank 0 and Bank 1 can be either 64K or 265K DRAM IC's.

	MCF0,MCF1 CODE	MEMORY ORGANIZATION	ADDRESS	ACCESS CONTROL SIGNAL
OPTION #1	00	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #2	01	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 EMPTY		
		BANK 2 EMPTY		
OPTION #3	10	BANK 0 256K x 8	0.0000-3.FFFF	RAS0
		BANK 1 256K x 8	4.0000-7.FFFF	RAS1
		BANK 2 EMPTY		
OPTION #4	11	BANK 0 64K x 8	0.0000-0.FFFF	RAS0
		BANK 1 64K x 8	1.0000-1.FFFF	RAS1
		BANK 2 256K x 8	2.0000-5.FFFF	RAS2

Figure 1 MEMORY CONFIGURATION MAP

EQUATIONS FOR RAS-B

64K DRAMS require address A0-A15, therefore A19-A16 determine access.
256K DRAMS require address A0-A17, therefore A19-A18 determine access.

```
RAS0B = /MCF1./MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)   OPTION #1
      + /MCF1. MCF0./19./18.         /REFRESH.(MEMRB+MEMWB)   OPTION #2
      +  MCF1./MCF0./19./18.         /REFRESH.(MEMRB+MEMWB)   OPTION #3
      +  MCF1. MCF0./19./18./17./16./REFRESH.(MEMRB+MEMWB)   OPTION #4
      +  REFRESH.MEMRB

RAS1B = /MCF1./MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)   OPTION #1
      +  MCF1./MCF0./19. 18.         /REFRESH.(MEMRB+MEMWB)   OPTION #3,
                                                        NO OPTION #2
      +  MCF1. MCF0./19./18./17. 16./REFRESH.(MEMRB+MEMWB)   OPTION #4
      +  REFRESH.MEMRB

RAS3B =  MCF1. MCF0./19./18. 17      /REFRESH.(MEMRB+MEMWB)   OPTION #4,
                                                   NO OPTION #1,#2,#3
      +  MCF1. MCF0./19. 18./17      /REFRESH.(MEMRB+MEMWB)
      +  REFRESH.MEMRB
```

EQUATIONS FOR MULTIPLEXED ADDRESSES MA-

	ROW ADDRESS (FIRST)	COLUMN ADDRESS (SECOND)	
MA0 :	A0	A8	Since these addresses will
MA1 :	A1	A9	be used for either/both
MA2 :	A2	A10	64K and 256K DRAMS, MA8
MA3 :	A3	A11	will be A16,A17 instead
MA4 :	A4	A12	of two sets of MAs.
MA5 :	A5	A13	(i.e. 64K MA0=A0/A8,
MA6 :	A6	A14	256K MA0=A0/A9,...etc.)
MA7 :	A7	A15	
MA8 :	A16	A17	

ADDRESS DECODE - I/O

Provides I/O decode for generating the chip selects for the DMA Controller and the DMA Segment Address Register plus the data directional control signals DBDIR and DBENB. Bus addresses A0-A15 are decoded and combined with Bus strobes IORB or IOWB to create the chip selects.

CHIP SELECT FUNCTION	ADDRESS	SIGNAL	EQUATION (A19-A16 = don't care) (A15,...,A8 = 0, ALWAYS)
DMA	X.0000-X.000F	DMACSB =	/A7./A6./A5./A4./AEN.(IORB + IOWB)
DMA SEGMENT REGISTER	X.0080-X.0083	WPRCSB =	A7./A6./A5./A4./A4./AEN.IOWB

Figure 2 I/O CONFIGURATION MAP

DMA READY

A system requirement is to have one WAIT cycle automatically inserted into each I/O transfer. When an IORB occurs, WAIT cycles will continually be inserted until IORB returns inactive or until a MEMWB or MEMRB occurs.

This one WAIT cycle is inserted automatically when the CPU is Bus Master. Therefore when the DMA is a Bus Master, it is necessary to insert one WAIT cycle into each DMA I/O transfer (that is every transfer) and honor any additional WAIT requests from the system.

TIMING GENERATOR

The input clock is OSC (= 14.31818 MHZ).
1.) It is divided by three to recreate the 4.77 MHz system processor clock which is used as the clock for the 8237.
2.) It is used to delay the memory access strobe MEM-B twice to create the timing for RAS-, MUX, and CAS.

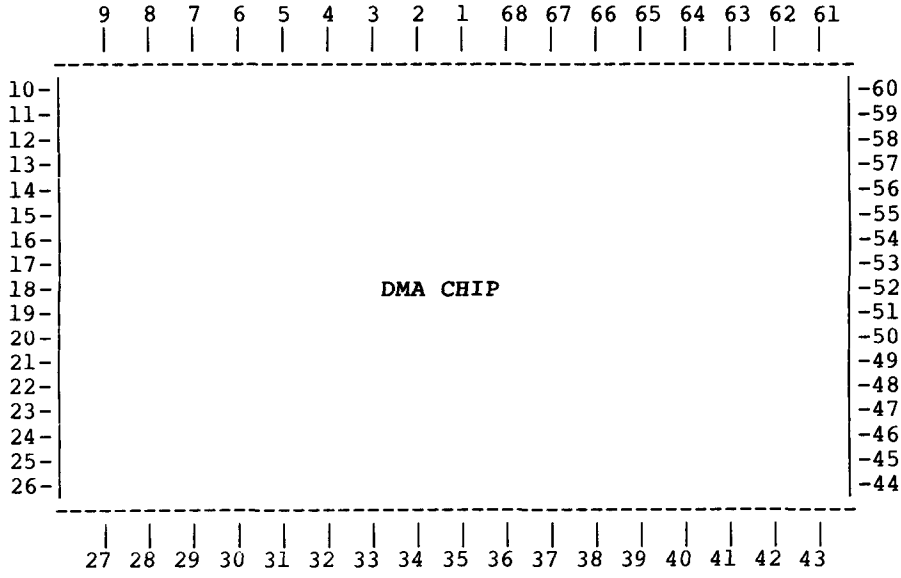
BUFFERS

Provide isolation and drive capability since this circuit will interface directly onto the system bus. These buffers include the bi-directional buffers for address and control strobes (CPU Bus Master - Receive control,address, DMA Bus Master - transmit control,address) but excludes the bi-directional data buffer. Since it must be shared by the memory, this part will be provided externally. Decoding from the ADDRESS DECODE I/O and MEMORY circuitry are combined to provide directional control signals DBDIR, DBENB for this data bus buffer.

FUNCTION	SIGNAL	EQUATION
DATA BUS DIRECTIONAL CONTROL	DBDIR	= DMACSB.IORB + /MCF1./MCF0./19./18./17. /REFRESH. MEMRB + /MCF1. MCF0./19./18. /REFRESH. MEMRB + MCF1. /MCF0./19. /REFRESH. MEMRB + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEMRB
DATA BUS BUFFER ENABLE	DBENB	= DMACSB + WPRCSB + /MCF1./MCF0./19./18./17. /REFRESH. MEM-B + /MCF1. MCF0./19./18. /REFRESH. MEM-B + MCF1. /MCF0./19. /REFRESH. MEM-B + MCF1. MCF0./19.(/18 + 18./17)./REFRESH. MEM-B
ADDRESS BUS, CONTROL BUS DIRECTIONAL CONTROL	DMAAENB	= 8257 Signal AEN inverted

Figure 3 BUFFER CONTROL SIGNALS

PIN LIST


9 8 7 6 5 4 3 2 1 68 67 66 65 64 63 62 61
10-
11-
12-
13-
14-
15-
16-
17-
18-
19-
20-
21-
22-
23-
24-
25-
26-
-60
-59
-58
-57
-56
-55
-54
-53
-52
-51
-50
-49
-48
-47
-46
-45
-44
DMA CHIP
27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43

DESCRIPTION OF EACH PIN FUNCTION

FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER
VSS	1	VDD	35
RFSHB	2	CASB	36
REFRESHB	3	RAS0B	37
MCF1	4	RAS1B	38
MCF0	5	RAS2B	39
WRB	6	MA0	40
FDCDMACKB	7	MA1	41
DACK1B	8	MA2	42
DACK3B	9	MA3	43
DMATC	10	MA4	44
FDCDMARQB	11	MA5	45
DRQ1B	12	MA6	46
DRQ3B	13	MA7	47
DBDIR	14	MA8	48
DBEN	15	A19	49
MEGAPIN	16	A18	50
OSC	17	A17	51
VSS2	18	A16	52
BREQB	19	A15	53
RESET	20	A14	54
AENA	21	A13	55
BRDY	22	A12	56
MEMWB	23	A11	57
MEMRB	24	A10	58
IOWB	25	A9	59
IORB	26	A8	60
D7	27	A7	61
D6	28	A6	62
D5	29	A5	63
D4	30	A4	64
D3	31	A3	65
D2	32	A2	66
D1	33	A1	67
D0	34	A0	68

PIN DEFINITIONS

NOTE: All negative true signals use the suffix "B".

INPUTS: (11 pins)

MCF0	Memory configuration OPTION Select.
MCF1	(See Figure 1 for details.)
RFSH	8237 CHANNEL 0 REQUEST (DREQ2) Input from timer. Set up as 16 microsec interval timer for REFRESH.
DRQ1	8237 CHANNEL 1 REQUEST (DREQ1)
FDCDMARQ	8237 CHANNEL 2 REQUEST (DREQ2) dedicated to FDC.
DRQ3	8237 CHANNEL 3 REQUEST (DREQ3)
READY	System READY signal for DMA.
RESET	System hardware master RESET.
OSC	Memory timing clock. Currently CLK14M.
AEN	CPU Bus Grant (8237 HLDA)
TEST	Input for TEST mode used by IC mfg.

BI-DIRECTIONAL: (32 pins)

BUSA19-BUSA16	System Segment Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
BUSA15-BUSA0	System Address (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
D00-D07	System Data Bus (WRITE-OUTPUT, READ- INPUT)
MRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
MWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IRB	System Memory Read strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)
IWB	System Memory Write strobe (CPU BUS MASTER- INPUT, DMA BUS MASTER- OUTPUT)

OUTPUTS: (20 pins)

MA00-MA08	External Memory multilplexed address
RAS0B-RAS2B	External Memory ROW strobes.
CASB	External Memory COLUMN strobe.
WRB	External Memory WRITE strobe.
DBDIR	Data Buffer directional control (Read=1).
DBENB	Data Buffer enable.
REFRESHB	8237 CHANNEL 0 ACKNOWLEDGE (DREQ0) Acknowledge from DMA channel 0 setup for refresh.
DACK1B	8237 CHANNEL 1 ACKNOWLEDGE (DREQ1)
FDCDMACKB	8237 CHANNEL 2 ACKNOWLEDGE (DREQ2)
DACK3B	8237 CHANNEL 3 ACKNOWLEDGE (DREQ3)
DMATC	8237 EOP (output only)
BREQB	CPU Bus Request (8237 HRQ)

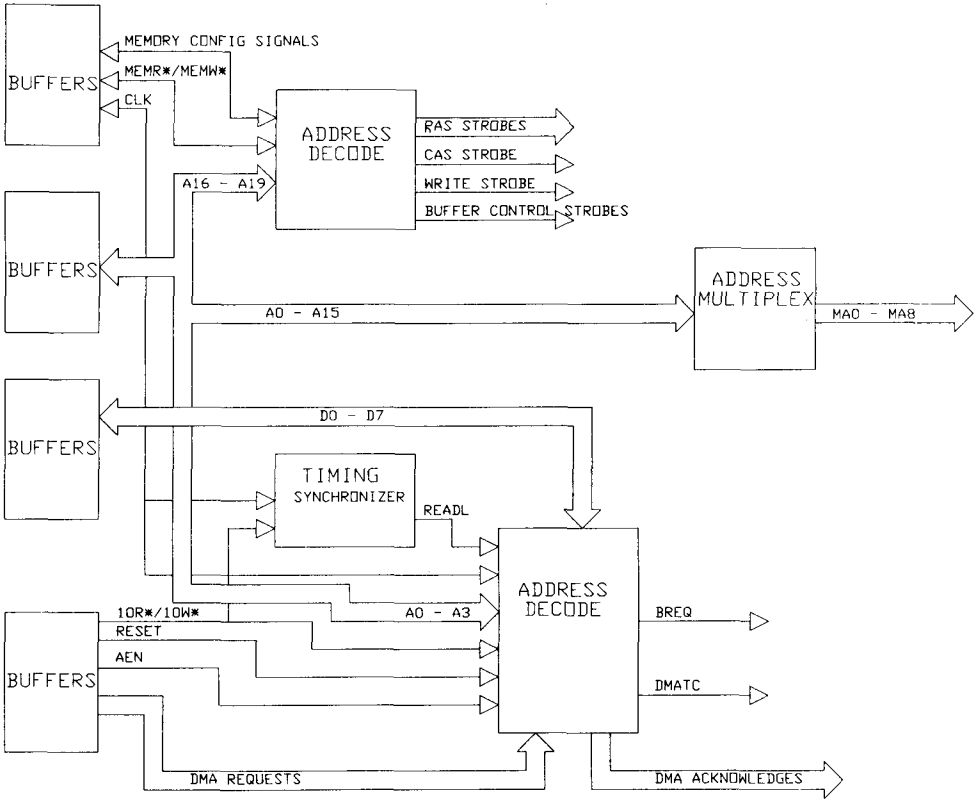
POWER: (4 pins)

VDD	+5 VDC
VSS	GND

TOTAL PIN COUNT = 68

PIN SENSE	DMA PINOUT			8237 PINOUT		
BIDIR	A0	-		A0	-	
BIDIR	A1	|	(BIDIR ENA	A1	|	(BIDIR ENA
BIDIR	A2	|-	= DMAAEN)	A2	|-	=8237 CNTL)
BIDIR	A3	-		A3	-	
TSFBAK	A4	-		A4	-	
TSFBAK	A5	|	(TS ENA	A5	|	(TS ENA
TSFBAK	A6	|-	= DMAAEN)	A6	|	= LOGIC 1)
TSFBAK	A7	-		A7	-	
TSFBAK	A8					
TSFBAK	A9					
TSFBAK	A10					
TSFBAK	A11					
TSFBAK	A12					
TSFBAK	A13					
TSFBAK	A14					
TSFBAK	A15					
TSFBAK	A16					
TSFBAK	A17					
TSFBAK	A18					
TSFBAK	A19					

PIN SENSE	DMA PINOUT	8237 PINOUT
BIDIR	D0	D0
BIDIR	D1	D1
BIDIR	D2	D2
BIDIR	D3	D3
BIDIR	D4	D4
BIDIR	D5	D5
BIDIR	D6	D6
BIDIR	D7	D7
OUTPUT	MAD0	
OUTPUT	MAD1	
OUTPUT	MAD2	
OUTPUT	MAD3	
OUTPUT	MAD4	
OUTPUT	MAD5	
OUTPUT	MAD6	
OUTPUT	MAD7	
TRISTATE	MAD8	
INPUT	RESET	RESET
INPUT	READY	RDY (MUXED)
OUTPUT	DMATC	EOP* (INVERTED)
OUTPUT	BREQ*	HRQ (INVERTED)
INPUT	OSC	CLK (MUXED)
INPUT	DRQ3	DREQ3
INPUT	FDCDMARQ*	DREQ2
INPUT	DRQ1*	DREQ1
INPUT	RFSH*	DREQ0 (MUXED)
OUTPUT	REFRESH*	DACK0
OUTPUT	DACK1*	DACK1
OUTPUT	FDCDMACK*	DACK2
OUTPUT	DACK3*	DACK3
OUTPUT	RAS0	
OUTPUT	RAS1	
OUTPUT	RAS2	
OUTPUT	CAS	AS (MUXED)
OUTPUT	WR*	AEN (MUXED)
INPUT	MCF1	CS (MUXED)
INPUT	MCF0	
OUTPUT	DBDIR	
OUTPUT	DBEN	
INPUT	AEN (SYSTEM)	HLDA
BIDIR	MEMW* -	MW* -
BIDIR	MEMR* | (BIDIR ENA	MR* | (BIDIR ENA
BIDIR	IOW* | = DMAAEN)	IOW* |- =8237 CNTL)
BIDIR	IOR* -	IOR* -
POWER	VDD	VDD
POWER	VDD	VDD
GROUND	VSS	VSS
GROUND	VSS	
	68 PINS	40 PINS



LOGIC BLOCK DIAGRAM

ELECTRICAL SPECIFICATIONS - DMA

ELECTRICAL PARAMETERS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0.0V)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	+150	DEGREES C.
VOLTAGE ON ANY PIN W.R.T.GROUND	-0.5	7.0	VOLTS

OPERATING ELECTRICAL SPECIFICATIONS:

OPERATING AMBIENT	MIN	TYP	MAX	UNITS
AIR TEMP. RANGE	0	25	70	DEGREES C
POWER SUPPLIES				
VDD	4.5	5.0	5.5	VOLTS
VSS	0	0	0	VOLTS
ICC			100	MILLIAMPS

NOTE: INCLUDE ALL RELEVENT CONDITIONS UNDER WHICH ICC IS TO BE MEASURED; IE, ALL INPUTS AT VSS OR VCC, CLOCK FREQUENCY, ETC.

TOTAL POWER DISSIPATION (Include output loading)			700	MILLIWATTS

LEAKAGE CURRENT	MIN	TYP	MAX
Vin = 0.0 v		20	microamps
Vin = 5.0 v		-20	microamps

INPUT VOLTAGES

LOGIC "0" (Vil)		0.8	volts
LOGIC "1" (Vih)	2.0		volts

OUTPUT VOLTAGES	CURRENT LOADING	MIN	TYP	MAX	UNITS
LOGIC "0" (Vol) @ 4.0 MA LOAD				0.4	volts
LOGIC "1" (Voh) @ 0.4 MA LOAD		2.4			volts

INPUT CAPACITANCE	MIN	TYP	MAX
All inputs 0.0 < Vin < 5.0	10		picofarads

OUTPUT CAPACITANCE			
All outputs Except Data (bi-directional)	50		picofarads

BI-DIRECTIONAL CAPACITANCE

SEE NOTES 3-6 IN THE FOLLOWING SECTION.

TIMING SPECIFICATION

MAXIMUM LOADING FOR EACH OUTPUT

Capacitive Load:50pf
Current Load: Ioh = 4.0 MA
Iol = 0.4 MA

INPUT/OUTPUT TIMING

(NOTE: ALL AC TESTING AND TIMING MEASUREMENTS WILL BE AT THE FOLLOWING CONDITIONS: VOH (OUTPUT 1 LEVEL) = 2.0V, AND VOL (OUTPUT 0 LEVEL) = .8V)

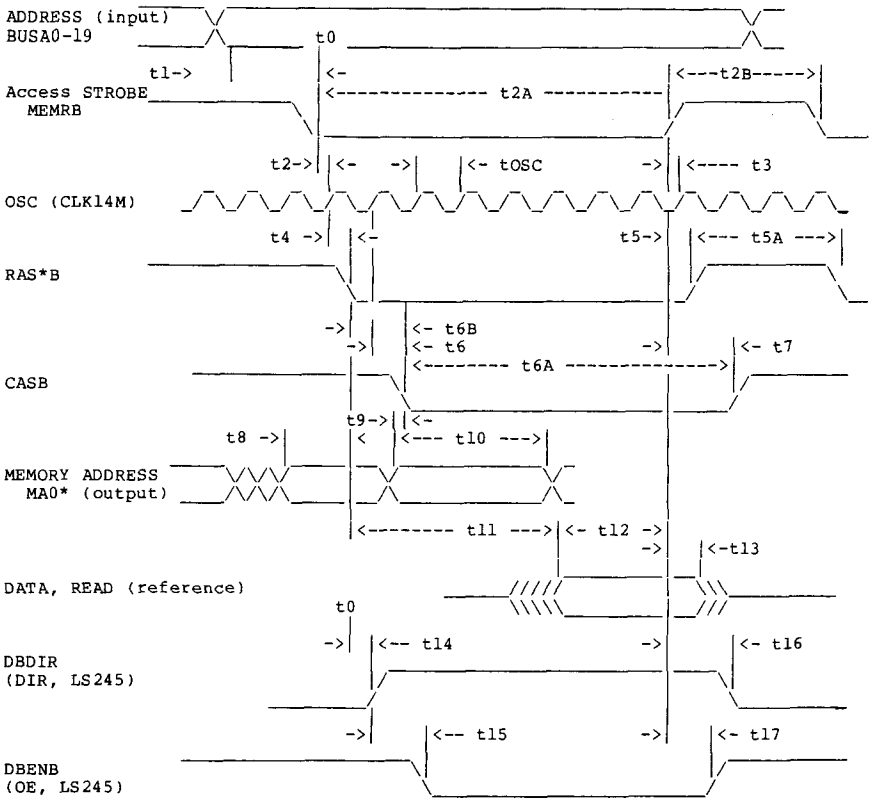


Figure 1. MEMORY TIMING PARAMETERS, READ

MEMORY TIMING PARAMETERS , READ

	min	typ	max	
t0 Reference time zero, STROBE lo tOSC Period of 14.31818 MHz		69.8		
t1 ADDRESS Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length		250		
t2B STROBE hi Length		250		
t3 STROBE hi Setup to OSC hi	don't care			
t4 RAS*B lo Delay from OSC hi	0		40	
t5 RAS*B hi Delay from STROBE hi	0		40	
t5A RAS*B hi Length	100			
t6 CAS*B lo Delay from OSC hi	0		40	
t6A CAS*B lo Length	75			
t6B CAS*B lo Delay from RAS*B lo		69.8	70	
t7 CAS*B hi Delay from STROBE hi		69.8	70	
t8 MA*-Row Address Valid Setup to RAS*B lo	20			NOTE 2
t9 MA*-Column Address Valid Setup to CAS*B lo	20			NOTE 2
t10 MA*-Column Address Hold	35			
t11 DATA Valid Delay from RAS*B True (reference)		150		NOTE 6
t12 DATA Valid Setup to STROBE hi	70			NOTE 3
t13 DATA Hold from STROBE False hi	0			
t14 DBDIR lo Delay from STROBE lo			40	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 4
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold from DBENB hi	0			NOTE 5

NOTE 1 Setup time t2 will be defined by the ASIC design. It should be of sufficient length to allow Clear on RAS flip-flop to go false and still meet setup time before next clock rising edge.

NOTE 2 Address outputs are loaded with 3 row x 8 DRAMS = 24 x 8 pf = 192 pf. each.

NOTE 3 Additional delay through LS245 needs to be added to match Bus Specs.
Bus requires +75 ns setup. LS245 into 45pf requires 20 ns. Therefore 75+20=95 ns.

NOTE 4 Applying the DIRection signal to the LS245 and allowing the part to settle before applying OUTput ENable reduces Bus and power noise. Also OUTput ENable should be removed first.

NOTE 5 OUTput ENable should be removed first before changing DIRection.

NOTE 6 Depends upon DRAM used.

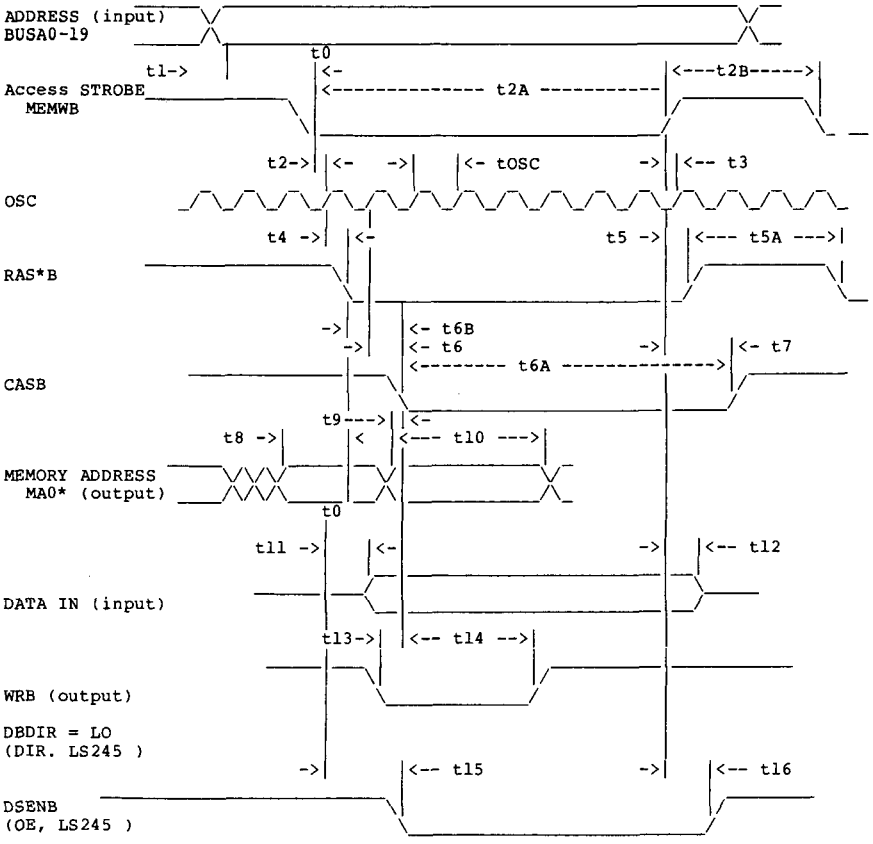


Figure 2. MEMORY TIMING PARAMETERS, WRITE

MEMORY TIMING PARAMETERS, WRITE

	min	typ	max	
t1 thru t10, see MEMORY TIMING PARAMETERS, READ				
t11 DATA Valid Delay after STROBE lo			50	NOTE 1 [1]
t12 DATA Valid Hold after STROBE hi	20			{2}
t13 WRB lo Setup to CASB lo	30			(3)
t14 WRB lo Hold after CASB lo	70			(3)
t15 DBENB lo Delay after STROBE lo		70		[1]
t16 DBENB Hold from STROBE hi	0			[1]

NOTE 1 For CPU generated MEMWB, data will appear about the same time as the STROBE, but for DMA generated MEMWB, data will appear before MEMWB.

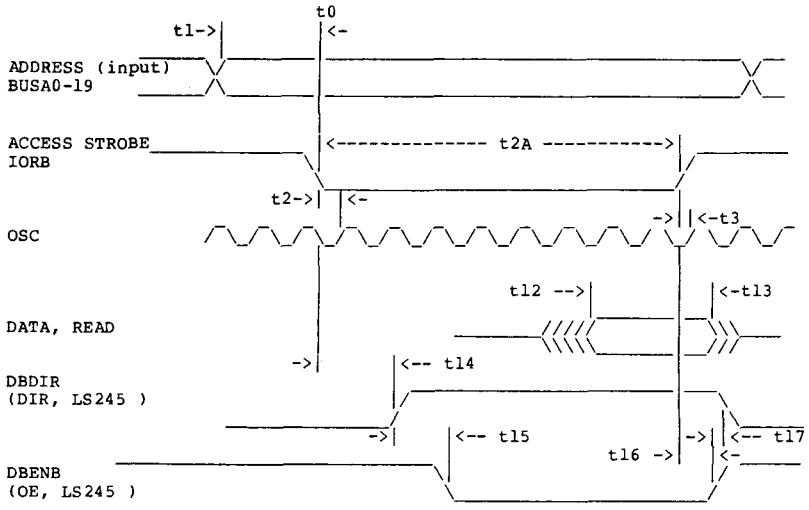


Figure 3. I/O CHIP SELECT PARAMETERS, READ

I/O CHIP SELECT PARAMETERS, READ

	min	typ	max	
t1 ADDRESS Valid Setup to STROBE lo	50			
t2 STROBE lo Setup to OSC hi	15			
t2A STROBE lo Length	420			
t3 STROBE hi Setup to OSC hi	20			
t12 DATA Valid Setup to STROBE hi	90			
t13 DATA Hold from STROBE hi	0			
t14 DBDIR hi Delay from STROBE lo			70	
t15 DBENB lo Delay after DBDIR hi		70		NOTE 1
t16 DBENB Hold from STROBE hi	0			
t17 DBDIR Hold after DBENB hi	0			NOTE 1

NOTE 1 ENable should be removed first before changing DIRection.

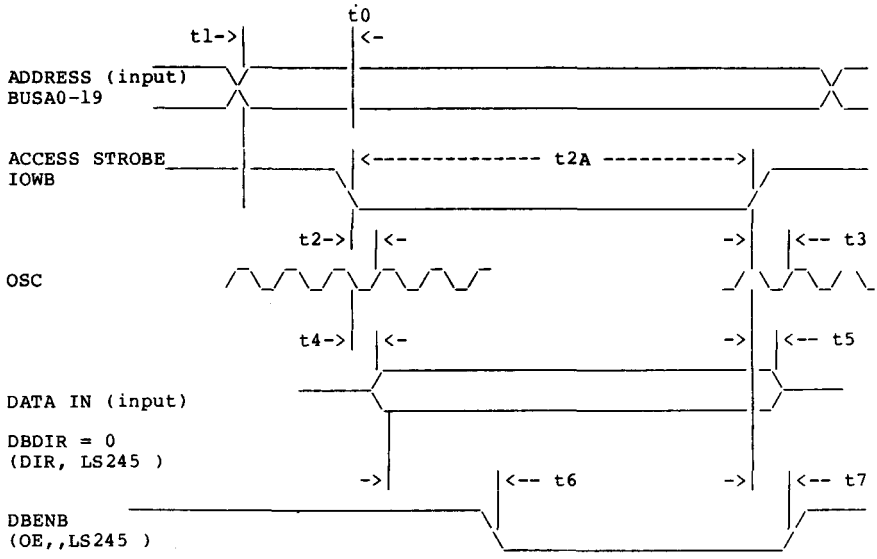


Figure 4. I/O CHIP SELECT PARAMETERS, WRITE

I/O CHIP SELECT PARAMETERS, WRITE

		min	typ	max
t1	ADDRESS Valid Setup to STROBE lo	50		
t2	STROBE lo Setup to OSC hi	15		
t2A	STROBE lo Length	420		
t3	STROBE hi Setup to OSC hi	20		
t4	DATA Valid Setup to STROBE lo		0	
t5	DATA Hold from STROBE hi	0		
t6	DBENB Delay after STROBE lo			70
t7	DBENB Hold from STROBE hi	0		

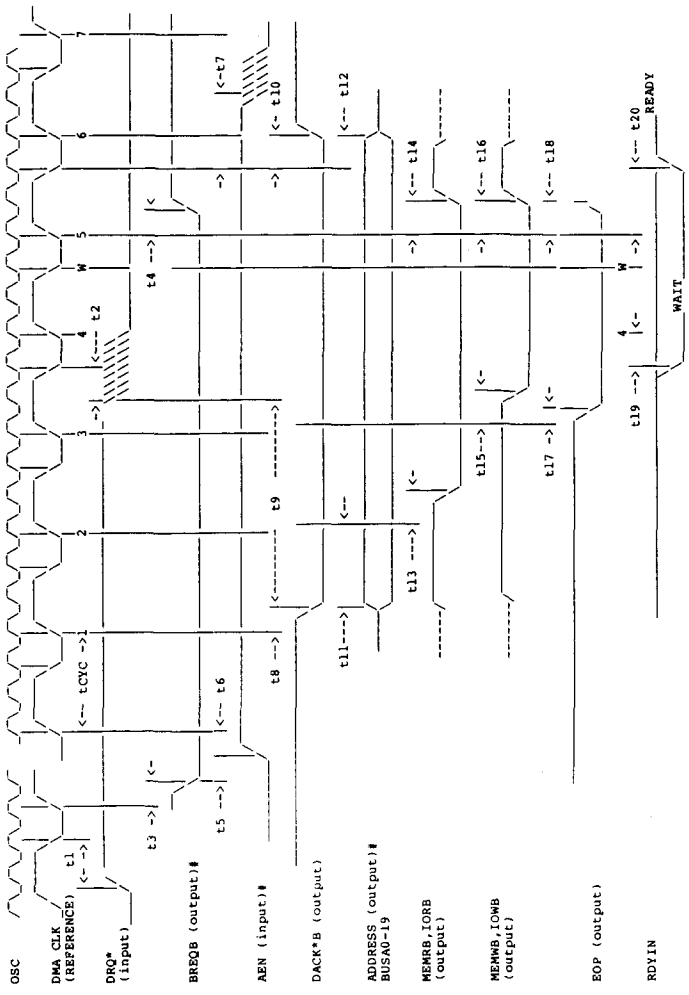


Figure 5. DMA BUS MASTER TIMING, READ / WRITE

DMA BUS MASTER TIMING, READ / WRITE

	min	typ	max	
t1 DRQ* True Setup to CLK lo	30			
t2 DRQ* False Setup to CLK lo	30			
t3 BREQB True Delay from CLK hi			120	8237A-5 tDQl
t4 BREQB False Delay from CLK hi			120	8237A-5 tDQl
t5 AEN True Delay after BREQB True	N x tCYC		+30	N =
t6 AEN True Setup to CLK Hi			40	
t7 AEN False delay from CLK hi			40	
t8 DACK*B True Delay from CLK lo			170	8237A-5 tAK
t9 DACK*B True Hold from AEN True	0			8237A-5 NOTE 6
t10 DACK*B False delay from CLK lo			170	8237A-5 tAK
t11 ADDRESS Valid Setup to CLK Hi	50			System Spec
t12 ADDRESS False delay from CLK hi	0			
t12 MEMRB or IORB True Delay from CLK hi			40	
t13 MEMRB or IORB False Delay after CLK hi			40	
t14 MEMWB or IOWB True Delay from CLK hi			40	
t15 MEMWB or IOWB False Delay after CLK hi			40	
t16 EOP True Delay after CLK hi			40	
t17 EOP False Delay after CLK hi			40	
t18 BRDY False Setup to CLK hi	30			
t19 BRDY False Hold after CLK hi	30			

PRINTER INTERFACE SPECIFICATION

PRINTER INTERFACE SPECIFICATION
CONTENTS

GENERAL DESCRIPTION.....1
SPECIFICATIONS.....3

PRINTER INTERFACE SPECIFICATION
TANDY PART # 8075068
APRIL 30, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075068 - Printer Interface I.C provides the interface between the system I/O bus and the printer Figure 1 shows Block diagram of Printer Interface chip. Figure 2 shows pin configurations of Printer Interface chip.

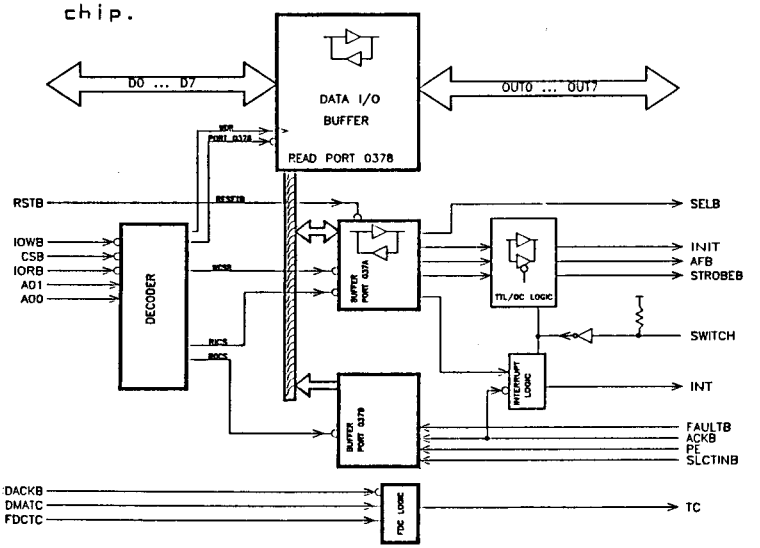


Figure 1.

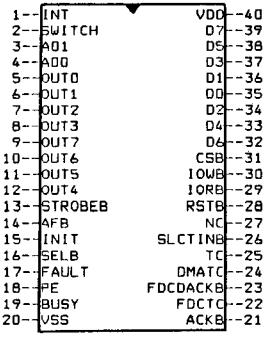


Figure 2.

1.2 DESCRIPTION OF EACH PINS:

Pin#	Pin Name	Type	Description
1	INT	output	Interrupt signal
2	SWITCH	input	Switch for totem pole output or open collector output on INITB, AF, STROBEB.
3	A01	input	CPU address line
4	A00	input	CPU address line
5	OUT0	input/output	Data I/O line
6	OUT1	input/output	Data I/O line
7	OUT2	input/output	Data I/O line
8	OUT3	input/output	Data I/O line
9	OUT7	input/output	Data I/O line
10	OUT6	input/output	Data I/O line
11	OUT5	input/output	Data I/O line
12	OUT4	input/output	Data I/O line
13	STROBEB	output	Printer Strobe signal
14	AFB	output	Printer Autofeed signal
15	INITB	output	Printer Initialize signal
16	SEL	output	Printer Select signal
17	FAULTB	input	Printer Fault signal
18	PE	input	Printer Paper empty signal
19	BUSY	input	Printer Busy signal
20	VSS	ground	Ground
21	ACKB	input	Printer Acknowledge signal
22	FDCTC	input	FDC Terminal Count
23	FDCDACKB	input	FDC-DMA Acknowledge signal
24	DMATC	input	DMA Terminal Count
25	TC	output	FDC Terminal Count signal
26	SLCTINB	input	Printer Select input
27	NC	--	Not used
28	RSTB	input	System Reset
29	IORB	input	CPU I/O Read strobe
30	IOWB	input	CPU I/O Write strobe
31	CSB	input	Chip select signal
32	D6	Input/output	CPU Data I/O
33	D4	Input/output	CPU Data I/O
34	D2	Input/output	CPU Data I/O
35	D0	Input/output	CPU Data I/O
36	D1	Input/output	CPU Data I/O
37	D3	Input/output	CPU Data I/O
38	D5	Input/output	CPU Data I/O
39	D7	Input/output	CPU Data I/O
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

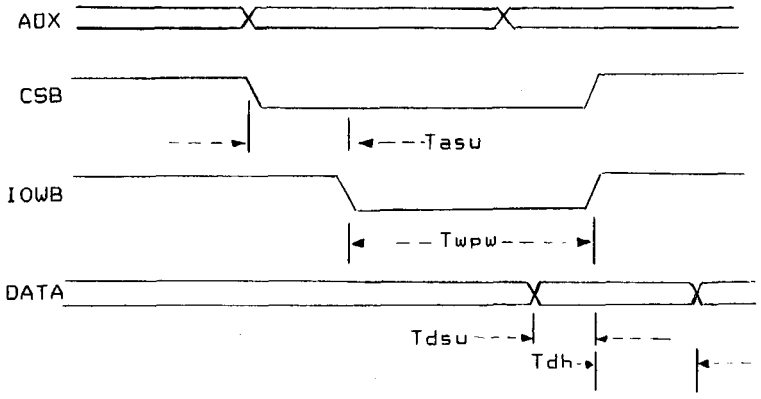
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

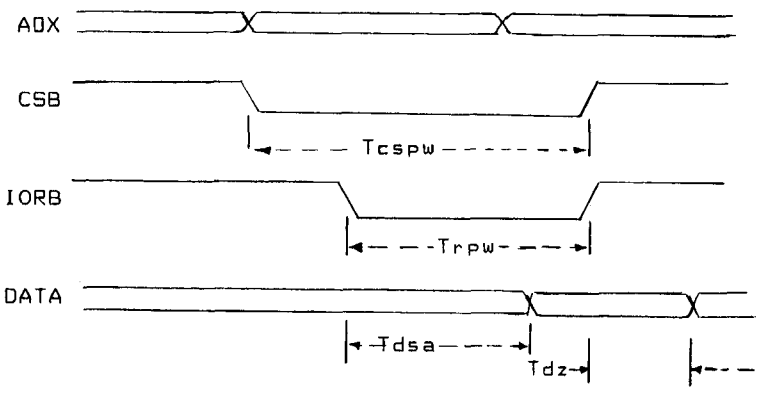
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	n	

KEYBOARD INTERFACE SPECIFICATION

KEYBOARD INTERFACE SPECIFICATION
CONTENTS

GENERAL DESCRIPTION.....1
SPECIFICATIONS.....3

KEYBOARD INTERFACE SPECIFICATION
TANDY PART # 8075069
MAY 05, 1986

1. GENERAL DESCRIPTION

1.1 The Tandy part# 8075069 - Keyboard Interface I.C provides two functions:

a. Interface between the system I/O bus and keyboard.

b. FDC support logic that generates DRIVE SELECT SIGNAL, MOTOR ON SIGNAL, FDC TERMINAL COUNT, FDC RESET and DMA/I.

Figure 1. shows block diagram of Keyboard Interface chip
Figure 2. shows pin configuration of Keyboard Interface chip.

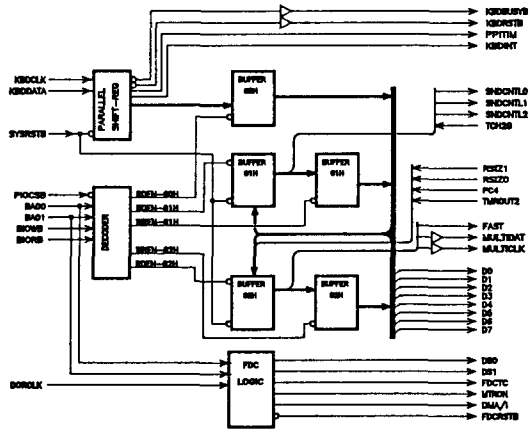


Figure 1.

1	KBDCLK	VDD	40
2	KBDDATA	MULTICLK	39
3	KBDBUSYB	MULTIDAT	38
4	KBDINT	FAST	37
5	RSIZ0	TCH2G	36
6	RSIZ1	PPITIM	35
7	D0	DS0	34
8	D1	DS1	33
9	D2	FDCRST	32
10	D3	DMA/I	31
11	D4	MTRON	30
12	D5	FDCTC	29
13	D6	SNDCNTL2	28
14	D7	SNDCNTL0	27
15	PIOCSB	SNDCNTL1	26
16	BA00	TMROUT2	25
17	BA01	PC4	24
18	BIORB	SYSRSTB	23
19	BIOWB	KBDRSTB	22
20	VSS	DORCLK	21

Figure 2.

1.2 DESCRIPTION OF EACH PIN:

Pin#	Pin Name	Type	Description
1	KBDCLK	input	Keyboard clock
2	KBDDATA	input	Keyboard data
3	KBDBUSYB	output	Keyboard busy signal
4	KBDINT	output	Keyboard interrupt signal
5	RSIZ0	input	Monochrome/color monitor mode
6	RSIZ1	input	Reserved
7	D0	input/output	Data I/O line
8	D1	input/output	Data I/O line
9	D2	input/output	Data I/O line
10	D3	input/output	Data I/O line
11	D4	input/output	Data I/O line
12	D5	input/output	Data I/O line
13	D6	input/output	Data I/O line
14	D7	input/output	Data I/O line
15	PIOCSB	input	Chip select strobe
16	BA00	input	CPU address line
17	BA01	input	CPU address line
18	BIORB	input	CPU I/O read strobe
19	BIOWB	input	CPU I/O write strobe
20	VSS	ground	Ground
21	DORCLK	input	Decode latch clock
22	KBDRSTB	output	Keyboard reset signal
23	SYSRSTB	input	System reset signal
24	PC4	input	Video memory size mode
25	TMROUT2	input	Timer counter from 8253 out2
26	SNDCNTL1	output	Sound control 1
27	SNDCNTL0	output	Sound control 0
28	SNDCNTL2	output	Sound control 2
29	FDCTC	output	FDC terminal count
30	MTRON	output	Motor ON signal to disk drive
31	DMA/I	output	DMA Request & FDC Interrupt enable
32	FDCRSTB	output	FDC reset signal
33	DS1	output	Drive select 1 signal
34	DS0	output	Drive select 0 signal
35	PPITIM	output	Timer Video signal
36	TCH2G	output	Timer channel 2 gate
37	FAST	input	4.77Mhz or 7.16Mhz mode select
38	MULTIDAT	output	Multi-data
39	MULTICLK	output	Multi-clock
40	VDD	power	+5 Volt Power Supply

2. ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature -65 C to 150 C
2.2 Operating Temperature 0 C to 70 C

3. ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating

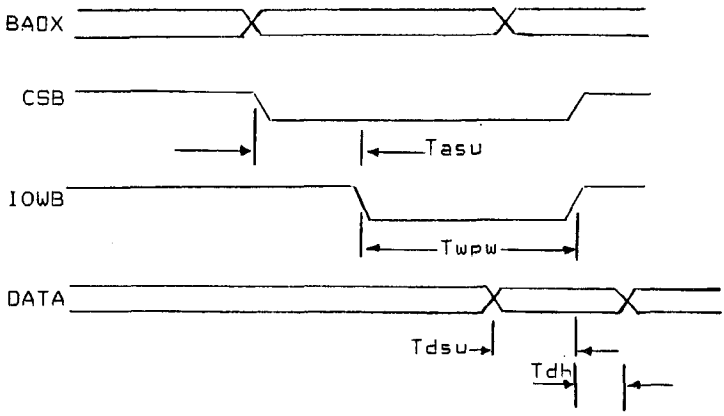
Parameter	Min.	Typ.	Max.	Units	Cond.
Voltage, any pin	-1.0		7.0	Volts	W.R.T ground
Power Dissipation			0.5	Watts	

3.2 D.C. Electrical Characteristics

Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
VDD	Supply Voltage	4.5	5.0	5.5	Volts	
Icc(q)	Quiescent current			50	uA	
Icc(o)	Operating Current			40	mA	
Vil	Input Low Voltage			0.8	Volts	TTL inputs
Vih	Input High Voltage	2.0			Volts	TTL inputs
Iin	Input Leakage	-10		10	uA	
Cin	Input Capacitance			7	pF	
Vol	Output Low Voltage			0.4	Volts	@4 mA
Voh	Output High Voltage	2.4			Volts	@-2 mA
Ioz	High Impedance Leak	-10		10	uA	

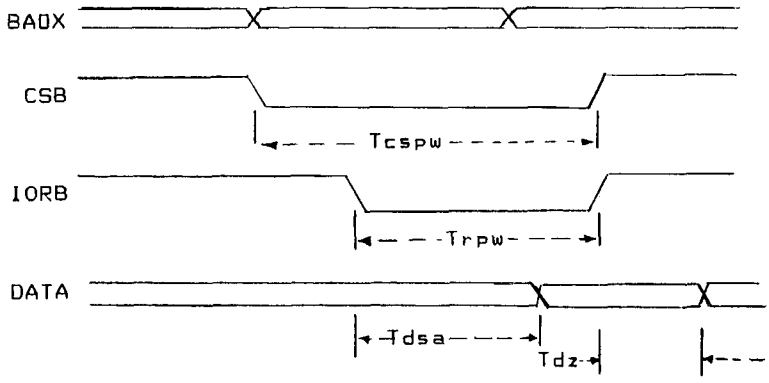
3.3 A.C Electrical Characteristics

3.3.1 Write Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tasu	Address Setup	15			nS	
Twpw	Write Pulse Width	69			nS	
Tdsu	Data Setup	29			nS	
Tdh	Data Hold	6			nS	

3.3.2 Read Cycle



Symb.	Parameter	Min.	Typ.	Max.	Units	Cond.
Tcspw	Chip Select Width	69			nS	
Trpw	Read Pulse Width	69			nS	
Tda	Data Access			69	nS	
Tdz	Bus Hold/release	6		25	ns	

TIMING CONTROL GENERATOR

TIMING CONTROL GENERATOR
CONTENTS

GENERAL DESCRIPTION
BLOCK DIAGRAM
SPECIFICATIONS
TIMING DIAGRAMS

TIMING CONTROL GENERATOR
TANDY PART # 8075306
MAY 07, 1986
REV 050886

1.0 GENERAL DESCRIPTION

1.1 The Tandy part # 8075306 - Timing Control Generator:

- creates eight clock outputs from two independent oscillator inputs.
- synchronizes the ready signals.
- synthesizes the system control strobes from the CPU status signals.
- interfaces the system signals (HOLD, HLDA) with the CPU signals (RQ/GT).
- creates two FDC chip selects and the DMA request delay.

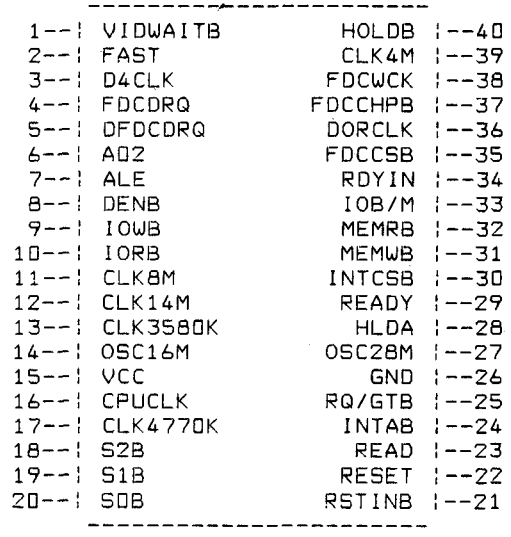
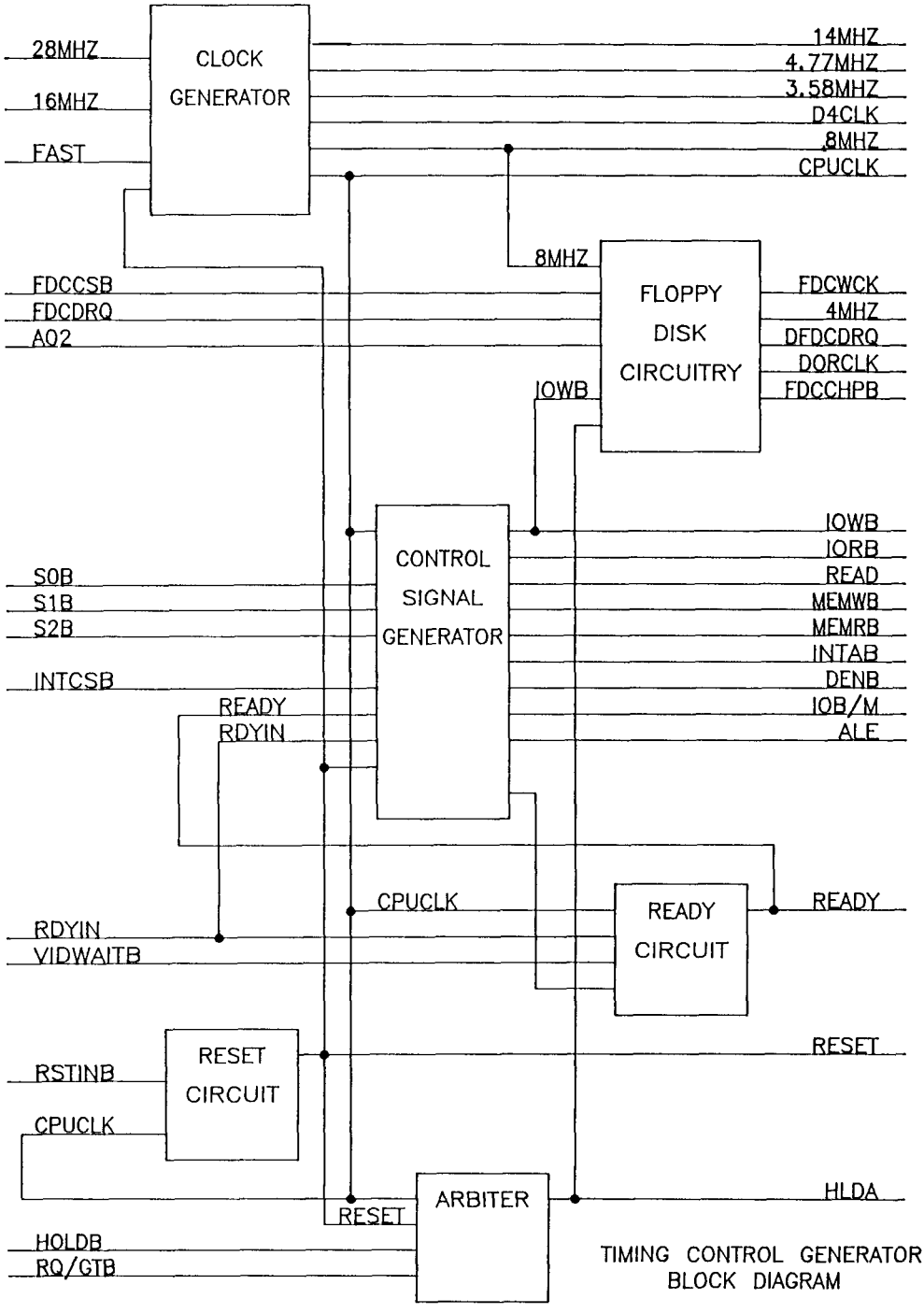


Figure 1. Pin Assignment

1.2 DESCRIPTION OF PINS:

Pin #	Pin Name	Type	Description
1	VIDWAITB	INPUT	Wait signal from video system (0 = Wait)
2	FAST	INPUT	Clock speed select
3	D4CLK	OUTPUT	CLK477M/4, Squarewave
4	FDCDRQ	INPUT	FDC DMA Request
5	DFDCDRQ	OUTPUT	Beginning of FDCDRQ delayed 1.0 microsec
6	A02	INPUT	System Address
7	ALE	OUTPUT	Address Latch Enable
8	DENB	OUTPUT	Data Enable
9	IOWB	OUTPUT	I/O Write
10	IORB	OUTPUT	I/O Read
11	CLK8M	OUTPUT	OSC16M/2, Squarewave
12	CLK14M	OUTPUT	OSC28M/2, Squarewave
13	CLK3580K	OUTPUT	OSC28M/8, Squarewave
14	OSC16M	INPUT	Input Frequency = 16.00000 MHz
15	VCC	POWER	
16	CPUCLK	OUTPUT	FAST=1, CPUCLK=7.16MHz (OSC28M/4, 50-50 cycle) FAST=0, CPUCLK=4.77MHz (OSC28M/6, 33-67 cycle)
17	CLK4770K	OUTPUT	CLK14M/3, 33% duty cycle
18	S2B	INPUT	8088 Status Signal
19	S1B	INPUT	8088 Status Signal
20	S0B	INPUT	8088 Status Signal
21	RSTINB	INPUT	Asynchronous system input
22	RESET	OUTPUT	8088 CPU Reset input
23	READ	OUTPUT	Directional Control for CPU Data buffer
24	INTAB	OUTPUT	Interrupt Acknowledge
25	RQ/GTB	INPUT/OUTPUT	Request/Acknowledge/Release
26	GND	GROUND	
27	OSC28M	INPUT	Input frequency = 28.63636 MHz
28	HLDA	OUTPUT	Bus Acknowledge
29	READY	OUTPUT	8088 CPU READY input
30	INTCSB	INPUT	8257 Interrupt Controller Chip Select
31	MEMWB	OUTPUT	Memory Write
32	MEMRB	OUTPUT	Memory Read
33	IOB/M	OUTPUT	1 = Memory access, 0 = I/O access
34	RDYIN	INPUT	Asynchronous system input (0 = Wait condition)
35	FDCCSB	INPUT	Previously decoded FDC Function I/O chip select
36	DORCLK	OUTPUT	Configuration register Chip Select
37	FDCCHPB	OUTPUT	FDC Chip Select
38	FDCWCK	OUTPUT	Pulse, Period = 2 microsec, 250(nom) pulse
39	CLK4M	OUTPUT	OSC16M/4, Squarewave
40	HOLDB	INPUT	Bus Request



TIMING CONTROL GENERATOR
BLOCK DIAGRAM

2.0 ENVIRONMENTAL SPECIFICATIONS

2.1 Storage Temperature: -65 min, +150 max degrees C
2.2 Operating temperature: 0 min, +25 typ, + 70 max degrees C

3.0 ELECTRICAL SPECIFICATIONS

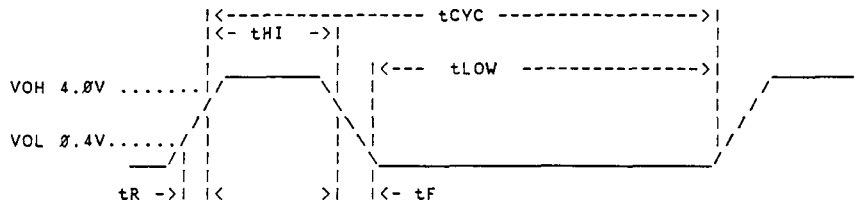
3.1 Absolute Maximum Rating:
Voltage on any pin w.r.t. Ground: -0.5 min, 7.0 max volts

3.2 Operating Electrical Specifications:

	min	typ	max	units
3.2.1 Operating Ambient:				
Air Temp. Range	0	25	70	degrees C
3.2.2 Power Supplies:				
VCC	4.5	5.0	5.5	volts
VSS	0	0	0	volts
ICC			100	milliamps
Total Power			700	milliwatts
3.2.3 Leakage Current, All Inputs:				
Vin = 0.0 v			-10	microamps
Vin = 5.0 v			+10	microamps
3.2.4 Input voltages:				
Logic "0"			.8	volts
Except RSTIN			.5	volts
Logic "1"	2.0			volts
Except RSTIN	3.5			volts
3.2.5 Output Voltages:				
logic "0" @ 4.0 mA load			.4	volts
logic "1" @ 4.0 mA load	2.4			volts
except all clocks	4.0			volts
3.2.6 INPUT CAPACITANCE (0.0 < Vin < 5.0)				
All inputs			10	pf
3.2.7 OUTPUT CAPACITANCE				
All loads			50	pf

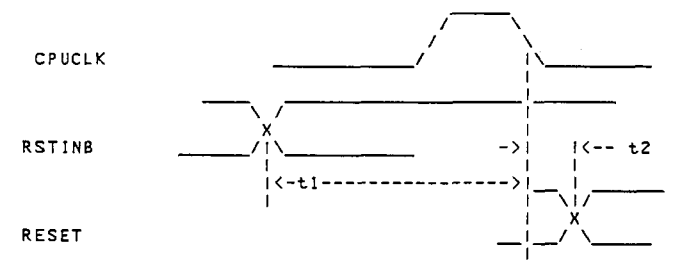
TIMING DIAGRAMS

FIGURE 1. CPUCLK



CLOCK PARAMETER	7.16 MHZ			4.77MHZ			
	min	typ	max	min	typ	max	
tHI Level at least 4.Øv	44	(69.5-tR-tF)		69	69.5		ns
tLOW Level not greater than Ø.4v	68	69.5		118	(14Ø-tR-tF)		ns
tR Rise time , Ø.4 to 4.Øv			8			1Ø	ns
tF fall time , 4.Ø to Ø.4v			7			1Ø	ns
tCYC		14Ø			21Ø		ns

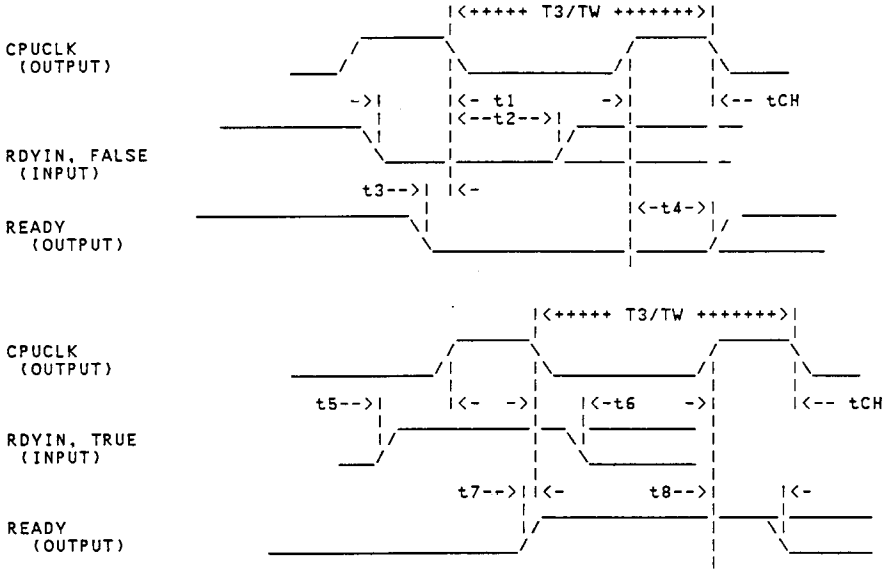
FIGURE 2. RESET



RESET PARAMETERS

t1 RSTIN Setup to CPUCLK low	Asynchronous input
t2 RESET Delay from CPUCLK low	4Ø ns max

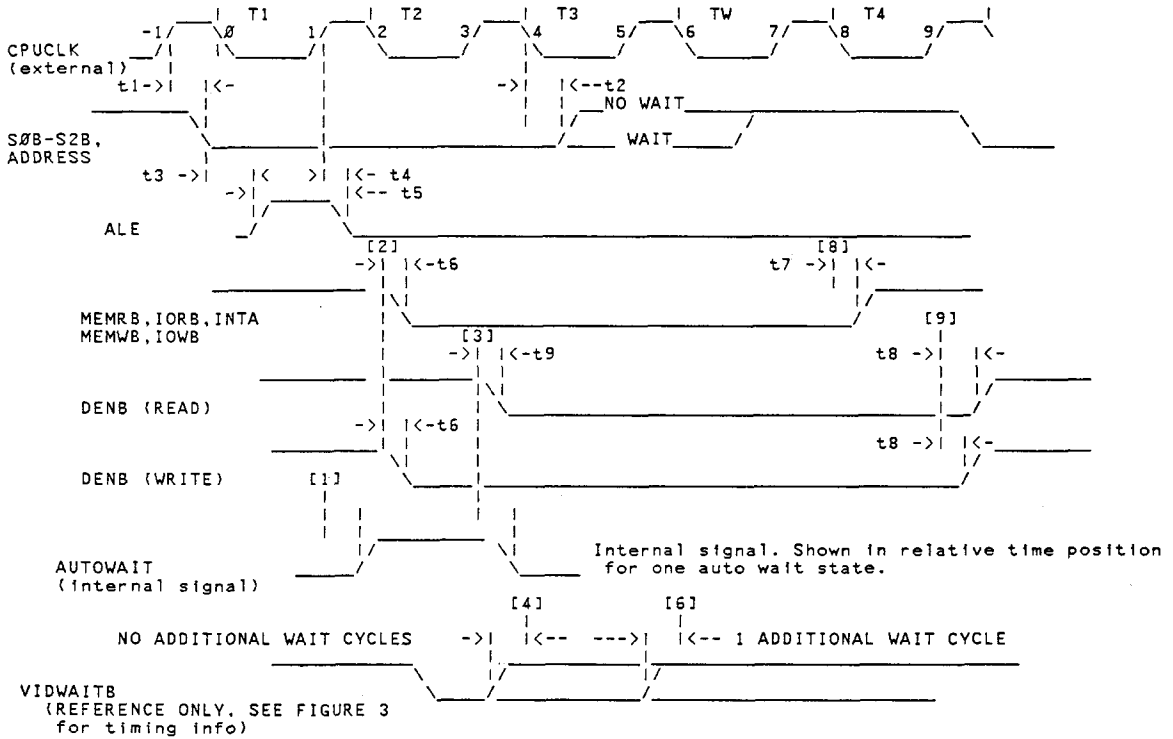
FIGURE 3. READY



READY PARAMETER

	min	max		
t1 RDYIN False Setup to CPUCLK low	35		ns	
t2 RDYIN False Hold after CPUCLK low	10		ns	
t3 READY False before CPUCLK low	-8		ns	tRYLCL 8088
t4 READY False Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088
t5 RDYIN True Setup to CPUCLK hi	35		ns	
t6 RDYIN True Hold after CPUCLK low	10		ns	
t7 READY True before CPUCLK low	0		ns	tRYHCH 8088
t8 READY True Hold after CPUCLK hi		tCH + 8	ns	tCHRYX 8088

FIGURE 4. CONTROL GENERATOR



CONTROL GENERATOR

	min	max		
t1 STATUS Active Delay from CLK hi	1Ø	6Ø	ns	tCHSV 8Ø88
t2 STATUS Inactive Delay from CLK low	1Ø	7Ø	ns	tCLSH 8Ø88
t3 ALE True Delay from Status Active		2Ø	ns	tSVLH 8288

t4 ALE False Delay from CLK hi		2Ø	ns
t5 ALE Pulse Width	55		ns
t6 STROBE True Delay from CLK low		3Ø	ns
t7 STROBE False Delay from CLK low		3Ø	ns
t8 STROBE False Delay from CLK hi		3Ø	ns
t9 STROBE True Delay from Clk hi		3Ø	ns

FIGURE 5A. ARBITTER/REQUEST

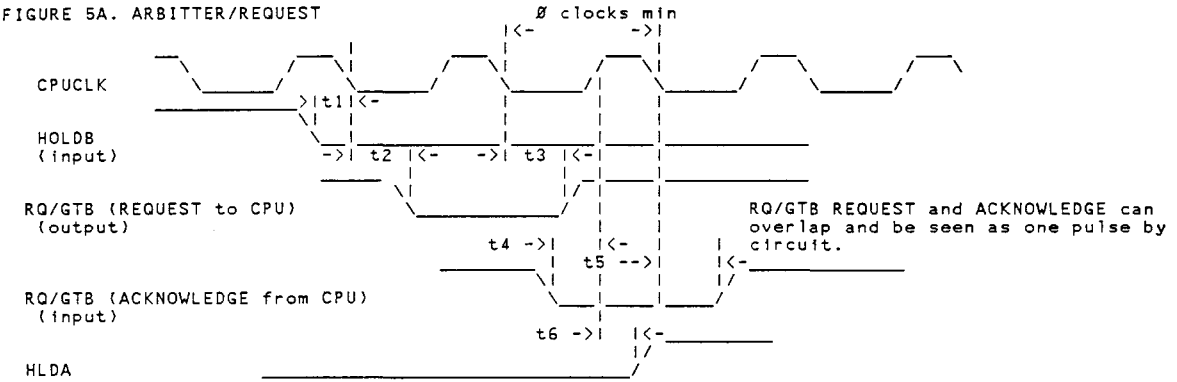
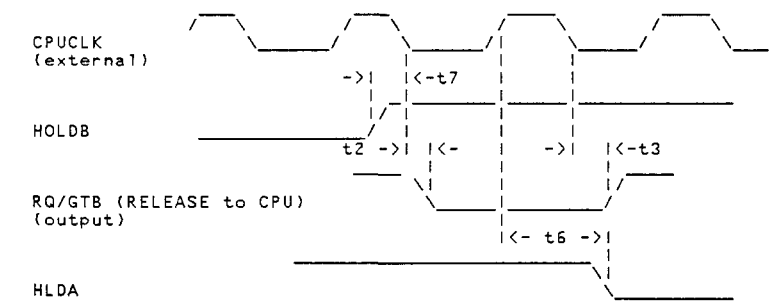


FIGURE 5B. ARBITTER/RELEASE

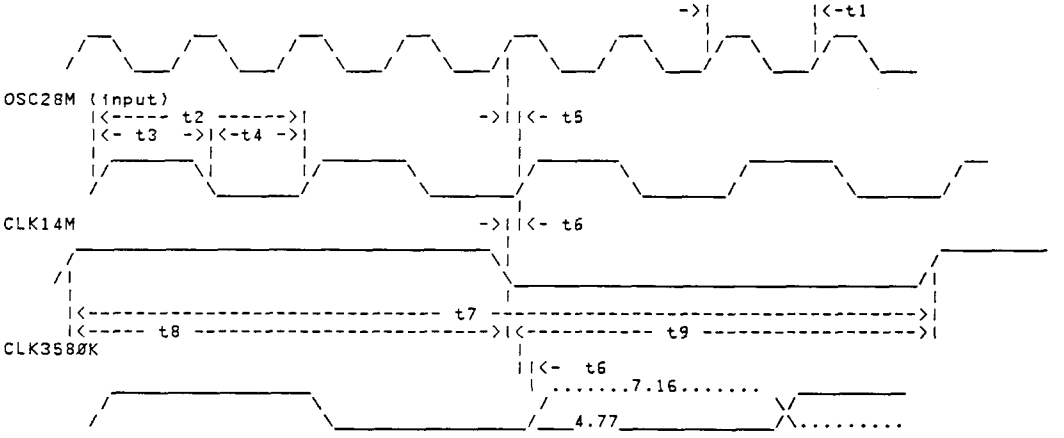


ABRITTER PARAMETER

	min	max		
t1 HOLDB (True) setup to CPUCLK low	2Ø		ns	
t2 CPUCLK low to RQ/GTB active (REQ/REL pulse)		5Ø	ns	tGVCH 8Ø88

t3 CPUCLK low to RQ/GTB inactive (REQ/REL pulse)		5Ø	ns	tCHGX 8Ø88
t4 RQ/GTB (True) setup to CPUCLK hi (ACK pulse)	2Ø		ns	tCLGL 8Ø88
t5 RQ/GTB (False) hold from CPUCLK low (ACK pulse)		5Ø	ns	tCLGH 8Ø88
t6 CPUCLK hi to HLDA Delay		3Ø	ns	
t7 HOLDB (False) Setup to CPUCLK low	2Ø		ns	

FIGURE 6. OSCILLATOR/CLOCK RELATIONSHIPS, 28 MHZ



CPUCLK (See Fig. 1 for Specs)

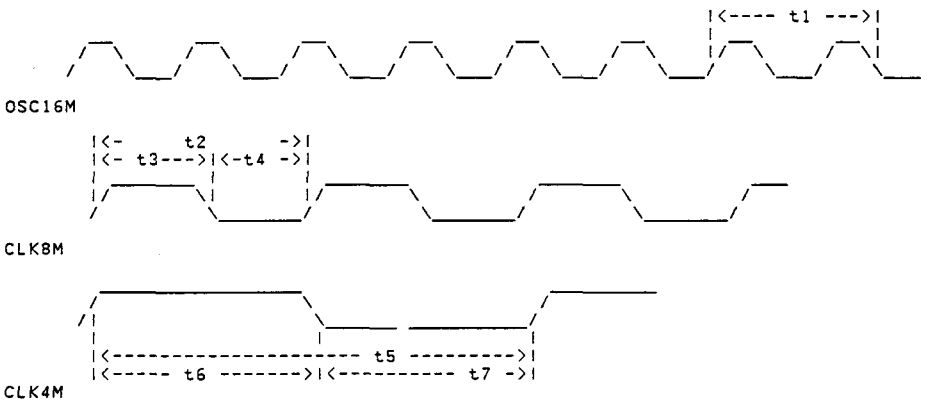
CLOCK PARAMETER	min	typ	max	
t1 OSC28M Period		34.9		NOTE 1
t2 CLK14M Period		t1 x 2		
t3 CLK14M high (includes tRISE)	-1Ø%	t2/2	+1Ø%	
t4 CLK14M low (includes tFALL)		(t2-t3)		
t5 OSC28M to CLK*M Output Delay skew		15		
t6 CLK*M to CLK*M Output Delay skew		15		
t7 CLK358ØK Period		t1 x 8		
t8 CLK358ØK high (includes tRISE)	-1Ø%	t7/2	+1Ø%	

t9	CLK3580K low (includes tFALL)	(t7-t8)	
tR	CLK*M		10 ns
tF	CLK*M		10 ns

NOTE 1 Use only one edge because the oscillator duty cycle symmetery can not be specified.

NOTE 2 Phase Relationship is important between the CLK14M clock and the outputs it generates.

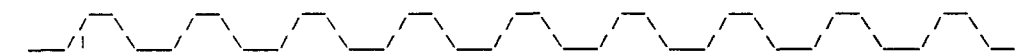
FIGURE 7. OSCILLATOR/CLOCK RELATIONSHIPS, 8MHZ



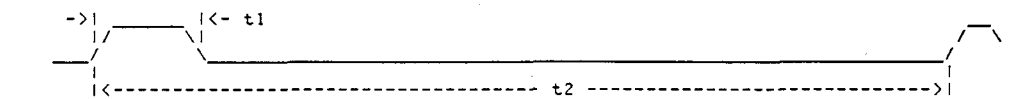
CLOCK PARAMETER		min	typ	max
t1	OSC16M Period		62.5	
t2	CLK8M Period		t1 x 2	
t3	CLK8M High (includes tRISE)	-10%	t2/2	+10%
t4	CLK8M Low (includes tFALL)		t2-t3	
t5	CLK4M Period		t1 x 4	
t6	CLK4M High (includes tRISE)	-10%	t5/2	+10%
t7	CLK4M Low (includes tFALL)		t5-t6	

tR		10 ns
tF		10 ns

FIGURE 8. FDCCLK/FDWCK RELATIONSHIPS



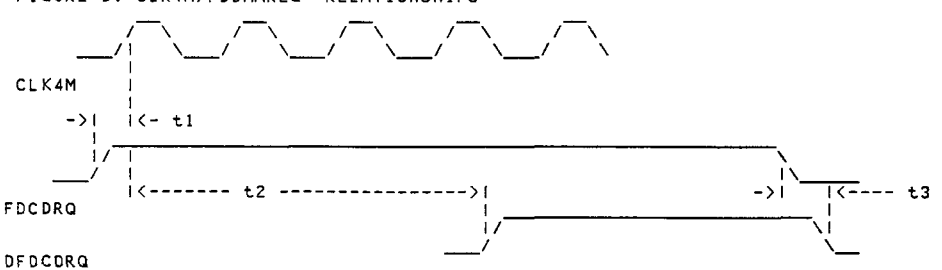
CLK4M (see FIG 7)



FDCWCK

CLOCK PARAMETER	min	typ	max	
t1 FDCWCK High (includes tRISE)		250		ns
t2 FDCWCK Period		2.0		us

FIGURE 9. CLK4M/FDDMAREQ RELATIONSHIPS



CLOCK PARAMETER					
	min	typ	max		
t1 FDCDRQ Setup to CLK4M	2Ø			ns	Asynchronous
t2 DFDCDRQ Delay TRUE	.75 us	1.Ø us	1.1	us	
t3 FDCDRQ False to DFDCDRQ False Delay			3Ø	ns	

8087 NUMERIC DATA COPROCESSOR

8087
NUMERIC DATA COPROCESSOR
8087/8087-2/8087-1

- **High Performance Numeric Data Coprocessor**
- **Adds Arithmetic, Trigonometric, Exponential, and Logarithmic Instructions to the Standard iAPX 86 and iAPX 186 Instruction Set For All Data Types**
- **All 24 Addressing Modes Available with 8086, 8088, 80186, 80188 CPUs.**
- **Compatible with Proposed IEEE Floating Point Standard**
- **CPU/8087 System Supports 8 Data Types: 16-, 32-, 64-Bit Integers, 32-, 64-, 80-Bit Floating Point, and 18-Digit BCD Operands**
- **Adds 8 x 80-Bit Individually Addressable Register Stack**
- **7 Built-in Exception Handling Functions**
- **MULTIBUS System Compatible Interface**

The 8087 Numeric Data Coprocessor provides the instructions and data types needed for high performance numeric applications, providing up to 100 times the performance of a CPU alone. The 8087 is implemented in N-channel, depletion load, silicon gate technology (HMOS), housed in a 40-pin package. Sixty-eight numeric processing instructions are added to the iAPX 86, 186 instruction sets, and eight 80-bit registers are added to the register set. The 8087 is compatible with the proposed IEEE Floating Point Standard.

The two-chip numeric data processing systems are referred to as follows;

iAPX 86/20—16-bit 8086 CPU with 8087
iAPX 88/20—8-bit 8088 CPU with 8087
iAPX 186/20—16-bit 80186 CPU with 8087
iAPX 188/20—8-bit 80188 CPU with 8087

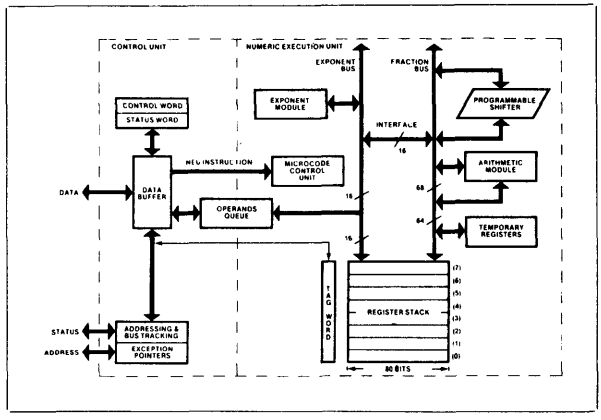


Figure 1. 8087 Block Diagram

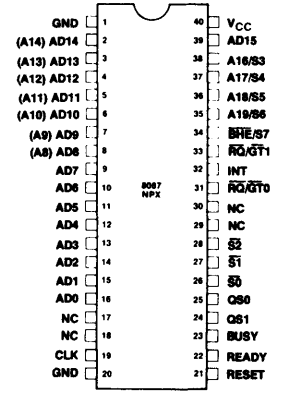


Figure 2. 8087 Pin Configuration

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October 1984
ORDER NUMBER: 205835-002

Table 1. 8087 Pin Description

Symbol	Type	Name and Function
AD15-AD0	I/O	**Address Data:** These lines constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7-D0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory operations. Eight-bit oriented devices tied to the lower half of the bus would normally use A0 to condition chip select functions. These lines are active HIGH. They are input/output lines for 8087-driven bus cycles and are inputs which the 8087 monitors when the CPU is in control of the bus. A15-A8 do not require an address latch in an iAPX 88/20 or iAPX 188/20. The 8087 will supply an address for the T_1-T_4 period.
A19/S6, A18/S5, A17/S4, A16/S3	I/O	**Address Memory:** During T_1 these are the four most significant address lines for memory operations. During memory operations, status information is available on these lines during T_2, T_3, T_W, and T_4. For 8087-controlled bus cycles, S6, S4, and S3 are reserved and currently one (HIGH), while S5 is always LOW.These lines are inputs which the 8087 monitors when the CPU is in control of the bus.
BHE/S7	I/O	**Bus High Enable:** During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15-D8. Eight-bit-oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read and write cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T_2, T_3, T_W, and T_4. The signal is active LOW. S7 is an input which the 8087 monitors during the CPU-controlled bus cycles.
$\overline{S2}$, $\overline{S1}$, $\overline{S0}$	I/O	**Status:** For 8087-driven bus cycles, these status lines are encoded as follows: $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ 0 (LOW) X X Unused 1 (HIGH) 0 0 Unused 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 Passive Status is driven active during T_4, remains valid during T_1 and T_2, and is returned to the passive state (1, 1, 1) during T_3 or during T_w when READY is HIGH. This status is used by the 8288 Bus Controller (or the 82188 Integrated Bus Controller with an 80186/80188 CPU) to generate all memory access control signals. Any change in $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_w is used to indicate the end of a bus cycle. These signals are monitored by the 8087 when the CPU is in control of the bus.
$\overline{RQ}/\overline{GT0}$	I/O	**Request/Grant:** This request/grant pin is used by the 8087 to gain control of the local bus from the CPU for operand transfers or on behalf of another bus master. It must be connected to one of the two processor request/grant pins. The request grant sequence on this pin is as follows: 1. A pulse one clock wide is passed to the CPU to indicate a local bus request by either the 8087 or the master connected to the 8087 $\overline{RQ}/\overline{GT1}$ pin. 2. The 8087 waits for the grant pulse and when it is received will either initiate bus transfer activity in the clock cycle following the grant or pass the grant out on the $\overline{RQ}/\overline{GT1}$ pin in this clock if the initial request was for another bus master. 3. The 8087 will generate a release pulse to the CPU one clock cycle after the completion of the last 8087 bus cycle or on receipt of the release pulse from the bus master on $\overline{RQ}/\overline{GT1}$. For iAPX 186/188 systems, the same sequence applies except $\overline{RQ}/\overline{GT}$ signals are converted to appropriate HOLD, HLDA signals by the 82188 Integrated Bus Controller. This is to conform with iAPX 186/188's HOLD, HLDA bus exchange protocol. Refer to the 82188 data sheet for further information.

Table 1. 8087 Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{RQ}/\overline{GT1}$	I/O	**Request/Grant:** This request/grant pin is used by another local bus master to force the 8087 to request the local bus. If the 8087 is not in control of the bus when the request is made the request/grant sequence is passed through the 8087 on the $\overline{RQ}/\overline{GT0}$ pin one cycle later. Subsequent grant and release pulses are also passed through the 8087 with a two and one clock delay, respectively, for resynchronization. $\overline{RQ}/\overline{GT1}$ has an internal pullup resistor, and so may be left unconnected. If the 8087 has control of the bus the request/grant sequence is as follows: 1. A pulse 1 CLK wide from another local bus master indicates a local bus request to the 8087 (pulse 1). 2. During the 8087's next T_4 or T_1 a pulse 1 CLK wide from the 8087 to the requesting master (pulse 2) indicates that the 8087 has allowed the local bus to float and that it will enter the "RQ/GT acknowledge" state at the next CLK. The 8087's control unit is disconnected logically from the local bus during "RQ/GT acknowledge." 3. A pulse 1 CLK wide from the requesting master indicates to the 8087 (pulse 3) that the "RQ/GT" request is about to end and that the 8087 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. For iAPX 186/188 systems, the $\overline{RQ}/\overline{GT1}$ line may be connected to the 82188 Integrated Bus Controller. In this case, a third processor with a HOLD, HLDA bus exchange system may acquire the bus from the 8087. For this configuration, $\overline{RQ}/\overline{GT1}$ will only be used if the 8087 is the bus master. Refer to 82188 data sheet for further information.
QS1, QS0	I	**QS1, QS0:** QS1 and QS0 provide the 8087 with status to allow tracking of the CPU instruction queue. **QS1** **QS0** 0 (LOW) 0 No Operation 0 1 First Byte of Op Code from Queue 1 (HIGH) 0 Empty the Queue 1 1 Subsequent Byte from Queue
INT	O	**Interrupt:** This line is used to indicate that an unmasked exception has occurred during numeric instruction execution when 8087 interrupts are enabled. This signal is typically routed to an 8259A for 8086 systems and to INT0 for iAPX 186/188 systems. INT is active HIGH.
BUSY	O	**Busy:** This signal indicates that the 8087 NEU is executing a numeric instruction. It is connected to the CPU's $\overline{TEST}$ pin to provide synchronization. In the case of an unmasked exception BUSY remains active until the exception is cleared. BUSY is active HIGH.
READY	I	**Ready:** READY is the acknowledgement from the addressed memory device that it will complete the data transfer. The RDY signal from memory is synchronized by the 8284A Clock Generator to form READY for 8086 systems. For iAPX 186/188 systems, RDY is synchronized by the 82188 Integrated Bus Controller to form READY. This signal is active HIGH.
RESET	I	**Reset:** RESET causes the processor to immediately terminate its present activity. The sighal must be active HIGH for at least four clock cycles. RESET is internally synchronized.
CLK	I	**Clock:** The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}		**Power:** V_{CC} is the +5V power supply pin.
GND		**Ground:** GND are the ground pins.

NOTE:
For the pin descriptions of the 8086, 8088, 80186 and 80188 CPU's, reference the respective data sheets (iAPX 86/10, iAPX 88/10, iAPX 186, iAPX 188).

APPLICATION AREAS

The 8087 provides functions meant specifically for high performance numeric processing requirements. Trigonometric, logarithmic, and exponential functions are built into the coprocessor hardware. These functions are essential in scientific, engineering, navigational, or military applications.

The 8087 also has capabilities meant for business or commercial computing. An 8087 can process Binary Coded Decimal (BCD) numbers up to 18 digits without roundoff errors. It can also perform arithmetic on integers as large as 64 bits $\pm 10^{18}$).

PROGRAMMING LANGUAGE SUPPORT

Programs for the 8087 can be written in Intel's high-level languages for iAPX 86/88 and iAPX 186/188 Systems; ASM-86 (the iAPX 86,88 assembly language), PL/M-86, FORTRAN-86, and PASCAL-86.

RELATED INFORMATION

For iAPX 86/10, iAPX 88/10, iAPX 186 or iAPX 188 details, refer to the respective data sheets. For iAPX 186 or iAPX 188 systems, also refer to the 82188 Integrated Bus Controller data sheet.

FUNCTIONAL DESCRIPTION

The 8087 Numeric Data Processor's architecture is designed for high performance numeric computing in conjunction with general purpose processing.

The 8087 is a numeric processor extension that provides arithmetic and logical instruction support for a variety of numeric data types. It also executes numerous built-in transcendental functions (e.g., tangent and log functions). The 8087 executes instructions as a coprocessor to a maximum mode CPU. It effectively extends the register and instruction set of the system and adds several new data types as well. Figure 3 presents the registers of the CPU+8087. Table 2 shows the range of data types supported by the 8087. The 8087 is treated as an extension to the CPU, providing register, data types, control, and instruction capabilities at the hardware level. At the programmers level the CPU and the 8087 are viewed as a single unified processor.

System Configuration

As a coprocessor to an 8086 or 8088, the 8087 is wired in parallel with the CPU as shown in Figure 4. Figure 5 shows the iAPX 186/188 system configuration. The CPU's status (S0-S2) and queue status lines (QS0-QS1) enable the 8087 to monitor and decode instructions in synchronization with the CPU and without any CPU overhead. For iAPX 186/188 systems, the queue status signals of the iAPX 186/188 are synchronized to 8087 requirements by the 82188 Integrated Bus Controller. Once started, the 8087 can process in parallel with, and independent of, the host CPU. For resynchronization, the 8087's BUSY signal informs the CPU that the 8087 is executing an instruction and the CPU WAIT instruction tests this signal to insure that the 8087 is ready to execute subsequent instructions. The 8087 can interrupt the CPU when it detects an error or exception. The

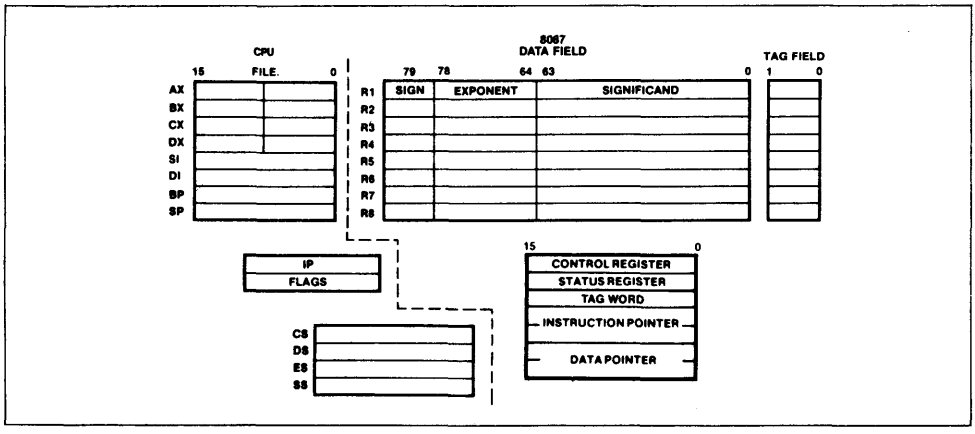


Figure 3. CPU+8087 Architecture

8087's interrupt request line is typically routed to the CPU through an 8259A Programmable Interrupt Controller for 8086, 8088 systems and INT0 for iAPX 186/188.

The 8087 uses one of the request/grant lines of the iAPX 86/88 architecture (typically $\overline{RQ}/\overline{GT0}$) to obtain control of the local bus for data transfers. The other request/grant line is available for general system use (for instance by an I/O processor in LOCAL mode). A bus master can also be connected to the 8087's $\overline{RQ}/\overline{GT1}$ line. In this configuration the 8087 will pass the request/grant handshake signals between the CPU and the attached master when the 8087 is not in control of the bus and will relinquish the bus to the master directly when the 8087 is in control. In this way two additional masters can be configured in an iAPX 86/88 system; one will share the 8086 bus with the 8087 on a first come first served basis, and the second will be guaranteed to be higher in priority than the 8087.

For iAPX 186/188 systems, $\overline{RQ}/\overline{GT0}$ and $\overline{RQ}/\overline{GT1}$ are connected to the corresponding inputs of the 82188 Integrated Bus Controller. Because the iAPX 186/188 has a HOLD, HLDA bus exchange protocol, an interface is needed which will translate $\overline{RQ}/\overline{GT}$ signals to corresponding HOLD, HDLA signals and visa versa. One of the functions of the 82188 IBC is to provide this translation. $\overline{RQ}/\overline{GT0}$ is translated to HOLD, HLDA signals which are then directly connected to the iAPX 186/188. The $\overline{RQ}/\overline{GT1}$ line is also translated into HOLD, HLDA signals (referred to as SYSHOLD, SYSHLDA signals) by the 82188 IBC. This allows a third processor (using a HOLD, HLDA bus exchange protocol) to gain control of the bus.

Unlike an iAPX 86/20 system, $\overline{RQ}/\overline{GT1}$ is only used when the 8087 has bus control. If the third processor requests the bus when the current bus master is the iAPX 186/188, the 82188 IBC will directly pass the request onto the iAPX 186/188 without going through the 8087. The third processor has the highest bus priority in the system. If the 8087 requests the bus while the third processor has bus control, the grant pulse will not be issued until the third processor releases the bus (using SYSHOLD). In this configuration, the third processor has the highest priority, the 8087 has the next highest, and the iAPX 186/188 has the lowest bus priority.

Table 2. 8087 Data Types

Data Formats	Range	Precision	Most Significant Byte
			7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0
Word Integer	10^4	16 Bits	I_{15} I_0 Two's Complement
Short Integer	10^9	32 Bits	I_{31} I_0 Two's Complement
Long Integer	10^{18}	64 Bits	I_{63} I_0 Two's Complement
Packed BCD	10^{18}	18 Digits	S — $D_{17}D_{16}$ D_1 D_0
Short Real	$10^{\pm 38}$	24 Bits	S E_7 E_0 F_1 F_{23} F_0 Implicit
Long Real	$10^{\pm 308}$	53 Bits	S E_{10} E_0 F_1 F_{52} F_0 Implicit
Temporary Real	$10^{\pm 4932}$	64 Bits	S E_{14} E_0 F_0 F_{63}

Integer: I

Packed BCD: $(-1)^S(D_{17}\ldots D_0)$

Real: $(-1)^S(2^{E\text{-BIAS}})(F_0 \cdot F_1 \ldots)$

Bias = 127 for Short Real
1023 for Long Real
16383 for Temp Real

Bus Operation

The 8087 bus structure, operation and timing are identical to all other processors in the iAPX 86/88 series (maximum mode configuration). The address is time multiplexed with the data on the first 16/8 lines of the address/data bus. A16 through A19 are time multiplexed with four status lines S3-S6. S3, S4 and S6 are always one (HIGH) for 8087-driven bus cycles while S5 is always zero (LOW). When the 8087 is monitoring CPU bus cycles (passive mode) S6 is also monitored by the 8087 to differentiate 8086/8088 activity from that of a local I/O processor or any other local bus master. (The 8086/8088 must be the only processor on the local bus to drive S6 LOW). S7 is multiplexed with and has the same value as $\overline{BHE}$ for all 8087 bus cycles.

The first three status lines, $\overline{S0}$-$\overline{S2}$, are used with an 8288 bus controller or 82188 Integrated Bus Controller to determine the type of bus cycle being run:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	X	X	Unused
1	0	0	Unused
1	0	1	Memory Data Read
1	1	0	Memory Data Write
1	1	1	Passive (no bus cycle)

Programming Interface

The 8087 includes the standard iAPX 86/10, 88/10 instruction set for general data manipulation and program control. It also includes 68 numeric instructions for extended precision integer, floating point, trigonometric, logarithmic, and exponential functions. Sample execution times for several 8087 functions are shown in Table 3. Overall performance is up to 100 times that of an iAPX 86/10 processor for numeric instructions.

Any instruction executed by the 8087 is the combined result of the CPU and 8087 activity. The CPU and the 8087 have specialized functions and registers providing fast concurrent operation. The CPU controls overall program execution while the 8087 uses the coprocessor interface to recognize and perform numeric operations.

Table 2 lists the eight data types the 8087 supports and presents the format for each type. Internally, the 8087 holds all numbers in the temporary real format. Load and store instructions automatically convert operands represented in memory as 16-, 32-, or 64-bit integers, 32- or 64-bit floating point numbers or 18-digit packed BCD numbers into temporary real format and vice versa. The 8087 also provides the capability to control round off, underflow, and overflow errors in each calculation.

Computations in the 8087 use the processor's register stack. These eight 80-bit registers provide the equivalent capacity of 20 32-bit registers. The 8087 register set can be accessed as a stack, with instructions operating on the top one or two stack elements, or as a fixed register set, with instructions operating on explicitly designated registers.

Table 5 lists the 8087's instructions by class. All appear as ESCAPE instructions to the host. Assembly language programs are written in ASM-86, the iAPX 86, 88 assembly language.

Table 3. Execution Times for Selected iAPX 86/20 Numeric Instructions and Corresponding iAPX 86/10 Emulation

Floating Point Instruction	Approximate Execution Time (μs)	
	iAPX 86/20 (5 MHz Clock)	iAPX 86/10 Emulation
Add/Subtract	17	1,600
Multiply (single precision)	19	1,600
Multiply (extended precision)	27	2,100
Divide	39	3,200
Compare	9	1,300
Load (double precision)	10	1,700
Store (double precision)	21	1,200
Square Root	36	19,600
Tangent	90	13,000
Exponentiation	100	17,100

NUMERIC PROCESSOR EXTENSION ARCHITECTURE

As Shown in Figure 1, the 8087 is internally divided into two processing elements, the control unit (CU) and the numeric execution unit (NEU). The NEU executes all numeric instructions, while the CU receives and decodes instructions, reads and writes memory operands and executes 8087 control instructions. The two elements are able to operate independently of one another, allowing the CU to maintain synchronization with the CPU while the NEU is busy processing a numeric instruction.

Control Unit

The CU keeps the 8087 operating in synchronization with its host CPU. 8087 instructions are intermixed with CPU instructions in a single instruction stream. The CPU fetches all instructions from memory; by monitoring the status ($\overline{S0}$-$\overline{S2}$, S6) emitted by the CPU, the control unit determines when an instruction is being fetched. The

Figure 4. iAPX 86/20, 88/20 System Configuration

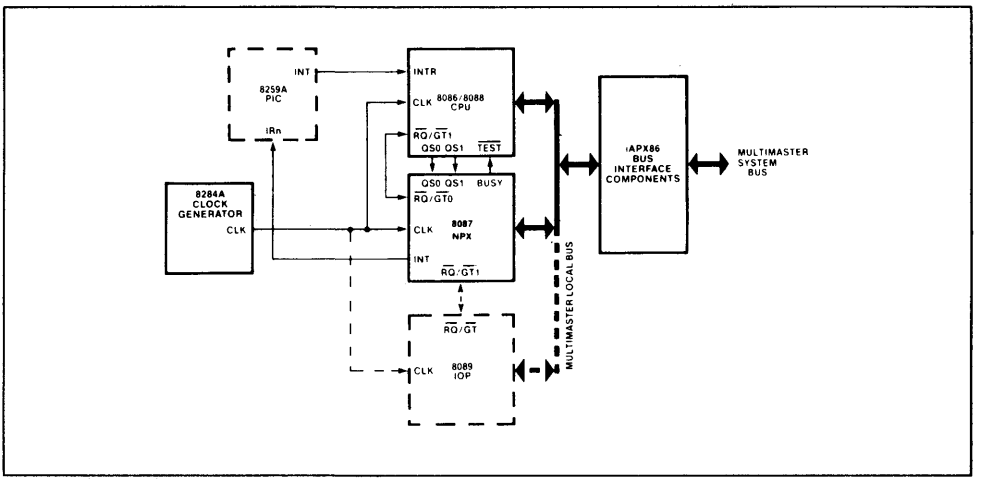
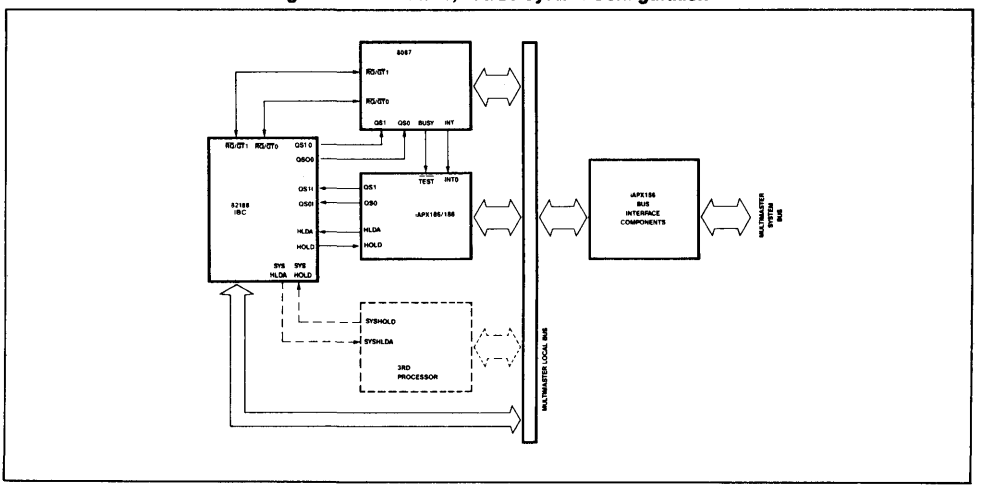


Figure 5. iAPX 186/20, 188/20 System Configuration



CU monitors the data bus in parallel with the CPU to obtain instructions that pertain to the 8087.

The CU maintains an instruction queue that is identical to the queue in the host CPU. The CU automatically determines if the CPU is an 8086/186 or an 8088/188 immediately after reset (by monitoring the $\overline{BHE}$/S7 line) and matches its queue length accordingly. By monitoring the CPU's queue status lines (QS0, QS1), the CU obtains and decodes instructions from the queue in synchronization with the CPU.

A numeric instruction appears as an ESCAPE instruction to the CPU. Both the CPU and 8087 decode and execute the ESCAPE instruction together. The 8087 only recognizes the numeric instructions shown in Table 5. The start of a numeric operation is acomplished when the CPU executes the ESCAPE instruction. The instruction may or may not identify a memory operand.

The CPU does, however, distinguish between ESC instructions that reference memory and those that do not. If the instruction refers to a memory operand, the CPU calculates the operand's address using any one of its available addressing modes, and then performs a "dummy read" of the word at that location. (Any location within the 1M byte address space is allowed.) This is a normal read cycle except that the CPU ignores the data it receives. If the ESC instruction does not contain a memory reference (e.g. an 8087 stack operation), the CPU simply proceeds to the next instruction.

An 8087 instruction can have one of three memory reference options; (1) not reference memory; (2) load an operand word from memory into the 8087; or (3) store an operand word from the 8087 into memory. If no memory reference is required, the 8087 simply executes its instruction. If a memory reference is required, the CU uses a "dummy read" cycle initiated by the CPU to capture and save the address that the CPU places on the bus. If the instruction is a load, the CU additionally captures the data word when it becomes available on the local data bus. If data required is longer than one word, the CU immediately obtains the bus from the CPU using the request/grant protocol and reads the rest of the information in consecutive bus cycles. In a store operation, the CU captures and saves the store address as in a load, and ignores the data word that follows in the "dummy read" cycle. When the 8087 is ready to perform the store, the CU obtains the bus from the CPU and writes the operand starting at the specified address.

Numeric Execution Unit

The NEU executes all instructions that involve the register stack; these include arithmetic, logical, transcendental, constant and data transfer instructions. The data path in the NEU is 84 bits wide (68 fraction bits, 15 exponent bits and a sign bit) which allows internal operand transfers to be performed at very high speeds.

When the NEU begins executing an instruction, it activates the 8087 BUSY signal. This signal can be used in conjunction with the CPU WAIT instruction to resynchronize both processors when the NEU has completed its current instruction.

Register Set

The CPU+8087 register set is shown in Figure 3. Each of the eight data registers in the 8087's register stack is 80 bits and is divided into "fields" corresponding to the 8087's temporary real data type.

At a given point in time the TOP field in the control word identifies the current top-of-stack register. A "push" operation decrements TOP by 1 and loads a value into the new top register. A "pop" operation stores the value from the current top register and then increments TOP by 1. Like CPU stacks in memory, the 8087 register stack grows "down" toward lower-addressed registers.

Instructions may address the data registers either implicitly or explicitly. Many instructions operate on the register at the top of the stack. These instructions implicitly address the register pointed to by the TOP. Other instructions allow the programmer to explicitly specify the register which is to be used. Explicit register addressing is "top-relative."

Status Word

The status word shown in Figure 6 reflects the overall state of the 8087; it may be stored in memory and then inspected by CPU code. The status word is a 16-bit register divided into fields as shown in Figure 6. The busy bit (bit 15) indicates whether the NEU is either executing an instruction or has an interrupt request pending (B = 1), or is idle (B = 0). Several instructions which store and manipulate the status word are executed exclusively by the CU, and these do not set the busy bit themselves.

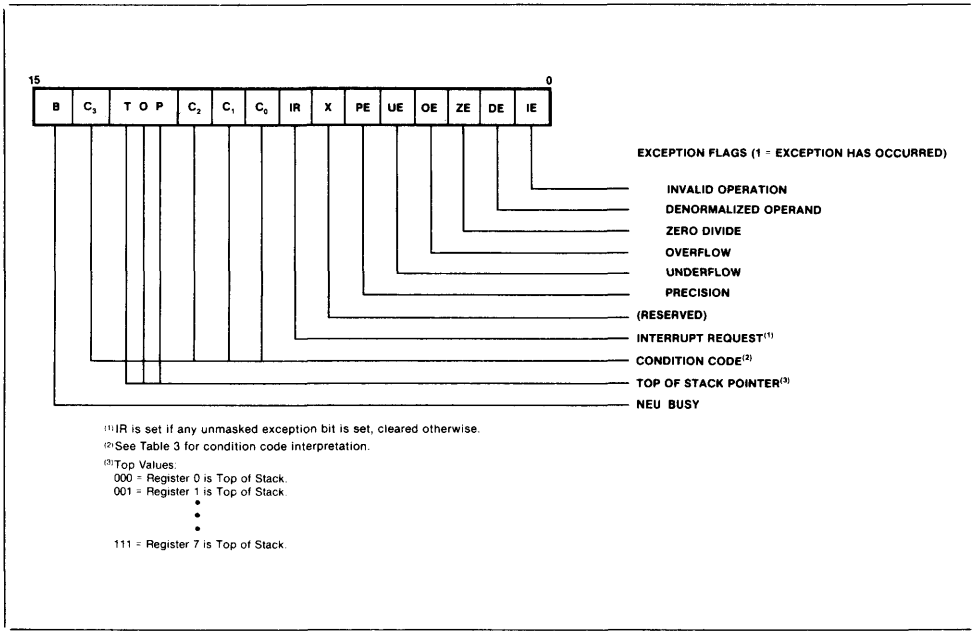


Figure 6. 8087 Status Word

The four numeric condition code bits (C_0-C_3) are similar to flags in a CPU: various instructions update these bits to reflect the outcome of 8087 operations. The effect of these instructions on the condition code bits is summarized in Table 4.

Bits 14–12 of the status word point to the 8087 register that is the current top-of-stack (TOP) as described above.

Bit 7 is the interrupt request bit. This bit is set if any unmasked exception bit is set and cleared otherwise.

Bits 5–0 are set to indicate that the NEU has detected an exception while executing an instruction.

Tag Word

The tag word marks the content of each register as shown in Figure 7. The principal function of the tag word is to optimize the 8087's performance. The tag word can be used, however, to interpret the contents of 8087 registers.

Instruction and Data Pointers

The instruction and data pointers (see Figure 8) are provided for user-written error handlers. Whenever the 8087 executes an NEU instruction, the CU saves the instruction address, the operand address (if present) and the instruction opcode. 8087 instructions can store this data into memory.

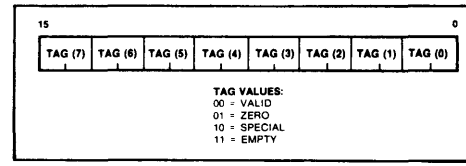


Figure 7. 8087 Tag Word

Table 4a. Condition Code Interpretation

Instruction Type	C_3	C_2	C_1	C_0	Interpretation
Compare, Test	0	0	X	0	ST > Source or 0 (FTST)
	0	0	X	1	ST < Source or 0 (FTST)
	1	0	X	0	ST = Source or 0 (FTST)
	1	1	X	1	ST is not comparable
Remainder	Q_1	0	Q_0	Q_2	Complete reduction with three low bits of quotient (See Table 4b)
	U	1	U	U	Incomplete Reduction
Examine	0	0	0	0	Valid, positive unnormalized
	0	0	0	1	Invalid, positive, exponent =0
	0	0	1	0	Valid, negative, unnormalized
	0	0	1	1	Invalid, negative, exponent =0
	0	1	0	0	Valid, positive, normalized
	0	1	0	1	Infinity, positive
	0	1	1	0	Valid, negative, normalized
	0	1	1	1	Infinity, negative
	1	0	0	0	Zero, positive
	1	0	0	1	Empty
	1	0	1	0	Zero, negative
	1	0	1	1	Empty
	1	1	0	0	Invalid, positive, exponent = 0
	1	1	0	1	Empty
	1	1	1	0	Invalid, negative, exponent = 0
	1	1	1	1	Empty

NOTES:
1. ST = Top of stack
2. X = value is not affected by instruction
3. U = value is undefined following instruction
4. Q_n = Quotient bit n

Table 4b. Condition Code Interpretation after FPREM Instruction As a Function of Dividend Value

Dividend Range	Q_2	Q_1	Q_0
Dividend < 2 * Modulus	C_3[1]	C_1[1]	Q_0
Dividend < 4 * Modulus	C_3[1]	Q_1	Q_0
Dividend ≥ 4 * Modulus	Q_2	Q_1	Q_0

NOTE:
1. Previous value of indicated bit, not affected by FPREM instruction execution.

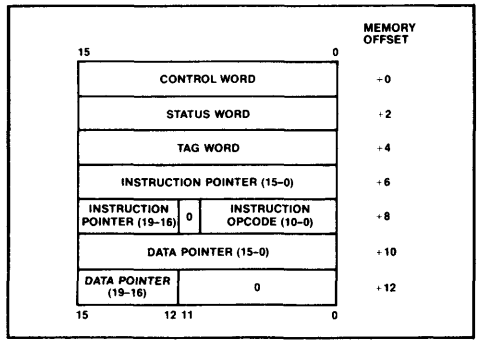


Figure 8. 8087 Instruction and Data Pointer Image in Memory

Control Word

The 8087 provides several processing options which are selected by loading a word from memory into the control word. Figure 9 shows the format and encoding of the fields in the control word.

The low order byte of this control word configures 8087 interrupts and exception masking. Bits 5–0 of the control word contain individual masks for each of the six exceptions that the 8087 recognizes and bit 7 contains a general mask bit for all 8087 interrupts. The high order byte of the control word configures the 8087 operating mode including precision, rounding, and infinity controls. The precision control bits (bits 9–8) can be used to set the 8087 internal operating precision at less than the default of temporary real precision. This can be useful in providing compatibility with earlier generation arithmetic processors of smaller precision than the 8087. The rounding control bits (bits 11–10) provide for directed rounding and true chop as well as the unbiased round to nearest mode specified in the proposed IEEE standard. Control over closure of the number space at infinity is also provided (either affine closure, $\pm\infty$, or projective closure, ∞, is treated as unsigned, may be specified).

Exception Handling

The 8087 detects six different exception conditions that can occur during instruction execution. Any or all exceptions will cause an interrupt if unmasked and interrupts are enabled.

If interrupts are disabled the 8087 will simply continue execution regardless of whether the host clears the exception. If a specific exception class is masked and that exception occurs, however, the 8087 will post the exception in the status register and perform an on-chip default exception handling procedure, thereby allowing processing to continue. The exceptions that the 8087 detects are the following:

1. INVALID OPERATION: Stack overflow, stack underflow, indeterminate form (0/0, $\infty - \infty$, etc.) or the use of a Non-Number (NAN) as an operand. An exponent value is reserved and any bit pattern with this value in the exponent field is termed a Non-Number and causes this exception. If this exception is masked, the 8087's default response is to generate a specific NAN called INDEFINITE, or to propagate already existing NANs as the calculation result.

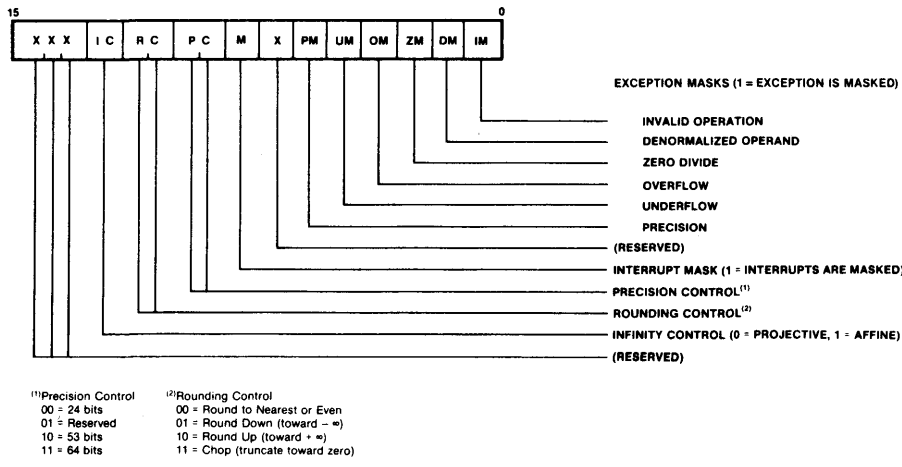


Figure 9. 8087 Control Word

2. OVERFLOW: The result is too large in magnitude to fit the specified format. The 8087 will generate an encoding for infinity if this exception is masked.

3. ZERO DIVISOR: The divisor is zero while the dividend is a non-infinite, non-zero number. Again, the 8087 will generate an encoding for infinity if this exception is masked.

4. UNDERFLOW: The result is non-zero but too small in magnitude to fit in the specified format. If this exception is masked the 8087 will denormalize (shift right) the fraction until the exponent is in range. This process is called gradual underflow.

5. DENORMALIZED OPERAND: At least one of the operands or the result is denormalized; it has the smallest exponent but a non-zero significand. Normal processing continues if this exception is masked off.

6. INEXACT RESULT: If the true result is not exactly representable in the specified format, the result is rounded according to the rounding mode, and this flag is set. If this exception is masked, processing will simply continue.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground .....−1.0V to +7V
Power Dissipation .....3.0 Watt

**NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		475	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	μA	$0V \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Capacitance of Inputs		10	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD0-15, A_{16}–A_{19}, BHE, S2-S0, RQ/GT) and CLK		15	pF	fc = 1 MHz
C_{OUT}	Capacitance of Outputs BUSY, INT		10	pF	fc = 1 MHz

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

TIMING REQUIREMENTS		8087		8087-2		8087-1 (Preliminary: See Note 7)			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
TCLCL	CLK Cycle Period	200	500	125	500	100	500	ns	
TCLCH	CLK Low Time	118		68		53		ns	
TCHCL	CLK High Time	69		44		39		ns	
TCH1CH2	CLK Rise Time		10		10		15	ns	From 1.0V to 3.5V
TCL2CL2	CLK Fall Time		10		10		15	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		20		15		ns	
TCLDX	Data in Hold Time	10		10		10		ns	
TRYHCH	READY Setup Time	118		68		53		ns	
TCHRYX	READY Hold Time	30		20		5		ns	
TRYLCL	READY Inactive to CLK**	- 8		- 8		-10		ns	
TGVCH	RQ/GT Setup Time	30		15		8		ns	
TCHGX	RQ/GT Hold Time	40		30		20		ns	
TQVCL	QS0-1 Setup Time	30		30		10		ns	
TCLQX	QS0-1 Hold Time	10		10		5		ns	
TSACH	Status Active Setup Time	30		30		30		ns	
TSNCL	Status Inactive Setup Time	30		30		30		ns	
TILIH	Input Rise Time (Except CLK)		20		20		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		15	ns	From 2.0V to 0.8V

**See Note 6

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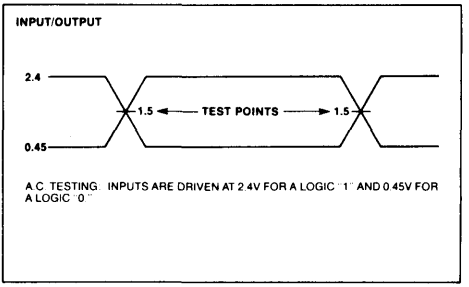
A.C. CHARACTERISTICS (Continued)

TIMING RESPONSES		8087		8087-2		8087-1 (Preliminary: See Note 7)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLML	Command Active Delay (See Notes 1,2)	10/0	35/70	10/0	35/70	10/0	35/70	ns	C_L = 20 - 100pF for all 8087 Outputs (in addition to 8087 self-load)
TCLMH	Command Inactive Delay (See Notes 1,2)	10/0	35/55	10/0	35/55	10/0	35/70	ns	
TRYHSH	Ready Active to Status Passive (See Note 5)		110		65		45	ns	
TCHSV	Status Active Delay	10	110	10	60	10	45	ns	
TCLSH	Status Inactive Delay	10	130	10	70	10	55	ns	
TCLAV	Address Valid Delay	10	110	10	60	10	55	ns	
TCLAX	Address Hold Time	10		10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50	TCLAX	45	ns	
TSVLH	Status Valid to ALE High (See Notes 1,2)		15/30		15/30		15/30	ns	
TCLLH	CLK Low to ALE Valid (See Notes 1,2)		15/30		15/30		15/30	ns	
TCHLL	ALE Inactive Delay (See Notes 1,2)		15/30		15/30		15/30	ns	
TCLDV	Data Valid Delay	10	110	10	60	10	50	ns	
TCHDX	Data Hold Time	10		10		10	45	ns	
TCVNV	Control Active Delay (See Notes 1,3)	5	45	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Notes 1,3)	10	45	10	45	10	45	ns	
TCHBV	BUSY and INT Valid Delay	10	150	10	85	10	65	ns	
TCHDTL	Direction Control Active Delay (See Notes 1,3)		50		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Notes 1,3)		30		30		30	ns	
TSVDTV	STATUS to DT/$\overline{R}$ Delay (See Notes 1,4)	0	30	0	30	0	30	ns	
TCLDTV	DT/$\overline{R}$ Active Delay (See Notes 1,4)	0	55	0	55	0	55	ns	
TCHDNV	$\overline{DEN}$ Active Delay (See Notes 1,4)	0	55	0	55	0	55	ns	
TCHDNX	$\overline{DEN}$ Inactive Delay (See Notes 1,4)	5	55	5	55	5	55	ns	
TCLGL	RQ/GT Active Delay	0	85	0	50	0	41	ns	C_L=40pF (in addition to 8087 self-load)
TCLGH	RQ/GT Inactive Delay	0	85	0	50	0	45	ns	
TOLOH	Output Rise Time		20		20		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		12		12		12	ns	From 2.0V to 0.8V

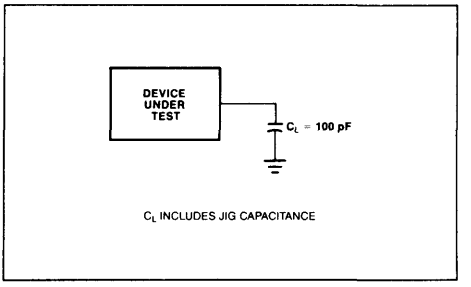
NOTES:
1. Signal at 8284A, 8288, or 82188 shown for reference only.
2. 8288 timing/82188 timing
3. 8288 timing
4. 82188 timing
5. Applies only to T_3 and wait states
6. Applies only to T_2 state (8ns into T_3)
7. IMPORTANT SYSTEM CONSIDERATION: Some 8087-1 timing parameters are constrained relative to the corresponding 8086-1 specifications. Therefore, 8086-1 systems incorporating the 8087-1 should be designed with the 8087-1 specifications.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0"

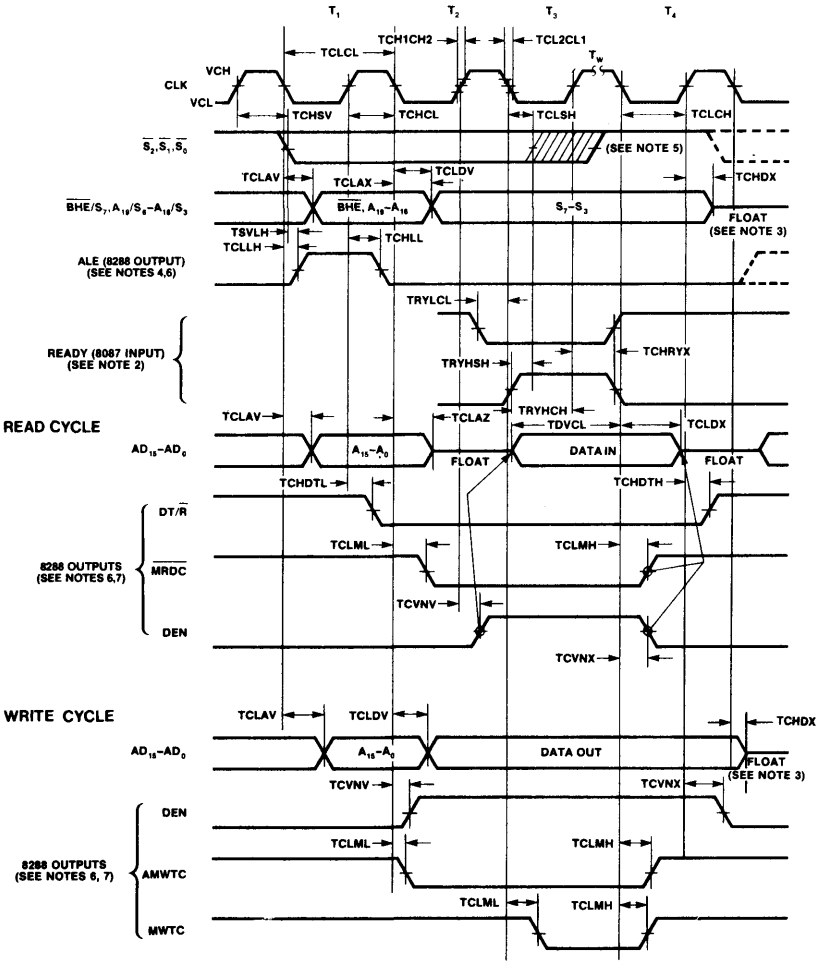
A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

WAVEFORMS

MASTER MODE (with 8288 references)

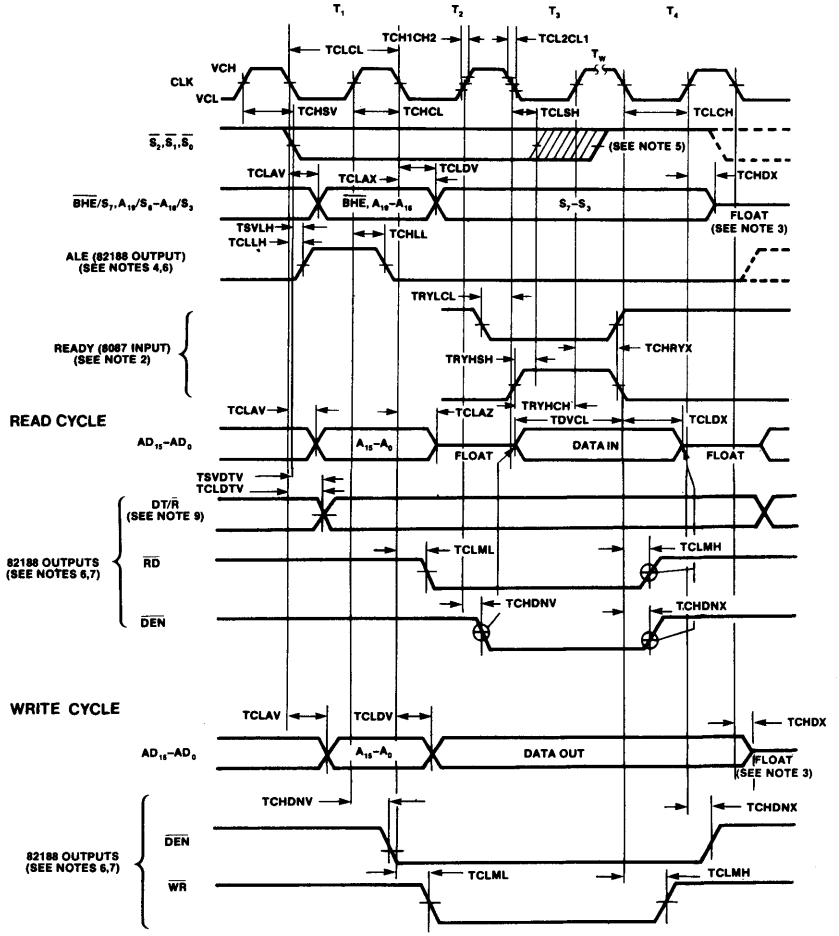


NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OL} AND V_{OH} UNLESS OTHERWISE SPECIFIED.
2. READY IS SAMPLED NEAR THE END OF T_2, T_3 AND T_W TO DETERMINE IF T_W MACHINE STATES ARE TO BE INSERTED.
3. THE LOCAL BUS FLOATS ONLY IF THE 8087 IS RETURNING CONTROL TO THE 8086/8088.
4. ALE RISES AT LATER OF (TSVLH, TCLLH).
5. STATUS INACTIVE IN STATE JUST PRIOR TO T_4.
6. SIGNALS AT 8284A OR 8288 ARE SHOWN FOR REFERENCE ONLY.
7. THE ISSUANCE OF 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$ AND DEN) LAGS THE ACTIVE HIGH 8288 CEN.
8. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

WAVEFORMS (Continued)

MASTER MODE (with 82188 references)



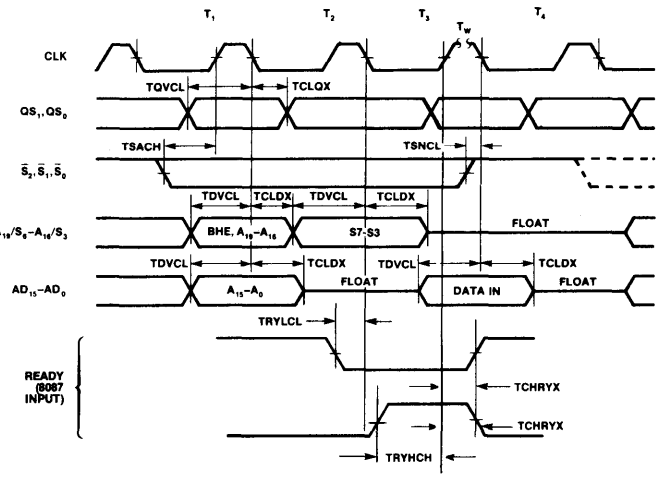
NOTES:

1. ALL SIGNALS SWITCH BETWEEN V_{OL} AND V_{OH} UNLESS OTHERWISE SPECIFIED.
2. READY IS SAMPLED NEAR THE END OF T_2, T_3 AND T_W TO DETERMINE IF T_W MACHINE STATES ARE TO BE INSERTED.
3. THE LOCAL BUS FLOATS ONLY IF THE 8087 IS RETURNING CONTROL TO THE 80186/80188
4. ALE RISES AT LATER OF (TSVLH, TCLLH).
5. STATUS INACTIVE IN STATE JUST PRIOR TO T_4.
6. SIGNALS AT 8284A OR 82188 ARE SHOWN FOR REFERENCE ONLY.
7. THE ISSUANCE OF 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, AND DEN) LAGS THE ACTIVE HIGH 8288 CEN.
8. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
9. DT/$\overline{R}$ BECOMES VALID AT THE LATER OF (TSVDTV, TCLDTV).

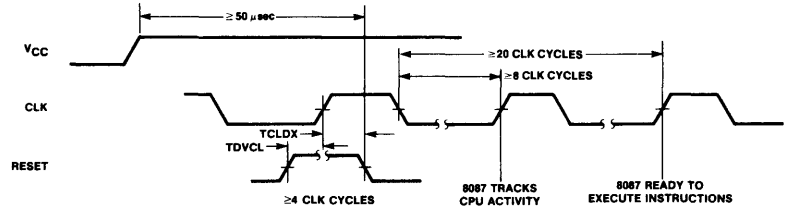
205835-003

WAVEFORMS (Continued)

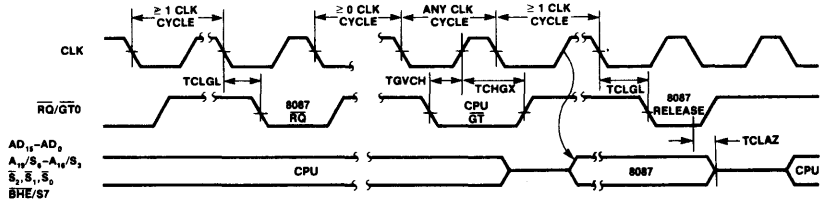
PASSIVE MODE



RESET TIMING



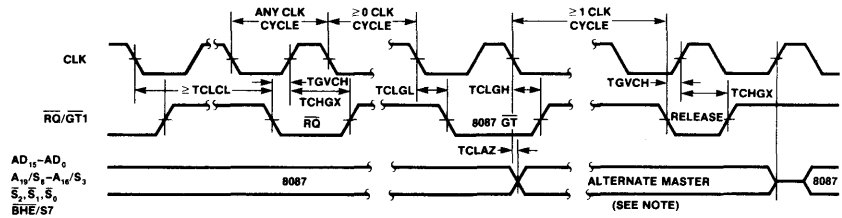
REQUEST/GRANT$_0$ TIMING



NOTE: THE CPU PROVIDES ACTIVE PULLUP OF $\overline{RQ}/\overline{GT0}$, SEE TCLGH SPEC.

WAVEFORMS (Continued)

REQUEST/GRANT$_1$ TIMING



NOTE: ALTERNATE MASTER MAY NOT DRIVE THE BUSES OUTSIDE OF THE REGION SHOWN WITHOUT RISKING BUS CONTENTION.

BUSY AND INTERRUPT TIMING

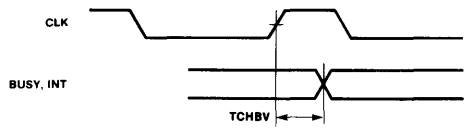


Table 5. 8087 Extensions to the 86/186 Instructions Sets

Data Transfer		Optional 8,16 Bit Displacement	Clock Count Range 32 Bit Real	32 Bit Integer	64 Bit Real	16 Bit Integer
FLD = LOAD	MF		00	01	10	11
Integer/Real Memory to ST(0)	ESCAPE MF 1 | MOD 0 0 0 R/M	DISP	38-56 + EA	52-60 + EA	40-60 + EA	46-54 + EA
Long Integer Memory to ST(0)	ESCAPE 1 1 1 | MOD 1 0 1 R/M	DISP	60-68 + EA			
Temporary Real Memory to ST(0)	ESCAPE 0 1 1 | MOD 1 0 1 R/M	DISP	53-65 + EA			
BCD Memory to ST(0)	ESCAPE 1 1 1 | MOD 1 0 0 R/M	DISP	290-310 + EA			
ST(i) to ST(0)	ESCAPE 0 0 1 | 1 1 0 0 0 ST(i)		17-22			
FST = STORE						
ST(0) to Integer/Real Memory	ESCAPE MF 1 | MOD 0 1 0 R/M	DISP	84-90 + EA	82-92 + EA	96-104 + EA	80-90 + EA
ST(0) to ST(i)	ESCAPE 1 0 1 | 1 1 0 1 0 ST(i)		15-22			
FSTP = STORE AND POP						
ST(0) to Integer/Real Memory	ESCAPE MF 1 | MOD 0 1 1 R/M	DISP	86-92 + EA	84-94 + EA	98-106 + EA	82-92 + EA
ST(0) to Long Integer Memory	ESCAPE 1 1 1 | MOD 1 1 1 R/M	DISP	94-105 + EA			
ST(0) to Temporary Real Memory	ESCAPE 0 1 1 | MOD 1 1 1 R/M	DISP	52-58 + EA			
ST(0) to BCD Memory	ESCAPE 1 1 1 | MOD 1 1 0 R/M	DISP	520-540 + EA			
ST(0) to ST(i)	ESCAPE 1 0 1 | 1 1 0 1 1 ST(i)		17-24			
FXCH = Exchange ST(i) and ST(0)	ESCAPE 0 0 1 | 1 1 0 0 1 ST(i)		10-15			
Comparison						
FCOM = Compare						
Integer/Real Memory to ST(0)	ESCAPE MF 0 | MOD 0 1 0 R/M	DISP	60-70 + EA	78-91 + EA	65-75 + EA	72-86 + EA
ST(i) to ST (0)	ESCAPE 0 0 0 | 1 1 0 1 0 ST(i)		40-50			
FCOMP = Compare and Pop						
Integer/Real Memory to ST(0)	ESCAPE MF 0 | MOD 0 1 1 R/M	DISP	63-73 + EA	80-93 + EA	67-77 + EA	74-88 + EA
ST(i) to ST(0)	ESCAPE 0 0 0 | 1 1 0 1 1 ST(i)		45-52			
FCOMPP = Compare ST(1) to ST(0) and Pop Twice	ESCAPE 1 1 0 | 1 1 0 1 1 0 0 1		45-55			
FTST = Test ST(0)	ESCAPE 0 0 1 | 1 1 1 0 0 1 0 0		38-48			
FXAM = Examine ST(0)	ESCAPE 0 0 1 | 1 1 1 0 0 1 0 1		12-23			

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Table 5. 8087 Extensions to the 86/186 Instruction Sets (cont.)

Constants		Optional 8,16 Bit Displacement	Clock Count Range 32 Bit Real	32 Bit Integer	64 Bit Real	16 Bit Integer
	MF =		00	01	10	11
FLDZ = LOAD + 0.0 into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 1 1 0		11–17			
FLD1 = LOAD + 1.0 into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 0 0 0		15–21			
FLDPI = LOAD π into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 0 1 1		16–22			
FLDL2T = LOAD $\log_2 10$ into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 0 0 1		16–22			
FLDL2E = LOAD $\log_2 e$ into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 0 1 0		15–21			
FLDLG2 = LOAD $\log_{10} 2$ into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 1 0 0		18–24			
FLDLN2 = LOAD $\log_e 2$ into ST(0)	ESCAPE 0 0 1 | 1 1 1 0 1 1 0 1		17–23			
Arithmetic						
FADD = Addition						
Integer/Real Memory with ST(0)	ESCAPE MF 0 | MOD 0 0 0 R/M	DISP	90–120 + EA	108–143 + EA	95–125 + EA	102–137 + EA
ST(i) and ST(0)	ESCAPE d P 0 | 1 1 0 0 0 ST(i)		70–100 (Note 1)			
FSUB = Subtraction						
Integer/Real Memory with ST(0)	ESCAPE MF 0 | MOD 1 0 R R/M	DISP	90–120 + EA	108–143 + EA	95–125 + EA	102–137 + EA
ST(i) and ST(0)	ESCAPE d P 0 | 1 1 1 0 R R/M		70–100 (Note 1)			
FMUL = Multiplication						
Integer/Real Memory with ST(0)	ESCAPE MF 0 | MOD 0 0 1 R/M	DISP	110–125 + EA	130–144 + EA	112–168 + EA	124–138 + EA
ST(i) and ST(0)	ESCAPE d P 0 | 1 1 0 0 1 R/M		90–145 (Note 1)			
FDIV = Division						
Integer/Real Memory with ST(0)	ESCAPE MF 0 | MOD 1 1 R R/M	DISP	215–225 + EA	230–243 + EA	220–230 + EA	224–238 + EA
ST(i) and ST(0)	ESCAPE d P 0 | 1 1 1 1 R R/M		193–203 (Note 1)			
FSQRT = Square Root of ST(0)	ESCAPE 0 0 1 | 1 1 1 1 1 0 1 0		180–186			
FSCALE = Scale ST(0) by ST(1)	ESCAPE 0 0 1 | 1 1 1 1 1 1 0 1		32–38			
FPREM = Partial Remainder of ST(0) ÷ ST(1)	ESCAPE 0 0 1 | 1 1 1 1 1 0 0 0		15–190			
FRNDINT = Round ST(0) to Integer	ESCAPE 0 0 1 | 1 1 1 1 1 1 0 0		16–50			

NOTE:
1. If P=1 then add 5 clocks.

Table 5. 8087 Extensions to the 86/186 Instructions Sets (cont.)

		Optional 8,16 Bit Displacement	Clock Count Range
FXTRACT = Extract Components of St(0)	ESCAPE 0 0 1 | 1 1 1 1 0 1 0 0		27–55
FABS = Absolute Value of ST(0)	ESCAPE 0 0 1 | 1 1 1 0 0 0 0 1		10–17
FCHS = Change Sign of ST(0)	ESCAPE 0 0 1 | 1 1 1 0 0 0 0 0		10–17
Transcendental			
FPTAN = Partial Tangent of ST(0)	ESCAPE 0 0 1 | 1 1 1 1 0 0 1 0		30–540
FPATAN = Partial Arctangent of ST(0) ÷ ST(1)	ESCAPE 0 0 1 | 1 1 1 1 0 0 1 1		250–800
F2XM1 = $2^{ST(0)} - 1$	ESCAPE 0 0 1 | 1 1 1 1 0 0 0 0		310–630
FYL2X = ST(1) • Log_2 |ST(0)|	ESCAPE 0 0 1 | 1 1 1 1 0 0 0 1		900–1100
FYL2XP1 = ST(1) • Log_2 [ST(0) + 1]	ESCAPE 0 0 1 | 1 1 1 1 1 0 0 1		700–1000
Processor Control			
FINIT = Initialized 8087	ESCAPE 0 1 1 | 1 1 1 0 0 0 1 1		2–8
FENI = Enable Interrupts	ESCAPE 0 1 1 | 1 1 1 0 0 0 0 0		2–8
FDISI = Disable Interrupts	ESCAPE 0 1 1 | 1 1 1 0 0 0 0 1		2–8
FLDCW = Load Control Word	ESCAPE 0 0 1 | MOD 1 0 1 R/M	DISP	7–14 + EA
FSTCW = Store Control Word	ESCAPE 0 0 1 | MOD 1 1 1 R/M	DISP	12–18 + EA
FSTSW = Store Status Word	ESCAPE 1 0 1 | MOD 1 1 1 R/M	DISP	12–18 + EA
FCLEX = Clear Exceptions	ESCAPE 0 1 1 | 1 1 1 0 0 0 1 0		2–8
FSTENV = Store Environment	ESCAPE 0 0 1 | MOD 1 1 0 R/M	DISP	40–50 + EA
FLDENV = Load Environment	ESCAPE 0 0 1 | MOD 1 0 0 R/M	DISP	35–45 + EA
FSAVE = Save State	ESCAPE 1 0 1 | MOD 1 1 0 R/M	DISP	197 – 207 + EA
FRSTOR = Restore State	ESCAPE 1 0 1 | MOD 1 0 0 R/M	DISP	197 – 207 + EA
FINCSTP = Increment Stack Pointer	ESCAPE 0 0 1 | 1 1 1 1 1 0 1 1 1		6–12
FDECSTP = Decrement Stack Pointer	ESCAPE 0 0 1 | 1 1 1 1 1 0 1 1 0		6–12

Table 5. 8087 Extensions to the 86/186 Instructions Sets (cont.)

		Clock Count Range
FFREE = Free ST(i)	ESCAPE 1 0 1 | 1 1 0 0 0 ST(i)	9-16
FNOP = No Operation	ESCAPE 0 0 1 | 1 1 0 1 0 0 0 0	10-16
FWAIT = CPU Wait for 8087	1 0 0 1 1 0 1 1	3 + 5n*

*n = number of times CPU examines TEST line before 8087 lowers BUSY.

NOTES:

1. if mod=00 then DISP=0*, disp-low and disp-high are absent
   if mod=01 then DISP=disp-low sign-extended to 16-bits, disp-high is absent
   if mod=10 then DISP=disp-high; disp-low
   if mod=11 then r/m is treated as an ST(i) field
2. if r/m=000 then EA=(BX) + (SI) +DISP
   if r/m=001 then EA=(BX) + (DI) +DISP
   if r/m=010 then EA=(BP) + (SI) +DISP
   if r/m=011 then EA=(BP) + (DI) +DISP
   if r/m=100 then EA=(SI) + DISP
   if r/m=101 then EA=(DI) + DISP
   if r/m=110 then EA=(BP) + DISP
   if r/m=111 then EA=(BX) + DISP

   *except if mod=000 and r/m=110 then EA =disp-high; disp-low.
3. MF= Memory Format
   00—32-bit Real
   01—32-bit Integer
   10—64-bit Real
   11—16-bit Integer
4. ST(0)= Current stack top
   ST(i) i^{th} register below stack top
5. d= Destination
   0—Destination is ST(0)
   1—Destination is ST(i)
6. P= Pop
   0—No pop
   1—Pop ST(0)
7. R= Reverse: When d=1 reverse the sense of R
   0—Destination (op) Source
   1—Source (op) Destination
8. For **FSQRT:** $-0 \leq ST(0) \leq +\infty$
   For **FSCALE:** $-2^{15} \leq ST(1) < +2^{15}$ and ST(1) integer
   For **F2XM1:** $0 \leq ST(0) \leq 2^{-1}$
   For **FYL2X:** $0 < ST(0) < \infty$
   $-\infty < ST(1) < +\infty$
   For **FYL2XP1:** $0 \leq |ST(0)| < (2 - \sqrt{2})/2$
   $-\infty < ST(1) < \infty$
   For **FPTAN:** $0 \leq ST(0) \leq \pi/4$
   For **FPATAN:** $0 \leq ST(0) < ST(1) < +\infty$

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