

# ROM BIOS Listing

```

;BOOT ROM - AT&T PERSONAL COMPUTER 6300
;Rev. 1.0 - MAY 1984

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;-----
;Filename: flags.src
;
; This file contains the temporary conditional assembly flag
; definitions and includes of the other assembly modules.
;-----
;-----
; Macro Definitions
;-----
; MASM does not let you code a 'jump intersegment direct' instruction, so
; this macro simulates that instruction.

jmpf macro arg1,arg2 ; ; USAGE: jmpf seg,off
      db 0Eah
      dw arg2
      dw arg1
      endm
;-----
; Code Declaration
;-----

0000 code segment public 'ROM' ; link code segments first
      assume cs:code, ds:nothing, es:nothing, ss:nothing

0000 ORG 0C000h

0000 flags_data1 proc
0000 00 chk_lo db 0 ; space for checksum of F000:C000 to F000:DFFF
0001 00 rom_id db 0 ; ROM identifier.
0002 E2CE h rom_st dw mastab ; offset of mastab in ROM.

0004 flags_data1 endp

0004 far_calls proc far ; far call table: the user does a far call to
; F000:C01X, a near call is done to the proper
; routine, and a far return back to the user.

0004 E8 E602 R call DString ; F000:C004 (3 bytes per near call)
0007 CB ret ; F000:C008 (1 byte per far return)
0008 E8 E619 R call DCrLf
000C E8 E626 R call DColon ; F000:C00C
000F CB ret
0010 E8 E632 R call DHexLong ; F000:C010
0013 CB ret
0014 E8 E63C R call DHexWord ; F000:C014
0017 CB ret
0018 E8 E643 R call DHexByte ; F000:C018
001B CB ret
001C E8 E650 R call DHexNib ; F000:C01C
001F CB ret
0020 E8 E665 R call DNum ; F000:C020
0023 CB ret
0024 E8 E66D R call DNumW ; F000:C024
0027 CB ret
0028 E8 E5E5 R call rom_checksum ; F000:C028
002B CB ret
002C E8 E1F6 R call rtc_chk ; F000:C02C
002F CB ret
0030 E8 E266 R call memstat ; F000:C030
0033 CB ret
0034 E8 CF9F R call h_init ; F000:C034
0037 CB ret
0038 E8 D640 R call h_fmt ; F000:C038
003B CB ret

003C DB8C R dw offset banner_m ; pointer to banner
003E 0000 dw 0 ; For aligning the copyright message.
0040 43 4F 50 59 52 49 db 'COPYRIGHT (C) '
47 48 54 20 28 43
29 20 20 20
0050 4F 4C 49 56 45 54 db 'OLIVETTI 1984 '
54 49 20 31 39 38
34 20 20 20

0060 far_calls endp

0060 code ends
;-----
; Includes of Assembly Modules
;-----
;include flags.asm (this module)
;include sysdata.asm
C ;-----
C ;Filename: sysdata.src
C ;
C ; This is the port equate and system data definition module.

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C ; (See flags.src for conditional assembly flags...)
C ;
C ;-----
C ; Global Constants
C ;-----
= 0000 C abs0_seg equ 00000h
= 0030 C stack_seg equ 00030h
= 0040 C data_seg equ 00040h
= 8000 C para_mono equ 08000h
= B800 C para_graph equ 08800h
= F000 C code_seg equ 0F000h
C
= 0007 C BEL equ 007h
= 0008 C BS equ 008h
= 000D C CR equ 00Dh
= 000A C LF equ 00Ah
= 0000 C NUL equ 0
C ;-----
C ; AT&T PERSONAL COMPUTER Addresses
C ;-----
C ;-----
C ; 18237A p_dma Controller Port Addresses
C ;-----
= 0000 C dma_addr_0 equ 00h ; 16-bit address register - channel 0 - refresh
= 0001 C dma_count_0 equ 01h ; 16-bit count register
= 0002 C dma_addr_1 equ 02h ; 16-bit address register - channel 1 - not used
= 0003 C dma_count_1 equ 03h ; 16-bit count register
= 0004 C dma_addr_2 equ 04h ; 16-bit address register - channel 2 - FDU
= 0005 C dma_count_2 equ 05h ; 16-bit count register
= 0006 C dma_addr_3 equ 06h ; 16-bit address register - channel 3 - display
= 0007 C dma_count_3 equ 07h ; 16-bit count register
C
= 0008 C dma_status equ 08h ; 8-bit read status register
= 0008 C dma_command equ 08h ; 8-bit write command register
= 0009 C dma_request equ 09h ; 4-bit write request register
= 000A C dma_mask_bit equ 0Ah ; 4-bit (write) set/clear one mask register bit
= 000B C dma_mode equ 0Bh ; 6-bit write mode register
= 000C C dma_ff_clr equ 0Ch ; (write) clear byte pointer flip/flop
= 000D C dma_temp equ 0Dh ; 8-bit read temporary register
= 000D C dma_master_clr equ 0Dh ; (write) master clear command
= 000E C dma_mask_clr equ 0Eh ; 4-bit (write) clear all mask register bits
= 000F C dma_mask_write equ 0Fh ; 4-bit write all mask register bits at once
C
= 0080 C dma_seg0_0 equ 080h ; RAM refresh - 4x4-bit high nibble segment port
= 0082 C dma_seg0_1 equ 082h ; not used
= 0081 C dma_seg0_2 equ 081h ; FDU
= 0083 C dma_seg0_3 equ 083h ; display TEMP
C ;-----
C ; 18237A p_dma controller constants
C ;-----
C ; dma_command port: ; bit #0: memory-to-memory/I/O enable
C ; ; bit #2: controller disable
C ; ; bit #3: compressed/normal timing
C ; ; bit #4: rotating/fixed priority
C ; ; bit #5: extended/late write selection
C ; ; bit #6: DREQ active low/high
C ; ; bit #7: DACK active high/low
= 0004 C dma_cmd_disable equ 004h ; controller disable (bit #2) command
= 0000 C dma_cmd_enable equ 000h ; memory-to-I/O, controller enable, normal
; fixed priority, late write, DREQ/DACK
C
= 0058 C dma_mode_0 equ 058h ; channel 0, read, autoinitialize, inc-
C ; ;rement, single mode for RAM refresh.
= 0041 C dma_mode_1 equ 041h ; channel 1, verify, autoinit disabled,
C ; ;increment, single mode for not used.
= 0056 C dma_mode_2 equ 056h ; channel 2, write, autoinitialize, inc-
C ; ;rement, single mode for FDU.
= 0043 C dma_mode_3 equ 043h ; channel 3, verify, autoinit disabled,
C ; ;increment, single mode for display.
C
; dma_mask_bit port: ; bits #0-1: channel select
; ; bit # 2: set/-clr mask bit (off/on)
= 0000 C dma_unmask_0 equ 000h ; turn on channel 0 for RAM refresh.
C ;-----
C ; 18259A Programmable Interrupt Controller Port Addresses
C ;-----
= CC2C C pic_0 equ 020h ; 8259A 'control' port (A0 = 0)
= 0021 C pic_1 equ 021h ; 8259A 'data' port (A0 = 1)
C ;-----
C ; 18259A Programmable Interrupt Controller Commands
C ;-----
= 0013 C pic_icw1 equ 013h ; ICW1 for both master & slave pic's
C ; bit #0 = 1: ICW4 to follow (w vector base)
C ; bit #1 = 1: single mode (no slaves or icw3)

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C ; bit #2 = 0: call address interval of 8 bytes
C ; (don't care if 8086 mode -- always vectors &
C ; byte interval)
C ; bit #3 = 0: edge triggered
= 0008 C pic_iow2 equ 008h ; interrupt vector base address (INTs 08h - 0Fh)
= 0008 C pic_iow3 equ 008h ; if cascade mode, and INT3 is a
C ; slave, 8259A is reprogrammed including iow3
C pic_iow4 equ 00Dh ; bit #0 = 1: 8086 mode
C ; bit #1 = 0: normal end_of_int
C ; bit #2 = 1: specify master for buffered mode
C ; ( specifies slave for buffered mode )
C ; bit #3 = 1: buffered mode
C ; bit #4 = 0: not special fully nested
= 00FF C pic_off_msk equ 0FFh ; pic interrupt mask bits (all interrupts off)
C
= 0020 C pic_neoi equ 020h ; non-specific end-of-interrupt
C
= 0060 C pic_seoi_0 equ 060h ; specific end-of-interrupt for IRO: 18253 p_timer
= 0061 C pic_seoi_1 equ 061h ; specific end-of-interrupt for IRO: 18041A kb
= 0066 C pic_seoi_6 equ 066h ; specific end-of-interrupt for IR6: fdu
C
C ;-----
C ; 18253 p_timer Port Addresses
C ;-----
= 0040 C p_8253_0 equ 040h ; 8253 p_timer 0 - rtc interrupt - IRO = INT 08h
= 0041 C p_8253_1 equ 041h ; 8253 p_timer 1 - memory refresh p_dma
= 0042 C p_8253_2 equ 042h ; 8253 p_timer 2 - tone generator for speaker
= 0043 C p_8253_ctrl equ 043h ; 8253 p_timer control port
C
C ;-----
C ; 18253 p_timer Control Bytes
C ;-----
C ; bit #0 -> Binary Code Decimal (BCD) Enable
C ; bits #1-3 -> Mode (0-5) 000 Mode 0: Interrupt on Terminal Count
C ; 001 Mode 1: Programmable One-Shot
C ; x10 Mode 2: Rate Generator
C ; x11 Mode 3: Square Wave Rate Generator
C ; 100 Mode 4: Software Triggered Strobe
C ; 101 Mode 5: Hardware Triggered Strobe
C ; bits #4-5 -> Read/Load Instruction (0-3)
C ; bits #6-7 -> Select Counter (0-2)
C
C ;-----
= 0036 C t0cmd equ 036h ; 00 11 011 0 -> p_8253_0, lsb lat, mode 3, no BCD
= 0074 C t1cmd equ 074h ; 01 11 010 0 -> p_8253_1, lsb lat, mode 2, no BCD
= 0086 C t2cmd equ 086h ; 10 11 011 0 -> p_8253_2, lsb lat, mode 3, no BCD
C
C ;-----
C ; 18253 p_timer Counts
C ;-----
C ; 8253 input is 1.2288 MHz (3.6864/3) or a period of 813.8 nsec = 0.814 usec
C ; Note: PC input is 1.19318 MHz or a period of 838.1 nsec = 0.838 usec
C
= 0000 C t0count equ 0 ; = 65,536 -> (1,228,800 Hz)/(65,536) = 18.75 inta/sec
C ; -> (1,193,180 Hz)/(65,536) = 18.21 inta/sec
C
C ; t1count equ 9 ; OLD refresh cycle = 9*(813.8 nsec) = 7.32 usec
= 0013 C t1count equ 19 ; REAL refresh cycle = 19*(813.8 nsec) = 15.5 usec
C ; < 15.625 usec minimum required. ( is 18 - safety???)
= 0266 C t2count equ 614 ; (1.2288 MHz)/(2*614) = 1.00 kHz tone
C
C ;-----
C ; 28530 Serial Communication Controller
C ;-----
C ; (scc_data_x port addresses are indexed from the scc_ctl_x
C ; port addresses. See com.src.)
C
= 0050 C scc_ctl_a equ 050h ; write to SCC pointer register (0-Fh).
= 0052 C scc_ctl_b equ 052h ; then read or write from selected register.
C
C ;-----
C ; 8041 Keyboard Controller
C ;-----
= 0050 C p_kscan equ 060h ; bit #7: reset interrupt pending
= 0061 C p_kctrl equ 061h ; bit #6: kb clock reset
C ; bit #5: I/O channel (NMI) enable
C ; bit #4: RAM parity (NMI) enable
C ; bits #3 & #2: not used
C ; bit #1: speaker data
= 0064 C kb_status equ 064h ; bit #0: speaker gate to p_8253_2
C ; bit #1: input buffer (ok to write byte)
C ; bit #0: output buffer (byte to be read)
C
C ;-----
C ; General Control Ports
C ;-----
= 0062 C ControlB equ 062h ; 8087, etc.
= 0065 C ComaControl equ 065h
= 0066 C sys_conf_a equ 066h ; bit #7: 2764/-2732 ROM's
C ; bit #6: not used
C ; bit #5: SCC 8530 chip installed
C ; bit #4: 8087 installed

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C ; bit #3: 256k x 1 RAM used
= 0067 C sys_conf_b equ 067h ; bits #2 - #0: RAM configuration
C ; bits #7 - #6: (number of FDUs)-1
C ; bits #5 - #4: reserved for monitor type
C ; bits #3 - #2: reserved for HDU type
C ; bit #1: "Fast" FDU start up
C ; bits #0: 96 tpi FDU
C
C -----
C ;
C ; 58174A Clock Calendar
C ;
C ; (See calendar.arc)
C ;
C -----
C ;
C ; FDU & HDU Disk Driver Error Codes
C ;
C -----
= 0080 C time_out equ 80h
= 0040 C seek_error equ 40h
= 0020 C fdc_error equ 20h
= 0010 C crc_error equ 10h
= 0009 C dma_seg_error equ 09h
= 0008 C dma_error equ 08h
= 0004 C sect_not_found equ 04h
= 0003 C write_protect equ 03h
= 0002 C addr_mark_error equ 02h
= 0001 C cmd_error equ 01h
C
C ;
C ; Game Card
C ;
C -----
= 0201 C game_card equ 201h
C
C ;
C ; Parallel Printer Interface
C ;
C ; (prt_stat_x & prt_cmd_x port addresses are indexed from the
C ; prt_data_x port addresses. See prt.arc.)
C ;
C -----
= 038C C prt_data_a equ 038Ch
C ; prt_stat_a equ 038Dh
C ; prt_cmd_a equ 038Eh
= 0378 C prt_data_b equ 0378h ; on mother board
C ; prt_stat_b equ 0379h
C ; prt_cmd_b equ 037Ah
= 0278 C prt_data_c equ 0278h
C ; prt_stat_c equ 0279h
C ; prt_cmd_c equ 027Ah
C
C ;
C ; Color and Monochrome Video Controller
C ;
C ; (xxxx_data, xxxx_mode, xxxx_status, xxxx_LPelear, and
C ; xxxx_LFPreset port addresses are indexed from the xxxx_Pointer
C ; port addresses for color & display. See vid.arc and graph.arc.)
C ;
C -----
C ; Color Controller.
= 03D4 C color_pointer equ 03D4h ; 6845 pointer to internal regs
C ; Monochrome Controller.
= 03B4 C v_pointer equ 03B4h ; 6845 pointer to internal regs
C
C ;
C ; INS8250 Asynchronous Communication Chip
C ;
C ; (com_int_x, com_ctl1_x, com_ctl2_x, com_stat_x, and
C ; com_mstat_x port addresses are indexed from the com_data_x
C ; port addresses. See com.arc.)
C ;
C -----
= 03F8 C com_data_a equ 03F8h ; channel A 8250 data register/low byte baud
C ; com_int_a equ 03F9h ; channel A 8250 high byte baud count register
= 03FA C com_id_a equ 03FAh ; channel A 8250 check for presence register
C ; com_ctl1_a equ 03FBh ; channel A 8250 line control register
C ; com_ctl2_a equ 03FCh ; channel A 8250 modem control register
C ; com_stat_a equ 03FDh ; channel A 8250 line status register
C ; com_mstat_a equ 03FEh ; channel A 8250 modem status register
= 02F8 C com_data_b equ 02F8h ; channel B 8250 data register/low byte baud
C ; com_int_b equ 02F9h ; channel B 8250 high byte baud count register
= 02FA C com_id_b equ 02FAh ; channel B 8250 check for presence register
C ; com_ctl1_b equ 02FBh ; channel B 8250 line control register
C ; com_ctl2_b equ 02FCh ; channel B 8250 modem control register
C ; com_stat_b equ 02FDh ; channel B 8250 line status register
C ; com_mstat_b equ 02FEh ; channel B 8250 modem status register
C
C ;
C ; Keyboard Constants
C ;
C -----
C ; --- shift flag equates within kb_flg
C

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C
= 0080 C insert_mode equ 80h ; insert state in action
= 0040 C caps_lock_mode equ 40h ; caps lock state toggled
= 0020 C num_lock_mode equ 20h ; num lock state toggled
= 0010 C scrll_lock_mode equ 10h ; scroll lock state toggled
= 0008 C pause_mode equ 08h ; pause toggled
= 0001 C dix_kb equ 01h ; deluxe keyboard
C
C ;---- shift flag equates within kb_flag_1
C
= 0080 C insert_shift equ 80h ; insert key depressed
= 0040 C caps_lock_shift equ 40h ; caps lock key depressed
= 0020 C num_lock_shift equ 20h ; num lock key depressed
= 0010 C scrll_lock_shift equ 10h ; scroll lock key depressed
= 0008 C alt_shift equ 08h ; alternate shift key depressed
= 0004 C cntrl_shift equ 04h ; control shift key depressed
= 0002 C left_shift equ 02h ; left shift key depressed
= 0001 C right_shift equ 01h ; right shift key depressed
C
C ;---- Scan codes for special function keys
C
= 0010 C cntrl_key equ 29 ; control key scan code
= 002A C left_shift_key equ 42 ; left shift scan code
= 0036 C right_shift_key equ 54 ; right shift scan code
= 0038 C alt_key equ 56 ; alt shift key scan code
= 003A C caps_lock_key equ 58 ; shift lock scan code
= 0045 C num_lock_key equ 69 ; number lock scan code
= 0046 C scrll_lock_key equ 70 ; scroll lock key scan code
= 0052 C insert_key equ 82 ; insert key scan code
= 0053 C delete_key equ 83 ; delete key scan code
C
C ;-----
C ; Data Declarations
C ;-----
C
C ; Interrupt Locations (dummy data segment to define constant offsets)
C ;-----
C
0000 C abs0 segment public 'RAM' ; at abs0_seg
C assume cs:nothing, ds:nothing, es:nothing, ss:nothing
C
C ;-----
C ; CPU Interrupt Routines
C ;-----
C
0000 C int0010cn dd ? ; divide by zero
0004 C int010cn dd ? ; single step trap
0008 C int020cn dd ? ; nmi parity trap
000C C int030cn dd ? ; break interrupt
0010 C int040cn dd ? ; divide overflow
0014 C int050cn dd ? ; print screen
C
0C18 C int060cn dd ?
001C C int070cn dd ?
C
C ;-----
C ; i8259A Hardware Interrupt Routines
C ;-----
C
0020 C int080cn dd ? ; 18253 rtc interrupt
0024 C int090cn dd ? ; 18041 kb interrupt
C
0028 C int0A0cn dd ?
002C C int0B0cn dd ?
0030 C int0C0cn dd ?
C
0034 C int0D0cn dd ? ; hard disk interrupt
0038 C int0E0cn dd ? ; floppy disk interrupt
C
003C C int0F0cn dd ?
C
C ;-----
C ; Software Interrupt Routines
C ;-----
C
0040 C int100cn dd ? ; display request
0044 C int110cn dd ? ; equipment request
0048 C int120cn dd ? ; memory size request
004C C int130cn dd ? ; disk I/O request
0050 C int140cn dd ? ; serial communication request
0054 C int150cn dd ? ; cassette request
0058 C int160cn dd ? ; kb request
005C C int170cn dd ? ; printer request
0060 C int180cn dd ? ; cassette BASIC pointer
0064 C int190cn dd ? ; boot-strap request
0068 C int1A0cn dd ? ; time of day request
006C C int1B0cn dd ? ; kb break pointer
0070 C int1C0cn dd ? ; p.timer break pointer
0074 C int1D0cn dd ? ; display parameter pointer
0078 C int1E0cn dd ? ; disk parameter pointer
007C C int1F0cn dd ? ; graphics character extensions pointer
C
0080 C abs0 ends
C
C ;-----
C ; RAM stack
C ;-----
C

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0000      C stack_ram      segment public 'RAM'      ; at stack_seg
          C
          C stack_ram      ends
          C
          C ;-----
          C ; System Data Area
          C ;-----
0000      C data          segment public 'RAM'      ; at data_seg
          C          assume cs:nothing, ds:nothing, es:nothing, ss:nothing
          C
          C ;-----
          C ; Data Area
          C ;-----
          C ; ROM Bios Data Area
0000      04 [      C rs232_addr      dw      4 dup (?) ; 0040:0000 addresses of rs232 adapters
          ]      C
          C
0008      04 [      C printer_addr     dw      4 dup (?) ; 0040:0008 addresses of printers
          ]      C
          C
0010      2????    C switch_bits     dw      ? ; 0040:0010 state of DIP switches
0012      ??      C mfg_tat        db      ? ; 0040:0012 initialization flag
0013      7????    C memory_size    dw      ? ; 0040:0013 memory size in kbytes
0015      02 [      C mfg_err_flag   db      2 dup (?) ; 0040:0015 error codes for manufacturing
          ]      C
          C
          C ; Keyboard Data Area
          C
0017      ??      C kb_flag        db      ? ; 0040:0017 keyboard shift flag status byte
0018      ??      C kb_flag_1     db      ? ; 0040:0018 second byte of keyboard status
0019      ??      C alt_input     db      ? ; 0040:0019 alternate keypad entry
001A      7????    C buffer_head   dw      ? ; 0040:001A keyboard output pointer offset
001C      7????    C buffer_tail   dw      ? ; 0040:001C keyboard input pointer offset
          C
001E      10 [     C kb_buffer     dw      16 dup (?) ; 0040:001E room for 15 entries: head =
          ]      C
          C
          C ; tail implies buffer is empty
          C
          C ; Floppy Diskette Data Area
          C
003E      ??      C seek_status   db      ? ; 0040:003E floppy disk restore status bits
003F      ??      C motor_status  db      ? ; 0040:003F floppy disk motor status bits
0040      ??      C motor_count   db      ? ; 0040:0040 floppy disk turn off counter
0041      ??      C diskette_status db      ? ; 0040:0041 floppy disk driver status byte
          C
0042      C cmd_block    label byte ; 0040:0042 HDU command block buffer
0042      C hd_error    label byte ; 0040:0042 HDU sense byte buffer
0042      07 [     C nec_status    db      7 dup (?) ; 0040:0042 status bytes from NEC controller
          ]      C
          C
          C ; Video Display Data Area
          C
0049      ??      C v_mode        db      ? ; 0040:0049 CRT mode
004A      7????    C v_width       dw      ? ; 0040:004A CRT number of columns (often db)
004C      7????    C v_height      dw      ? ; 0040:004C CRT length of video ram in bytes
004E      7????    C v_top         dw      ? ; 0040:004E CRT video ram buffer address
0050      08 [     C v_curpos     dw      8 dup (?) ; 0040:0050 cursor for each of up to 8 pages
          ]      C
          C
          C
0060      7????    C v_cursize     dw      ? ; 0040:0060 v_curs_type sets cursor value
0062      ??      C v_page        db      ? ; 0040:0062
0063      7????    C v_base6045   dw      ? ; 0040:0063
0065      ??      C v_3x8        db      ? ; 0040:0065
0066      ??      C v_colorpal    db      ? ; 0040:0066
          C
          C ; Optional Post Data Area
          C
0067      7????    C io_rom_init   dw      ? ; 0040:0067 option ROM init routine offset
0069      7????    C io_rom_seg    dw      ? ; 0040:0069 option ROM init routine segment
006B      ??      C intr_flag     db      ? ; 0040:006B occurrence of interrupt flag
          C
          C ; 18253 p_timer Data Area
          C
006C      7????    C t_low_order   dw      ? ; 0040:006C low word of 18253_p_timer count
006E      7????    C t_hi_order    dw      ? ; 0040:006E high word of 18253_p_timer count
0070      ??      C t_overflow    db      ? ; 0040:0070 time rolled over flag
          C
          C ; System Data Area
          C
0071      ??      C bioa_break    db      ? ; 0040:0071 bit #7 set if break key hit
0072      7????    C reset_flag    dw      ? ; 0040:0072 = 1234h if keyboard reset hit
          C
          C ; Fixed Disk Data Area
          C
0074      ??      C disk_status   db      ? ; 0040:0074 fixed disk driver status byte
0075      ??      C hf_num        db      ? ; 0040:0075 fixed disk drive count

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0076 ??      C control_byte db ? ; 0040:0076 fixed disk control byte options
0077 ??      C port_off db ? ; 0040:0077 fixed disk port offset
C
C ; Printer & RS-232 Time-Out Data Areas
C
0078 04 [ 00 00 00 00 ] C printer_t_out db 4 dup (?); 0040:0078 printer time-out variables
C
C
007C 04 [ 00 00 00 00 ] C serial_t_out db 4 dup (?); 0040:007C RS-232 time-out variables
C
C
C ; Additional Keyboard Data Area
C
0080 ?????   C buffer_start dw ? ; 0040:0080 offset of kb_buffer = 001E
0082 ?????   C buffer_end dw ? ; 0040:0082 offset of kb_buffer_end = 003E
C
C ;-----
C ; Data Area
C ;-----
C
C ; Master Table Pointer.
C
0084 ???????? C master_tbl_ptr dd ? ; 0040:0084 pointer to master table
C
0088         C data ends
C
C ;-----
C ; Video RAM
C ;-----
C
0000         C v_ram segment public 'RAM' ; at para_mono
0000         C v_ram ends
0060         C code segment public 'ROM'
assume cs:code, ds:nothing, es:nothing, ss:nothing
C
0060         C font_lo_8x16 label byte ; 2048 bytes
include fontlo16.asm
C
0060         C fontlo16 proc near ; System Font Table for M24
C
0060 00 00 00 00 00 00 00 00 DB 00h,00h,00h,00h,00h,00h,00h,00h
C
0068 00 00 00 00 00 00 00 00 DB 00h,00h,00h,00h,00h,00h,00h,00h ; 0
C
0070 00 00 00 7E 81 A5 81 00 DB 00h,00h,07eh,081h,0a5h,081h,081h,0bdh
C
0078 81 BD 00 00 00 00 00 00 DB 099h,081h,07eh,00h,00h,00h,00h,00h ; 1
C
0080 00 00 00 7E FF DB FF FF DB 00h,00h,07eh,0ffh,0dbh,0ffh,0ffh,0c3h
C
0088 FF C3 00 00 00 00 00 00 DB 0e7h,0e7h,0ffh,07eh,00h,00h,00h,00h ; 2
C
0090 00 00 00 00 36 7F 7F DB 00h,00h,00h,036h,07fh,07fh,07fh,07fh
C
0098 7F 7F 00 00 00 00 00 00 DB 03eh,01eh,08h,00h,00h,00h,00h,00h ; 3
C
00A0 3E 1C 08 00 00 1C 3E DB 00h,00h,00h,08h,01eh,03eh,07fh,03eh
C
00A8 7F 3E 00 00 00 00 00 00 DB 01eh,08h,00h,00h,00h,00h,00h,00h ; 4
C
00B0 1C 08 00 00 00 00 00 DB 00h,00h,018h,03ch,03eh,0e7h,0e7h,0e7h
C
00B8 E7 E7 18 18 3C 00 00 00 DB 018h,018h,03ch,00h,00h,00h,00h,00h ; 5
C
00C0 00 00 00 18 3C 7E FF DB 00h,00h,018h,03ch,07eh,0ffh,0ffh,07eh
C
00C8 FF 7E 18 3C 00 00 00 00 DB 018h,018h,03ch,00h,00h,00h,00h,00h ; 6
C
00D0 00 00 00 00 00 18 3C DB 00h,00h,00h,00h,00h,018h,03ch,03ch
C
00D8 3C 3C 18 00 00 00 00 00 DB 018h,00h,00h,00h,00h,00h,00h,00h ; 7
C
00E0 00 00 00 FF FF FF FF FF DB 0ffh,0ffh,0ffh,0ffh,0ffh,0ffh,0e3h,0e3h,0e3h
C
00E8 C3 C3 00 00 00 00 00 00 DB 0c3h,0e7h,0ffh,0ffh,0ffh,0ffh,0ffh,0ffh ; 8
C
00F0 FF FF 00 00 00 3C 24 DB 00h,00h,00h,00h,03ch,024h,042h,042h
C
00F8 24 3C 00 00 00 00 00 DB 024h,03ch,00h,00h,00h,00h,00h,00h ; 9
C
C100 FF FF FF FF FF C3 99 DB 0ffh,0ffh,0ffh,0ffh,0e3h,099h,0bdh,0bdh
C
C108 BD 99 C3 FF FF FF FF DB 0bdh,099h,0e3h,0ffh,0ffh,0ffh,0ffh,0ffh ; a
C
C110 00 00 1F 07 0D 19 78 DB 00h,00h,01fh,07h,0dh,019h,078h,0cch
C
C118 CC CC 78 00 00 00 00 DB 0cch,0cch,078h,00h,00h,00h,00h,00h ; b
C
C120 00 00 00 3C 66 66 66 DB 00h,00h,03ch,066h,066h,066h,03ch,018h
C
C128 7E 18 18 00 00 00 00 DB 07eh,018h,018h,00h,00h,00h,00h,00h ; c
C
C130 00 00 18 14 12 12 14 DB 00h,00h,018h,014h,012h,012h,012h,014h
C
C138 10 70 F0 F0 60 60 00 DB 010h,070h,0f0h,0f0h,060h,00h,00h,00h ; d
C
00 00

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# ROM BIOS Listing

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C140 00 00 1F 11 1F 11  C DB 00h,00h,01f0h,011h,01f0h,011h,011h,011h
      11 11  C
C148 13 37 77 72 20 00  C DB 013h,037h,077h,072h,020h,00h,00h,00h ; e
      00 00  C
C150 00 00 18 18 DB 3C  C DB 00h,00h,018h,018h,0db0h,03ch,0e7h,03ah
      87 3C  C
C158 DB 18 18 00 00 00  C DB 0db0h,018h,018h,00h,00h,00h,00h,00h ; f
      00 00  C
C160 00 00 40 60 70 7C  C DB 00h,00h,040h,060h,070h,07eh,07fh,07eh
      7F 7C  C
C168 70 60 40 00 00 00  C DB 07eh,060h,040h,00h,00h,00h,00h,00h ; 10
      00 00  C
C170 00 00 01 03 07 1F  C DB 00h,00h,01h,03h,07h,01f0h,07fh,01f0h
      7F 1F  C
C178 07 03 01 00 00 00  C DB 07h,03h,01h,00h,00h,00h,00h,00h ; 11
      00 00  C
C180 00 00 18 3C 7E 18  C DB 00h,00h,018h,03ch,07eh,018h,018h,018h
      18 18  C
C188 7E 3C 18 00 00 00  C DB 07eh,03ch,018h,00h,00h,00h,00h,00h ; 12
      00 00  C
C190 00 00 33 33 33 33  C DB 00h,00h,033h,033h,033h,033h,033h,033h
      33 33  C
C198 00 00 33 00 00 00  C DB 00h,00h,033h,00h,00h,00h,00h,00h ; 13
      00 00  C
C1A0 00 00 7F DB DB DB  C DB 00h,00h,07fh,0db0h,0db0h,0db0h,07bh,01bh
      7B 1B  C
C1A8 1B 1B 18 00 00 00  C DB 01bh,01bh,01bh,00h,00h,00h,00h,00h ; 14
      00 00  C
C1B0 00 3E 63 30 1C 36  C DB 00h,03eh,063h,030h,01ch,036h,063h,063h
      63 63  C
C1B8 36 1C 06 63 3E 00  C DB 036h,01ch,06h,063h,03eh,00h,00h,00h ; 15
      00 00  C
C1C0 00 00 00 00 00 00  C DB 00h,00h,00h,00h,00h,00h,00h,00h
      00 00  C
C1C8 7E 7E 7E 00 00 00  C DB 07eh,07eh,07eh,00h,00h,00h,00h,00h ; 16
      00 00  C
C1D0 00 00 18 3C 7E 18  C DB 00h,00h,018h,03ch,07eh,018h,018h,018h
      18 18  C
C1D8 7E 3C 18 FF 00 00  C DB 07eh,03ch,018h,07fh,00h,00h,00h,00h ; 17
      00 00  C
C1E0 00 00 18 3C 7E 18  C DB 00h,00h,018h,03ch,07eh,018h,018h,018h
      18 18  C
C1E8 18 18 18 00 00 00  C DB 018h,018h,018h,00h,00h,00h,00h,00h ; 18
      00 00  C
C1F0 00 00 18 18 18 18  C DB 00h,00h,018h,018h,018h,018h,018h,018h
      18 18  C
C1F8 7E 3C 18 00 00 00  C DB 07eh,03ch,018h,00h,00h,00h,00h,00h ; 19
      00 00  C
C200 00 00 00 00 0C 06  C DB 00h,00h,00h,00h,00h,06h,07fh,06h
      7F 06  C
C208 0C 00 00 00 00 00  C DB 0eh,00h,00h,00h,00h,00h,00h,00h ; 1a
      00 00  C
C210 00 00 00 00 18 30  C DB 00h,00h,00h,00h,018h,030h,07fh,030h
      7F 30  C
C218 18 00 00 00 00 00  C DB 018h,00h,00h,00h,00h,00h,00h,00h ; 1b
      00 00  C
C220 00 00 00 00 60 60  C DB 00h,00h,00h,00h,060h,060h,060h,060h
      60 60  C
C228 7F 7F 00 00 00 00  C DB 07fh,07fh,00h,00h,00h,00h,00h,00h ; 1c
      00 00  C
C230 00 00 00 00 24 42  C DB 00h,00h,00h,00h,024h,042h,07fh,042h
      FF 42  C
C238 24 00 00 00 00 00  C DB 024h,00h,00h,00h,00h,00h,00h,00h ; 1d
      00 00  C
C240 00 00 00 00 00 00  C DB 00h,00h,00h,00h,00h,00h,00h,018h
      00 18  C
C248 3C 7E FF 00 00 00  C DB 03ch,07eh,07fh,00h,00h,00h,00h,00h ; 1e
      00 00  C
C250 00 00 00 00 00 FF  C DB 00h,00h,00h,00h,00h,07fh,07eh,03eh
      7E 3C  C
C258 18 00 00 00 00 00  C DB 018h,00h,00h,00h,00h,00h,00h,00h ; 1f
      00 00  C
C260 00 00 00 00 00 00  C DB 00h,00h,00h,00h,00h,00h,00h,00h
      00 00  C
C268 00 00 00 00 00 00  C DB 00h,00h,00h,00h,00h,00h,00h,00h ; ' 20
      00 00  C
C270 00 00 18 3C 3C 3C  C DB 00h,00h,018h,03ch,03ch,018h,018h,018h
      18 18  C
C278 00 18 18 00 00 00  C DB 00h,018h,018h,00h,00h,00h,00h,00h ; '1' 21
      00 00  C
C280 00 00 66 66 24 00  C DB 00h,00h,066h,066h,024h,00h,00h,00h
      00 00  C
C288 00 00 00 00 00 00  C DB 00h,00h,00h,00h,00h,00h,00h,00h ; '1' 22
      00 00  C
C290 00 00 36 36 7F 36  C DB 00h,00h,036h,036h,07fh,036h,036h,036h
      36 36  C
C298 7F 36 36 00 00 00  C DB 07fh,036h,036h,00h,00h,00h,00h,00h ; '# 23
      00 00  C
C2A0 08 08 3E 63 60 60  C DB 08h,08h,03eh,063h,060h,060h,03ah,03h
      3E 03  C
C2A8 03 63 3E 08 00 00  C DB 03h,063h,03eh,08h,08h,00h,00h,00h ; '8' 24
      00 00  C
C2B0 00 00 61 63 06 06  C DB 00h,00h,00h,061h,063h,06h,0eh,018h
      0C 18  C
C2B8 30 63 43 00 00 00  C DB 030h,063h,043h,00h,00h,00h,00h,00h ; '5' 25
      00 00  C
C2C0 00 00 1C 36 36 1C  C DB 00h,00h,01ch,036h,036h,01ch,03bh,06eh
      3B 6E  C
C2C8 66 66 3B 00 00 00  C DB 066h,066h,03bh,00h,00h,00h,00h,00h ; '&' 26
      00 00  C

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ROM BIOS  
Listing

C2D0	00 00 30 30 30 60	C	DB	00h,00h,030h,030h,030h,060h,00h,00h
00 00	00	C		
C2D8	00 00 00 00 00 00	C	DB	00h,00h,00h,00h,00h,00h,00h,00h ;'1' 27
00 00	00	C		
C2E0	00 00 0C 18 30 30	C	DB	00h,00h,0ch,018h,030h,030h,030h,030h
30 30	00	C		
C2E8	30 18 0C 00 00 00	C	DB	030h,018h,0ch,00b,00b,00b,00h,00h ;'(' 28
00 00	00	C		
C2F0	00 00 30 18 0C 0C	C	DB	00h,00h,030h,018h,0ch,0ch,0ch,0ch
0C 0C	00	C		
C2F8	0C 18 30 00 00 00	C	DB	0ch,018h,030h,00h,00h,00h,00h,00h ;')' 29
00 00	00	C		
C300	00 00 00 00 66 3C	C	DB	00h,00h,00h,00h,066h,030h,07fh,030h
FF 3C	00	C		
C308	66 00 00 00 00 00	C	DB	066h,00h,00h,00h,00h,00h,00h,00h ;'!' 2a
00 00	00	C		
C310	00 00 00 00 18 18	C	DB	00h,00h,00h,00h,018h,018h,07eh,018h
7E 18	00	C		
C318	18 00 00 00 00 00	C	DB	018h,00h,00h,00h,00h,00h,00h,00h ;'+ ' 2b
00 00	00	C		
C320	00 00 00 00 00 00	C	DB	00h,00h,00h,00h,00h,00h,00h,00h
00 00	00	C		
C328	18 18 18 30 00 00	C	DB	018h,018h,018h,030h,00h,00h,00h,00h ;',' 2c
00 00	00	C		
C330	00 00 00 00 00 00	C	DB	00h,00h,00b,00b,00b,00b,07eh,00h
7E 00	00	C		
C338	00 00 00 00 00 00	C	DB	00h,00h,00h,00h,00h,00h,00h,00h ;'- ' 2d
00 00	00	C		
C340	00 00 00 00 00 00	C	DB	00h,00h,00b,00b,00b,00b,00h,00h
00 00	00	C		
C348	00 18 18 00 00 00	C	DB	00h,018h,018h,00b,00b,00h,00h,00h ;',' 2e
00 00	00	C		
C350	00 00 01 03 06 0C	C	DB	00h,00h,01b,03b,06b,0ch,018h,030h
18 30	00	C		
C358	60 40 00 00 00 00	C	DB	060h,040h,00h,00h,00h,00h,00h,00h ;'/' 2f
00 00	00	C		
C360	00 00 3E 63 67 6F	C	DB	00h,00h,03eh,063h,067h,06fh,07bh,073h
7B 73	00	C		
C368	63 63 3E 00 00 00	C	DB	063h,063h,03eh,00b,00b,00h,00h,00h ;'0' 30
00 00	00	C		
C370	00 00 0C 1C 3C 0C	C	DB	00h,00h,0ch,01ch,03ch,0ch,0ch,0ch
0C 0C	00	C		
C378	0C 0C 3F 00 00 00	C	DB	0ch,0ch,03fh,00h,00h,00b,00b,00h ;'1' 31
00 00	00	C		
C380	00 00 3E 63 03 06	C	DB	00h,00h,03eh,063h,03b,06h,0ch,018h
0C 18	00	C		
C388	30 63 7F 00 00 00	C	DB	030h,063h,07fh,00b,00b,00h,00h,00h ;'2' 32
00 00	00	C		
C390	00 00 3E 63 03 03	C	DB	00h,00h,03eh,063h,03b,03b,03eh,03h
3E 03	00	C		
C398	03 63 3E 00 00 00	C	DB	03h,063h,03eh,00b,00b,00h,00h,00h ;'3' 33
00 00	00	C		
C3A0	00 00 06 0E 1E 36	C	DB	00h,00h,06h,0eh,01eh,036h,066h,07fh
66 7F	00	C		
C3A8	06 0F 00 00 00 00	C	DB	06h,06h,07fh,00b,00b,00h,00h,00h ;'4' 34
00 00	00	C		
C3B0	00 00 7F 60 60 60	C	DB	00h,00h,07fh,060h,060h,060h,07eh,03h
7E 03	00	C		
C3B8	03 63 3E 00 00 00	C	DB	03h,063h,03eh,00b,00b,00h,00h,00h ;'5' 35
00 00	00	C		
C3C0	00 00 1C 30 60 60	C	DB	00h,00h,01ch,030h,060h,060h,07eh,063h
7E 63	00	C		
C3C8	63 63 3E 00 00 00	C	DB	063h,063h,03eh,00b,00b,00h,00h,00h ;'6' 36
00 00	00	C		
C3D0	00 00 7F 63 03 06	C	DB	00h,00h,07fh,063h,03b,06h,0ch,018h
0C 18	00	C		
C3D8	18 18 18 00 00 00	C	DB	018h,018h,018h,00b,00b,00h,00h,00h ;'7' 37
00 00	00	C		
C3E0	00 00 3E 63 63 63	C	DB	00h,00h,03eh,063h,063h,063h,03eh,063h
3E 63	00	C		
C3E8	63 63 3E 00 00 00	C	DB	063h,063h,03eh,00b,00b,00h,00h,00h ;'8' 38
00 00	00	C		
C3F0	00 00 3E 63 63 63	C	DB	00h,00h,03eh,063h,063h,063h,03fh,03h
3F 03	00	C		
C3F8	03 06 1C 00 00 00	C	DB	03h,06h,01ch,00h,00h,00h,00h,00h ;'9' 39
00 00	00	C		
C400	00 00 00 18 00 00	C	DB	00h,00h,00h,018h,018h,00h,00h,00h
00 00	00	C		
C408	18 18 00 00 00 00	C	DB	018h,018h,00h,00b,00b,00h,00h,00h ;':' 3a
00 00	00	C		
C410	00 00 00 18 00 00	C	DB	00h,00h,00h,018h,018h,00h,00h,00h
00 00	00	C		
C418	18 18 30 00 00 00	C	DB	018h,018h,030h,00b,00b,00h,00h,00h ;';' 3b
00 00	00	C		
C420	00 00 06 0C 18 30	C	DB	00h,00h,06h,0ch,018h,030h,060h,030h
60 30	00	C		
C428	18 0C 06 00 00 00	C	DB	018h,0ch,06h,00h,00b,00h,00h,00h ;' < ' 3c
00 00	00	C		
C430	00 00 00 00 7E 00	C	DB	00h,00h,00b,00b,07eh,00h,00b,00b
00 00	00	C		
C438	7E 00 00 00 00 00	C	DB	07eh,00b,00b,00b,00b,00h,00h,00h ;'= ' 3d
00 00	00	C		
C440	00 00 60 30 18 0C	C	DB	00h,00h,060h,030h,018h,00b,06h,0ch
06 0C	00	C		
C448	18 30 60 00 00 00	C	DB	018h,030h,060h,00b,00h,00h,00h,00h ;' > ' 3e
00 00	00	C		
C450	00 00 3E 63 63 06	C	DB	00h,00h,03eh,063h,063h,06h,0ch,0ch
0C 0C	00	C		
C458	00 0C 0C 00 00 00	C	DB	00h,0ch,0ch,00h,00b,00h,00h,00h ;'? ' 3f
00 00	00	C		

# ROM BIOS Listing

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C460 00 00 3E 63 63 6F      C      DB 00h,00h,030h,063h,063h,06fh,06fh,06fh
      6F 6F      C      DB 060h,060h,030h,00h,00h,00h,00h,00h ;'E' 40
C468 0E 60 3E 00 00 00      C      DB 00h,00h,08h,010h,036h,063h,063h,07fh
      00 00      C      DB 063h,063h,063h,00h,00h,00h,00h,00h ;'A' 41
C470 00 00 08 1C 36 63      C      DB 00h,00h,070h,033h,033h,032h,030h,033h
      63 7F      C      DB 033h,033h,070h,00h,00h,00h,00h,00h ;'B' 42
C478 63 63 63 00 00 00      C      DB 00h,00h,010h,033h,060h,060h,060h,060h
      00 00      C      DB 060h,033h,010h,00h,00h,00h,00h,00h ;'C' 43
C480 00 00 7E 33 33 32      C      DB 00h,00h,070h,036h,033h,033h,033h,033h
      3E 33      C      DB 033h,036h,070h,00h,00h,00h,00h,00h ;'D' 44
C488 33 33 78 00 00 00      C      DB 00h,00h,07fh,033h,030h,034h,030h,034h
      00 00      C      DB 030h,033h,07fh,00h,00h,00h,00h,00h ;'E' 45
C490 00 00 1E 33 60 60      C      DB 00h,00h,07fh,031h,034h,030h,030h,034h
      60 60      C      DB 030h,030h,078h,00h,00h,00h,00h,00h ;'F' 46
C498 60 33 1E 00 00 00      C      DB 00h,00h,010h,033h,060h,060h,060h,06fh
      00 00      C      DB 063h,033h,010h,00h,00h,00h,00h,00h ;'G' 47
C4A0 00 00 7C 36 33 33      C      DB 00h,00h,063h,063h,063h,063h,07fh,063h
      33 33      C      DB 063h,063h,063h,00h,00h,00h,00h,00h ;'H' 48
C4A8 33 36 7C 00 00 00      C      DB 00h,00h,030h,018h,018h,018h,018h,018h
      00 00      C      DB 018h,018h,030h,00h,00h,00h,00h,00h ;'I' 49
C4B0 00 00 7F 33 30 34      C      DB 00h,00h,070h,060h,060h,060h,060h,060h
      3C 34      C      DB 066h,066h,030h,00h,00h,00h,00h,00h ;'J' 4a
C4B8 30 33 7F 00 00 00      C      DB 00h,00h,073h,033h,036h,036h,030h,036h
      00 00      C      DB 036h,033h,073h,00h,00h,00h,00h,00h ;'K' 4b
C4C0 00 00 7F 31 34 3C      C      DB 00h,00h,078h,030h,030h,030h,030h,030h
      3C 34      C      DB 030h,033h,07fh,00h,00h,00h,00h,00h ;'L' 4c
C4C8 30 30 78 00 00 00      C      DB 00h,00h,063h,077h,07fh,066h,063h,063h
      00 00      C      DB 063h,063h,063h,00h,00h,00h,00h,00h ;'M' 4d
C4D0 00 00 1E 33 60 60      C      DB 00h,00h,063h,073h,07fh,066h,063h,063h
      60 6F      C      DB 063h,063h,063h,00h,00h,00h,00h,00h ;'N' 4e
C4D8 63 33 1D 00 00 00      C      DB 00h,00h,010h,036h,063h,063h,063h,063h
      00 00      C      DB 063h,036h,010h,00h,00h,00h,00h,00h ;'O' 4f
C4E0 00 00 63 63 63 63      C      DB 00h,00h,070h,033h,033h,033h,030h,030h
      7F 63      C      DB 030h,030h,078h,00h,00h,00h,00h,00h ;'P' 50
C4E8 63 63 63 00 00 00      C      DB 00h,00h,010h,036h,063h,063h,063h,063h
      00 00      C      DB 066h,030h,010h,066h,030h,00h,00h,00h ;'Q' 51
C4F0 00 00 3C 18 18 18      C      DB 00h,00h,070h,033h,033h,033h,030h,036h
      18 18      C      DB 033h,033h,033h,00h,00h,00h,00h,00h ;'R' 52
C4F8 18 18 3C 00 00 00      C      DB 00h,00h,030h,063h,063h,063h,030h,010h,066h
      00 00      C      DB 063h,063h,030h,00h,00h,00h,00h,00h ;'S' 53
C500 00 00 0F 06 06 06      C      DB 00h,00h,070h,050h,018h,018h,018h,018h
      06 06      C      DB 018h,018h,030h,00h,00h,00h,00h,00h ;'T' 54
C508 66 66 3C 00 00 00      C      DB 00h,00h,063h,063h,063h,063h,063h,063h
      00 00      C      DB 063h,063h,030h,00h,00h,00h,00h,00h ;'U' 55
C510 00 00 73 33 36 36      C      DB 00h,00h,063h,063h,063h,063h,063h,063h
      3C 36      C      DB 036h,010h,08h,00h,00h,00h,00h,00h ;'V' 56
C518 36 33 73 00 00 00      C      DB 00h,00h,063h,063h,063h,063h,063h,066h
      00 00      C      DB 066h,07fh,036h,00h,00h,00h,00h,00h ;'W' 57
C520 00 00 78 30 30 30      C      DB 00h,00h,063h,063h,063h,063h,036h,010h,036h
      30 30      C      DB 063h,063h,063h,00h,00h,00h,00h,00h ;'X' 58
C528 30 33 7F 00 00 00      C
      00 00      C
C530 00 00 73 33 36 36      C
      3C 36      C
C538 36 33 73 00 00 00      C
      00 00      C
C540 00 00 78 30 30 30      C
      30 30      C
C548 30 33 7F 00 00 00      C
      00 00      C
C550 00 00 73 33 36 36      C
      3C 36      C
C558 36 33 73 00 00 00      C
      00 00      C
C560 00 00 78 30 30 30      C
      30 30      C
C568 30 30 78 00 00 00      C
      00 00      C
C570 00 00 1C 36 63 63      C
      63 63      C
C578 6B 3E 1C 06 03 00      C
      00 00      C
C580 00 00 7E 33 33 33      C
      3E 36      C
C588 33 33 33 00 00 00      C
      00 00      C
C590 00 00 3E 63 63 30      C
      1C 06      C
C598 63 63 3E 00 00 00      C
      00 00      C
C5A0 00 00 7E 5A 18 18      C
      18 18      C
C5A8 18 18 3C 00 00 00      C
      00 00      C
C5B0 00 00 63 63 63 63      C
      63 63      C
C5B8 63 63 3E 00 00 00      C
      00 00      C
C5C0 00 00 63 63 63 63      C
      63 63      C
C5C8 36 1C 08 00 00 00      C
      00 00      C
C5D0 00 00 63 63 63 63      C
      63 6B      C
C5D8 6B 7F 36 00 00 00      C
      00 00      C
C5E0 00 00 63 63 63 36      C
      1C 36      C
C5E8 63 63 63 00 00 00      C
      00 00      C

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C5F0	00 00 66 66 66 66	C	DB 00h,00h,066h,066h,066h,066h,066h,066h,066h,066h,066h,066h
	66 3c	C	
C5F8	18 18 3c 00 00 00	C	DB 018h,018h,03ch,00h,00h,00h,00h,00h,00h ; 'Y' 59
	00 00	C	
C600	00 00 7f 63 06 0c	C	DB 00h,00h,07fh,063h,066h,06h,018h,030h
	18 30	C	
C608	60 63 7f 00 00 00	C	DB 060h,063h,07fh,00h,00h,00h,00h,00h ; 'Z' 5a
	00 00	C	
C610	00 00 3c 30 30 30	C	DB 00h,00h,03ch,030h,030h,030h,030h,030h
	30 30	C	
C618	30 30 3c 00 00 00	C	DB 030h,030h,03ch,00h,00h,00h,00h,00h ; '[' 5b
	00 00	C	
C620	00 00 40 60 30 18	C	DB 00h,00h,040h,060h,030h,018h,00h,06h
	0c 06	C	
C628	03 01 00 00 00 00	C	DB 03h,01h,00h,00h,00h,00h,00h,00h ; '\ ' 5c
	00 00	C	
C630	00 00 3c 0c 0c 0c	C	DB 00h,00h,03ch,0ch,0ch,0ch,0ch,0ch
	0c 0c	C	
C638	0c 0c 3c 00 00 00	C	DB 0ch,0ch,03ch,00h,00h,00h,00h,00h ; ']' 5d
	00 00	C	
C640	08 1c 36 63 00 00	C	DB 08h,01ch,036h,063h,00h,00h,00h,00h
	00 00	C	
C648	00 00 00 00 00 00	C	DB 00h,00h,00h,00h,00h,00h,00h,00h ; '\ ' 5e
	00 00	C	
C650	00 00 00 00 00 00	C	DB 00h,00h,00h,00h,00h,00h,00h,00h
	00 00	C	
C658	00 00 00 00 00 00	C	DB 00h,00h,00h,00h,00h,00h,07fh,00h ; '_ ' 5f
	7f 00	C	
C660	18 18 0c 00 00 00	C	DB 018h,018h,0ch,00h,00h,00h,00h,00h
	00 00	C	
C668	00 00 00 00 00 00	C	DB 00h,00h,00h,00h,00h,00h,00h,00h ; '\ ' 60
	00 00	C	
C670	00 00 00 00 00 3c	C	DB 00h,00h,00h,00h,00h,03ch,06h,03ch
	06 3e	C	
C678	66 66 3b 00 00 00	C	DB 066h,066h,03bh,00h,00h,00h,00h,00h ; 'a' 61
	00 00	C	
C680	00 00 70 30 30 3e	C	DB 00h,00h,070h,030h,030h,030h,033h,033h
	33 33	C	
C688	33 33 6e 00 00 00	C	DB 033h,033h,06eh,00h,00h,00h,00h,00h ; 'b' 62
	00 00	C	
C690	00 00 00 00 00 3e	C	DB 00h,00h,00h,00h,00h,03ch,063h,066h
	63 60	C	
C698	60 63 3e 00 00 00	C	DB 060h,063h,03eh,00h,00h,00h,00h,00h ; 'c' 63
	00 00	C	
C6A0	00 00 0e 06 06 3e	C	DB 00h,00h,0eh,06h,06h,03ch,066h,066h
	66 66	C	
C6A8	66 66 3b 00 00 00	C	DB 066h,066h,03bh,00h,00h,00h,00h,00h ; 'd' 64
	00 00	C	
C6B0	00 00 00 00 00 3e	C	DB 00h,00h,00h,00h,00h,03ch,063h,07fh
	63 7f	C	
C6B8	60 63 3e 00 00 00	C	DB 060h,063h,03eh,00h,00h,00h,00h,00h ; 'e' 65
	00 00	C	
C6C0	00 00 1e 33 30 00	C	DB 00h,00h,01eh,033h,030h,030h,07eh,030h
	7e 30	C	
C6C8	30 30 78 00 00 00	C	DB 030h,030h,078h,00h,00h,00h,00h,00h ; 'f' 66
	00 00	C	
C6D0	00 00 00 00 00 3b	C	DB 00h,00h,00h,00h,00h,03bh,066h,066h
	66 66	C	
C6D8	66 66 3e 06 66 3c	C	DB 066h,066h,03eh,06h,066h,03ch,00h,00h ; 'g' 67
	00 00	C	
C6E0	00 00 70 30 36 3b	C	DB 00h,00h,070h,030h,036h,03bh,033h,033h
	33 33	C	
C6E8	33 33 73 00 00 00	C	DB 033h,033h,073h,00h,00h,00h,00h,00h ; 'h' 68
	00 00	C	
C6F0	00 00 0c 0c 00 1c	C	DB 00h,00h,0ch,0ch,00h,01eh,0ch,00h
	0c 0c	C	
C6F8	0c 0c 1e 00 00 00	C	DB 0ch,0ch,01eh,00h,00h,00h,00h,00h ; 'i' 69
	00 00	C	
C700	00 00 0c 0c 00 1c	C	DB 00h,00h,0ch,0ch,00h,01eh,0ch,00h
	0c 0c	C	
C708	0c 0c 0c 0c 78	C	DB 0ch,0ch,0ch,0ch,0ch,078h,00h,00h ; 'j' 6a
	00 00	C	
C710	00 00 70 30 30 33	C	DB 00h,00h,070h,030h,030h,033h,036h,03ch
	36 3c	C	
C718	36 33 73 00 00 00	C	DB 036h,033h,073h,00h,00h,00h,00h,00h ; 'k' 6b
	00 00	C	
C720	00 00 1c 0c 0c 0c	C	DB 00h,00h,01ch,0ch,0ch,0ch,0ch,00h
	0c 0c	C	
C728	0c 0c 1e 00 00 00	C	DB 0ch,0ch,01eh,00h,00h,00h,00h,00h ; 'l' 6c
	00 00	C	
C730	00 00 00 00 00 66	C	DB 00h,00h,00h,00h,00h,066h,07fh,066h
	7f 6b	C	
C738	66 6b 6b 00 00 00	C	DB 066h,06bh,06bh,00h,00h,00h,00h,00h ; 'm' 6d
	00 00	C	
C740	00 00 00 00 00 6e	C	DB 00h,00h,00h,00h,00h,06eh,033h,033h
	33 33	C	
C748	33 33 33 00 00 00	C	DB 033h,033h,033h,00h,00h,00h,00h,00h ; 'n' 6e
	00 00	C	
C750	00 00 00 00 00 3e	C	DB 00h,00h,00h,00h,00h,03ch,063h,063h
	63 63	C	
C758	63 63 3e 00 00 00	C	DB 063h,063h,03eh,00h,00h,00h,00h,00h ; 'o' 6f
	00 00	C	
C760	00 00 00 00 00 6e	C	DB 00h,00h,00h,00h,00h,06eh,033h,033h
	33 33	C	
C768	33 33 3e 30 30 78	C	DB 033h,033h,03eh,030h,030h,078h,00h,00h ; 'p' 70
	00 00	C	
C770	00 00 00 00 00 3b	C	DB 00h,00h,00h,00h,00h,03bh,066h,066h
	66 66	C	
C778	66 66 3e 06 06 0f	C	DB 066h,066h,03eh,06h,06h,07fh,00h,00h ; 'q' 71
	00 00	C	

# ROM BIOS Listing

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C780 00 00 00 00 00 6E C DB 00h,00h,00h,00h,00h,06eh,03bh,030h
      3B 30 C
C788 30 30 78 00 00 00 C DB 030h,030h,078h,00h,00h,00h,00h,00h ;'p' 72
      00 00 C
C790 00 00 00 00 00 3E C DB 00h,00h,00h,00h,00h,03eh,06bh,038h
      63 38 C
C798 0E 63 3E 00 00 00 C DB 0eh,063h,03eh,00h,00h,00h,00h,00h ;'a' 73
      00 00 C
C7A0 00 00 00 08 18 7E C DB 00h,00h,00h,08h,018h,07eh,018h,018h
      18 18 C
C7A8 18 1B 0E 00 00 00 C DB 018h,01bh,0eh,00h,00h,00h,00h,00h ;'t' 74
      00 00 C
C7B0 00 00 00 00 00 66 C DB 00h,00h,00h,00h,00h,066h,066h,066h
      66 66 C
C7B8 66 66 3B 00 00 00 C DB 066h,066h,03bh,00h,00h,00h,00h,00h ;'u' 75
      00 00 C
C7C0 00 00 00 00 00 63 C DB 00h,00h,00h,00h,00h,063h,063h,063h
      63 63 C
C7C8 36 1C 08 00 00 00 C DB 036h,01ch,08h,00h,00h,00h,00h,00h ;'v' 76
      00 00 C
C7D0 00 00 00 00 00 63 C DB 00h,00h,00h,00h,00h,063h,06bh,06bh
      6B 6B C
C7D8 68 7F 36 00 00 00 C DB 06bh,07fh,036h,00h,00h,00h,00h,00h ;'w' 77
      00 00 C
C7E0 00 00 00 00 00 63 C DB 00h,00h,00h,00h,00h,063h,036h,01eh
      36 1C C
C7E8 1C 36 63 00 00 00 C DB 01eh,036h,063h,00h,00h,00h,00h,00h ;'x' 78
      00 00 C
C7F0 00 00 00 00 00 63 C DB 00h,00h,00h,00h,00h,063h,066h,066h
      66 66 C
C7F8 66 66 3E 06 66 3C C DB 066h,066h,03eh,06h,066h,03eh,00h,00h ;'y' 79
      00 00 C
C800 00 00 00 00 00 7F C DB 00h,00h,00h,00h,00h,07fh,066h,0eh
      66 0C C
C808 18 33 7F 00 00 00 C DB 018h,033h,07fh,00h,00h,00h,00h,00h ;'z' 7a
      00 00 C
C810 00 00 0E 18 18 18 C DB 00h,00h,0eh,018h,018h,018h,070h,018h
      70 18 C
C818 18 18 0E 00 00 00 C DB 018h,018h,0eh,00h,00h,00h,00h,00h ;'[' 7b
      00 00 C
C820 00 00 18 18 18 18 C DB 00h,00h,018h,018h,018h,018h,00h,018h
      00 18 C
C828 18 18 18 00 00 00 C DB 018h,018h,018h,00h,00h,00h,00h,00h ;'|' 7c
      00 00 C
C830 00 00 70 18 18 18 C DB 00h,00h,070h,018h,018h,018h,0eh,018h
      0E 18 C
C838 18 18 70 00 00 00 C DB 018h,018h,070h,00h,00h,00h,00h,00h ;']' 7d
      00 00 C
C840 00 00 3B 6E 00 00 C DB 00h,00h,03bh,06eh,00h,00h,00h,00h
      00 00 C
C848 00 00 00 00 00 00 C DB 00h,00h,00h,00h,00h,00h,00h,00h ;'``' 7e
      00 00 C
C850 00 00 00 00 08 1C C DB 00h,00h,00h,00h,08h,01eh,036h,063h
      36 63 C
C858 63 7F 00 00 00 00 C DB 063h,07fh,00h,00h,00h,00h,00h,00h ;'``' 7f
      00 00 C
      C ;End of font matrix
C860 C fontlo16 endp
      C
C860 C font_hi_8x8 label byte ; 1024 bytes
      C include fonthi8.asm
C860 C fonthi8 proc near
      C ; SystemFont ; <hi_mediumres> (M24) 8 x 8 font table for M24
      C
C860 1E 33 60 33 C DB 01eh,033h,060h,033h
C868 1E 08 04 06 C DB 0eh,08h,04h,06h ; 0
C86C 66 00 66 66 C DB 066h,00h,066h,066h ; 1
C870 66 66 66 3B C DB 066h,066h,066h,03bh ; 1
C874 06 0C 00 1E C DB 06h,0eh,00h,01eh
C878 33 3F 31 3E C DB 03bh,03fh,030h,01eh ; 2
C87C 08 14 00 3C C DB 08h,014h,00h,03eh
C87E 06 3E 66 3B C DB 06h,03eh,066h,03bh ; 3
C880 00 36 00 3C C DB 00h,036h,00h,03eh
C884 06 3E 66 3E C DB 06h,03eh,066h,03bh ; 4
C888 30 18 00 3C C DB 030h,018h,00h,03eh
C88C 06 3E 66 3B C DB 06h,03eh,066h,03bh ; 5
C890 08 14 08 3C C DB 08h,014h,08h,03eh
C894 06 3E 66 3E C DB 06h,03eh,066h,03bh ; 6
C898 3C 66 60 66 C DB 03ch,066h,060h,066h
C89C 3C 08 04 08 C DB 03ch,08h,04h,08h ; 7
C8A0 18 34 00 3E C DB 018h,034h,00h,03eh
C8A4 63 7F 60 3E C DB 063h,07fh,060h,03eh ; 8
C8A8 00 36 00 3E C DB 00h,036h,00h,03eh
C8AC 63 7F 60 3E C DB 063h,07fh,060h,03eh ; 9
C8B0 30 18 00 3C C DB 030h,018h,00h,03eh
C8B4 66 7E 60 3C C DB 066h,07eh,060h,03eh ; a
C8B8 00 36 00 1C C DB 00h,036h,00h,01ch
C8BC 0C 0C 0C 1E C DB 0ch,0ch,0ch,01eh ; b
C8C0 08 14 00 1C C DB 08h,014h,00h,01eh
C8C4 0C 0C 0C 1E C DB 0ch,0ch,0ch,01eh ; c
C8C8 30 18 00 1C C DB 030h,018h,00h,01ch
C8CC 0C 0C 0C 1E C DB 0ch,0ch,0ch,01eh ; d
C8D0 66 00 18 3C C DB 066h,00h,018h,03eh
C8D4 66 7E 66 66 C DB 066h,07eh,066h,066h ; e
C8D8 18 24 18 3C C DB 018h,024h,018h,03eh
C8DC 66 7E 66 66 C DB 066h,07eh,066h,066h ; f
C8E0 0C 18 7F 31 C DB 0ch,018h,07fh,031h
C8E4 3C 30 31 7F C DB 03ch,030h,031h,07fh ; 10

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# ROM BIOS Listing

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C8E8 00 36 4B 0F      C      DB 00h,036h,04bh,0fh
C8EC 38 58 5D 36      C      DB 038h,058h,05dh,036h ; 11
CB70 00 1F 28 49      C      DB 00h,01fh,028h,049h
CB74 4F 79 48 4F      C      DB 04fh,079h,048h,04fh ; 12
CB78 08 14 00 1C      C      DB 08h,014h,00h,01ch
CB7C 36 63 36 1C      C      DB 036h,063h,036h,01ch ; 13
C900 00 36 00 1C      C      DB 00h,036h,00h,01ch
C904 36 63 36 1C      C      DB 036h,063h,036h,01ch ; 14
C908 30 18 00 1C      C      DB 030h,018h,00h,01ch
C90C 36 63 36 1C      C      DB 036h,063h,036h,01ch ; 15
C910 08 14 00 66      C      DB 08h,014h,00h,066h
C914 66 66 66 3B      C      DB 066h,066h,066h,03bh ; 16
C918 30 18 00 66      C      DB 030h,018h,00h,066h
C91C 66 66 66 3B      C      DB 066h,066h,066h,03bh ; 17
C920 66 00 66 66      C      DB 066h,00h,066h,066h
C924 66 3E 06 78      C      DB 066h,03eh,06h,078h ; 18
C928 00 36 00 1C      C      DB 00h,036h,00h,01ch
C92C 36 63 36 1C      C      DB 036h,063h,036h,01ch ; 19
C930 00 63 00 63      C      DB 00h,063h,00h,063h
C934 63 63 63 3E      C      DB 063h,063h,063h,03eh ; 1a
C938 08 08 3E 40      C      DB 08h,08h,03eh,040h
C93C 40 3E 08 08      C      DB 040h,03eh,08h,08h ; 1b
C940 0E 18 18 3C      C      DB 0eh,018h,018h,03ch
C944 18 18 39 7E      C      DB 018h,018h,039h,07eh ; 1c
C948 22 14 08 3E      C      DB 022h,014h,08h,03eh ; 1d
C94C 08 3E 08 08      C      DB 08h,03eh,08h,08h ; 1e
C950 70 48 72 42      C      DB 070h,048h,072h,042h
C954 47 42 42 01      C      DB 047h,042h,042h,01h ; 1e
C958 0C 12 10 38      C      DB 0eh,012h,010h,038h
C95C 10 10 50 20      C      DB 010h,010h,050h,020h ; 1f
C960 06 0C 00 3C      C      DB 06h,0ch,00h,03ch
C964 06 3E 66 3B      C      DB 06h,03eh,066h,03bh ; ' ' 20
C968 06 0C 00 1C      C      DB 06h,0ch,00h,01ch
C96C 0C 0C 0E 1E      C      DB 0eh,0ch,0eh,01eh ; ' ' 21
C970 06 0C 00 1C      C      DB 06h,0ch,00h,01ch
C974 36 63 36 1C      C      DB 036h,063h,036h,01ch ; ' ' 22
C978 06 0C 00 66      C      DB 06h,0ch,00h,066h
C97C 66 66 66 3B      C      DB 066h,066h,066h,03bh ; ' ' 23
C980 33 CC 00 7C      C      DB 033h,0cch,00h,07ch
C984 66 66 66 66      C      DB 066h,066h,066h,066h ; ' ' 24
C988 33 CC 63 73      C      DB 033h,0cch,063h,073h
C98C 7A 6F 67 63      C      DB 07bh,06fh,067h,063h
C990 06 3C 06 3E      C      DB 00h,03ch,06h,03eh
C994 66 38 00 7F      C      DB 066h,03bh,00h,07fh ; ' ' 26
C998 00 1C 36 63      C      DB 00h,01ch,036h,063h
C99C 36 1C 00 7F      C      DB 036h,01ch,00h,07fh ; ' ' 27
C9A0 18 00 18 18      C      DB 018h,00h,018h,018h
C9A4 30 46 3C 00      C      DB 030h,046h,03ch,00h ; ' ' 28
C9A8 00 00 7F 60      C      DB 00h,00h,07fh,060h
C9AC 60 00 00 00      C      DB 060h,00h,00h,00h ; ' ' 29
C9B0 00 00 7F 03      C      DB 00h,00h,07fh,03h
C9B4 03 00 00 00      C      DB 03h,00h,00h,00h ; ' ' 2a
C9B8 20 62 24 28      C      DB 020h,062h,024h,028h
C9BC 16 21 82 07      C      DB 016h,021h,028h,07h ; ' ' 2b
C9C0 20 62 24 2A      C      DB 020h,062h,024h,02ah
C9C4 16 2A 0F 02      C      DB 016h,02ah,0fh,02h ; ' ' 2c
C9C8 18 18 00 18      C      DB 018h,018h,00h,018h
C9CC 18 3C 3E 18      C      DB 018h,03ch,03eh,018h ; ' ' 2d
C9D0 00 1B 36 6C      C      DB 00h,01bh,036h,06ch
C9D4 36 1B 00 00      C      DB 036h,01bh,00h,00h ; ' ' 2e
C9D8 00 6C 36 18      C      DB 00h,06ch,036h,018h
C9DC 36 6C 00 00      C      DB 036h,06ch,00h,00h ; ' ' 2f
C9E0 22 88 22 88      C      DB 022h,088h,022h,088h
C9E4 22 88 22 88      C      DB 022h,088h,022h,088h ; '0' 30
C9E8 55 AA 55 AA      C      DB 055h,0aah,055h,0aah
C9EC 55 AA 55 AA      C      DB 055h,0aah,055h,0aah ; ' ' 31
C9F0 CE 77 CE 77      C      DB 0ceh,077h,0ceh,077h
C9F4 CE 77 CE 77      C      DB 0ceh,077h,0ceh,077h ; ' ' 32
C9F8 18 18 18 18      C      DB 018h,018h,018h,018h
C9FC 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 33
CA00 18 18 18 18      C      DB 018h,018h,018h,018h
CA04 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 34
CA08 18 18 18 18      C      DB 018h,018h,018h,018h
CA0C 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 35
CA10 36 36 18 18      C      DB 036h,036h,036h,018h
CA14 36 36 36 36      C      DB 036h,036h,036h,036h ; ' ' 36
CA18 00 00 00 FE      C      DB 00h,00h,00h,0feh
CA1C 36 36 36 36      C      DB 036h,036h,036h,036h ; ' ' 37
CA20 00 00 18 18      C      DB 00h,00h,018h,018h
CA24 18 18 18 18      C      DB 018h,018h,018h,018h ; '0' 38
CA28 36 36 18 36      C      DB 036h,036h,018h,036h
CA2C 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 39
CA30 36 36 18 18      C      DB 036h,036h,036h,018h
CA34 36 36 36 36      C      DB 036h,036h,036h,036h ; ' ' 3a
CA38 00 00 FE 06      C      DB 00h,00h,0feh,06h
CA3C 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 3b
CA40 36 36 18 18      C      DB 036h,036h,018h,018h
CA44 FE 00 00 00      C      DB 0feh,00h,00h,00h ; ' < ' 3c
CA48 36 36 36 FE      C      DB 036h,036h,036h,0feh
CA4C 00 00 00 00      C      DB 00h,00h,00h,00h ; ' ' 3d
CA50 18 18 18 18      C      DB 018h,018h,018h,018h
CA54 18 00 00 00      C      DB 018h,00h,00h,00h ; ' ' 3e
CA58 00 00 00 18      C      DB 00h,00h,00h,018h
CA5C 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 3f
CA60 18 18 18 18      C      DB 018h,018h,018h,018h
CA64 00 00 00 00      C      DB 00h,00h,00h,00h ; ' ' 40
CA68 18 18 18 18      C      DB 018h,018h,018h,018h
CA6C 00 00 00 00      C      DB 00h,00h,00h,00h ; ' ' 41
CA70 00 00 00 FF      C      DB 00h,00h,00h,0ffh
CA74 18 18 18 18      C      DB 018h,018h,018h,018h ; ' ' 42

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# ROM BIOS Listing

CA78	18	18	1F	C	DB	018h,018h,018h,01fh		
CA7C	18	18	18	C	DB	018h,018h,018h,018h	; 'C' 43	
CAB0	00	00	00	FF	C	DB	00h,00h,00h,00fh	
CAB4	00	00	00	00	C	DB	00h,00h,00h,00h	; 'D' 44
CAB8	18	18	1F	FF	C	DB	018h,018h,018h,00fh	
CABC	18	18	18	C	DB	018h,018h,018h,018h	; 'E' 45	
CA90	18	18	1F	18	C	DB	018h,018h,01fh,018h	
CA94	1F	18	18	18	C	DB	01fh,018h,018h,018h	; 'F' 46
CA98	36	36	36	37	C	DB	036h,036h,036h,037h	
CA9C	36	36	36	36	C	DB	036h,036h,036h,036h	; 'G' 47
CA84	36	36	37	30	C	DB	036h,036h,037h,030h	
CAA9	3F	00	00	00	C	DB	03fh,00h,00h,00h	; 'H' 48
CAAB	00	00	3F	30	C	DB	00h,00h,03fh,030h	; 'I' 49
CAAC	37	36	36	36	C	DB	037h,036h,036h,036h	; 'J' 4a
CABD	36	36	FF	00	C	DB	036h,036h,07fh,00h	; 'K' 4b
CABA	FF	00	00	00	C	DB	00fh,00h,00h,00h	; 'L' 4c
CABE	00	00	FF	00	C	DB	00h,00h,00fh,00h	; 'M' 4d
CABC	FF	36	36	36	C	DB	07fh,036h,036h,036h	; 'N' 4e
CAC0	36	36	37	30	C	DB	036h,036h,037h,030h	; 'O' 4f
CAC4	37	34	34	34	C	DB	037h,034h,034h,034h	; 'P' 50
CAC8	00	00	FF	00	C	DB	00h,00h,00fh,00h	; 'Q' 51
CACC	FF	00	00	00	C	DB	00fh,00h,00h,00h	; 'R' 52
CADD	36	36	FF	00	C	DB	036h,036h,07fh,00h	; 'S' 53
CAD8	FF	36	36	36	C	DB	07fh,036h,036h,036h	; 'T' 54
CADB	18	18	FF	00	C	DB	018h,018h,00fh,00h	; 'U' 55
CADC	FF	00	00	00	C	DB	00fh,00h,00h,00h	; 'V' 56
CAE0	36	36	36	FF	C	DB	036h,036h,036h,00fh	; 'W' 57
CAE4	00	00	00	00	C	DB	00h,00h,00h,00h	; 'X' 58
CAE8	00	00	FF	00	C	DB	00h,00h,00fh,00h	; 'Y' 59
CABC	FF	18	18	18	C	DB	00fh,018h,018h,018h	; 'Z' 5a
CAFO	00	00	00	FF	C	DB	00h,00h,00h,00fh	; '0' 5b
CAF4	36	36	36	36	C	DB	036h,036h,036h,036h	; '1' 5c
CAF8	36	36	36	3F	C	DB	036h,036h,036h,03fh	; '2' 5d
CAFC	00	00	00	00	C	DB	00h,00h,00h,00h	; '3' 5e
CB00	18	18	1F	18	C	DB	018h,018h,01fh,018h	; '4' 5f
CB04	1F	00	00	00	C	DB	01fh,00h,00h,00h	; '5' 60
CB08	00	00	1F	18	C	DB	00h,00h,01fh,018h	; '6' 61
CB0C	1F	18	18	18	C	DB	01fh,018h,018h,018h	; '7' 62
CB10	00	00	00	3F	C	DB	00h,00h,00h,03fh	; '8' 63
CB14	36	36	36	36	C	DB	036h,036h,036h,036h	; '9' 64
CB18	36	36	36	FF	C	DB	036h,036h,036h,00fh	; 'A' 65
CB1C	36	36	36	36	C	DB	036h,036h,036h,036h	; 'B' 66
CB20	18	18	FF	18	C	DB	018h,018h,00fh,018h	; 'C' 67
CB24	FF	18	18	18	C	DB	00fh,018h,018h,018h	; 'D' 68
CB28	18	18	18	FF	C	DB	018h,018h,018h,00fh	; 'E' 69
CB2C	00	00	00	00	C	DB	00h,00h,00h,00h	; 'F' 6a
CB30	00	00	00	1F	C	DB	00h,00h,00h,01fh	; 'G' 6b
CB34	18	18	18	18	C	DB	018h,018h,018h,018h	; 'H' 6c
CB38	FF	FF	FF	FF	C	DB	07fh,07fh,07fh,07fh	; 'I' 6d
CB3C	FF	FF	FF	FF	C	DB	00fh,00fh,00fh,00fh	; 'J' 6e
CB40	00	00	00	00	C	DB	00h,00h,00h,00h	; 'K' 6f
CB44	FF	FF	FF	FF	C	DB	00fh,00fh,00fh,00fh	; 'L' 70
CB48	F0	F0	F0	F0	C	DB	0f0h,0f0h,0f0h,0f0h	; 'M' 71
CB4C	F0	F0	F0	F0	C	DB	0f0h,0f0h,0f0h,0f0h	; 'N' 72
CB50	0F	0F	0F	0F	C	DB	0fh,0fh,0fh,0fh	; 'O' 73
CB54	0F	0F	0F	0F	C	DB	0fh,0fh,0fh,0fh	; 'P' 74
CB58	FF	FF	FF	FF	C	DB	00fh,00fh,00fh,00fh	; 'Q' 75
CB5C	00	00	00	00	C	DB	00h,00h,00h,00h	; 'R' 76
CB60	00	00	3B	6E	C	DB	00h,00h,03bh,06eh	; 'S' 77
CB64	6C	6C	6E	3E	C	DB	06ch,06ch,06eh,03bh	; 'T' 78
CB68	3E	63	7E	63	C	DB	03eh,063h,07eh,063h	; 'U' 79
CB6C	63	7E	60	60	C	DB	063h,07eh,060h,060h	; 'V' 7a
CB70	00	7E	32	30	C	DB	00h,07eh,032h,030h	; 'W' 7b
CB74	30	30	30	7E	C	DB	030h,030h,030h,07eh	; 'X' 7c
CB78	00	01	7F	54	C	DB	00h,01h,07fh,054h	; 'Y' 7d
CB7C	14	14	14	14	C	DB	014h,014h,014h,014h	; 'Z' 7e
CB80	00	7F	61	30	C	DB	00h,07fh,061h,030h	; '0' 7f
CB84	18	30	61	7F	C	DB	018h,030h,061h,07fh	; '1' 80
CB88	00	00	1F	34	C	DB	00h,00h,01fh,034h	; '2' 81
CB8C	62	62	34	1E	C	DB	062h,062h,034h,018h	; '3' 82
CB90	00	36	36	36	C	DB	00h,036h,036h,036h	; '4' 83
CB94	3C	30	30	60	C	DB	03ch,030h,030h,060h	; '5' 84
CB98	00	3B	6E	0C	C	DB	00h,03bh,06eh,00h	; '6' 85
CB9C	0C	0C	00	00	C	DB	0ch,0ch,00h,00h	; '7' 86
CB9E	66	3C	1E	3C	C	DB	066h,03ch,018h,03bh	; '8' 87
CBAB	00	1C	36	63	C	DB	00h,01ch,036h,063h	; '9' 88
CBAC	7F	63	36	1C	C	DB	07fh,063h,036h,01ch	; 'A' 89
CBBD	00	1C	36	63	C	DB	00h,01ch,036h,063h	; 'B' 8a
CBBC	63	36	7E	7F	C	DB	063h,036h,036h,07fh	; 'C' 8b
CBBE	1E	30	18	0C	C	DB	01eh,030h,018h,00h	; 'D' 8c
CBBC	3E	66	66	3C	C	DB	03eh,066h,066h,03ch	; 'E' 8d
CBCC	00	00	7E	DB	C	DB	00h,00h,07eh,0dbh	; 'F' 8e
CBCE	DB	6E	7E	DB	C	DB	0dbh,06eh,07eh,0dbh	; 'G' 8f
CBCC	DB	7E	60	0C	C	DB	0dbh,07eh,060h,0c0h	; 'H' 90
CBDD	00	1C	30	60	C	DB	00h,01ch,030h,060h	; 'I' 91
CBDE	7C	60	1C	0C	C	DB	07ch,060h,030h,01ch	; 'J' 92
CBDE	00	00	3E	63	C	DB	00h,00h,03eh,063h	; 'K' 93
CBDC	63	63	63	63	C	DB	063h,063h,063h,063h	; 'L' 94
CBE0	00	00	3E	00	C	DB	00h,00h,03eh,00h	; 'M' 95
CBE4	3E	00	3E	00	C	DB	03eh,00h,03eh,00h	; 'N' 96
CBE8	18	18	7E	18	C	DB	018h,018h,07eh,018h	; 'O' 97
CBEC	18	00	7E	00	C	DB	018h,00h,07eh,00h	; 'P' 98
CBF0	18	0C	0C	0C	C	DB	018h,00h,06h,00h	; 'Q' 99
CBF4	18	00	3E	00	C	DB	018h,00h,03eh,00h	; 'R' 9a
CBF8	0C	18	30	18	C	DB	0ch,018h,030h,018h	; 'S' 9b
CBFC	0C	00	3E	00	C	DB	0ch,00h,03eh,00h	; 'T' 9c
CC00	0E	1B	1B	18	C	DB	0eh,01bh,01bh,018h	; 'U' 9d
CC04	18	18	18	18	C	DB	018h,018h,018h,018h	; 'V' 9e
CC08	18	18	18	18	C	DB	018h,018h,018h,018h	; 'W' 9f

# ROM BIOS Listing

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CC0C 18 D8 D8 70      C      DB 018h,0d8h,0d8h,070h ;'u' 75
CC10 00 18 18 00      C      DB 00h,018h,018h,00h
CC14 3E 00 18 18      C      DB 03eh,00h,018h,018h ;'v' 76
CC18 00 00 3B 6E      C      DB 00h,00h,03bh,06eh
CC1C 00 3B 6E 00      C      DB 00h,03bh,06eh,00h ;'w' 77
CC20 00 38 6C 6C      C      DB 00h,038h,06eh,06eh
CC24 38 00 00 00      C      DB 038h,00h,00h,00h
CC28 00 18 3C 3C      C      DB 00h,018h,03eh,03eh ;'x' 78
CC2C 18 00 00 00      C      DB 018h,00h,00h,00h ;'y' 79
CC30 00 00 00 18      C      DB 00h,00h,00h,018h
CC34 18 00 00 00      C      DB 018h,00h,00h,00h ;'z' 7a
CC38 0F 0C 0C 0C      C      DB 0Fh,0Ch,0Ch,0Ch
CC3C 0C 6C 3C 1C      C      DB 0Ch,06Ch,03eh,01eh ;{' 7b
CC40 6C 36 36 36      C      DB 06Ch,036h,036h,036h
CC44 36 00 00 00      C      DB 036h,00h,00h,00h ;'|' 7c
CC48 08 14 04 08      C      DB 08h,014h,04h,08h
CC4C 10 1C 00 00      C      DB 010h,01Ch,00h,00h ;'}' 7d
CC50 00 1C 1C 1C      C      DB 00h,01Ch,01eh,01eh
CC54 1C 1C 00 00      C      DB 01Ch,01Ch,00h,00h ;'' 7e
CC58 00 00 00 00      C      DB 00h,00h,00h,00h ; 7f
CC5C 00 00 00 00      C      ;End of font matrix

CC60      C      font18 endp
CC60      C      oode ends

C      include kbdata.asm
C      ;-----
C      ;      Filename:      kb.data:      USA-ASCII
C      ;
C      ;      This module includes the keyboard scan code translation data
C      ;      for different keyboards.
C      ;
C      ;-----
CC60      C      oode segment public 'ROM'
CC60      C      assume cs:oode, ds:nothing, es:nothing, ss:nothing
C      C
C      kb_data1 proc
C      ;-----
C      ;      special_cases
C      ;-----
C      kbina equ 0C0h ; kb_insert_lock (min_case)
C      kbcap equ 0C1h ; kb_caps_lock
C      kbnum equ 0C2h ; kb_num_lock
C      kbscr equ 0C3h ; kb_scroll_lock
C      kbalt equ 0C4h ; kb_alt_lock
C      kbctl equ 0C5h ; kb_control_lock
C      kblsh equ 0C6h ; kb_l_shift_lock
C      kbrsh equ 0C7h ; kb_r_shift_lock
C
C      kbrea equ 0C8h ; kb_reset (mid_case)
C      kbbrk equ 0C9h ; kb_break
C      kbpau equ 0CAh ; kb_pause
C      kbprt equ 0CBh ; kb_print_screen
C      kbnul equ 0CCh ; kb_null
C      kNONE equ 0CDh ; kb_none
C
C      kdec9 equ 0CEh ; kb_alt_dec_9
C      kdec8 equ 0CFh ; kb_alt_dec_8
C      kdec7 equ 0D0h ; kb_alt_dec_7
C      kdec6 equ 0D1h ; kb_alt_dec_6
C      kdec5 equ 0D2h ; kb_alt_dec_5
C      kdec4 equ 0D3h ; kb_alt_dec_4
C      kdec3 equ 0D4h ; kb_alt_dec_3
C      kdec2 equ 0D5h ; kb_alt_dec_2
C      kdec1 equ 0D6h ; kb_alt_dec_1
C      kdec0 equ 0D7h ; kb_alt_dec_0
C
C      kdbl0 equ 0D8h ; kb_double_zero (max_case)
C      ;-----
C      ;      7 CapLk Bytes
C      ;-----
CC60      C      kb_cap_flags label byte
CC60 00      C      db 00000000b ; scancode 00 (00h) - 07 (07h) ESC to '6'
CC61 00      C      db 00000000b ; scancode 08 (08h) - 15 (0Fh) '' to HT
CC62 FF      C      db 11111111b ; scancode 16 (10h) - 23 (17h) 'q' to 't'
CC63 C3      C      db 11000011b ; scancode 24 (18h) - 31 (1Fh) 'a' & 'p' to 'A' & 'A'
CC64 FE      C      db 11111110b ; scancode 32 (20h) - 39 (27h) 'd' to 'l' & 'l'
CC65 0F      C      db 00001111b ; scancode 40 (28h) - 47 (2Fh) '' to '' to 't' to 't'
CC66 E0      C      db 11100000b ; scancode 48 (30h) - 55 (37h) 'b' to 'm' to 'l' to 'h'
C      ;-----
C      ;      Alphabetic (Migratory) |O|I|W|E|U| |
C      ;      | K8 | K8a |
C      ;-----
CC67      C      kb_data_table label byte
CC67 1B1B      C      dw (1Bh) * 100h + (1Bh) ; 01 01h ESC ESC (BASE)
CC69 1B1B      C      dw (1Bh) * 100h + (1Bh) ; ESC ESC (SHIFT)
CC5B 1B1B      C      dw (1Bh) * 100h + (1Bh) ; ESC ESC (CTL)
CC6D CD0C      C      dw kNONE * 100h + kNONE ; None None (ALT)

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# ROM BIOS Listing

CC6F	3131	C	dw	(31h) * 100h + (31h)	:	02	02h	1	1
CC71	2121	C	dw	(21h) * 100h + (21h)	:			1	1
CC73	CBCD	C	dw	kNONE * 100h + kNONE	:			None	None
CC75	7800	C	dw	7800h	:			X120	
CC77	3232	C	dw	(32h) * 100h + (32h)	:	03	03h	2	2
CC79	2240	C	dw	(22h) * 100h + (20h)	:			#	#
CC7B	CDCD	C	dw	kNONE * 100h + kbnul	:			None	NUL=X03(^#)
CC7D	7900	C	dw	7900h	:			X121	
CC7F	3333	C	dw	(33h) * 100h + (33h)	:	04	04h	3	3
CC81	2323	C	dw	(23h) * 100h + (23h)	:			#	#
CC83	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None
CC85	7A00	C	dw	7A00h	:			X122	
CC87	3434	C	dw	(34h) * 100h + (34h)	:	05	05h	4	4
CC89	2424	C	dw	(24h) * 100h + (24h)	:			#	#
CC8B	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None
CC8D	7800	C	dw	7800h	:			X123	
CC8F	3535	C	dw	(35h) * 100h + (35h)	:	06	06h	5	5
CC91	2525	C	dw	(25h) * 100h + (25h)	:			#	#
CC93	CDCB	C	dw	kNONE * 100h + kNONE	:			None	None
CC95	7C00	C	dw	7C00h	:			X124	
CC97	3636	C	dw	(36h) * 100h + (36h)	:	07	07h	6	6
CC99	2652	C	dw	(26h) * 100h + (52h)	:			#	#
CC9B	CD1E	C	dw	kNONE * 100h + (1Eh)	:			None	RS (**)
CC9D	7D00	C	dw	7D00h	:			X125	
CC9F	3737	C	dw	(37h) * 100h + (37h)	:	08	08h	7	7
CCA1	2726	C	dw	(27h) * 100h + (26h)	:			#	#
CCA3	CDCB	C	dw	kNONE * 100h + kNONE	:			None	None
CCA5	7800	C	dw	7800h	:			X126	
CCA7	3838	C	dw	(38h) * 100h + (38h)	:	09	09h	8	8
CCA9	282A	C	dw	(28h) * 100h + (2Ah)	:			(	(
CCAB	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None
CCAD	7F00	C	dw	7F00h	:			X127	
CCAF	3939	C	dw	(39h) * 100h + (39h)	:	10	0Ah	9	9
CCB1	2928	C	dw	(29h) * 100h + (28h)	:			(	(
CCB3	C0C0	C	dw	kNONE * 100h + kNONE	:			None	None
CCB5	8000	C	dw	8000h	:			X128	
CCB7	3030	C	dw	(30h) * 100h + (30h)	:	11	0Bh	0	0
CCB9	5F29	C	dw	(5Fh) * 100h + (29h)	:			US (_)	None
CCBB	1FCD	C	dw	(1Fh) * 100h + kNONE	:			X129	
CCBD	8100	C	dw	8100h	:			-	-
CCBF	2B2D	C	dw	(2Dh) * 100h + (2Bh)	:	12	0Ch	=	=
CCC1	3D5F	C	dw	(3Dh) * 100h + (5Fh)	:			None	US (_)
CCC3	C01F	C	dw	kNONE * 100h + (1Fh)	:			X130	
CCC5	8200	C	dw	8200h	:			=	=
CCC7	583D	C	dw	(58h) * 100h + (3Dh)	:	13	0Dh	=	=
CCC9	782B	C	dw	(78h) * 100h + (2Bh)	:			+	+
CCCB	18CD	C	dw	(18h) * 100h + kNONE	:			RS (**)	None
CCCD	8300	C	dw	8300h	:			X131	
CCCF	0808	C	dw	(08h) * 100h + (08h)	:	14	0Eh	BS	BS
CCD1	0808	C	dw	(08h) * 100h + (08h)	:			BS	BS
CCD3	7F7F	C	dw	(7Fh) * 100h + (7Fh)	:			DEL	DEL
CCD5	CBCD	C	dw	kNONE * 100h + kNONE	:			None	None
CCD7	0959	C	dw	(09h) * 100h + (09h)	:	15	0Fh	HT	HT
CCD9	0F00	C	dw	0F00h	:			BHT=X15	
CCDB	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None
CCDD	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None
CCDF	7171	C	dw	(71h) * 100h + (71h)	:	16	10h	Q	Q
CCE1	5151	C	dw	(51h) * 100h + (51h)	:			Q	Q
CCE3	1111	C	dw	(11h) * 100h + (11h)	:			DC1(^Q) DC1(^Q)	
CCE5	1000	C	dw	1000h	:			X16	
CCE7	7777	C	dw	(77h) * 100h + (77h)	:	17	11h	W	W
CCE9	5757	C	dw	(57h) * 100h + (57h)	:			W	W
CCEB	1717	C	dw	(17h) * 100h + (17h)	:			ETB(^W) ETB(^W)	
CCED	1100	C	dw	1100h	:			X17	
CCEF	6565	C	dw	(65h) * 100h + (65h)	:	18	12h	e	e
CCF1	4545	C	dw	(45h) * 100h + (45h)	:			E	E
CCF3	0505	C	dw	(05h) * 100h + (05h)	:			ENQ(^E) ENQ(^E)	
CCF5	1200	C	dw	1200h	:			X18	
CCF7	7272	C	dw	(72h) * 100h + (72h)	:	19	13h	r	r
CCF9	5252	C	dw	(52h) * 100h + (52h)	:			R	R
CCFB	1212	C	dw	(12h) * 100h + (12h)	:			DC2(^R) DC2(^R)	
CCFD	1300	C	dw	1300h	:			X19	
CCFF	7474	C	dw	(74h) * 100h + (74h)	:	20	14h	t	t
CD01	5454	C	dw	(54h) * 100h + (54h)	:			T	T
CD03	1414	C	dw	(14h) * 100h + (14h)	:			DC4(^T) DC4(^T)	
CD05	1400	C	dw	1400h	:			X20	
CD07	7979	C	dw	(79h) * 100h + (79h)	:	21	15h	y	y
CD09	5959	C	dw	(59h) * 100h + (59h)	:			Y	Y
CD0B	1919	C	dw	(19h) * 100h + (19h)	:			EM(^Y) EM(^Y)	
CD0D	1500	C	dw	1500h	:			X21	
CD0F	7575	C	dw	(75h) * 100h + (75h)	:	22	16h	u	u
CD11	5555	C	dw	(55h) * 100h + (55h)	:			U	U
CD13	1515	C	dw	(15h) * 100h + (15h)	:			NAK(^U) NAK(^U)	
CD15	1600	C	dw	1600h	:			X22	
CD17	6969	C	dw	(69h) * 100h + (69h)	:	23	17h	1	1
CD19	4949	C	dw	(49h) * 100h + (49h)	:			I	I
CD1B	0909	C	dw	(09h) * 100h + (09h)	:			HT(^I) HT(^I)	
CD1D	1700	C	dw	1700h	:			X23	
CD1F	6F6F	C	dw	(6Fh) * 100h + (6Fh)	:	24	18h	o	o
CD21	4F4F	C	dw	(4Fh) * 100h + (4Fh)	:			0	0
CD23	0F0F	C	dw	(0Fh) * 100h + (0Fh)	:			SI(^O) SI(^O)	
CD25	1800	C	dw	1800h	:			X24	
CD27	7070	C	dw	(70h) * 100h + (70h)	:	25	19h	p	p
CD29	5050	C	dw	(50h) * 100h + (50h)	:			P	P
CD2B	1010	C	dw	(10h) * 100h + (10h)	:			DLE(^P) DLE(^P)	
CD2D	1900	C	dw	1900h	:			X25	
CD2F	405B	C	dw	(40h) * 100h + (5Bh)	:	26	1Ah	#	[
CD31	607B	C	dw	(60h) * 100h + (7Bh)	:			[	[
CD33	CC1B	C	dw	kbnul * 100h + (1Bh)	:			NUL=X03(^#) ESC(^I)	
CD35	CDCD	C	dw	kNONE * 100h + kNONE	:			None	None



# ROM BIOS Listing

CD37 5B5D	C	dw	(5Bh) * 100h + (5Dh)	;	27 1Bh	[	]
CD39 7B7D	C	dw	(7Bh) * 100h + (7Dh)	;		[	]
CD3B 1B1D	C	dw	(1Bh) * 100h + (1Dh)	;		ESC('^) GS (^)	
CD3D CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CD3F 0D0D	C	dw	(0Dh) * 100h + (0Dh)	;	28 1Ch	CR	CR
CD41 0D0D	C	dw	(0Dh) * 100h + (0Dh)	;		CR	CR
CD43 0A0A	C	dw	(6Ah) * 100h + (0Ah)	;		LF	LF
CD45 CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CD47 C5C5	C	dw	kb0t1 * 100h + kb0t1	;	29 1Dh	Ctrl	Ctrl
CD49 C5C5	C	dw	kb0t1 * 100h + kb0t1	;		Ctrl	Ctrl
CD4B C5C5	C	dw	kb0t1 * 100h + kb0t1	;		Ctrl	Ctrl
CD4D C5C5	C	dw	kb0t1 * 100h + kb0t1	;		Ctrl	Ctrl
CD4F 6161	C	dw	(61h) * 100h + (61h)	;	30 1Eh	a	a
CD51 8181	C	dw	(81h) * 100h + (81h)	;		A	A
CD53 0101	C	dw	(01h) * 100h + (01h)	;		SOH('^A) SOH('^A)	
CD55 1800	C	dw	1800h	;		X30	
CD57 7373	C	dw	(73h) * 100h + (73h)	;	31 1Fh	s	s
CD59 5353	C	dw	(53h) * 100h + (53h)	;		S	S
CD5B 1313	C	dw	(13h) * 100h + (13h)	;		DC3('^S) DC3('^S)	
CD5D 1F00	C	dw	1F00h	;		X31	
CD5F 6464	C	dw	(64h) * 100h + (64h)	;	32 20h	d	d
CD61 4444	C	dw	(44h) * 100h + (44h)	;		D	D
CD63 0404	C	dw	(04h) * 100h + (04h)	;		ROT('^D) ROT('^D)	
CD65 2000	C	dw	2000h	;		X32	
CD67 6666	C	dw	(66h) * 100h + (66h)	;	33 21h	f	f
CD69 4646	C	dw	(46h) * 100h + (46h)	;		F	F
CD6B 0606	C	dw	(06h) * 100h + (06h)	;		ACK('^P) ACK('^P)	
CD6D 2100	C	dw	2100h	;		X33	
CD6F 6767	C	dw	(67h) * 100h + (67h)	;	34 22h	g	g
CD71 4747	C	dw	(47h) * 100h + (47h)	;		G	G
CD73 0707	C	dw	(07h) * 100h + (07h)	;		BEL('^O) BEL('^O)	
CD75 2200	C	dw	2200h	;		X34	
CD77 6868	C	dw	(68h) * 100h + (68h)	;	35 23h	h	h
CD79 4848	C	dw	(48h) * 100h + (48h)	;		H	H
CD7B 0808	C	dw	(08h) * 100h + (08h)	;		BS('^H) BS('^H)	
CD7D 2300	C	dw	2300h	;		X35	
CD7F 6A6A	C	dw	(6Ah) * 100h + (6Ah)	;	36 24h	j	j
CD81 4A4A	C	dw	(4Ah) * 100h + (4Ah)	;		J	J
CD83 0A0A	C	dw	(0Ah) * 100h + (0Ah)	;		LF('^J) LF('^J)	
CD85 2400	C	dw	2400h	;		X36	
CD87 68B8	C	dw	(6Bh) * 100h + (6Bh)	;	37 25h	k	k
CD89 48B8	C	dw	(4Bh) * 100h + (4Bh)	;		K	K
CD8B 0808	C	dw	(0Bh) * 100h + (0Bh)	;		VT('^X) VT('^X)	
CD8D 2500	C	dw	2500h	;		X37	
CD8F 6C6C	C	dw	(6Ch) * 100h + (6Ch)	;	38 26h	l	l
CD91 8C8C	C	dw	(8Ch) * 100h + (8Ch)	;		L	L
CD93 0C0C	C	dw	(0Ch) * 100h + (0Ch)	;		PF('^L) PF('^L)	
CD95 2600	C	dw	2600h	;		X38	
CD97 3B3B	C	dw	(3Bh) * 100h + (3Bh)	;	39 27h	:	:
CD99 2B3A	C	dw	(2Bh) * 100h + (3Ah)	;		:	:
CD9B CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CD9D CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CD9F 3A27	C	dw	(3Ah) * 100h + (27h)	;	40 28h	:	:
CDA1 2A22	C	dw	(2Ah) * 100h + (22h)	;		#	#
CDA3 CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CDA5 CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CDAD 5D60	C	dw	(5Dh) * 100h + (60h)	;	41 29h	]	-
CDAD 7D7E	C	dw	(7Dh) * 100h + (7Eh)	;		] -	
CDAB 19CD	C	dw	(19h) * 100h + kNONE	;		GS (^)] None	
CDAD CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CDAF C6C6	C	dw	kblsh * 100h + kblsh	;	42 2Ah	LShft	LShft
CDB1 C6C6	C	dw	kblsh * 100h + kblsh	;		LShft	LShft
CDB3 C6C6	C	dw	kblsh * 100h + kblsh	;		LShft	LShft
CDB5 C6C6	C	dw	kblsh * 100h + kblsh	;		LShft	LShft
CDB7 5C5C	C	dw	(5Ch) * 100h + (5Ch)	;	43 2Bh	\	\
CDB9 7C7C	C	dw	(7Ch) * 100h + (7Ch)	;		\	\
CDDB 1C1C	C	dw	(1Ch) * 100h + (1Ch)	;		FS (^\) FS (^\)	
CDDB CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CDDB 7A7A	C	dw	(7Ah) * 100h + (7Ah)	;	44 2Ch	z	z
CDDB 5A5A	C	dw	(5Ah) * 100h + (5Ah)	;		Z	Z
CDDB 1A1A	C	dw	(1Ah) * 100h + (1Ah)	;		SUB('^Z) SUB('^Z)	
CDDB 2C00	C	dw	2C00h	;		X44	
CDDB 7878	C	dw	(78h) * 100h + (78h)	;	45 2Dh	x	x
CDDB 5858	C	dw	(58h) * 100h + (58h)	;		XAN('^X) XAN('^X)	
CDDB 1818	C	dw	(18h) * 100h + (18h)	;		X45	
CDDB 6363	C	dw	(63h) * 100h + (63h)	;	46 2Eh	o	o
CDDB 4343	C	dw	(43h) * 100h + (43h)	;		C	C
CDDB 0303	C	dw	(03h) * 100h + (03h)	;		STX('^C) STX('^C)	
CDDB 2800	C	dw	2800h	;		X46	
CDDB 7676	C	dw	(76h) * 100h + (76h)	;	47 2Fh	v	v
CDDB 5656	C	dw	(56h) * 100h + (56h)	;		V	V
CDDB 1616	C	dw	(16h) * 100h + (16h)	;		STW('^V) STW('^V)	
CDDB 2F00	C	dw	2F00h	;		X47	
CDDB 6262	C	dw	(62h) * 100h + (62h)	;	48 30h	b	b
CDDB 4242	C	dw	(42h) * 100h + (42h)	;		B	B
CDDB 0202	C	dw	(02h) * 100h + (02h)	;		STX('^B) STX('^B)	
CDDB 3000	C	dw	3000h	;		X48	
CDDB 68E8	C	dw	(6Eh) * 100h + (6Eh)	;	49 31h	n	n
CDDB 48E8	C	dw	(8Eh) * 100h + (8Eh)	;		N	N
CDDB 08E8	C	dw	(0Eh) * 100h + (0Eh)	;		SO (^N) SO (^N)	
CDDB 3100	C	dw	3100h	;		X49	
CDDB 6D6D	C	dw	(6Dh) * 100h + (6Dh)	;	50 32h	m	m
CDDB 4D4D	C	dw	(4Dh) * 100h + (4Dh)	;		M	M
CDDB 0D4D	C	dw	(0Dh) * 100h + (0Dh)	;		CR (^M) CR (^M)	
CDDB 3200	C	dw	3200h	;		X50	
CDDB 2C2C	C	dw	(2Ch) * 100h + (2Ch)	;	51 33h	<	<
CDDB 3C3C	C	dw	(3Ch) * 100h + (3Ch)	;		<	<
CDDB CDCD	C	dw	kNONE * 100h + kNONE	;		None	None
CDDB CDCD	C	dw	kNONE * 100h + kNONE	;		None	None

# ROM BIOS Listing

CE0F	2E2E	C	dw	(2Eh) * 100h + (2Eh)	52 34h	.	.
CE01	3E3E	C	dw	(3Eh) * 100h + (3Eh)	;	>	>
CE03	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CE05	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CE07	2F2F	C	dw	(2Fh) * 100h + (2Fh)	53 35h	/	/
CE09	3F3F	C	dw	(3Fh) * 100h + (3Fh)	;	?	?
CE0B	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CE0D	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
-----							
		C	Alphabetic (Non-Migratory)			Olivetti   Other	
		C				KB   KBs	
-----							
CE0F	CTC7	C	dw	kbrsh * 100h + kbrsh	54 36h	RSht	RSht
CE11	CTC7	C	dw	kbrsh * 100h + kbrsh	;	RSht	RSht
CE13	CTC7	C	dw	kbrsh * 100h + kbrsh	;	RSht	RSht
CE15	CTC7	C	dw	kbrsh * 100h + kbrsh	;	RSht	RSht
CE17	242A	C	dw	(24h) * 100h + (24h)	55 37h	#	#
CE19	C8C8	C	dw	kbprt * 100h + kbprt	;	PrtSc	PrtSc
CE1B	7200	C	dw	kNONE * 100h + kNONE	;	X114	None
CE1D	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CE1F	C8C8	C	dw	kbal1 * 100h + kbal1	56 38h	ALT	ALT
CE21	C8C8	C	dw	kbal1 * 100h + kbal1	;	ALT	ALT
CE23	C8C8	C	dw	kbal1 * 100h + kbal1	;	ALT	ALT
CE25	C8C8	C	dw	kbal1 * 100h + kbal1	;	ALT	ALT
CE27	2020	C	dw	(20h) * 100h + (20h)	57 39h	SP	SP
CE29	2020	C	dw	(20h) * 100h + (20h)	;	SP	SP
CE2B	2020	C	dw	(20h) * 100h + (20h)	;	SP	SP
CE2D	2020	C	dw	(20h) * 100h + (20h)	;	SP	SP
CE2F	C1C1	C	dw	kbcap * 100h + kbcap	58 3Ah	CapLk	CapLk
CE31	C1C1	C	dw	kbcap * 100h + kbcap	;	CapLk	CapLk
CE33	C1C1	C	dw	kbcap * 100h + kbcap	;	CapLk	CapLk
CE35	C1C1	C	dw	kbcap * 100h + kbcap	;	CapLk	CapLk
CE37	3800	C	dw	3800h	59 3Bh	F01=X59	
CE39	5800	C	dw	5800h	;	F11=X84	
CE3B	5800	C	dw	5800h	;	F21=X94	
CE3D	6800	C	dw	6800h	;	F31=X104	
CE3F	3C00	C	dw	3C00h	60 3Ch	F02=X60	
CE41	5900	C	dw	5900h	;	F12=X85	
CE43	5F00	C	dw	5F00h	;	F22=X95	
CE45	6900	C	dw	6900h	;	F32=X105	
CE47	3D00	C	dw	3D00h	61 3Dh	F03=X61	
CE49	5600	C	dw	5600h	;	F13=X86	
CE4B	6000	C	dw	6000h	;	F23=X96	
CE4D	6A00	C	dw	6A00h	;	F33=X106	
CE4F	3800	C	dw	3800h	62 3Eh	F04=X62	
CE51	5700	C	dw	5700h	;	F14=X87	
CE53	6100	C	dw	6100h	;	F24=X97	
CE55	6800	C	dw	6800h	;	F34=X107	
CE57	3F00	C	dw	3F00h	63 3Fh	F05=X63	
CE59	5800	C	dw	5800h	;	F15=X88	
CE5B	6200	C	dw	6200h	;	F25=X98	
CE5D	6C00	C	dw	6C00h	;	F35=X108	
CE5F	4000	C	dw	4000h	64 40h	F06=X64	
CE61	5900	C	dw	5900h	;	F16=X89	
CE63	6300	C	dw	6300h	;	F26=X99	
CE65	6000	C	dw	6000h	;	F36=X109	
CE67	4100	C	dw	4100h	65 41h	F07=X65	
CE69	5A00	C	dw	5A00h	;	F17=X90	
CE6B	6400	C	dw	6400h	;	F27=X100	
CE6D	6E00	C	dw	6E00h	;	F37=X110	
CE6F	4200	C	dw	4200h	66 42h	F08=X66	
CE71	5800	C	dw	5800h	;	F18=X91	
CE73	6500	C	dw	6500h	;	F28=X101	
CE75	6F00	C	dw	6F00h	;	F38=X111	
CE77	4300	C	dw	4300h	67 43h	F09=X67	
CE79	5C00	C	dw	5C00h	;	F19=X92	
CE7B	6600	C	dw	6600h	;	F29=X102	
CE7D	7000	C	dw	7000h	;	F39=X112	
CE7F	4400	C	dw	4400h	68 44h	F10=X68	
CE81	5900	C	dw	5900h	;	F20=X93	
CE83	6700	C	dw	6700h	;	F30=X103	
CE85	7100	C	dw	7100h	;	F40=X113	
CE87	C2C2	C	dw	kbnun * 100h + kbnun	69 45h	NumLk	NumLk
CE89	C2C2	C	dw	kbnun * 100h + kbnun	;	NumLk	NumLk
CE8B	C8C8	C	dw	pause * 100h + pause	;	Pause	Pause
CE8D	C2C2	C	dw	kbnun * 100h + kbnun	;	NumLk	NumLk
CE8F	C3C3	C	dw	kbscr * 100h + kbscr	70 46h	SerLk	SerLk
CE91	C3C3	C	dw	kbscr * 100h + kbscr	;	SerLk	SerLk
CE93	C9C9	C	dw	kbrbk * 100h + kbrbk	;	Break	Break
CE95	C3C3	C	dw	kbscr * 100h + kbscr	;	SerLk	SerLk
-----							
		C	Numeric Keypad			Olivetti   Other	
		C				KB   KBs	
-----							
CE97	4700	C	dw	4700h	71 47h	Home=X71	
CE99	3737	C	dw	(37h) * 100h + (37h)	;	7	7
CE9B	7700	C	dw	7700h	;	X119	
CE9D	D0D0	C	dw	kdec7 * 100h + kdec7	;	XDec7	XDec7
CE9F	4800	C	dw	4800h	72 48h	Up =X72	
CEA1	3838	C	dw	(38h) * 100h + (38h)	;	8	8
CEA3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEA5	FCFC	C	dw	kdec8 * 100h + kdec8	;	XDec8	XDec8
CEA7	4900	C	dw	4900h	73 49h	F80=X73	
CEA9	3339	C	dw	(39h) * 100h + (39h)	;	9	9
CEAB	8400	C	dw	8400h	;	X132	
CEAD	CECE	C	dw	kdec9 * 100h + kdec9	;	XDec9	XDec9

# ROM BIOS Listing

CEAF	2B2D	C	dw	(2Dh) * 100h + (2Dh)	74 4Ah	-	-
CEB1	2B2D	C	dw	(2Dh) * 100h + (2Dh)	;	-	-
CEB3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEB5	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEB7	4B00	C	dw	4B00h	75 4Bh	Left=X75	
CEB9	3434	C	dw	(34h) * 100h + (34h)	;	4	4
CEBB	7300	C	dw	7300h	;	X115	
CEBD	D3D3	C	dw	kdec4 * 100h + kdec4	;	XDec4	XDec4
CEBF	CDCD	C	dw	kNONE * 100h + kNONE	76 4Ch	None	None
CEC1	3535	C	dw	(35h) * 100h + (35h)	;	5	5
CEC3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEC5	D2D2	C	dw	kdec5 * 100h + kdec5	;	XDec5	XDec5
CEC7	4D00	C	dw	4D00h	77 4Dh	Rght=X77	
CEC9	3636	C	dw	(36h) * 100h + (36h)	;	6	6
CECB	7400	C	dw	7400h	;	X116	
CECD	D1D1	C	dw	kdec6 * 100h + kdec6	;	XDec6	XDec6
CECF	2B2B	C	dw	(2Bh) * 100h + (2Bh)	78 4Eh	+	+
CED1	2B2B	C	dw	(2Bh) * 100h + (2Bh)	;	None	None
CED3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CED5	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CED7	4F00	C	dw	4F00h	79 4Fh	End=X79	
CED9	3131	C	dw	(31h) * 100h + (31h)	;	1	1
CEDB	7500	C	dw	7500h	;	X117	
CEDD	D6D6	C	dw	kdec1 * 100h + kdec1	;	XDec1	XDec1
CEDF	5000	C	dw	5000h	80 50h	Down=X80	
CEE1	3232	C	dw	(32h) * 100h + (32h)	;	2	2
CEE3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEE5	D5D5	C	dw	kdec2 * 100h + kdec2	;	XDec2	XDec2
CEE7	5100	C	dw	5100h	81 51h	PgDn=X81	
CEE9	3333	C	dw	(33h) * 100h + (33h)	;	3	3
CEEB	7600	C	dw	7600h	;	X118	
CEED	D4D4	C	dw	kdec3 * 100h + kdec3	;	XDec3	XDec3
CEEF	C0C0	C	dw	kbin4 * 100h + kbin4	82 52h	INS=X82	INS=X82
CEF1	3030	C	dw	(30h) * 100h + (30h)	;	0	0
CEF3	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CEF5	D7D7	C	dw	kdec0 * 100h + kdec0	;	XDec0	XDec0
CEF7	5300	C	dw	5300h	83 53h	DEL=X83	
CEF9	2E2E	C	dw	(2Eh) * 100h + (2Eh)	;	.	.
CEFB	C8C8	C	dw	kbr4 * 100h + kbr4	;	Reset	Reset
CEFD	C8C8	C	dw	kbr4 * 100h + kbr4	;	Reset	Reset
-----							
				Function Keypad		Olivetti   Other	
						KB	Kbs
-----							
CEFF	D8D8	C	dw	kdb10 * 100h + kdb10	84 54h	00	00
CF01	D8D8	C	dw	kdb10 * 100h + kdb10	;	00	00
CF03	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF05	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF07	C8C8	C	dw	kbrprt * 100h + kbrprt	85 55h	PrtSc	PrtSc
CF09	C8C8	C	dw	kbrprt * 100h + kbrprt	;	PrtSc	PrtSc
CF0B	7200	C	dw	7200h	;	X114	
CF0D	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF0F	CACA	C	dw	pause * 100h + pause	86 56h	Pause	Pause
CF11	CACA	C	dw	pause * 100h + pause	;	Pause	Pause
CF13	CACA	C	dw	pause * 100h + pause	;	Pause	Pause
CF15	CACA	C	dw	pause * 100h + pause	;	Pause	Pause
CF17	0D0D	C	dw	(0Dh) * 100h + (0Dh)	87 57h	CR	CR
CF19	0D0D	C	dw	(0Dh) * 100h + (0Dh)	;	CR	CR
CF1B	0A0A	C	dw	(0Ah) * 100h + (0Ah)	;	LF	LF
CF1D	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF1F	4B00	C	dw	4B00h	88 58h	Left=X75	
CF21	7300	C	dw	7300h	;	Rev Word = X115	
CF23	7300	C	dw	7300h	;	Rev Word = X115	
CF25	7300	C	dw	7300h	;	Rev Word = X115	
CF27	5000	C	dw	5000h	89 59h	Down=X80	
CF29	5000	C	dw	5000h	;	Down=X80	
CF2B	5000	C	dw	5000h	;	Down=X80	
CF2D	5000	C	dw	5000h	;	Down=X80	
CF2F	4D00	C	dw	4D00h	90 5Ah	Rght=X77	
CF31	7400	C	dw	7400h	;	Adv Word = X116	
CF33	7400	C	dw	7400h	;	Adv Word = X116	
CF35	7400	C	dw	7400h	;	Adv Word = X116	
CF37	4800	C	dw	4800h	91 5Bh	Up = X72	
CF39	4700	C	dw	4700h	;	Home=X71	
CF3B	4700	C	dw	4700h	;	Home=X71	
CF3D	4700	C	dw	4700h	;	Home=X71	
CF3F	C9C9	C	dw	kbrbrk * 100h + kbrbrk	92 5Ch	Break	Break
CF41	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF43	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF45	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF47	C9C9	C	dw	kbrbrk * 100h + kbrbrk	93 5Dh	Break	Break
CF49	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF4B	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF4D	C9C9	C	dw	kbrbrk * 100h + kbrbrk	;	Break	Break
CF4F	C2C2	C	dw	kbnnum * 100h + kbnnum	94 5Eh	NumLk	NumLk
CF51	C2C2	C	dw	kbnnum * 100h + kbnnum	;	NumLk	NumLk
CF53	CACA	C	dw	pause * 100h + pause	;	Pause	Pause
CF55	C2C2	C	dw	kbnnum * 100h + kbnnum	;	NumLk	NumLk
CF57	2F2F	C	dw	(2Fh) * 100h + (2Fh)	95 5Fh	/	/
CF59	2F2F	C	dw	(2Fh) * 100h + (2Fh)	;	/	/
CF5B	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF5D	CDCD	C	dw	kNONE * 100h + kNONE	;	None	None
CF5F	5400	C	dw	5400h	96 60h	F11=X84	
CF61	5400	C	dw	5400h	;	F11=X84	
CF63	5400	C	dw	5400h	;	F11=X84	
CF65	5400	C	dw	5400h	;	F11=X84	
CF67	5500	C	dw	5500h	97 61h	F12=X85	
CF69	5500	C	dw	5500h	;	F12=X85	

# ROM BIOS Listing

```

CF6B 5500      C dw 5500h      ;          F12=X85
CF6D 5500      C dw 5500h      ;          F12=X85
CF6F 5600      C dw 5600h      ; 98 62h   F13=X86
CF71 5600      C dw 5600h      ;          F13=X86
CF73 5600      C dw 5600h      ;          F13=X86
CF75 5600      C dw 5600h      ;          F13=X86
CF77 5700      C dw 5700h      ; 99 63h   F14=X87
CF79 5700      C dw 5700h      ;          F14=X87
CF7B 5700      C dw 5700h      ;          F14=X87
CF7D 5700      C dw 5700h      ;          F14=X87
CF7F 5800      C dw 5800h      ; 100 64h  F15=X88
CF81 5800      C dw 5800h      ;          F15=X88
CF83 5800      C dw 5800h      ;          F15=X88
CF85 5800      C dw 5800h      ;          F15=X88
CF87 5900      C dw 5900h      ; 101 65h  F16=X89
CF89 5900      C dw 5900h      ;          F16=X89
CF8B 5900      C dw 5900h      ;          F16=X89
CF8D 5900      C dw 5900h      ;          F16=X89
CF8F 5A00      C dw 5A00h      ; 102 66h  F17=X90
CF91 5A00      C dw 5A00h      ;          F17=X90
CF93 5A00      C dw 5A00h      ;          F17=X90
CF95 5A00      C dw 5A00h      ;          F17=X90
CF97 5B00      C dw 5B00h      ; 103 67h  F18=X91
CF99 5B00      C dw 5B00h      ;          F18=X91
CF9B 5B00      C dw 5B00h      ;          F18=X91
CF9D 5B00      C dw 5B00h      ;          F18=X91
CF9F          C
C kb_data1     endp
CF9F          C
C ocode ends
C include hdu.asm
C
C ;
C ;      Filename:      hdu.asm
C ;
C ;      This module includes HDU support.
C ;
C ;
C ;
CF9F          C
C ocode segment public 'ROM'
C assume es:code, ds:nothing, es:nothing
C
C ; ##### COMMANDS AVAILABLE FROM INTERRUPT 13 #####
C
= 0000      C reset_int     equ 00h      ;reset disks (according to drive#) and
C ; assign_param
= 0001      C status_int   equ 01h      ;return status of last operation
C ; (disk_status) in al
= 0002      C read_int     equ 02h      ;read sectors from disk
C ;write_int     equ 03h      ;write sectors to disk
C ;ohktrk_int   equ 04h      ;ohseek track
C ;fattrk_int   equ 05h      ;format track
C ;ftrbad_int   equ 06h      ;format track back
= 0007      C ftrdrv_int   equ 07h      ;format drive starting at the
C ; indicated track
C
C ;read_param_int equ 08h      ;read the current drive parameters
= 0009      C assign_param_int equ 09h      ;assign parameters to drives
C ;rlong_int    equ 0Ah      ;read long (512 data + 4 ecc)
C ;wlong_int    equ 0Bh      ;write long
C ;seek_int     equ 0Ch      ;seek cylinder
C ;reset2_int   equ 0Dh      ;same as 00h
C ;rbuff_int    equ 0Eh      ;read sector buffer
= 000F      C wbuff_int    equ 0Fh      ;write sector buffer
C
= 0010      C tst_drv_rdy_int equ 10h      ;test drive ready
= 0011      C reoal_int    equ 11h      ;reocalibrate drive (seek track 00)
= 0012      C ramingd_int  equ 12h      ;controller ram diagnostic
C ;drvdiaq_int  equ 13h      ;drive diagnostic
= 0014      C hxdiaq_int   equ 14h      ;controller internal diagnostic
= 0014      C max_int      equ 14h      ;maximum interrupt command number
C
C ; ##### INT13 STATUS CODES #####
C
C ; These are put into the disk_status byte in data_seg when there is an error.
C
= 0007      C ;reset_err    equ 05h      ;disk reset (int13-00) failed
= 000B      C ;int_err      equ 07h      ;assign parameter (int13-09) failed
= 000D      C ;badtrack_err equ 0Bh      ;bad track
= 0011      C ;ecc_used_err equ 11h      ;ecc used to correct data
= 00FF      C ;sense_err    equ 0Fh      ;request sense failed
C
C ; ##### CONTROLLER INFORMATION #####
C
C ; drives_per_bx equ 2          ;max number of drives on a controller
C ; drives_per_pc  equ 8          ;max number of drives on a pc
C ; bxes_per_pc    equ 4          ;max number of bxes on a pc
C ; ports_per_bx   equ 4          ;number of i/o ports for a controller
= 0011      C sectors_per_track equ 17      ;compatible fixed format
C
C ; ##### CONTROLLER PORTS #####
C
= 0320      C read_port     equ 320h      ;read data port
= 0320      C write_port    equ 320h      ;write data port
= 0320      C status_port   equ 321h      ;read controller hardware status
= 0321      C reset_port    equ 321h      ;write to reset controller hardware
= 0322      C switch_port   equ 322h      ;read the drivetype switches
= 0322      C select_port   equ 322h      ;write to select controller

```

```

= 0323      C mask_port      equ    323h          ;write to mask_p_dma and interrupts
C
C ; ##### CONTROLLER REGISTER BITS #####
C
C ; This is the completion status byte received in the read_port after
C ; command completion.
C
C ;completion_status:
= 0002      C ; h_o_drive      equ    0E0h          ; bits #7 to 5
C ; h_o_err        equ    002h          ; bit #1
C
C ; This is the controller hardware status read from status_port.
C
= 0020      C ;hdu_status:
C ; hdu_irq5       equ    020h          ; bit #5
= 0008      C ; hdu_dreq3      equ    010h          ; bit #4
= 0004      C ; hdu_bay        equ    008h          ; bit #3
= 0002      C ; hdu_cd         equ    008h          ; bit #2
= 0001      C ; hdu_io         equ    002h          ; bit #1
C ; hdu_req        equ    001h          ; bit #0
C
C ; This is the controller p_dma and interrupt mask written to mask_port.
C
= 0002      C ;mask_port_cmd: mask_port_bank equ    008h          ; bit #3
= 0001      C ; mask_port_inte equ    002h          ; bit #1
C ; mask_port_dmae equ    001h          ; bit #0
C
C ; These are the bits for a drive in the switch.
C
C ; switch_mask    equ    00110011b
C
C ; ##### CONTROLLER COMMANDS #####
C
C ; The first byte of the cmd_block (CDB) is the controller command.
C ; The upper 3 bits are the class (either 0 or 7, all reset or all set).
C ; The lower 5 bits are the opcode (0 to 31).
C
C ; odb_0          record class:3, opcode:5
C
C ; Class 0 Controller Commands: 0007?????.
C
= 0000      C ; tat_drv_rdy_bx equ    00h
= 0001      C ; read_bx        equ    01h
C ; reserved      equ    02h
= 0003      C ; sense_bx       equ    03h
= 0004      C ; fatdrv_bx      equ    04h
= 0005      C ; chktrk_bx     equ    05h
= 0006      C ; fattrk_bx     equ    06h
= 0007      C ; fatbad_bx     equ    07h
= 0008      C ; read_bx       equ    08h
C ; Reserved      equ    09h
= 000A      C ; write_bx      equ    0Ah
= 000B      C ; seek_bx       equ    0Bh
= 000C      C ; assign_param_bx equ    0Ch
= 000D      C ; read_sec_bx   equ    0Dh
= 000E      C ; rbuff_bx      equ    0Eh
= 000F      C ; wbuff_bx      equ    0Fh
C
C ; Class 7 Controller Commands: 111??????.
C
= 0080      C ; randing_bx    equ    0E0h
C ; reserved      equ    0E1h
C ; reserved      equ    0E2h
= 00E3      C ; drvdiag_bx   equ    0E3h
= 00E4      C ; bxdiag_bx    equ    0E4h
= 00E5      C ; rlong_bx     equ    0E5h
= 00E6      C ; wlong_bx     equ    0E6h
C
C ; ##### CONTROLLER CDB BYTES #####
C
C ; The remainder of the cmd_block bytes (CDB) are defined as follows:
C
C ; odb_1 record zsf:2, drivenum:1, headnum:5
C
C ; odb_2          record cylhi:2, secnum:6
C
C ; odb_3          record cylinder:8
C
C ; odb_4          record zsf:3, interleave:5
C
C ; odb_5          record retry:1, use_sec:1, zsg:3, stepcode:3
C
C ; ##### SENSE BYTES FOR REQUEST SENSE COMMAND #####
C
C ; Bytes returned when a Request sense command is issued in response to an error.
C
C ; sense0:       sense0_val_addr equ    080h          ; bit #7
C ; sense0_type    equ    030h          ; bits #5 & 4
C ; sense0_code    equ    00Fh          ; bits #3 to 0
= 003F      C ; sense0_mask    equ    03Fh          ; sense0_type+sense0_code
C
C ; sense1:       sense1_drive      equ    020h          ; bit #5
C ; sense1_head    equ    01Fh          ; bits #4 to 0
C
C ; sense2:       sense2_cylhi      equ    0C0h          ; bits #7 & 6
C ; sense2_sector  equ    03Fh          ; bit #5 to 0
C
C ; sense3:       sense2_cylinder    equ    0FFh          ; bits #7 to 0
C
C ; ##### HARD DISK PARAMETER TABLE #####

```

# ROM BIOS Listing

```

C
C ; This is a table which is indexed by the switch settings to determine
C ; the parameters for each drive.
C
C parameter_table struc
C
0000 0132 C p_cyls dw 306d ;number of cylinders
0002 04 C p_heads db 4d ;number of heads
0003 0132 C p_write_cur dw 306d ;reduced write current
0005 0000 C p_precomp dw 0d ;write precompensation
0007 08 C p_sec_len db 11d ;maximum sec burst length
0008 05 C p_control_byte db 5d ;enable retry, enable eec, 70usec steps
0009 0C C p_timeout db 0ch ;standard timeout
000A B4 C p_fat_timeout db 0b4h ;timeout for format drive
000B 28 C p_drvdiag_timeout db 028h ;timeout for test drive ready
000C 00 00 00 00 C p_ss[] db 0,0,0,0
0010 C parameter_table ends
C
C ; ##### p_dma SYSTEM (8237) #####
C
= 0047 C read_mode equ 0100011b ;write to dma_mode
C ;7:6 single mode
C ;5:5 address incorment
C ;4:4 autointn disable
C ;3:2 read
C ;1:0 channel 3
C
= 004B C write_mode equ 01001011b ;write to dma_mode
C ;7:6 single mode
C ;5:5 address incorment
C ;4:4 autointn disable
C ;3:2 write
C ;1:0 channel 3
C
= 0003 C allow_dma3 equ 00000011b ;write to dma_mask_bit to allow
= 0007 C disallow_dma3 equ 00000111b ;or disallow_dma3 interrupt
= 0082 C hdu_dma_seg equ 082h ;port sets top 4 bits of 20-bit p_dma address
C
C ; ##### MACROS #####
C
C ; Input to a register from a port.
C ; Won't work when the index has to cause a carry to high byte.
C
C inport macro inrg,inpt
C mov dx,inpt ;get the port number for the base controller
C add dl,byte ptr ds:[port_off] ;add port_off for the correct bx
C in inrg,dx
C endm
C
C ; Output from a register to a port.
C ; Ditto.
C
C outport macro outpt,outrg
C mov dx,outpt ;get the port number for the base controller
C add dl,byte ptr ds:[port_off] ;add port_off for the correct bx
C out dx,outrg
C endm
C
C ;===== hd2.asm =====
C ; Power on self test
C ;=====
C
C assume cs:code, ds:nothing, es:nothing, ss:nothing
C
CF9F h_init proc near
C
C ; Install vectors.
C
C assume cs:code, ds:abs0, es:abs0, ss:nothing
C
CF9F 33 C0 C xor ax,ax ; satisfy assumptions
CFA1 8E D8 C mov da,ax ; ds = es = ax = abs0_seg
CFA3 8E C0 C mov es,ax
C
CFA5 FA C cll ; disable during critical code.
C
C ; Install HDU hardware interrupt service routine.
C
CFA6 C7 06 003a R D62F R C mov word ptr ds:[int0D10em+0000h],es:(offset h_int)
CFA8 8C 0E 0036 R C mov word ptr ds:[int0D10em+0002h],es
C
C ; Transfer old FDU int 13 vector to the new int 40 FDU location.
C
CFB0 A1 004C R C mov ax,word ptr ds:[int1310em+0000h]
CFB3 A3 0100 C mov word ptr ds:[(4*40h)+0000h],ax
CFB6 A1 004E R C mov ax,word ptr ds:[int1310em+0002h]
CFB9 A3 0102 C mov word ptr ds:[(4*40h)+0002h],ax
C
C ; Install new HDU request int 13 vector.
C
CFBC C7 06 004C R D1AB R C mov word ptr ds:[int1310em+0000h],es:(offset h_1e)
CFC2 8C 0E 004E R C mov word ptr ds:[int1310em+0002h],es
C
C ; Install new HDU boot-strap int 19 vector
C
CFC6 C7 06 0064 R D0E9 R C mov word ptr ds:[int1910em+0000h],es:(offset h_boot)

```

# ROM BIOS Listing

```

CFCC 8C 0E 0066 R      C      mov     word ptr ds:[int19locn+0002h],cs
C      ; Install new int 41 HDU parameter table pointer
C      C
CFDB C7 06 0104 D14B R  C      mov     word ptr ds:[(4*41h)+0000h],cs:(offset hdu_parm_tbl)
CFDE 8C 0E 0106         C      mov     word ptr ds:[(4*41h)+0002h],cs
C      C
CFDA FB                C      sti                     ; exit critical code.
C      C
C      ; Initialize stuff in low memory.
C      C
C      assume cs:code, ds:data, es:abs0, ss:nothing
C      C
CFDB B8 0040           C      mov     ax,data_seg           ; satisfy assumptions.
CFDE 8E D8             C      mov     ds,ax
C      C
CFE0 C6 06 0074 R 00   C      mov     byte ptr ds:[disk_status],0           ; clear errors.
CFE5 C6 06 0075 R 01   C      mov     byte ptr ds:[bf_num],1             ; assume 1 hard disk.
C      C
C      ; Reset the controller.
C      C
CFEA B9 000A         C      mov     cx,10                    ;try to reset controller up to 10 times
CFED                          C      init_controller_lp:
C      C
CFED 8A 16 0075 R     C      mov     dl,byte ptr ds:[bf_num]           ;get the current hd number
CFE1 D0 E2           C      shl     dl,1                          ;make it look like
CFE2 80 E2 FC        C      and     dl,11111100b                 ;an index
CFE3 88 16 0077 R     C      mov     byte ptr ds:[port_off],dl        ;fake for reset_bx
CFE4 E8 D5B1 R       C      call    reset_bx                      ;reset that controller
C      C
C      ; Set up dl to call int13.
C      C
CFFD B6 00           C      mov     dh,0                          ;clear dh
CFFF 8A 16 0075 R     C      mov     dl,byte ptr ds:[bf_num]           ;number of HDUs (incremented in this
D003 FE CA           C      dec     dl                              ; loop)
D005 80 CA 80        C      or      dl,80h                         ;compensate for zero-origin
C      ;flag as a hard disk number
C      C
C      ; Test the controller.
C      C
D008 B4 12           C      mov     ah,randimg_int                ;set up for int13 - controller ram test
D00A CD 13           C      int     13h                            ;
D00C 72 5C           C      jc      post_no_more_drives           ;if error returned
C      C
D00E B4 14           C      mov     ah,bxdimg_int                 ;set up for int13 - controller internal test
C      ; test
D010 CD 13           C      int     13h                            ;
D012 72 56           C      jc      post_no_more_drives           ;if error returned
C      C
C      ; Set up p_timer for timeout of tst_rdy.
C      C
D014 C7 06 006C R 0000 C      mov     word ptr ds:[t_low_order],0*18 ; start counting at zero seconds
C      ; t_low_order counts
C      ; 18times/sec.
C      C
D01A 81 3E 0072 R 1234 C      cmp     word ptr ds:[reset_flag],01234h ; test flag for reset function.
D020 75 06           C      jne     init_start_timer             ; skip if not CTL ALT DEL reboot
C      C
D022                          C      init_drive_lp:
C      C
D022 C7 06 006C R 0132   C      mov     word ptr ds:[t_low_order],17*18 ; only give 3 seconds if
C      ; warm boot or not first disk
C      ; t_low_order counts
C      ; 18times/sec.
C      C
D028                          C      init_start_timer:
C      C
D028 FA             C      cli
D029 EA 21           C      in     al,pic_1                       ; get interrupt mask
D02B 24 FE           C      and     al,0FFh                       ; un-mask p_timer interrupt IRO
D02D B6 21           C      out    al,pic_1,al                   ; set the controller
D02F FB             C      sti
C      C
D030 B4 09           C      mov     ah,assign_param_int           ;assign drive parameters according to
D032 CD 13           C      int     13h                            ;
D034 72 3B           C      jc      post_lose                     ;switch settings on bx board
C      C
D036                          C      init_try_drive:
D036 B4 10           C      mov     ah,tst_drv_rdy_int           ;test drive ready
D038 CD 13           C      int     13h                            ;
D03A 73 0B           C      jnc     init_drive_win                ;
D03C 81 3E 006C R 0168 C      cmp     word ptr ds:[t_low_order],20*18 ; t_low_order counts
C      ; 18times/sec.
D042 72 F2           C      jb     init_try_drive                 ;if not given enough time yet, go back
D044 EB 24 90        C      jmp     post_no_more_drives           ;if given enough time and still losing
C      C
D047                          C      init_drive_win:
D047 B4 11           C      mov     ah,recal_int                 ;recalibrate drive
D0A9 CD 13           C      int     13h                            ;
D0AB 72 24           C      jc      post_lose                     ;
C      C
C      assume es:code
C      C
D0AD 8C C8           C      mov     ax,cs                          ;satisfy assumption
D0AF 8E C0           C      mov     es,ax
D0B1 33 DB           C      xor     bx,bx                          ;initialize offset (es:bx)
C      C

```

# ROM BIOS Listing

```

D053 B4 0F          C      mov     ah,whbuff_int      ;write sector buffer as a test
D055 B0 01          C      mov     al,01                ;one block length
D057 CD 13          C      int     13h
D059 72 16          C      jc      post_lose
C
C      ; Looks like we got another hard disk!
C
D05B FE 06 0075 R   C      inc     byte ptr ds:[hf_num]   ;point to the next one
D05F FE C2          C      inc     dl                    ;register for calling int13
D061 F6 06 0075 R 01 C      test    byte ptr ds:[hf_num],01h ;have we proceeded to a new controller?
D066 74 BA          C      jz      init_drive_lp         ;no, go init second drive on this one
D068 EB 83          C      jmp     init_controller_lp     ;and go back .
C
C      ; Come here when an attempt to initialize a drive or controller fails.
C      ; If (at least) one good controller is found, then continue.
C
D06A FE 0E 0075 R   C      post_no_more_drives:
D06E EB 13 90          C      dec     byte ptr ds:[hf_num]   ;restore hf_num
C
C      jmp     post_win           ; could be FDU system only
C
C      ; Come here if there was clearly an error during initialization.
C
D071 FE 0E 0075 R   C      post_lose:
D071 FE 0E 0075 R   C      dec     byte ptr ds:[hf_num]   ;anticipation disproved
C
C      ; Output an error message
C
C      ;post_message:
D075 BD 000F          C      mov     bp,0fh                ;error flag
D078 BE D0A2 R       C      mov     si,oa:(offset h_bad_m) ;string for error '1701' (HDU)
D07B E8 E5FA R       C      call    D805String            ;display message on screen
D07E E8 D0B8 R       C      call    show_sense           ;display the sense bits
D081 EB 1B          C      jmp     short p_disp
C
D083 FE 06 0075 R   C      post_win:
D083 A0 0075 R       C      mov     al,byte ptr ds:[hf_num] ; number of hard disks.
D086 0A C0          C      or      al,al                 ; are there any fixed disks.
D088 75 08          C      jnz     p_some
C
D08A BE D0AE R       C      mov     si,oa:(offset h_aba_m)  ; message for no HDU
D08D E8 E5FA R       C      call    D805String
D090 EB 09          C      jmp     short p_disp
C
D092 FE 08 E650 R    C      p_some:
D092 E8 E650 R       C      call    DHexNib              ; display the number
C
D095 BE D0A6 R       C      mov     si,oa:(offset h_good_m) ; message for 'HDU'
D098 E8 E5FA R       C      call    D805String
C
D09B E8 E619 R       C      p_disp: call    DCrLf
C
D09E E8 D5FA R       C      call    disable_disk_interrups
D0A1 C3              C      ret
C
D0A2 20 4E 6F 74    C      h_bad_m      db      ' Not'           ; purposely no NUL!!!!
D0A6 20 52 65 61 64 79 C      h_good_m     db      ' Ready ',NUL
D0A2 20 00          C
D0AE 20 4E 6F 74 20 50 C      h_aba_m      db      ' Not Present',NUL
D0A6 72 65 73 65 6E 74 C
D0A6 00          C
C
D0BB h_init endp
D0BB show_sense proc near
C
C      ; Displays the error sense code as (ab), where a is the type and b is the code.
C
D0BB B8 0E28          C      mov     ax,(0Eh*100h)+'('     ;display a '('
D0BE CD 10          C      INT     10h
C
D0C0 A0 0042 R       C      mov     al,byte ptr ds:[hd_error] ;get the error code
D0C3 24 3F          C      and     al,sense0_mask         ;isolate the type and code bits
D0C5 E8 E643 R       C      call    DHexbyte              ;display error type and code
C
D0C8 B8 0E29          C      mov     ax,(0Eh*100h)+'('     ;display a '('
D0CB CD 10          C      INT     10h
C
D0CD C3              C      ret
C
D0CE show_sense endp
D0CE maybe_show_sense proc near
C
C      ; Show sense information if switch 8 is zero (closed) and 6 is one (open).
C      ; To be used for field maintenance.
C
D0CE 50          C      push    ax
D0CF 80 3E 0074 R 00 C      cmp     byte ptr ds:[disk_status],0
D0D4 74 11          C      je      s_exit                ;if no error, do not display
C
C      import s_exit
C      mov     al,switch_port     ;read the switches
C      mov     dx,switch_port     ;get the port number for the base controller
C      add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D0D9 EC          C      in     al,dx
D0DE 24 A0          C      and     al,0A0h
D0E0 3C 80          C      cmp     al,080h
C
C      ;mask switches 8 and 6
C      ;are they =10b?

```



# ROM BIOS Listing

```

DOE2 75 03          C          jne     m_exit
DOE4 EB DOB8 R      C          call    show_sense          ;if so, display sense
DOE7 58             C          m_exit:
DOE8 C3             C          pop     ax                ;back to caller
DOE9               C          maybe_show_sense      endp

C          ;===== hd3.asm          ;=====
C          ; This is called from the ROM Bios after the hard disk has been initialized.
C          ; It attempts to read and initiate a master boot block from logical sector 0 of
C          ; the floppy disk, and then from the hard disk.
C          ;=====

C          assume cs:code, ds:nothing, es:nothing, ss:nothing

DOE9               C          h_boot proc far
C          ; Install vectors.
C          assume cs:code, ds:abs0, es:abs0, ss:nothing
C          xor     ax,ax                ; satisfy assumptions
C          mov     ds,ax                ; ds = es = ax = abs0_seg
C          mov     es,ax
C          ori     ; disable during critical code.
C          ; Install new int 01 HDU parameter table pointer.
DOF0 C7 06 0104 D14B R C          mov     word ptr ds:[(0*41b)+0000h],cs:(offset hdu_parm_tbl)
DOF6 8C 0E 0106     C          mov     word ptr ds:[(4*41b)+0002h],cs
C          ; Install new FDU parameter table pointer.
C          mov     word ptr ds:[int1E0cm+0000h],cs:(offset fd_parms)
C          mov     word ptr ds:[int1E0cm+0002h],cs
DOFA .FB           C          sti                 ; exit critical code.
C          ; Attempt to reset the diskette. Motor startup time requires 3 tries.
C          assume cs:code, ds:data, es:abs0, ss:nothing
C          mov     ax,data_seg          ; satisfy assumptions.
DOFB B8 0040       C          mov     ds,ax
DOFE BE D8         C          mov     cx,3                ; 3 retries
D100 B9 0003       C          mov     dx,0                ; drive number zero (soft disk A:)
D103 B2 00         C          call    boot_a_disk          ;try to boot from floppy
D105 EB D12A R     C          je      b_try_hdu           ;failed - try the hard disk
D108 72 02         C          jmp     short b_ok           ;jump to the boot code if we succeeded
D10A EB 13         C          ; else boot from the hard disk.
C          b_try_hdu:
D10C               C          mov     cx,3                ; 3 retries
D10E B9 0003       C          mov     dx,80h             ;drive number 80h (hard disk C:)
D10F B2 80         C          call    boot_a_disk          ;try to boot from hard disk
D111 EB D12A R     C          je      b_failed           ;if this failed too, then exit.
D114 72 0E         C          cmp     word ptr es:[07C00h+510d],0AA55h ;is it the code?
D116 26 81 3E 7DFE AA55 C          jne     b_failed           ;code tester
D11D 75 05         C          b_ok:
D11F               C          jmp     dword ptr es:[boot_indirect] ;jump to boot code if correct
D11F 2E: FF 2E D126 R C          b_failed:
D124 CD 18         C          int     18h                ; initiate reboot through ROM BASIC INT.
D126 7C00          C          boot_indirect dw 07C00h      ; jump indirect to boot code at 0:7C00
D128 0000          C          dw     abs0_seg
D12A               C          h_boot endp
C          boot_a_disk proc
D12A               C          ; Set d:disk number and call this proc.
C          ; It will reset and try to read cx times (in case there is a read error).
C          ; If it succeeds, it will return with CY=0. If it fails, it will leave CY=1.
C          b_lp:
D12A B4 00         C          mov     ah,reset_int        ;reset the disk
D12C CD 13         C          int     13h
D12E 72 14         C          jc      b_lost             ;if the operation lost
D130 B4 02         C          mov     ah,read_int        ;if it worked, read from the disk
D132 B0 01         C          mov     al,1                ;one sector
D134 BB 7C00       C          mov     bx,07C00h          ;offset for the boot_area.
D137 51           C          push    cx                 ;save the retry count
D138 B5 00         C          mov     ch,0                ;cylinder 0
D13A B1 01         C          mov     cl,1                ;sector 1 (lowest sector)
D13C B6 00         C          mov     dh,0                ;head 0

```

# ROM BIOS Listing

```

D13E CD 13          C          int    13h          ;attempt read
D140 59            C          pop     ox          ;restore retry count
D141 72 01        C          jc     b_lost       ;if it worked, return to caller
D143 C3           C          ret          ;return with no carry
D144             C          b_lost:
D144 80 FC 80      C          cmp     ah,time_out   ;if it was a timeout,
D147 50 E1        C          loopne b_lp         ;otherwise, another chance
D149 F9          C          stc          ;dropped through loop
D14A C3          C          ret          ;return with carry
D14B             C          boot_a_disk  endp
D14B             C
D14B             C          hdu_param_tbl:
D14B             C          ; The next six are the supported drives:
D14B 0132        C          parameter_table <2d,,,00h>      ;type 0: 5mb drive
D14D 02          C
D14E 0132        C
D150 0000        C
D152 0B          C
D153 00          C
D154 0C          C
D155 B4          C
D156 28          C
D157 00 00 00 00 C
D15B 0177        C          parameter_table <375d,8d,375d>    ;type 1: 24mb drive
D15D 08          C
D15E 0177        C
D160 0000        C
D162 0B          C
D163 05          C
D164 0C          C
D165 B4          C
D166 28          C
D167 00 00 00 00 C
D16B 0132        C          parameter_table <6d,128d,256d>    ;type 2: 15mb drive
D16D 06          C
D16E 0080        C
D170 0100        C
D172 0B          C
D173 05          C
D174 0C          C
D175 B4          C
D176 28          C
D177 00 00 00 00 C
D17B 0132        C          parameter_table <>                ;type 3: 10mb drive
D17D 04          C
D17E 0132        C
D180 0000        C
D182 0B          C
D183 05          C
D184 0C          C
D185 B4          C
D186 28          C
D187 00 00 00 00 C
D18B 0132        C          parameter_table <,2d,128d,306d>    ; (default)
D18D 02          C          ;type 4: Syquest SQ306
D18E 0080        C
D190 0132        C
D192 0B          C
D193 05          C
D194 0C          C
D195 B4          C
D196 28          C
D197 00 00 00 00 C
D19B 0284        C          parameter_table <644d,5d,128d,128d> ;type 5: CDC Wron
D19D 05          C
D19E 0080        C
D1A0 0080        C
D1A2 0B          C
D1A3 05          C
D1A4 0C          C
D1A5 B4          C
D1A6 28          C
D1A7 00 00 00 00 C
D1A8             C
D1A8             C          ; ...End of hard disk parameters.
D1A8             C
D1A8             C          ;===== hd4.asm =====
D1A8             C          ; Interrupt 13h - HDU I/O request
D1A8             C          ;=====
D1AB             C          h_io  proc  far
D1AB             C          assume cs:code, ds:nothing, es:nothing, ss:nothing
D1AB             C
D1AB             C          ; Debugging code to display all calls to this procedure.

```

# ROM BIOS Listing

```

C
C ;
C ;      push   ax
C ;      mov    al,ah
C ;      call  DHexByte
C ;      mov    al,dl
C ;      call  DHexWib
C ;      call  DColon
C ;      pop    ax
C
C
C      test   dl,080h                ; test HDU flag bit #7.
D1AE 75 05                          ; is this an HDU command?
D1B0 CD 40                          ; if not, pass to the FDU driver
C
C      ret_from_#0:
D1B2 D1B2 CA 0002                    ; and then return, saving flags
C      ret    2
C
C      hard_disk_int13:
D1B5 D1B5 FB                          ; enable interrupts
D1B6 80 FC 00                        ; is this a reset command?
D1B9 75 09                          ; if so, must reset FDU also
D1BB CD 40
C
C      cmp    dl,87h                ; is the number absurd?
D1BD 80 FA 87                        ; if so, return without HDU
D1C0 77 F0
C
C      mov    ah,reset_int          ; perform a hard disk reset
D1C2 B4 00
C
C      h_save_regs:
D1C4 D1C4 57                          push   di
D1C5 56                              push   si
D1C6 06                              push   es
D1C7 1E                              push   ds
D1C8 53                              push   bx
D1C9 51                              push   cx
D1CA 52                              push   dx
C
C ; Set up ds: segment.
C
C      assume  es:code, ds:data, es:nothing, as:nothing
C
C      push   ax
D1CB 50
D1CC B8 0040                          mov    ax,data_seg
D1CF 8E D8                          mov    ds,ax
D1D1 58                              pop    ax
C
C      mov    byte ptr ds:[control_byte],dl ;retain drive specifier
D1D2 88 16 0076 R
C
C      cmp    ah,status_int          ;is it a status request?
D1D6 80 FC 01
D1D9 75 03                          jne    h_make_odb
D1DB B9 D263 R                        jmp    status ;treat as a special case
C
C ; Set up some of the CDB.
C
C      h_make_odb:
D1DE D1DE C9                          dec    cl ;bx sectors are 0-16, not 1-17
D1E0 88 0E 0044 R                    byte ptr ds:[cmd_block+2],cl ;cylinder-hi and sector
D1E4 88 2E 0045 R                    mov    byte ptr ds:[cmd_block+3],ch ;cylinder-low
D1E8 A2 0046 R                        mov    byte ptr ds:[cmd_block+4],al ;interleave or block count
C
C      push   ea
D1EB 06                              push   bx
D1EC 53                              push   bx
D1ED B8 D5C1 R                        call   get_drive_type_vector ;point to parms for this drive
D1F0 26: 8A 47 08                    mov    al,es:[bx+p_control_byte] ;get the control byte
D1FA 5B                              pop    bx
D1FB 58                              pop    cx
D1FC 07                              pop    ea
D1FE A2 0047 R                        mov    byte ptr ds:[cmd_block+5],al ;put it in the odb
C
C ; Set up the port_off with the port offset for the drive.
C
C      mov    al,dl                  ; HDU drive number
D1F9 8A C2
D1FB 24 7F                          and    al,07Fh ;mask off HDU flag bit #7
D1FD 3A 06 0075 R                    cmp    al,byte ptr ds:[hfn_num] ; count of HDU's
D201 73 57                          jae    h_bad_command ; error if too high
C
C      push   ax
D203 50
D204 D0 E0                          shl    al,1 ;multiply by 2
D206 24 FC                          and    al,11111100b ;provide port offset
D208 A2 0077 R                        mov    byte ptr ds:[port_off],al ;store for use by port routine
D20B 58                              pop    ax
C
C      mov    ol,drivenum           ;shift for odb drive#
D20C B1 05                          shl    ol,ol
D20E D2 E0                          shl    dh,(mask headnum) ;get the bits for head number
D210 80 E6 1F                        and    dh,(mask headnum) ;share drive# with head number
D213 0A C6                          or     al,dh ;store in the drive/head byte
D215 A2 0043 R                        mov    byte ptr ds:[cmd_block+1],al
C
C ; Set up an index to use the h_cmd_table.
C
C      cmp    ah,max_int            ;highest-numbered valid int13 command
D218 80 FC 14
D21B 77 3D                          jae    h_bad_command ;error if out of range
C
C      mov    al,ah                 ;get the command code
D21D 8A C4
D21F D0 E0                          shl    al,1 ;multiply command by 4...
D221 D0 E0                          shl    al,1 ;for indexing of table
D223 B4 08                          mov    ah,0 ;zero top 8 bits
D225 05 D26D R                        add    ax,offset h_cmd_table ;now we point to the command in the table
D228 B8 F0                          mov    si,ax ;we'll use es:[si] to index the table

```

# ROM BIOS Listing

```

C
C
C ; Now we can finish setup of the command.
C ; If it's a p_dma operation, the command subroutine will be
C ; called with al=p_dma mode byte for 8237.
D22A 2E: 8A A4 0000      mov     ah,cs:[si].bx_opcode      ;get the opcode for the cdb
D22F 88 26 0028 R      mov     byte ptr ds:[cmd_block+0],ah ;and put it in place
D233 2E: 8A 84 0003      mov     al,cs:[si].h_cmd_mode_dma ;p_dma mode byte (read/write)
D238 06 06 0074 R 00    mov     byte ptr ds:[disk_status],0 ; clear errors.
D23D 2E: FF 94 0001      call    cs:[si].h_cmd_subr       ;call subroutine to execute command
C
C
C h_finish:
D242                call    disable_disk_interrupts
D242                call    maybe_show_sense
D245                call    maybe_show_sense
C
C
D248 8A 26 0074 R      mov     ah,byte ptr ds:[disk_status] ; get the status code from oper.
D24C 80 FC 01          cmp     ah,1                      ; if nonzero, clear CF
D24F F5                omd                                ; now CF reflects error status.
C
C
D250 5A                pop     dx
D251 59                pop     cx
D252 5B                pop     bx
D253 1F                pop     ds
D254 07                pop     es
D255 5E                pop     si
D256 5F                pop     di
C
C
D257 CA 0002          ret     2                          ;return, preserving flags
C
C
C
C
D25A                h_bad_command:
D25A C6 06 0074 R 01    mov     byte ptr ds:[disk_status],cmd_error ;bad command to int13
D25F 80 00              mov     al,0                      ;clear burst length
D261 EB DF              jmp     h_finish                  ;and exit
C
C ; Special code for return_status.
C
D263                status:
D263 A0 0074 R          mov     al,byte ptr ds:[disk_status] ;return status from last command
D266 C6 06 0074 R 00    mov     byte ptr ds:[disk_status],0 ;this command was successful
D26B EB D5              jmp     h_finish                  ;and exit
C
C ; This is the structure for the table which allows command dispatch.
C
C h_cmd_struct      struct
C bx_opcode         db     0h        ;opcode for the bx (cdb byte 0)
C h_cmd_subr        dw     0h        ;address of command routine
C h_cmd_mode_dma    db     0h        ;code for 8237 read/write
C h_cmd_struct      ends
C
C ; This is the table itself. Each entry corresponds to a command.
C
D26D                h_cmd_table:
C
C h_cmd_struct      <assign_param_bx,assign_param>      ;00 reset
C
C
C h_cmd_struct      <0h, 0h>                          ;01 status
C
C
C h_cmd_struct      <read_bx, h_dma, read_mode>        ;02 read
C
C
C h_cmd_struct      <write_bx, h_dma, write_mode>      ;03 write
C
C
C h_cmd_struct      <chktrk_bx, h_ndma>                ;04 chktrk
C
C
C h_cmd_struct      <fmttrk_bx, h_ndma>                ;05 fmttrk
C
C
C h_cmd_struct      <fmtbad_bx, h_ndma>                ;06 fmtbad
C
C
C h_cmd_struct      <fmtdrv_bx, h_ndma>                ;07 fmtdrv
C
C
C h_cmd_struct      <0h, read_param>                  ;08 read_param
C
C
C h_cmd_struct      <assign_param_bx,assign_param>      ;09 assign_param
C
C

```

```

D295 E5          C      h_omd_struct <rlong_bx,      h_dma,  read_mode> ;0a rlong
D296 D2C1 R     C
D298 47         C
D299 E6          C      h_omd_struct <wlong_bx,      h_dma,  write_mode> ;0b wlong
D29A D2C1 R     C
D29C 4B         C
D29D 0B          C      h_omd_struct <seek_bx,       h_ndma> ;0c seek
D29E D33E R     C
D2A0 00         C
D2A1 0C          C      h_omd_struct <assign_param_bx,assign_param> ;0d reset
D2A2 D504 R     C
D2A4 00         C
D2A5 0E          C      h_omd_struct <rbuf_bx,       h_dma,  read_mode> ;0e rbuff
D2A6 D2C1 R     C
D2A8 47         C
D2A9 0F          C      h_omd_struct <wbuf_bx,       h_dma,  write_mode> ;0f wbuff
D2AA D2C1 R     C
D2AC 4B         C
D2AD 00          C      h_omd_struct <tst_drv_rdy_bx,h_ndma> ;10 tst_drv_rdy
D2AE D33E R     C
D2B0 00         C
D2B1 01          C      h_omd_struct <recal_bx,      h_ndma> ;11 recal
D2B2 D33E R     C
D2B4 00         C
D2B5 E0          C      h_omd_struct <randiag_bx,    h_ndma> ;12 randiag
D2B6 D33E R     C
D2B8 00         C
D2B9 E3          C      h_omd_struct <drvdia_bx,    h_ndma> ;13 drvgdiag
D2BA D33E R     C
D2BC 00         C
D2BD E4          C      h_omd_struct <bxdiag_bx,    h_ndma> ;14 bxdiag
D2BE D33E R     C
D2C0 00         C

D2C1             C      h_io      endp
C
; This procedure is called by int13 when a command requires a p_dma operation.
; The al register should contain the h_omd_mode_dma.
C
D2C1             C      h_dma      proc
C
D2C1 FA          C      cli ; disable interrupts
D2C2 E6 0B       C      out dma_mode,al ; set the p_dma mode
C
; Convert es:bx to an absolute 20-bit address for data.
C
D2C4 8C C0       C      mov ax,es ; get es
D2C6 B1 04       C      mov ol,4 ; rotate 4 bits (*16)
D2C8 D3 C0       C      rol ax,ol ; now it's aligned with bx
D2CA 8A E8       C      mov ch,al ; save the top nibble of address
D2CC 24 F0       C      and al,0F0h ; clear low nibble
C
D2CE 03 D6       C      add bx,ax ; add the offset of the address
D2D0 80 D5 00    C      adc ch,0 ; propagate CF (20-bit addition)
C ; ch = 20-bit address hi nibble
C ; bx = 20-bit offset of address
C
D2D3 E6 0C       C      out dma_ff_olr,al ; clear the first/last ff
C
D2D5 8A C3       C      mov al,bl
D2D7 E6 06       C      out dma_addr_3,al ; output low byte of address
C
D2D9 8A C7       C      mov al,bh
D2DB E6 06       C      out dma_addr_3,al ; output high byte of address
C
D2DD 8A C5       C      mov al,oh ; restore top nibble of address
D2DF 24 0F       C      and al,0Fh ; mask the nibble
D2E1 E6 82       C      out hdu_dma_seg,al ; to bank select register
C
D2E3 A0 0042 R   C      mov al,byte ptr ds:[omd_block*0] ; get command from omd_block
C
; If it is a rlong or wlong, it's limited to one block (516 chars)
; Note that if rlong or wlong is requested, the length is not checked.
C
D2E6 3C E5       C      cmp al,rlong_bx ; is command rlong_bx?
D2E8 74 38       C      je h_dma_long ; is command wlong_bx?
D2EA 3C E6       C      cmp al,wlong_bx ; is command rlong_bx?
D2EC 74 34       C      je h_dma_long ; is command wlong_bx?
C
; If it is a rbuff or wbuff, it's forced to one block (512 chars)
; Note that if rbuff or wbuff is requested, the length is not checked.
C
D2EE 3C 0E       C      cmp al,rbuff_bx ; is command rbuff_bx?
D2F0 74 3A       C      je h_dma_buff ; is command wbuff_bx?
D2F2 3C 0F       C      cmp al,wbuff_bx ; is command rbuff_bx?
D2F4 74 36       C      je h_dma_buff ; is command wbuff_bx?
C
; Set up the number of bytes for a normal command.

```

# ROM BIOS Listing

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D2F6 80 3E 0046 R 80      C      cmp     byte ptr ds:[cmd_block+4],080h ; too many blocks requested?
D2FB 77 39                C      ja      h_dma_err ; (64k RAM/512 bytes per sector)
C      ; Determine number of bytes to transfer.
C      ;
D2FD B1 09                C      mov     cl,9h ; multiply 512 times
D2FF A0 0046 R           C      mov     al,byte ptr ds:[cmd_block+4] ; ...block count
D302 D3 E0                C      shl     ax,cl ; to make byte count
C      ;
D304 48                    C      h_dma_len:
D304 48                    C      dec     ax ; ax = byte count - 1
C      ;
D305 E6 07                C      out     dma_count_3,al ; output low byte of count
D307 86 C4                C      xchg   al,ah ;
D309 E6 07                C      out     dma_count_3,al ; output high byte of count
D30B 86 C4                C      xchg   al,ah ; ax = byte count - 1
C      ;
D30D FB                    C      sti ; critical code is over
C      ;
D30E 03 C3                C      add     ax,bx ; compute last byte to transfer
D310 72 24                C      je      h_dma_err ; if carry flag set, overflow!!
C      ; Enable and allow interrupts from p_dma, and issue command.
C      ;
D312 B0 03                C      mov     al,(mask_port_inte+mask_port_dmae)
D314 E8 D3DD R           C      call   command ; send the cdb out to the bx
D317 72 31                C      je      h_err_chk ; return error
C      ;
D319 B0 03                C      mov     al,allow_dma3 ; allow interrupts
D31B E6 0A                C      out     dma_mask_bit,al ; from the p_dma channel
C      ;
D31D E8 D43B R           C      call   h_cmd_wait ; wait for command completion
D320 EB 28                C      jmp     short h_err_chk ; check for possible error
C      ;
C      ; For rlong and wlong commands:
C      ;
D322 C6 06 0046 R 01      C      h_dma_long:
D322 C6 06 0046 R 01      C      mov     byte ptr ds:[cmd_block+4],01h ; one block maximum
D327 B8 0204              C      mov     ax,512d + 4d ; length of data + eoc
D32A EB D8                C      jmp     h_dma_len
C      ; For rbuff and wbuff commands:
C      ;
D32C C6 06 0046 R 01      C      h_dma_buff:
D32C C6 06 0046 R 01      C      mov     byte ptr ds:[cmd_block+4],01h ; one block maximum
D331 B8 0200              C      mov     ax,512d ; length of data
D334 EB CE                C      jmp     h_dma_len
C      ;
D336 C6 06 0074 R 09      C      h_dma_err:
D336 FB                    C      sti ; enable interrupts
D337 F9                    C      stc ; set carry flag.
D338 C6 06 0074 R 09      C      mov     byte ptr ds:[disk_status],dma_seg_error
D33B C3                    C      ret
C      ;
D33E h_dma endp
C      ;
C      ; This procedure is called by int13 when a non-p_dma command is requested.
C      ;
D33E h_ndma proc
C      ;
D33E B0 02                C      mov     al,mask_port_inte ; allow bx interrupt at cmd completion
D340 E8 D3DD R           C      call   command ; send the cdb out to the bx
D343 72 05                C      je      h_err_chk ; return error
C      ;
D345 E8 D33B R           C      call   h_cmd_wait ; wait for the command to complete
D348 EB 00                C      jmp     short h_err_chk ; check for possible error
C      ;
D34A h_ndma endp
C      ;
D34A h_err_chk proc
C      ;
D34A 80 3E 0074 R 00      C      cmp     byte ptr ds:[disk_stat+],0 ; check status flag from command
D34F 75 01                C      jne    h_had_err ;
D351 C3                    C      ret ; no error - looking good
C      ; Perform request sense command same drive number.
C      ;
D352 C6 06 0042 R 03      C      h_had_err:
D352 C6 06 0042 R 03      C      mov     byte ptr ds:[cmd_block+0],sense_bx
D357 B0 00                C      mov     al,0 ; interrupt and p_dma for bx
D359 E8 D3DD R           C      call   command ; send out the command
D35C 72 75                C      je      e_loss ; sense command lost
C      ;
D35E B9 0004              C      mov     cx,4 ; accept 4 data + 1 status byte
D361 B8 0000              C      mov     ax,0
D364 8B F8                C      mov     di,ax ; used as index of array
C      ;
D366 e_read_sense:
D366 B4 08                C      mov     ah,(hdu_bay+hdu_io+hdu_req) ; bay-ed-io-req
D368 E8 D418 R           C      call   wait_for_status ; wait for status byte ready
D36B 72 66                C      je      e_loss ; jump if error
C      ;
D36D BA 0320              C      inport dx,read_port ; read data
D370 02 16 0077 R        C      add     di,byte ptr ds:[port_off] ; get the port number for the base controller
; add port_off for the correct bx

```

# ROM BIOS Listing

```

D374 EC          C+   in      al,dx
D375 88 85 0042 R C     mov     byte ptr ds:[hd_error+di],al ; store in array
D379 47          C     inc     di
D37A E2 EA      C     loop   o_read_sense
C
D37C B4 0F      C     mov     ah,(hdu_bsy+hdu_od+hdu_io+hdu_req) ;bsy+od+io+req
D37E E8 D418 R C     call   wait_for_status ; wait for status byte ready
D381 72 50      C     jc     o_loss ; jump if error
C
D383 BA 0320    C+    inport  al,read_port ; read the status byte
D386 02 16 0077 R C+    mov     dx,read_port ;get the port number for the base controller
D38A EC          C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
C
D38B A8 02      C     test   al,h_c_err ; check status byte
D38D 75 44      C     jnz    o_loss ; leave if we had sense error
C
D38F A0 0042 R C     mov     al,byte ptr ds:[hd_error+0] ; get first sense byte
D392 24 3F      C     and     al,sense0_mask ; isolate the type and code bits
D394 BB D49F R C     mov     bx,offset bx_error_table ;
D397 28: D7     C     xlat   ds:byte ptr bx_error_table ; get the dos error code
D399 42 0074 R C     mov     byte ptr ds:[disk_status],al ; store the status
D39C 3C 11      C     cmp     al,eoc_used_err ; was it a correctable eoc err?
D39E 75 32      C     jne    h_err_ret ; if not, return
C
; Read eoc burst length.
C
D3A0 C6 06 0042 R OD C     mov     byte ptr ds:[cmd_block+0],read_eoc_bx
D3A5 B0 00      C     mov     al,0 ; interrupt mask = no interrupts
D3A7 E8 D3DD R C     call   command
D3AA 72 27      C     jc     o_loss
C
D3AC B4 0B      C     mov     ah,(hdu_bsy+hdu_io+hdu_req) ; bsy+od+io+req
D3AE E8 D418 R C     call   wait_for_status
D3B1 72 20      C     jc     o_loss
C
D3B3 BA 0320    C+    inport  al,read_port ; read the burst length
D3B6 02 16 0077 R C+    mov     dx,read_port ;get the port number for the base controller
D3BA EC          C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D3BB 8A C8      C+    mov     cl,al ; save it for a moment
C
D3BD B4 0F      C     mov     ah,(hdu_bsy+hdu_od+hdu_io+hdu_req) ;bsy+od+io+req
D3BF E8 D418 R C     call   wait_for_status ; read the status byte
D3C2 72 0F      C     jc     o_loss
C
D3C4 BA 0320    C+    inport  al,read_port ;get the port number for the base controller
D3C7 02 16 0077 R C+    mov     dx,read_port ;add port_off for the correct bx
D3CB EC          C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D3CC A8 02      C+    test   al,h_c_err ; check completion status
D3CE 75 03      C     jnz    o_loss
C
D3D0 8A C1      C     mov     al,cl ; get burst length back
D3D2          C     h_err_ret:
D3D2 C3          C     ret
C
; Sense failed. Try to recover.
C
D3D3          C     o_loss:
D3D3 E8 D504 R C     call   assign_params ;reset controller and assign parameters
D3D6 C6 06 0074 R FF C     mov     byte ptr ds:[disk_status],sense_err ;sense failed
D3DB F9          C     stc
D3DC C3          C     ret
C
D3DD          C     h_err_chk   endp
C
; Send a CDB to the bx.
; The al register should be set to a mask_port_cmd.
C
D3DD          C     command   proc
C
D3DD          C     output   select_port,al ;select controller
D3DD BA 0322    C+    mov     dx,select_port ;get the port number for the base controller
D3E0 02 16 0077 R C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D3E4 EE          C+    out     dx,al
C
D3E5 BA 0323    C+    output   mask_port,al ;allow interrupts and maybe p_dms
D3E8 02 16 0077 R C+    mov     dx,mask_port ;get the port number for the base controller
D3EC EE          C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D3ED          C+    out     dx,al
C
D3ED B4 0D      C     mov     ah,(hdu_bsy+hdu_od+hdu_req) ;bsy+od+io+req
D3EF E8 D418 R C     call   wait_for_status ;wait for controller to setup for cmd
D3F2 72 23      C     jc     c_finish ;leave if timed out
D3F4 FC          C     cld
D3F5 BE 0042 R C     mov     si,ds:(offset cmd_block) ;clear direction; count up with [si]
C
D3F8          C     send_odb_byte:
D3F8 AC          C     lodsb
D3F8          C     outport  write_port,al ;get a byte of odb
D3F9 BA 0320    C+    mov     dx,write_port ;get the port number for the base controller
D3FC 02 16 0077 R C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D400 EE          C+    out     dx,al
D401 B9 0000    C     mov     cx,0 ;prepare for loop
C
D404          C     o_wait:
D404          C     inport  al,status_port ;check status
D404 BA 0321    C+    mov     dx,status_port ;get the port number for the base controller
D407 02 16 0077 R C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D40B EC          C+    in     al,dx
D40C A8 01      C     test   al,hdu_req ;is status valid?
D40E E1 F4      C     loopz  o_wait ;wait for valid or timeout

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# ROM BIOS Listing

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D410 24 07      C      and    al,07h          ;mask low 3 bits
D412 3C 05      C      cmp     al,(hdu_ed+hdu_req) ;is it still looking for ed+out?
D414 74 E2      C      je     send_cdb_byte      ;yes - go send another byte
D416 F8         C      cld
D417 C3         C      ret                    ;done sending all bytes, so return
D418            C
C      command endp
C
C      ; Wait for status from bx (specified in ah), or else time out.
C
D418            C      wait_for_status proc
C
D418 50         C      push  ax
D419 51         C      push  ox
D41A B9 0000    C      mov   ox,0
D41D            C      r_waiting:
C      inport  al,status_port      ;read bx status
C+     mov   dx,status_port      ;get the port number for the base controller
C+     add   di,byte ptr ds:[port_off] ;add port_off for the correct bx
D424 EC         C+     in    al,dx
D425 A8 01      C      test  al,hdu_req          ;look for validity of status
D427 E1 F4      C      loopz r_waiting        ;loop if not valid yet
D429 24 0F      C      and   al,0fh            ;get low 4 bits
D42B 3A C4      C      cmp   al,ah            ;test for the specified status
D42D 74 09      C      je    bx_ready          ;test for the specified status
D42F C6 06 0074 R 80 C      mov   byte ptr ds:[disk_status],time_out ;took too long to select
D434 F9         C      stc                    ;flag error
D435            C      r_finish:
D435 59         C      pop   ox
D436 58         C      pop   ax
D437 C3         C      ret
C
D438            C      bx_ready:
D438 F8         C      cld                    ;got the req
D439 EB FA      C      jmp   r_finish
D43B            C      wait_for_status endp
C
C      ; Wait for a command to complete.
C
D43B            C      h_cmd_wait   proc
C
D43B FA         C      cli
D43C 84 21      C      in    al,pic_1          ; get interrupt mask
D43E 24 DF      C      and  al,0DFh          ; un-mask EDU interrupt IB5
D440 86 21      C      out  pic_1,al         ; set the controller
D442 FB         C      sti
C
C      assume es:abs0
C
D443 33 C0      C      xor   ax,ax
D445 8E C0      C      mov  es,ax            ; es = ax = abs0_seg
D447 26: C4 36 0104 C      les  si,dword ptr es:[(h*16)h] ; es points to abs0_seg segment
C                                     ; es:si points to hdu_parm_tbl
C
C      assume es:nothing
C
C      ; Determine timeout count.
C
D44C 87 03      C      mov  bh,0             ;zero top byte of count
D44E 26: 8A 5C 09 C      mov  bl,es:byte ptr [si].p_timeout ;standard timeout
D452 80 3E 0042 R 04 C      cmp  byte ptr ds:[cmd_block*0],fmtdrv_bx ;but is it a format
C                                     ;drive command?
D457 75 07      C      jne  w1
D459 26: 8A 5C 0A C      mov  bl,es:byte ptr [si].p_fmt_timeout ;fmtdrv timeout
D45D EB 0C 90    C      jmp  w2
D460            C      w1:
D460 80 3E 0042 R E3 C      cmp  byte ptr ds:[cmd_block*0],drvdiag_bx ;but is it a drive
C                                     ;diagnostic?
D465 75 04      C      jne  w2
D467 26: 8A 5C 0B C      mov  bl,es:byte ptr [si].p_drvdiag_timeout ;drvdiag timeout
C
C      ; Now we can wait for the interrupt.
C
D46B            C      w2:
D46B D1 E3      C      shl  bx,1              ;double the timeout for the
C                                     ;8086.
C
D46D            C      wait_for_irq5:
C      inport  al,status_port      ;read status byte
D46D BA 0321    C+     mov  dx,status_port      ;get the port number for the base controller
D470 02 16 0077 R C+     add  di,byte ptr ds:[port_off] ;add port_off for the correct bx
D474 EC         C+     in    al,dx
D475 A8 20      C      test  al,hdu_irq5        ;was there an interrupt yet?
D477 75 0D      C      jnz  w_ita_done
D479 E2 F2      C      loop wait_for_irq5
C
D47B 4B         C      dec  bx                ;outer timing loop
D47C 75 EF      C      jnz  wait_for_irq5
C
D47E C6 06 0074 R 80 C      mov  byte ptr ds:[disk_status],time_out ;we fell through
D483 EB 0F 90    C      jmp  w_finish
C
D486            C      w_ita_done:
C      inport  al,read_port        ;read status byte
D486 BA 0320    C+     mov  dx,read_port        ;get the port number for the base controller
D489 02 16 0077 R C+     add  di,byte ptr ds:[port_off] ;add port_off for the correct bx
D48D EC         C+     in    al,dx
D48E 24 02      C      and  al,h_err           ;get completion error bit
D490 08 06 0074 R C      or   byte ptr ds:[disk_status],al ;h_err_ohk will look at it

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# ROM BIOS Listing

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D494          C   w_finish:
D494          C     mov     al,0                ;turn off controller interrupts
D496 BA 0323  C+    outport mask_port,al
D499 02 16 0077 R C+    mov     dx,mask_port        ;get the port number for the base controller
D49D EE      C+    add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
C          C+    out     dx,al
C          C     ret
D49E C3      C
D49F          C   h_cmd_wait   endp
D49F          C   h_data1 proc
D49F          C
D49F          C   bx_error_table:
D49F          C   ; Type 0 errors
D49F 00 20 40 20 C     db     0, fdc_error, seek_error, fdc_error
D4A3 80 00 20 00 C     db     time_out, 0, fdc_error, 0
D4A7 40 00 00 00 C     db     seek_error, 0, 0, 0
D4AB 00 00 00 00 C     db     0, 0, 0, 0
C          C   ;Type 1 errors
D4AF 10 10 02 00 C     db     crc_error, crc_error, addr_mark_error, 0
D4B3 04 40 00 00 C     db     sect_not_found, seek_error, 0, 0
D4B7 11 0B 00 00 C     db     ecc_used_err, badtrack_err, 0, 0
D4BB 00 00 00 00 C     db     0, 0, 0, 0
C          C   ;Type 2 errors
D4BF 01 02 00 00 C     db     cmd_error, addr_mark_error, 0, 0
D4C3 0C [      C     db     12 dup(0)
C          C
C          C   ;Type 3 errors
D4CF 20 20 10 00 C     db     fdc_error, fdc_error, crc_error, 0
D4D3 0C [      C     db     12 dup(0)
C          C
C          C
D4DF          C   h_data1 endp
C          C
C          C   ;===== hd5.asm =====
C          C
D4DF          C   read_param   proc
D4DF 06      C+    push    es                ;save caller's es: register
D4E0 E8 D5C1 R C+    call    get_drivetype_vector ;loads es with pointer & bx with offset
C          C
D4E3 26: 8B 0F C     mov     cx,es:[bx].p_cyls     ;get number of cylinders
D4E6 83 89 02 C     sub     cx,2d                ;subtract 2: zero origin and diag track
D4E9 86 89      C     xchg   cx,01                ;put low-order in cx
D4EB D0 C9      C     ror    cx,1                 ;put high-order 2 bits
D4ED 80 C9      C     ror    cx,1                 ;in top of cx
D4EF 80 C9 11    C     or     cx,sectora_per_track ;fixed, not variable
C          C
D4F2 26: 8A 77 02 C     mov     dh,es:[bx].p_heads   ;number of heads
D4F6 FE CE      C     dec     dh                  ;zero origin
C          C
D4F8 8A 16 0075 R C+    mov     di,byte ptr ds:[bf_num] ;count of hard disks
C          C
D4FC 07      C     pop     es
C          C
C          C
D4FD 58      C     pop     ax                ;save the return address
D4FE 5B      C     pop     bx                ;trash the dx
D4FF 5B      C     pop     bx                ;and cx from the caller
C          C
D500 51      C     push    cx                ;push new parameters
D501 52      C     push    dx                ;for caller to receive
D502 50      C     push    ax                ;replace return address
C          C
D503 C3      C     read_param   ret
D504          C   read_param   endp
C          C
C          C   ; Perform a reset and assign parameters for the drives.
C          C   ; Note: parameters must be assigned for BOTH drives on the chosen controller.
C          C
D504          C   assign_param  proc
D504 E8 D5B1 R C+    call    reset_bx
C          C
D507 06      C     push    es
C          C
D508 C6 06 0042 R 0C C     mov     byte ptr ds:[cmd_block+0],assign_param_bx ;set cdb
D50D C6 06 0043 R 00 C     mov     byte ptr ds:[cmd_block+1],0 ;assume drive 0
D512 80 26 0076 R FE C     and     byte ptr ds:[control_byte],0feh
D517 E8 D532 R C+    call    assign_param_1 ;assign params
D51A T2 14      C     je     ap_finish ;jump if OK
C          C
D51C 07      C     pop     es
D51D 06      C     push    es
C          C
D51E C6 06 0042 R 0C C     mov     byte ptr ds:[cmd_block+0],assign_param_bx ;set cdb
D523 C6 06 0043 R 20 C     mov     byte ptr ds:[cmd_block+1],(mask_drivenum) ;assume drive 1
D528 80 26 0076 R 01 C     and     byte ptr ds:[control_byte],01h
D52D E8 D532 R C+    call    assign_param_1 ;assign params
C          C
D530          C   ap_finish:
D530 07      C     pop     es
D531 C3      C     ret
C          C
D532          C   assign_param  endp
C          C

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# ROM BIOS Listing

```

D532          C      assign_param_1  proc
D532 B0 00      C          mov     ax,0           ;no interrupts desired
D534 E8 D3DD R  C          call    command        ;send the odb
D537 72 63      C          jc     a_finish
C
C      ; Send the 8 bytes of drive parameters as PIO.
C
D539 E8 D5C1 R  C          call    get_drivetype_vector ;snare pointer to the table
C
C      ; send mab before lab
C
D53C 26: 8A 47 01 C          mov     al,es:byte ptr [bx].p_cyls+1
D540 E8 D59D R  C          call    data_out
D543 72 57      C          jc     a_finish
C
D545 26: 8A 07   C          mov     al,es:byte ptr [bx].p_cyls
D548 E8 D59D R  C          call    data_out
D54B 72 4F      C          jc     a_finish
C
D54D 26: 8A 47 02 C          mov     al,es:[bx].p_heads
D551 E8 D59D R  C          call    data_out
D554 72 46      C          jc     a_finish
C
D556 26: 8A 47 04 C          mov     al,es:byte ptr [bx].p_write_cur+1
D55A E8 D59D R  C          call    data_out
D55D 72 3D      C          jc     a_finish
C
D55F 26: 8A 47 03 C          mov     al,es:byte ptr [bx].p_write_cur
D563 E8 D59D R  C          call    data_out
D566 72 34      C          jc     a_finish
C
D568 26: 8A 47 06 C          mov     al,es:byte ptr [bx].p_precomp+1
D56C E8 D59D R  C          call    data_out
D56F 72 2B      C          jc     a_finish
C
D571 26: 8A 47 05 C          mov     al,es:byte ptr [bx].p_precomp
D575 E8 D59D R  C          call    data_out
D578 72 22      C          jc     a_finish
C
D57A 26: 8A 47 07 C          mov     al,es:[bx].p_eec_len
D57E E8 D59D R  C          call    data_out
D581 72 19      C          jc     a_finish
C
C      ; Note that control byte is handled differently... See near h_make_odb.
C
D583 B4 0F      C          mov     ah,(hdu_bay+hdu_od+hdu_io+hdu_req) ;bay+od+io+req
D585 E8 D418 R  C          call    wait_for_status
D588 72 12      C          jc     a_finish
C
C      import al,read_port ;read the status byte
D58A BA 0320    C+         mov     dx,read_port ;get the port number for the base controller
D58D 02 16 0077 R C+         add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D591 EC         C+         in     al,dx
D592 A8 02     C          test    al,h_0_err ;did we do ok?
D594 74 06     C          js     a_finish
D596 C6 06 0074 R 07 C          mov     byte ptr ds:[disk_status],init_err ;no
D598 F9         C          stc
C
C      a_finish:
D59C          C          ret
D59C C3          C
D59D          C      assign_param_1  endp
C
C      ; Send a byte of data out the write_port.
C
D59D          C      data_out      proc
C
D59D          C          push    ax
D59E B4 09      C          mov     ah,(hdu_bay+hdu_req) ;bay+od+io+req
D5A0 E8 D418 R  C          call    wait_for_status
D5A3 58        C          pop     ax
D5A4 73 01      C          jnc    do_ready ;if it didn't time out, output the data
D5A6 C3          C          ret
C
D5A7          C      do_ready:
C          outputport write_port,al ;write it out
D5A7 BA 0320    C+         mov     dx,write_port ;get the port number for the base controller
D5AA 02 16 0077 R C+         add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D5AE EE        C+         out     dx,al
D5AF F8        C          cld
D5B0 C3          C          ret ;no problem
C
D5B1          C      data_out      endp
C
D5B1          C      reset_bx     proc
C
D5B1          C          outputport reset_port,al ;reset controller
D5B1 BA 0321    C+         mov     dx,reset_port ;get the port number for the base controller
D5B4 02 16 0077 R C+         add     di,byte ptr ds:[port_off] ;add port_off for the correct bx
D5B8 EE        C+         out     dx,al
D5B9 51        C          push    cx
D5BA B9 0100    C          mov     cx,100h ;wait in a loop
D5BD E2 FE     C          loop   $
D5BF 59        C          pop     cx
D5C0 C3          C          ret
C      reset_bx     endp
C
C      ; Returns with es:[bx] pointing to the drivetype vector for the selected drive.
C

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# ROM BIOS Listing

```

C ;           The bits are selected from the switch as follows:
C ;
C ;           switch      | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
C ;           bit         | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
C ;           drive 0     | 0 | 1 |   |   | 2 | 3 |   |   |
C ;           drive 1     |   |   | 0 | 1 |   |   | 2 | 3 |
C ;
C ;
D5C1          get_drivetype_vector    proc
D5C1 50
C           push    ax
C           assume  es:abs0
D5C2 33 C0          xor    ax,ax                ; es = ax = abs0_seg
D5C4 8E C0          mov    es,ax                ; es points to abs0_seg segment
D5C6 26: C4 1E 0104 les    bx,dword ptr es:[4*41h] ; es:bx points to hdu_parm_tbl
C           assume  es:nothing
C ;
D5CB 52           push    dx
C           inport  al,switch_port ;read switches on controller board
D5CC BA 0322        mov    dx,switch_port ;get the port number for the base controller
D5CF 02 16 0077 R  add    di,byte ptr ds:[port_off] ;add port_off for the correct bx
D5D3 EC           C+
D5D4 5A           C+
D5D5 24 7F        pop    dx
C           and    al,07fh      ;ignore top switch!
D5D7 F6 06 0076 R 01 test  byte ptr ds:[control_byte],01h ;was this controller drive one?
D5DC 75 04        jnz    &_mask
D5DE D0 B8        shr    al,1                ;to get drive zero,
D5E0 D0 B8        shr    al,1                ;shift twice right
C           &_mask:
D5E2             and    al,00110011b      ;get switch_mask bits for this drivetype
D5E4 8A E0        mov    ab,al
D5E6 D0 EC        shr    ab,1                ;..into bits 2&3
D5E8 D0 EC        shr    ab,1
D5EA 0A C4        or     al,ab              ;combine with low 2 bits
C           ;
D5EC D0 B0        shl    al,1                ;multiply by 16 for offset in table
D5EE D0 B0        shl    al,1
D5F0 D0 B0        shl    al,1
D5F2 D0 B0        shl    al,1
D5F4 B4 00        mov    ab,0
D5F6 03 D8        add    bx,ax              ;add offset to base of param_table
C           ;
D5F8 58           pop    ax
D5F9 C3           ret
D5FA           get_drivetype_vector    endp
C ;
D5FA           disable_disk_interrupts proc
C ;
C ;           ; Disables interrupts from all bx controllers on the system.
C ;
D5FA 52           push    dx
D5FB 51           push    cx
D5FC 50           push    ax
D5FD 1E           push    ds
C ;
C ;           ; Set up ds: segment.
C ;
C           assume  ds:data
D5FE B8 0040        mov    ax,data_seg        ; satisfy assumptions.
D601 8E D8        mov    ds,ax
C ;
D603 FA           cli
D604 E4 21        in     al,pio_1           ; get interrupt mask
D606 0C 20        or     al,020h           ; turn off IR5
D608 E6 21        out    pio_1,al         ; add set the new mask
D60A F8           sti
C ;
D60B B5 00        mov    ch,0
D60D 8A 0E 0075 R mov    cl,byte ptr ds:[hf_num] ;number of drives
D611 41           inc    cx
D612 D1 E9        shr    cx,1              ;...number of controllers
D614 74 10        jz     v_disallow        ;if zero, disallow
C ;
D616           v_reset_bx:
C ;
C ;           ; Reset controller cx by sending mask byte.
C ;
D616 B0 00        mov    al,0
D618 8B D1        mov    dx,cx
D61A 4A           dec    dx
D61B D1 E2        shl    dx,1              ;wake it an offset (4 ports/bx)
D61D D1 E2        shl    dx,1
D61F 81 C2 0323    add    dx,mask_port
D623 EE           out    dx,al
C           ;now bx-> controller
D624 E2 F0        loop  v_reset_bx
C ;
D626           v_disallow:
D626 B0 07        mov    al,disallow_dma3 ;command to turn off dma3 interrupts
D628 E6 0A        out    dma_mask_bit,al ;send it
C ;
C ;           assume  ds:nothing
D62A 1F           pop    ds

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# ROM BIOS Listing

```

D62B 58          C          pop     ax
D62C 59          C          pop     cx
D62D 5A          C          pop     dx
D62E C3          C          ret
D62F             C          disable_disk_interrupts endp
C
C          ;=====
C          ; Interrupt 0Dh - handle interrupt from controller
C          ;=====
C          ; This is run when the hard disk causes an interrupt due to command completion.
C
D62F             C          h_int  proc
C
D62F 50          C          push    ax
C
D630 B0 20       C          mov     al,pic_neoi          ;command for 8259
D632 B6 20       C          out    pic_0,al
C
D634 B0 07       C          mov     al,disallow_dma3    ;command for 8237
D636 B6 0A       C          out    dma_mask_bit,al
C
D638 B4 21       C          in     al,pic_1          ; get interrupt mask
D63A 0C 20       C          or     al,020h           ; turn off IR5
D63C B6 21       C          out    pic_1,al          ; and set the new mask
C
D63E 58          C          pop     ax
D63F CF          C          iret
C
D640             C          h_int  endp
C
C          ;===== dtofmt.asm =====
C          ; HDU Physical Formatting Utility
C          ;
C          ; Formatting utility to perform physical format of hard disk drive
C          ; using DTC-5150BI controller. Calls int 13h to provide disk services.
C          ;
C          ; Use this program when you first use a new disk. Then use FDISK and
C          ; FORMAT programs to finish the job.
C          ;
C          ; The user can supply an argument number for any hard disk on the system.
C          ; ex: 1=drive 0, 2=drive d.
C          ;=====
C          assume cs:code, ds:nothing, es:nothing, ss:nothing
C
D640             C          h_fmt  proc  near
C
C          ; Write greeting and prompt for drive number.
C          ; Drives are numbered the same way as in the industry standard "FDISK" utility.
C
D640 BE D64C R   C          mov     si,cs:(offset h_intro_m) ;greeting string
D643 B8 E5FA R   C          call   DRomString
C
D646 32 E4       C          xor     ah,ah              ; ah = 0.
D648 CD 16       C          INT    16h              ; get a keystroke.
C
D64A 3C 71       C          cmp     al,'q'             ;check for quit code
D64C 74 45       C          je     finished          ;exit if user typed a q
D64E 3C 51       C          cmp     al,'Q'
D650 74 41       C          je     finished
C
D652 B8 E619 R   C          call   DCrLf
C
D655 2C 31       C          sub     al,'1'             ; range should be '1' to '8'
D657 72 3E       C          je     no_hard_disk      ; if negative, incorrect number
D659 0C 80       C          or     al,080h           ; set HDU flag bit #7.
D65B 8A D0       C          mov     di,al             ; prepare drive code for int13
C
C          ; Create a 512 byte sector buffer of 6Ch (on the stack!).
C
D65D FC          C          cld                      ; clear direction flag.
D65E 06          C          push   es                ; save registers.
D65F 16          C          push   es
D660 07          C          pop    es
D661 81 EC 0200 C          sub    sp,512             ; es gets ss.
C          ; make room on stack!
C
D665 8B FC       C          mov    di,sp              ; es:di points to stack buffer.
D667 B8 6C6C     C          mov    ax,06C6Ch         ; word fill pattern.
D66A B9 0100     C          mov    cx,(512/2)        ; number of words to fill.
D66D F3/ AB      C          rep   stosw              ; fill stack buffer.
C          ; di saves original stack pointer
C
C          ; Write the stack sector buffer with the 06Ch code to fill data fields on drive.
C
D66F B8 0F01     C          mov    ax,(wbuff_int*100h)+1 ; prepare for write sector of 1 buffer.
D672 B8 DC       C          mov    bx,sp              ; es:bx points to stack buffer (of 06Ch)
C          ; cx is zero.
C          ; clear head number.
D674 B6 00       C          mov    dh,0
C
D676 CD 13       C          INT    13h              ; call for write sector buffer
C
D678 B8 E7       C          mov    sp,di              ; restore original stack pointer.
D67A 07          C          pop    es                ; restore registers.
C
D67B 72 1A       C          jc     no_hard_disk      ; error writing sector buffer
C
C          ; Print message that we are formatting the drive.
C

```

# ROM BIOS Listing

```

D67D BE D733 R      C      mov     si,cs:(offset h_fmt_m) ;text for informational message
D680 EB E5FA R      C      call    DROMString
C
C      ; Format the drive.
C
D683 B8 0706        C      mov     ax,(fmtdrv_int*100h)+6 ; format drive with interleave of 6
D686 B9 0001        C      mov     cx,01h ; start with sector zero
C
C      ; Note that dx is retained from above.
C
D689 CD 13          C      INT     13h ; format the drive
D68B 72 12          C      je     format_error ; problem during format
C
D68D BE D750 R      C      mov     si,cs:(offset h_pass_m)
D690 EB E5FA R      C      call    DROMString
C
C      finished:
D693 EB E619 R      C      call    DCrLf
D696 C3              C      ret     ; return to caller
C
C      no_hard_disk:
D697 BE D784 R      C      mov     si,cs:(offset h_none_m) ;give error message
D69A EB E5FA R      C      call    DROMString
D69D EB F4           C      jmp     short finished ;exit
C
C      format_error:
D69F BE DTBT R      C      mov     si,cs:(offset h_err_m) ;give error message
D6A2 EB E5FA R      C      call    DROMString
C
C      mov     al,ah ; print error code in ah
D6A5 8A CA          C      call    DHexByte
D6A7 EB E643 R      C      jmp     short finished
C
D6AA EB E7          C      jmp     short finished
C
D6AC              C      h_fmt     endp
C
D6AC              C      h_data2  proc
C
D6AC 46 69 78 65 64 20 C      h_intro_m  db     'Fixed Disk Formatting Utility',CR,LF
      44 69 73 68 20 46
      6F 72 6D 61 74 74
      69 6E 67 20 55 74
      69 6C 69 74 79 0D
      0A
C
D6CB 11 6C 6C 20 6A 61 C      db     'All data on the specified fixed disk will be erased.'
      74 61 20 6F 6E 20
      74 68 65 20 73 70
      65 63 69 66 69 65
      64 20 66 69 78 65
      64 20 64 69 73 6B
      20 77 69 6C 6C 20
      62 65 20 65 72 61
      73 65 64 2E
C
D6FF 0D 04          C      db     CR,LF
DT01 45 6E 74 65 72 20 C      db     'Enter fixed disk number (1 to 8) or "Q" to quit: ',NUL
      66 69 78 65 64 20
      64 69 73 68 20 6E
      75 6D 62 65 72 20
      28 31 20 74 6F 20
      38 29 20 6F 72 20
      22 51 22 20 74 6F
      20 71 75 69 74 3A
      20 00
C
D733 0D 0A 46 6F 72 6D C      h_fmt_m     db     CR,LF,'Formatting Fixed Disk...',CR,LF,NUL
      61 74 74 69 6E 67
      20 46 69 78 65 64
      20 44 69 73 6B 2E
      2E 2E 0D 0A 00
C
D750 46 6F 72 6D 61 74 C      h_pass_m    db     'Format is complete.',CR,LF
      20 69 73 20 63 6F
      6D 70 6C 65 74 65
      2E 0D 0A
C
D765 50 72 6F 63 65 65 C      db     'Proceed with FDISK and FORMAT.',NUL
      64 20 77 69 74 68
      20 46 44 49 53 4B
      20 61 6E 64 20 46
      4F 52 4B 41 54 2E
      00
C
D784 45 72 72 6F 72 3A C      h_none_m    db     'Error: No fixed disk drive exists for this number.',NUL
      20 4E 6F 20 66 69
      78 65 64 20 64 69
      73 68 20 64 72 69
      76 65 20 65 78 69
      73 74 73 20 66 6F
      72 20 74 68 69 73
      20 6E 75 6D 62 65
      72 2E 00
C
D7B7 46 6F 72 6D 61 74 C      h_err_m     db     'Format Error. Code: ',NUL
      20 45 72 72 6F 72
      2E 20 20 43 6F 64
      65 3A 20 00
C
DTCD              C      h_data2  endp
C

```

# ROM BIOS Listing

```

D7CD          C   oode   ends
              C   include graph.asm
              C   ;
              C   ;=====
              C   ;   Filename:       graph.src
              C   ;
              C   ;   This module includes the four graphics functions for INT 10h.
              C   ;
              C   ;=====
              C   ;
              C   ; page
              C   ;-----
              C   ;   INT 10h Graphics Support
              C   ;
              C   ;   Must preserve bx, cx, dx and return values in ax
              C   ;
              C   ;   All other registers are saved and restored by video dispatcher.
              C   ;
              C   ;   Entered with the following in registers:
              C   ;       al, bx, cx, dx intact (set by INT 10 invoker)
              C   ;       ah = v_mode
              C   ;-----
D7CD          C   oode   segment public 'ROM'
              C   assume  es:code, ds:data, es:v_ram, ss:nothing
              C   ;
              C   ;-----
              C   ;   Read Light Pen           function oode = 0Ah
              C   ;
              C   ;   Input:  None.
              C   ;   Output: ah      = 0 light pen switch not down/not triggered
              C   ;         ah      = 1 implies:
              C   ;         (dh,dl) = (row,col) of character light pen
              C   ;         dh      = position from (0,0)
              C   ;         ch      = raster line (0-199)
              C   ;         bx      = pixel column (0-319,0-639)
              C   ;
              C   ;   Trash:  None.   ???
              C   ;-----
D7CD          C   grf_light_pen  proc   near
D7CD          D7CD 32 BA   C   xor   ah,ah           ; return ah = 0 for now (al intact)...
D7CD          D7CF C3   C   ret
D7D0          C   grf_light_pen  endp
              C   ;
              C   ; page
              C   ;-----
              C   ;   Read Dot           function oode = 0Dh
              C   ;
              C   ;   reads a pixel from the indicated location returning its value.
              C   ;   valid in graphics modes only.
              C   ;
              C   ;   Input:
              C   ;       AH = CRT Mode
              C   ;       DX = row (0..199 in Med. & Hi-Res., 0..399 in Ultra Res Mode)
              C   ;       CX = column (0..319 in Med, 0..639 in Hi & Ultra Res. Modes)
              C   ;
              C   ;   Output:
              C   ;       AL = dot value read
              C   ;       AH = mask of pixel in byte (from g_addr)
              C   ;
              C   ;   Saved:  BX, CX, DX (Video dispatcher saves the rest)
              C   ;-----
D7D0          C   grf_read_dot  proc   near
D7D0          D7D0 52   C   push  dx
D7D0          D7D1 51   C   push  cx           ; save registers
D7D2          D7D2 50   C   push  ax           ; save crt mode (high byte)
D7D3          D7D3 88 DB15 R  C   call  g_addr       ; compute address & mask
D7D6          D7D6 8A C9   C   mov   al,ah        ; copy mask
D7D8          D7D8 26: 22 05 C   and  al,byte ptr es:[di] ; AND with byte containing pixel
D7DB          D7DB 5A   C   pop  dx            ; dh = crt mode
D7DC          D7DC FE C1   C   inc  ol            ; prep for wraparound left (B & W)
D7DE          D7DE 80 FE 05 C   cmp  dh,5          ; color?
D7E1          D7E1 7F 02   C   jg   &_jsfy_dot   ; jump if not
D7E3          D7E3 FE C1   C   inc  ol            ; prep for wraparound left (color)
D7E5          D7E5          C   g_jsfy_dot:
D7E5          D7E5 D2 C0   C   rol  al,ol        ; right justify pixel
D7E7          D7E7 59   C   pop  cx            ; restore registers
D7E8          D7E8 5A   C   pop  dx
D7E9          D7E9 53   C   ret
D7EA          C   grf_read_dot  endp
              C   ;
              C   ; page
              C   ;-----
              C   ;   Write Dot           function code = 0Ch
              C   ;
              C   ;   writes a pixel, with the indicated value, at the indicated location.

```

# ROM BIOS Listing

```

C ; valid in graphics modes only.
C ;
C ;
C ; Input: AL = dot value to write (1 or 2 bits depending on mode,
C ; right justified). Bit 7 = 1 specifies XOR the value
C ; with the pixel at DX, CX
C ; AH = CRT Mode
C ; DX = row (0-399) (the actual value depends on the mode)
C ; CX = column (0-639) (the values are not range checked)
C ;
C ; Saved: AI, BI, CI, DI (Video dispatcher saves the rest)
C ;
-----
D7EA grf_write_dot proc near
C ;
C ; push dx ; preserve working registers
C ; push ox
C ; push ax
C ;
C ; call g_addr ; compute address & mask
C ; mov al,byte ptr es:[di] ; fetch byte from video memory
C ; pop dx ; get v_mode & dot value to write
C ; push dx ; resave
C ; or di,di ; is the XOR bit set?
C ; js g_xorbit ; jump if yes
C ; not ah ; invert mask
C ; and al,ah ; clear bits for new pixel
C ; not ah ; restore mask for later
C ; g_xorbit:
C ; inc ol ; prep for wraparound right (b&w)
C ; cmp dh,5 ; color ?
C ; jg g_align_dot ; jump if no
C ; inc ol ; prep for wraparound right (color)
C ; g_align_dot:
C ; ror di,ol ; align new pixel
C ; and di,ah ; strip off non-pixel bits (xor bit, etc)
C ; xor al,di ; OR or XOR in new pixel depending on xor bit
C ; mov byte ptr es:[di],al ; update video memory
C ;
C ; pop ax ; restore registers
C ; pop ox
C ; pop dx
C ; ret
C ;
D815 grf_write_dot endp
C ;
C ; page
C ; =====
C ; This subroutine determines the video RAM byte location
C ; of the indicated row column value. The current graphics mode
C ; is taken into account.
C ;
C ; INPUT:
C ; AH = current graphics mode
C ; DX = row value (0-399)
C ; CX = column value (0-639)
C ;
C ; OUTPUT:
C ; DI = byte address of pixel location in video ram
C ; AH = mask of pixel in byte
C ; CL = # of bits from left end of byte to leftmost bit in mask
C ;
C ; DESTROYED:
C ; AL, CX, DI, BP
C ;
-----
D815 g_addr proc near
C ; convert row-count to a "mod 8" value;
C ; multiply it by 2000H for offset to start of v_ram subarea
C ;
C ; push ox ; save column count
C ; mov bp,1 ; shift count; assume not 640x400
C ; mov sb,cd ; multiplier; assume not 640x400
C ; cmp ah,64 ; video mode 64 or 72?
C ; jb g_skp_1 ; -no: jmp
C ; mov bp,2 ; -yes; change shift count
C ; mov cx,3 ; -yes: change multiplier
C ;
C ; g_skp_1:
C ; xor di,di ; init offset amount
C ; and cx,dx ; get least sig. bit(s) from row count
C ; js g_skp_3 ; jmp if nothing to add
C ; g_skp_2:
C ; add di,2000H ; add v_ram sub-area size
C ; loop g_skp_2 ; do it again (maybe)
C ;
C ; add bytes for the row coordinate to the offset into the v_ram subarea
C ;
C ; g_skp_3:
C ; push di ; temp. store offset
C ; mov di,dx ; DX--row count
C ; mov cx,bp ; CX--mode-related shift val
C ; shr di,ol ; get #rows into a v_ram subarea
C ;
C ; mov dx,di ; save a copy for a moment
C ; mov cx,0406H ; mult. di by 80 [rows-->byte offset]

```

# ROM BIOS Listing

```

D83E D3 E7      C      sal    di,cl      ;      [fast multiply-
D840 8A CD      C      mov    cl,oh        ;      by-80]
D842 D3 E2      C      sal    dx,cl
D844 03 FA      C      add    di,dx        ; #subarea byte offset for this row
C
D846 59          C      pop    cx            ; retrieve subarea beginning's offset
D847 03 F9      C      add    di,cx        ; offset from start of v_ram
D849 5A          C      pop    dx            ; restore column count
C
C ; find column offset
C
D84A B9 0703     C      mov    cx,703H      ; initialize for black & white
D84D 80 FC 05     C      cmp    ah,5          ; color ?
D850 7F 03       C      jg    g_skp_4        ; CX = 703H (black & white)
D852 B9 0302     C      mov    cx,302H      ; CX = 302H (color)
D855                C      g_skp_4:
C
C ; CL = shift count to divide column by pixels per byte ...
C ; 3 for b&w (divide by 8), 2 for color (divide by 4)
C ; CH = remainder's mask during division (7 for b&w , 3 for color)
C ; DX = column
C ; DI = address to column 0 of requested row
C
D855 22 EA       C      and    ob,di        ; get division's remainder in CH
D857 D3 EA       C      shr    dx,cl        ; perform division
C
C ; DX = quotient = column's byte offset from start of row
C ; CH = remainder (= pixel's offset into byte)
C
D859 03 FA      C      add    di,dx        ; DI = pixel's byte address
C
C ; NOW:
C ; DI = address of byte containing the pixel
C ; CH = pixel offset into byte (remainder)
C ; CL = 3 (black & white) or 2 (color)
C
D85B 80 F9 03    C      cmp    ol,3          ; black & white?
D85E 74 02       C      je    g_bitmask    ; jump if yes
D860 D0 E5       C      shl    ch,1         ; color: convert to bit offset
C
C g_bitmask:
D862                C      xchg  cl,ob        ; load CL, preserve "mode"
D864 B4 80       C      mov    ah,80H      ; set high bit in byte
D866 D2 EC       C      shr    ah,cl        ; mask pixel's leftmost bit
D868 80 FD 03    C      cmp    ob,3          ; black & white?
D86B 74 06       C      je    g_skp_5        ; jump if yes
D86D 8A C4      C      mov    al,ah        ; color: create 2-bit mask
D86F D0 E8       C      shr    al,1
D871 0A E0       C      or     ah,al
C
C g_skp_5:
D873                C      ret                ; DI = byte address, AH = pixel mask,
C ; CL = bit offset: pixel's leftmost bit
C
D874                C      g_addr endp
C
C page
C ;-----
C ;
C ; Scroll Up In Graphics Mode
C ;
C ; Scroll up the number of lines specified within the specified screen
C ; area (window).
C ;
C ; Input:
C ; AL = number of lines to be scrolled up ( zero
C ; means clear the window)
C ; BH = fill pattern to be used
C ; CH,CL = upper left corner of window in which to scroll
C ; DH,DL = lower right corner of window in which to scroll
C ; DS = data segment
C ; ES = graphics refresh ram segment
C ;
C ; Saved: BX, CX, DX (Video dispatcher saves the rest)
C ;
C ;-----
C
D874                C      grf_graphics_up proc near
C
D874 53          C      push  bx            ; save
D875 51          C      push  cx            ; the
D876 52          C      push  dx            ; registers
C
C ;
D877 BD 0050     C      old   flag = increment (from v_scroll_up)
C      mov    bp,80      ; offset to next scanline (CLD => +80)
C
D87A 50          C      push  ax            ; save mode, # rows to scroll
D87B 8B C1      C      mov    ax,cx        ; compute address of window's
D87D E8 DB5F B   C      call  g_sura_off    ; upper left corner
D880 8B F8       C      mov    di,ax        ; save in DI for string instructions
C
D882 06          C      push  es            ; set DS to video ram for string inst.
D883 1F          C      pop   ds
C
D884 2B D1       C      sub    dx,cx        ; compute window's dimensions
D886 81 C2 0101 C      add    dx,101H      ; DH = height, DL = width
C
D88A 58          C      pop   ax            ; AH = mode, AL = # rows to scroll
C
D88B B3 02       C      mov    bl,2         ; # interlace areas = 2 for modes 4,5,6
D88D BA CB       C      mov    cl,bl        ; # scanlines per i.a. = 4 for modes 7,2

```



# ROM BIOS Listing

```

D88F 80 FC 40      C      cmp     ah,64
D892 72 06        C      jb      g_tst_mod      ;jump if mode = 4,5,6
D894 83 04        C      mov     bl,4          ;# interlace areas = 4 for modes 64 & 72
D896 74 02        C      je      g_tst_mod      ;jump if mode = 64
D898 D0 F9        C      sar     cl,1          ;# scanlines per i.a. = 2 for mode 72
D89A             C
D89A D2 E0        C      sal     al,cl         ;convert number of rows to number of
D89C D2 E6        C      sal     dh,cl         ; scanlines per interlace area
D89E 8B C8        C      mov     cx,ax         ;CH = mode, CL = # scanlines to scroll
D8A0 80 FD 06     C      cmp     ch,6          ;are we in a medium resolution mode ?
D8A3 7D 04        C      jge     g_set_up      ;jump if no
D8A5 D1 E7        C      sal     di,1          ;double number of bytes per character
D8A7 D0 E2        C      sal     dl,1
D8A9             C
D8A9 g_set_up:      ;set address of lines to scroll in refresh ram memory
D8AB and     cx,00FFH     ;CX = # of scanlines to scroll per i.a.
D8AD 74 3C        C      jz      g_filler      ;if zero, go fill all of window
D8AF             C
D8AF 8B C1        C      mov     ax,ox         ;make CH = # scanlines to fill per i.a.
D8B1 84 E9        C      mov     ch,cl         ; AI = # scanlines to scroll = "
D8B3 86 F5        C      rcbg   dh,oh         ; CH = # scanlines in window = "
D8B5             C
D8B5 8B F7        C      mov     si,di         ;compute address of scanline to be
D8B7 B1 04        C      mov     cl,4          ; scrolled to top of window:
D8B9 D3 E0        C      sal     ax,cl         ; <window's address> *
D8BB 03 F0        C      add     si,ax         ; ((# scanlines to scroll per i.a.) *
D8BD D1 E0        C      sal     ax,1          ; (<# bytes per scanline = 80>))
D8BF D1 E0        C      sal     ax,1
D8C1 03 F0        C      add     si,ax
D8C3             C
D8C3 8A E5        C      mov     ah,oh         ;compute # of scanlines per i.a.
D8C5 2A E6        C      sub     ah,dh         ; to be moved
D8C7             C
D8C7 33 C9        C      xor     cx,ox         ;CH = 0 for REP counter
D8C9             C
D8C9 jmp     short g_scroller ;go scroll up and fill
D8CB             C
D8CB grf_graphics_up endp
D8CD             C
D8CD page
D8CE             C
D8CE ;-----
D8CF ;
D8CF ; Scroll rows in graphics refresh memory
D8D0 ;
D8D1 ; Input:
D8D2 ; AH = Number of scanlines per interlace area to be moved
D8D3 ; BL = Number of interlace areas
D8D4 ; CH = 0
D8D5 ; DI = Destination scanline address of first byte to fill
D8D6 ; SI = Source scanline address of first byte to fill
D8D7 ; DL = Number of bytes to fill in each scanline
D8D8 ; BP = offset to next scanline (+/- 80)
D8D9 ;
D8DA ; Output:
D8DB ; DI = address of first byte to be filled
D8DC ; AH = 0
D8DD ;
D8DE ; BL,BH,CH,DL,DH,BP preserved
D8DF ;-----
D8E0             C
D8E0 g_scroller   proc   near
D8E1             C
D8E1 56             C      push  si             ;save original source
D8E2 57             C      push  di             ; and destination addresses
D8E3 53             C      push  bx             ;save interlace areas count (BL)
D8E4             C
D8E4 g_m_area:      ;Move Interlace Areas Loop
D8E5 57             C      push  di             ;save interlace area
D8E6 56             C      push  si             ; addresses
D8E7 84 CA        C      mov     cl,di         ;count of bytes to be moved
D8E8 D0 F3/ A4     C      rep     movsb         ;move the scanline
D8E9 D2 5E        C      pop     si             ;restore interlace area
D8EA D3 5F        C      pop     di             ; addresses
D8EB D4 81 CT 2000 C      add     di,2000H      ;next interlace area
D8EC D8 B1 C6 2000 C      add     si,2000H      ; addresses
D8ED DC FE CB     C      dec     bl             ;loop to move one scanline in
D8EE D8 D5 EC     C      jnz     g_m_area     ; each interlace area
D8EF             C
D8EF 5B             C      pop     bx             ;restore interlace areas count (BL)
D8F0 5F             C      pop     di             ;restore original source
D8F1 5E             C      pop     si             ; and destination addresses
D8F2 83 FD        C      add     di,bp         ;address next scanline in
D8F3 83 F5        C      add     si,bp         ; each interlace area
D8F4 DC CC        C      dec     ah             ;loop to move "all" scanlines in
D8F5 D8 E9        C      jnz     g_scroller   ; each interlace area
D8F6             C
D8F6 jmp     short g_filler ;now fill in the gap
D8F7             C
D8F7 g_scroller   endp
D8F8             C
D8F8 page
D8F9             C
D8F9 ;-----
D8FA ; Fill rows in graphics refresh memory with the fill pattern
D8FB ;
D8FC ;
D8FD ; Input:
D8FE ; BL = Number of interlace areas

```

# ROM BIOS Listing

```

C ;           BH =   Fill pattern to be used
C ;           CH =   0
C ;           DL =   Number of bytes to fill in each scanline
C ;           DH =   Number of scanlines to fill in each interlace area
C ;           DI =   Destination scanline address of first byte to fill
C ;           BP =   offset to next scanline (+/- 80)
C ;
C ;           Output: AL =   fill pattern
C ;                   AH =   0
C ;
C ;-----
D8EB          C   grf_filler      proc near
C
D8EB 8A C7    C           mov     al,bh           ;AL = fill pattern for STOSB instruction
C
D8ED          C   grf_i_lp:      ;Fill Interlace Areas Loop
D8ED 57      C           push    di           ;save interlace area address
D8EE 52      C           push    dx           ;save scanlines count (DH)
C
D8EF          C   grf_a_lp:      ;Fill Scanlines Loop
D8EF 57      C           push    di           ;save scanline address
D8F0 8A CA    C           mov     cl,di         ;count of bytes to fill in scanline
D8F2 F3/ AA   C           rep     stosb        ;fill scanline
D8F4 5F      C           pop     di           ;restore scanline address
D8F5 03 FD    C           add     di,bp         ;next scanline in interlace area
D8F7 FE CE    C           dec     dh           ;fill an interlace area
D8F9 75 F4    C           jnz    grf_a_lp
C
D8FB 5A      C           pop     dx           ;restore scanlines count (DH)
D8FC 5F      C           pop     di           ;restore interlace area address
D8FD 81 C7 2000 C           add     di,2000H     ;next interlace area address
D901 FE CB    C           dec     bl           ;fill next interlace area
D903 75 B8    C           jnz    grf_i_lp
C
D905 5A      C           pop     dx           ;restore
D906 59      C           pop     cx           ;       the
D907 5B      C           pop     bx           ;       registers
D908 C3      C           ret                ;exit scroll routine
C
D909          C   grf_filler      endp
C
C   page
C ;-----
C ;           Scroll Down In Graphics Mode
C ;
C ;           Scroll down the number of lines specified within the specified screen
C ;           area (window).
C ;
C ;           Input:
C ;           AL = number of lines to be scrolled up ( zero
C ;                 means clear the window)
C ;           BH = fill pattern to be used
C ;           CH,CL = upper left corner of window in which to scroll
C ;           DH,DL = lower right corner of window in which to scroll
C ;           DS = data segment
C ;           ES = graphics refresh ram segment
C ;
C ;           Saved: BX, CX, DX (Video dispatcher saves the rest)
C ;
C ;-----
D909          C   grf_graphics_down  proc near
C
D909 53      C           push    bx           ; save
D90A 51      C           push    ox           ;       the
D90B 52      C           push    dx           ;       registers
C
D90C BD FF B0 C ;           std     bp,-80     ;dir. flag = decrement (from v_scroll_ds)
C ;           ;offset to next scanline (STD => -80)
C
D90F 50      C           push    ax           ;save mode, # rows to scroll
D910 8B C2    C           mov     ax,dx         ;compute address of window's
D912 EB 0B 5F R C           call    g_cursor_of  ; lower right corner
D915 8B F8    C           mov     di,ax         ; save in DI for string instructions
C
D917 06      C           push    es           ;set DS to video ram for string inst.
D918 1F      C           pop     ds
C
D919 2B D1    C           sub     dx,ox         ;compute window's dimensions
D91B 81 C2 010 C           add     dx,1C1H      ; DH = height, DL = width
C
D91F 58      C           pop     ax           ;AH = mode, AL = # rows to scroll
C
D920 B3 02    C           mov     bl,2         ;# interlace areas = 2 for modes 4,5,6
D922 8A CB    C           mov     ol,bl        ;# scanlines per i.a. = 4 for modes 72
D924 80 FC 40 C           cmp     ah,64        ;
C           ;
D927 72 06    C           jb     g_cmp_mod     ;jump if mode = 4,5,6
D929 B3 04    C           mov     bl,4         ;# interlace areas = 4 for modes 64 & 72
D92B 74 02    C           je     g_cmp_mod     ;jump if mode = 64
D92D D0 F9    C           sar     ol,1         ;# scanlines per i.a. = 2 for mode 72
C
D92F          C   g_cmp_mod:
D92F D2 E0    C           sal     al,cl        ;convert number of rows to number of
D931 D2 E6    C           sal     dh,cl        ; scanlines per interlace area
D933 80 FC 06 C           cmp     ah,6         ;are we in a medium resolution mode ?
D936 7D 05    C           jge    g_setdown    ;jump if no
D938 D1 E7    C           sal     di,1         ;double number of bytes per character

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# ROM BIOS Listing

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D93A D0 E2      C      sal    dl,1
D93C 47         C      inc    dl                ;address last byte in bottom row
C
C      g_setdown: ;get address of lines to scroll in refresh RAM memory
D93D BE 0050   C      mov    si,80          ;address bottom scanline in i.a.
D940 D3 E6     C      sal    si,01
D942 83 EE 50   C      sub    si,80
D945 03 FE     C      add    di,si
D947 8B C8     C      mov    cx,ax
D949 81 E1 00FF C      and    cx,00FFH
D94D 74 9C     C      jz     g_filler
C
D94F 8B C1     C      mov    ax,cx
D951 8A E9     C      mov    ch,01
D953 86 F5     C      xchg  dh,ch
C
D955 8B F7     C      mov    si,di
D957 B1 04     C      mov    cl,4
D959 D3 D0     C      sal    ax,cl
D95B 2B F0     C      sub    si,ax
D95D D1 E0     C      sal    ax,1
D95F D1 E0     C      sal    ax,1
D961 2B F0     C      sub    si,ax
C
D963 8A E5     C      mov    ah,05
D965 2A E6     C      sub    ah,dh
C
D967 33 C9     C      xor    cx,cx
C
D969 E9 D8C9 R  C      jmp    g_scroller      ;go scroll down and fill
C
D96C          C      grf_graphics_down   endp
C
C      page
C      ;-----
C      ;
C      ; graphics_read - read the character at the current cursor
C      ; position on the screen, or zero.
C      ;
C      ; Input: none
C      ;
C      ; Output: AL = character at the current cursor position or zero
C      ;
C      ; Saved: BX, CX, DX (video dispatcher saves the rest)
C      ;-----
C
D96C          C      grf_graphics_read   proc   near
C
D96C 53         C      push   bx                ; save
D96D 51         C      push   cx                ; the
D96E 52         C      push   dx                ; registers
C
D96F 8A DC     C      mov    bl,ah              ;BL saves v_mode
D971 A1 0050 R C      mov    ax,word ptr ds:[v_cursor]
D974 EB D85F R C      call  g_our_off          ;get address of cursor position
D977 8B F0     C      mov    si,ax              ;save as a pointer for later
C
D979 8A C3     C      mov    al,bl              ;AL saves v_mode
D97B B9 0004   C      mov    cx,4
D97E 33 DB     C      xor    bx,bx              ;# scanlines per i.a. = 4 for modes 72
D980 3C 40     C      cmp    al,64              ;make BX=0 for modes 4,5,6
D982 72 08     C      jb     g_lda_r            ;jump if mode = 4,5,6
D984 B3 04     C      mov    bl,4              ;make BX=4 for mode 64
D986 74 04     C      je     g_lda_r            ;jump if mode = 64
D988 D1 F9     C      sar    cx,1              ;# scanlines per i.a. = 2 for mode 72
D98A 33 DB     C      xor    bx,bx              ;make BX=0 for mode 72
C
D98C          C      g_lda_r:              ;(BX= font pointer offset in master table)
D98C C5 3E 0084 R C      lds    di,dword ptr ds:[master_tbl_ptr] ;get pointer to master table
D990 C5 79 06   C      lds    di,dword ptr ds:[di+6][bx] ;get pointer to font's 1st 128 chars
D993 1E       C      push  ds
D994 06       C      push  es
D995 1F       C      pop   ds
D996 07       C      pop   es
C
D997 D1 E3     C      sal    bx,1              ;make BX=8 for modes 4,5,6,72
D999 83 C3 08   C      add    bx,8              ; BX=16 for mode 64
C
D99C 2B E3     C      sub    sp,bx              ;get stack space for font bytes
D99E 8B EC     C      mov    bp,sp              ;save pointer to stack space
D9A0 BA 0002   C      mov    dx,2              ;number of interlace areas (modes 4,5,6)
D9A3 3C 06     C      cmp    al,6              ;check graphics mode
D9A5 7C 33     C      jll   g_rd_med           ;jump if in medium resolution mode (4,5)
D9A7 74 03     C      je     g_rd_loop         ;jump if in 640x200 resolution mode (6)
C
D9A9 BA 0004   C      ; we're in super resolution (640x400) mode (64 & 72)
C      mov    dx,4              ;number of interlace areas
C
D9AC          C      g_rd_loop:           ;Read Scanlines Loop for both 640x200 and 640x400
D9AC push    cx                ;save # of scanlines per interlace area
D9AD push    si                ;save current addr. in interlace area #1
D9AE 8B CA     C      mov    cx,dx              ;init. counter: # of interlace areas
C
D9B0          C      g_rd_la:             ;Read Interlace Area Loop
D9B0 8A 04     C      mov    al,[si]
D9B2 8B 46 00 C      mov    [bp],al
D9B5 45       C      inc    bp
D9B6 81 C6 2000 C      add    si,2000H
D9B8 E2 F4     C      loop  g_rd_la

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# ROM BIOS Listing

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C
C
D9BC 5E          C      pop     si          ;restore interlace area #1 address
D9BD 83 C6 50   C      add     si,80       ;address next scanline in each i.a.
D9C0 59         C      pop     cx          ;restore # of scanlines counter
D9C1 E2 B9     C      loop   g_rdloop
C
C
D9C3 83 FA 04   C      cmp     dx,4        ;are we in mode 64 or 72 (640x400)?
D9C4 75 47     C      jno    g_matchb    ;jump if no (reverse video not allowed)
D9C8 8B F5     C      mov     si,bp      ;point to first byte in stack save area
D9CA 2B F3     C      sub     si,bx
D9CC F6 04 80   C      test   byte ptr [si],80H ;is upper left bit of char = 0 or 1 ?
D9CF 74 3E     C      jz     g_matchb    ;jump if 0 (not reversed video)
D9D1 8B CB     C      mov     cx,bx      ;number of char bytes counter
D9D3          C      g_unreverse_video_loop:
D9D3 F6 14     C      not    byte ptr [si] ;reverse the reversed byte for matching
D9D5 46     C      inc    si          ;address next char byte
D9D6 E2 FB     C      loop   g_unreverse_video_loop
D9D8 EB 35     C      jmp    short g_matchb ;now find the char in the font table
C
C
D9DA          C      g_rd_med:          ;Read Medium Resolution
D9DA D1 E6     C      sal    si,1       ;double graf ram pointer (2 bytes/char)
C
C
D9DC          C      g_medget:         ;Get font bytes in medium resolution (320 X 200) mode
D9DC 51         C      push   cx          ;save # scanlines per i.a. counter
D9DD 56         C      push   si          ;save current scanline address
D9DE B9 0002   C      mov    cx,2       ;init. # interlace areas counter
D9E1          C      g_med_la:
D9E1 51         C      push   cx          ;save i.a. counter
D9E2 8B 04     C      mov    ax,[si]    ;get 2 bytes of 1 char from video memory
D9E4 86 E0     C      xorb  ah,al      ;order them logically
C
C
D9E6 F7 D0     C      not    ax          ;map background pixels to 0,
D9E8 8B D0     C      mov    dx,ax      ; foreground pixels to 1
D9EA D1 E2     C      shl    dx,1
D9EC 23 D0     C      and   dx,ax
D9EE F7 D2     C      not    dx
C
C
D9F0 32 C0     C      xor    al,al      ;clear result accumulator
D9F2 B9 0008   C      mov    cx,8       ;prepare to process 8 bits
D9F5          C      g_med_bit:
D9F5 D1 EA     C      shr    dx,1       ;ignore unused bit
D9F7 E1 EA     C      shr    dx,1       ;load carry with mapped pixel value
D9F9 D0 D8     C      ror    al,1       ;rotate it into result accumulator
D9FB E2 F8     C      loop  g_med_bit  ;process next bit of character
C
C
D9FD 8B 46 00   C      mov    [bp],al    ;save font byte on reserved stack
DA00 45     C      inc   bp          ;bump reserved stack pointer
DA01 81 C6 2000 C      add   si,2000H   ;address next interlace area
DA05 59     C      pop   cx          ;restore i.a. counter
DA06 E2 D9     C      loop  g_med_la  ;process next i.a. of character
C
C
DA08 5E     C      pop   si          ;restore scanline address
DA09 83 C6 50   C      add   si,80      ;address next scanline
DA0C 59     C      pop   cx          ;restore scanlines counter
DA0D E2 CD     C      loop  g_medget  ;process next scanline of character
C
C
DA0F          C      g_matchb:         ;Match Font Byte: find character
C
C
DA0F 2B EB     C      sub   bp,bx      ;point to first byte in stack save area
DA11 8B F5     C      mov   si,bp      ;pointer to font bytes from graf ram
DA13 32 C0     C      xor   al,al      ;index to font bytes (start with 0)
DA15          C      g_f_cont:         ; Get Font Byte Match Control
DA15 16     C      push  ds         ;setup string compare registers
DA16 1F     C      pop   ds         ;DS:SI -> stack area w/grafix ram bytes
DA17 B9 0080   C      mov   cx,128    ;loop control = 1st 128 ascii chars.
C
C
DA1A          C      g_f_match:       ;Get Font Byte Match Loop
DA1A 51     C      push  cx         ;save loop counter
DA1B 8B CB     C      mov   cx,bx      ;counter for string compare
DA1D 57     C      push  di         ;save font pointer
DA1E 56     C      push  si         ;save pointer to stack save area
DA1F F3/ A6   C      rep  scasd       ;scan bytes match font bytes ?
DA21 5E     C      pop   si         ;retrieve pointer to stack save area
DA22 5F     C      pop   di         ;retrieve pointer to font byte table
DA23 59     C      pop   cx         ;restore loop counter
DA24 74 2D     C      jz    g_f_exit   ;if match go to exit code
DA26 03 FB     C      add   di,bx      ;address next font in table
DA28 FE C0     C      inc  al          ;bump ascii index
DA2A E2 EE     C      loop  g_f_match  ;go back if more chars to search for
C
C
; no match in first 128 ascii character set - look for user's second set
C
C
DA2C 0A C0     C      or    al,al      ;have we scanned both 128 char 1/2s ?
DA2E 74 23     C      jz    g_f_exit   ;jump if yes to exit code
DA30 83 FB 10   C      cmp   bx,16      ;are we in mode 64 ?
DA33 74 08     C      je    g_8x16_2   ;jump if yes
C
C
DA35 8E D9     C      mov  ds,cx       ;save zero to segment register
C
C
DA37 C4 3E 007C R C      assume ds:aba0
DA37 0A 00 7C R C      lea  di,dword ptr ds:[int1Floocn] ;get pointer to 2nd half of 8x8 font
DA3B EB 0C     C      assume ds:data
C
C
; see if font is really there
C
C
DA3D          C      g_8x16_2:
DA3D 2E: 8E 1E ESP2 R C      mov  ds,word ptr es:[set_ds_word] ;set DS to data segment
DA42 C5 3E 00B4 R C      lds  di,dword ptr ds:[master_tbl_ptr] ;get pointer to master table
DA46 C4 7D 0E     C      lea  di,dword ptr ds:[di+1] ;get pointer to 2nd half of 8x16 font
C
C
DA49          C      g_test_addr:
DA49 8C C0     C      mov  ax,es       ;check if font table is set up

```

# ROM BIOS Listing

```

D48B 0B C7      C      or      ax,di          ;if zeros, then no user font table
D48D 74 04      C      js       g_f_exit        ;no table, just go to exit
D48F 80 80      C      mov      al,128          ;offset to 2nd 1/2 of ascii set
D491 EB C2      C      jmp      short g_f_cont    ;go back to try rest of ascii set

D493           C      g_f_exit:                ;either the character is found, or al = 0
D495 03 E3      C      add      sp,bx           ;restore stack pointer
D497 5A         C      pop      dx             ;restore
D499 59         C      pop      cx             ;       the
D49B 5B         C      pop      bx             ;       registers
D49D C3         C      ret

D499           C      grf_graphics_read      endp

C      page
C      ;=====
C      ;
C      ; graphics_write - write a character to the screen
C      ;
C      ; Input: AL = character to write
C      ;         BL = foreground color attribute
C      ;         bit 7 = 1: xor character with graphics ram
C      ;         CX = number of characters to write
C      ;         DS = data segment
C      ;         ES = graphics ram segment
C      ;
C      ; Saved: BX, CX, DI (video dispatcher saves the rest)
C      ;
C      ;-----

D499           C      grf_graphics_write   proc   near

D499 53         C      push     bx           ;save
D49A 51         C      push     cx           ;   the
D49B 52         C      push     dx           ;   registers

D49C 8B D0      C      mov      dx,ax          ;DH= ort mode, DL= char to write
C      ; locate beginning of character in graphics ram
D49E A1 0050 R  C      mov      ax,word ptr ds:[v_curpos]
D4A1 8B D85F R  C      call    g_cur_off       ;get address of cursor position
D4A4 8B F8      C      mov      di,ax          ; pointer to graphics location
C      ; determine if character is from 1st or 2nd half of table
D4A6 90 FA 80   C      cmp      di,128         ;is it in first 1/2 of ASCII set ?
D4A9 72 26      C      jb       g_selfont      ;jump if in 1st 1/2 (0 -> 127)

C      ; character (128 -> 255) is in 2nd 1/2 of font table

D4AB 80 EA 80   C      sub      di,128         ;make zero origin for font table lookup
D4AD 80 FE 40   C      cmp      db,64         ;are we in mode 64 ?
D4AF 75 09      C      jne     g_8x8_2        ;jump if no

D4B3 C5 36 0084 R C      lds     si,dword ptr ds:[master_tbl_ptr] ;get pointer to master table
D4B7 C5 74 0E   C      lds     si,dword ptr ds:[si+1a] ;get pointer to 2nd half of 8x16 font

D4B9 EB 08      C      jmp      short g_addr_test ;see if font table is really there

D4BB           C      g_8x8_2:                ;get 2nd half of 8x8 font table
D4BD 33 F6      C      xor      si,si          ;move zero to segment register
D4BF 8E DE      C      mov     ds,si
D4C1 assume ds:abs0
D4C3 lds     si,dword ptr ds:[int1Floor] ;get pointer to 2nd half of 8x8 font
D4C5 assume ds:data

D4C7           C      g_addr_test:
D4C9 mov     ax,ds          ;check if font table is set up
D4CB or     ax,si          ;if zeros, then no 2nd half of table
D4CD jnz    g_detmode      ;continue if font table is present
D4CF xor     dx,di         ;substitute null character
D4D1 mov     ds,word ptr cs:[set_ds_word] ;restore data segment register
D4D3 jmp     short g_selfont ;and continue in 1st half of font table

C      ; character (0 -> 127) is in 1st 1/2 of font table

D4D5           C      g_selfont:
D4D7 push    bx            ;preserve register

D4D9 33 D8      C      xor     bx,bx          ;make BX=0 for modes 4,5,6
D4DB 8B F4 40   C      cmp     db,64         ;
D4DD jb     g_lds_w        ;jump if mode = 4,5,6
D4DF mov     bl,4          ;make BX=4 for mode 64
D4E1 je     g_lds_w        ;jump if mode = 64
D4E3 xor     bx,bx          ;make BX=0 for mode 72

D4E5           C      g_lds_w:                ;(BX= font pointer offset in master table)
D4E7 lds     si,dword ptr ds:[master_tbl_ptr] ;get pointer to master table
D4E9 lds     si,dword ptr ds:[si-6][bx] ;get pointer to font's 1st 128 chars

D4EB           C      pop     bx            ;restore register

D4ED           C      g_detmode:                ;determine graphics mode
D4EF push    cx
D4F1 xor     ax,ax          ;get ascii code in AX
D4F3 mov     al,di         ;
D4F5 mov     cl,3          ;
D4F7 sal     ax,cl        ; 8 (font bytes per character)
D4F9 pop     cx
D4FB add     si,ax          ;and add to address of font table
D4FD C

D499           C      mov     dl,4          ;# scanlines per i.a. (modes 4,5,6,64)

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# ROM BIOS Listing

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DAB5 80 FE 06      C      cmp      dh,6           ;which resolution are we using?
DAB8 7C 49         C      jll      g_med_wr      ;jump if medium resolution (modes 4 & 5)
DABA 74 0F         C      je      g_hi_wr       ;jump if 640x200 resolution (mode 6)
                        C
                        C      ;we're in 640x400 resolution
DABC 80 FE 48     C      cmp      db,72        ;mode 7?
DABF B6 04         C      mov      db,4         ; interlace areas = 4 for modes 64 & 72
DAC1 75 04         C      jne      g_super_wr
                        C
DAC3               C      g_tinytext:        ;640x400 resolution (mode 72)
DAC3 B2 02         C      mov      di,2         ; # scanlines per i.a. = 2 for mode 72
DAC5 EB 09         C      jmp      short g_rephar
                        C
DAC7               C      g_super_wr:        ;640x400 resolution (mode 64)
DAC7 03 F0         C      add      si,ax        ;multiply ascii code by 16 bytes/char
DAC9 EB 05         C      jmp      short g_rephar
                        C
DACB               C      g_bi_wr:          ;Hi-resolution Character Write
DACB B6 02         C      mov      dh,2        ;interlace areas count (even/odd)
DACD 80 CB 01      C      or      bl,1         ;mode 6 doesn't allow reverse video
                        C
DADO               C      g_rephar:         ;Repeat Character Loop
DADO 51             C      push     cx           ;save character repeat count
DAD1 56             C      push     si           ;save source address (font table)
DAD2 57             C      push     di           ;save destination addr. (grafix ram)
DAD3 33 C9         C      xor      cx,ox        ;prepare loop counter
DAD5 8A CA         C      mov      ol,dl       ;scanlines per interlace area counter
                        C
DAD7               C      g_linelp:        ;Scanline Loop
DAD7 51             C      push     dx           ;save scanlines per i.a. counter
DAD8 57             C      push     di           ;save interlace area #1 address
DAD9 8A CE         C      mov      ol,dh       ;init. interlace areas counter (2 or 4)
                        C
DADB               C      g_i_a_lp:        ;Interlace Area Loop
DADB AC             C      lodsb          ;get byte from font table
DADC F6 C3 01      C      test     bl,1         ;reverse video?
DADF 75 02         C      jnz      g_t_xor     ;jump if no
DAE1 F6 D0         C      not      al          ;reverse video
DAB3               C      g_t_xor:         ;Test For XOR
DAB3 0A DB         C      or      bl,bl       ;XOR the char. with grafix ram?
DAE5 79 03         C      jns     g_w_byte     ;jump if no
DAE7 26: 32 05     C      xor      al,es:[di]  ;XOR with grafix ram
DARA               C      g_w_byte:        ;Write Byte
DARA 26: 88 05     C      mov      mov     es:[di],al ;write byte in grafix ram
DAB4 26: 00 00     C      add      di,2000H    ;address next interlace area
DAF1 B2 E8         C      loop    g_i_a_lp
                        C
DAF3 5F             C      pop      di           ;restore interlace area #1 address
DAF4 83 C7 50      C      add     di,80        ;address next scanline in each i.a.
DAF7 59             C      pop      cx           ;restore scanlines per i.a. counter
DAF8 B2 DD         C      loop    g_linelp
                        C
DAFA 5F             C      pop      di           ;restore char's grafix ram address
DAFB 47             C      inc     di           ;address next character in grafix ram
DAFC 58             C      pop      si           ;restore char's font table address
DAFD 59             C      pop      cx           ;restore character repeat count
DAFE B2 DD         C      loop    g_rephar    ;repeat the character
DB00 EB 55 90      C      jmp      g_return     ;exit
                        C
DB03               C      g_med_wr:        ;Medium Resolution Character Write
DB03 D1 E7         C      sal     di,1         ;double graf ram pointer (2 bytes/char)
DB05 8A D3         C      mov     di,bl        ;DL saves XOR bit input param (bit 7)
DB07 81 E3 0003    C      and    bx,0003H     ;BX: foreground color (& table offset)
DB08 2E: 8A 9F DB5B R C      mov     bl,es:g_color_table[bx] ;propagate color through byte
DB10 8A FB         C      mov     bh,bl        ;propagate color through word
DB12 8B EB         C      mov     bp,bx        ;BP saves word of color masks
                        C
DB14               C      g_char_lp:       ;Repeat Character Loop
DB14 51             C      push     cx           ;save character repeat counter
DB15 56             C      push     si           ;save source address (font table)
DB16 57             C      push     di           ;save destination addr. (grafix ram)
DB17 B9 0004       C      mov     cx,4         ;init. scanlines per i.a. counter
                        C
DB1A               C      g_scan_lp:       ;Scanline Loop
DB1A 51             C      push     cx           ;save scanlines per i.a. counter
DB1B 57             C      push     di           ;save interlace area #1 address
DB1C B9 0002       C      mov     cx,2         ;init. interlace areas counter
                        C
DB1F               C      g_i_a_lp:        ;Interlace Area Loop
DB1F 51             C      push     cx           ;save i.a. counter
DB20 AC             C      lodsb          ;get
                        C
DB1F 51             C      push     cx           ;save i.a. counter
DB20 AC             C      lodsb          ;get a byte from the font table
DB21 8A E0         C      mov     ah,al        ;copy it
DB23 B9 0008       C      mov     cx,8         ;init. loop counter (8 bits/byte)
                        C
DB26               C      g_exp_byt:       ;Expand Byte Loop
DB26 D0 EC         C      shr     ah,1         ;load carry with font byte bit
DB28 D1 DB         C      ror     bx,1         ;rotate it into expansion accumulator
DB2A D0 EB         C      shr     al,1         ;load carry with same bit as before
DB2C D1 DB         C      ror     bx,1         ;double the bit
DB2E E2 F6         C      loop   g_exp_byt    ;expand font byte bits
                        C
DB30 23 DD         C      and    bx,bp        ;color pixels with foreground color
DB32 86 FB         C      xchg   bh,bl        ;reorder the bytes for grafix ram
DB34 0A D2         C      or     di,dl        ;is the XOR bit set ?
DB36 79 03         C      jns     g_med_store  ;jump if no
DB38 26: 33 1D     C      xor     bx,es:[di]  ;XOR with grafix ram

```

```

DB3B          C  _end_store:
DB3B 26: 89 1D C      mov     es:[di],bx      ;update grafix ram
DB3E 81 C7 2000 C      add     di,2000H          ;address next interlace area
DB42 59       C      pop     cx              ;restore i.a. loop counter
DB43 E2 DA    C      loop    g_ia_lp          ;next interlace area
C
DB45 5F       C      pop     di              ;restore interlace area #1 address
DB46 83 C7 50 C      add     di,80            ;address next scanline in each i.a.
DB49 59       C      pop     cx              ;restore scanline loop counter
DB4A E2 CE    C      loop    g_scan_lp       ;next scanline
C
DB4C 5F       C      pop     di              ;restore char's grafix ram address
DB4D 47       C      inc     di              ;address next character in grafix ram
DB4E 47       C      inc     di              ;
DB4F 5E       C      pop     si              ;restore char's font table address
DB50 59       C      pop     cx              ;restore character repeat count
DB51 E2 C1    C      loop    g_char_lp       ;repeat the character
C
DB53 8A E3    C      mov     ab,bl           ;return AX with last word written
DB55 8A C7    C      mov     al,bh
C
C  _return:
DB57          C      _return:                ;Return from Write Char
DB57 5A       C      pop     dx              ;restore
DB58 59       C      pop     cx              ; the
DB59 5B       C      pop     bx              ; registers
DB5A C3       C      ret
C
DB5B          C  _color_table label byte ;Table of foreground colors extended to byte
C
DB5B 00       C      db     00000000B        ;color 0 (bit pattern: 00)
DB5C 55       C      db     01010101B        ;color 1 (bit pattern: 10)
DB5D AA       C      db     10101010B        ;color 2 (bit pattern: 01)
DB5E FF       C      db     11111111B        ;color 3 (bit pattern: 11)
C
DB5F          C  grf_graphics_write endp
C
C  page
C ;-----
C ;
C ; Get offset into graphics ram refresh memory which corresponds to
C ; the current cursor position (or any arbitrary character position).
C ;
C ; Input: AX = current cursor position (AL = Column #, AH = Row #)
C ;
C ; Output: AX = offset into graphics ram
C ;-----
C
DB5F          C  _cura_off proc near

```

# ROM BIOS Listing

```

DB5F 51          C          push    cx          ;save work register
DB60 8A EB      C          mov     ah,ah       ;hold column number
DB62 8A C4      C          mov     al,ah       ;row number to al
C
C
DB64 B1 01      C          mov     cl,1        ;mode 72 shift count (multiply * 2)
DB66 80 3E 0049 R 48 C          cmp     byte ptr ds:[v_mode],72
DB68 74 02      C          js     &_72        ;jump if mode 72
DB6D FE C1      C          inc     cl          ;mode 72 shift count (multiply * 3)
C
C
DB6F           C          &_72:
DB6F D2 E0      C          shl     al,cl       ;multiply row # by rows per byte
DB71 32 C9      C          xor     cl,cl       ;zero out the shift count
DB73 86 E9      C          xchg   ch,cl       ;move column number for add
DB75 F6 26 004A R C          mul     byte ptr ds:[v_width] ;multiply by bytes per column
DB79 03 C1      C          add     ax,cx       ;compute offset into refresh ram
DB7B 59         C          pop     cx          ;restore register
DB7C C3         C          ret                ;and return to caller
C
C
DB7D           C          &_cura_off      endp
C
DB7D           C          code ends
C          include pwrup1.asm
C
C
C          ;=====
C          ;          Filename:          pwrup1.asm
C          ;
C          ;          This module includes CPU, ROM, 8253 p_dma p_timer, & 8237 p_dma
C          ;          Controller tests.
C          ;
C          ;=====
C
DB7D           C          code segment public 'ROM'
C          assume cs:code, ds:nothing, es:nothing, as:nothing
C
DB7D           C          pi_data1      proc      near
C
DB7D 90         C          even                ; word-align stack_rom
C
DB7E DBB2 R      C          stack_rom      dw      i_rom          ; return from i_opu
DB80 DBB8 R      C          dw      i_rom_ret    ; return from rom_checkoum
DB82 DDC7 R      C          dw      i_dmat       ; return from i_rom
DB84 DDD3 R      C          dw      i_dmat_ret    ; return from rto_ohk
DB86 DDE2 R      C          dw      i_dmac        ; return from i_dmat
DB88 DD51 R      C          dw      i_dmac_ret    ; return from asstat
DB8A DDE8 R      C          dw      i_pic         ; return from i_dmac
C
C
DB8C 52 65 73 69 64 65 C          banner_m      db      'Resident Diagnostics',CR,LF
C          6E 74 20 44 69 61
C          67 6E 6F 73 74 69
C          63 73 0D 0A
C
DBA2 52 65 76 20 31 2E C          db          'Rev 1.0 May 1984',CR,LF,LF,NUL
C          30 20 20 4D 61 79
C          20 31 39 38 34 0D
C          0A 0A 00
C
C
DBB7 0D 0A 50 72 69 6D C          bt_m          db          CR,LF,'Primary Boot-Strap...',CR,LF,NUL
C          61 72 79 20 42 6F
C          6F 74 2D 53 74 72
C          61 70 2E 2E 2E 0D
C          0A 00
C
C
DBD1 50 72 69 6D 61 72 C          bt_merr       db          'Primary Boot-Strap DISK READ ERROR.',CR,NUL
C          79 20 42 6F 6F 74
C          2D 53 74 72 61 70
C          20 44 49 53 4B 20
C          52 45 41 44 20 45
C          52 52 4F 52 2E 0D
C          00
C
C
DBF6 20 20 20 20 20 20 C          ; This line must have same number of blanks as the preceding has characters:
C          bt_spaces      db          ' ',CR,NUL
C          20 20 20 20 20 20
C          20 20 20 20 20 20
C          20 20 20 20 20 20
C          20 20 20 20 20 20
C          20 20 20 20 20 20
C          20 20 20 20 20 0D
C          00
C
C
DC1B 2A 20 49 6C 6C 65 C          ill_m1       db          '* Illegal Interrupt No. ',NUL
C          67 61 20 49 6E
C          74 65 72 72 75 70
C          74 20 4E 6F 2E 20
C          00
C
C
DC3A 68 20 61 74 20 00 C          ill_m2       db          'h at ',NUL
C          20 2A 00
C          ill_m3       db          ' ',NUL
C
C
DC3D 20 50 61 73 73 0D C          pass_m      db          ' Pass',CR,LF,NUL
C          0A 00
C
DC45 20 46 61 69 6C 00 C          fail_m      db          ' Fail',NUL
C
C
DC4B 43 50 55 20 28 69 C          i_cpu_m     db          'CPU (i8086) ',NUL          ; Pass/Fail
C          38 30 38 36 29 20
C          00
C
DC58 52 4F 4D 20 4D 6F C          i_rom_m     db          'ROM Module ',NUL          ; Pass/Fail
C          64 75 6C 65 20 20
C          00
C
DC65 44 4D 41 20 54 69 C          i_dmat_m    db          'DMA Timer ',NUL          ; Pass/Fail
C          6D 65 72 20 20 20
C          00
C
DC72 44 4D 41 20 43 6F C          i_dmac_m    db          'DMA Control ',NUL          ; Pass/Fail
C          6E 74 72 6F 6C 20
C          00
C

```



# ROM BIOS Listing

```

DCTF 49 6E 78 65 72 72 C i_pic_m db 'Interrupts ',NUL ; Pass/Fail/Fail:Hx
      75 70 74 73 20 20 C
      00 C
DC8C 56 69 64 65 6F 20 C i_d_m db 'Video Board ',NUL ; Pass/Fail
      42 6F 61 72 64 20 C
      00 C
DC99 4E 50 55 20 28 69 C i_npu_m db 'NPU (18087) ',NUL ; Pass/Fail
      38 30 38 37 29 20 C
      00 C
DCA6 52 54 20 43 6C 6F C i_rtc_m db 'RT Clock ',NUL ; Pass/Fail/Fail:L0,HI,WR
      63 68 20 20 20 20 C
      00 C
DCB3 3A 4C 4F 00 C i_rtc_lo_m db ':L0',NUL ; Error #1 (must remain in
DCB7 3A 4E 49 00 C i_rtc_hi_m db ':HI',NUL ; Error #2 order for addr.
DCB8 3A 4E 52 00 C i_rtc_wr_m db ':WR',NUL ; Error #3 calculation)
DCBF 48 65 79 62 6F 61 C i_kb_m db 'Keyboard ',NUL ; Pass/Fail/Fail:ST
      72 64 20 20 20 20 C
      00 C
DCCC 3A 53 54 00 C i_kb_st_m db ':ST',NUL
DCD0 50 72 69 6E 74 65 C iprt_m db 'Printer Port',NUL ; Pass/Fail:xx
      72 20 50 6F 72 74 C
      00 C
DCDD 53 65 72 69 61 6C C i_com_m db 'Serial Comm.',NUL ; Pass/Fail:xx
      20 43 6F 6D 6D 2E C
      00 C
DCEA 20 6B 62 20 52 41 C i_RAM_m db ' kb RAM ',NUL ; Pass/Fail:00:xxxx:www:rrrr
      40 20 20 00 C
DCFA 4F 70 74 69 6F 6E C i_optROM_m db 'Optional ROM',NUL ; Pass/Fail:xxxx
      61 6C 20 52 4F 4D C
      00 C
DD01 46 6C 6F 70 70 79 C i_fduA_m db 'Floppy (A) ',NUL ; Ready/Not Ready/Fail:xx
      20 28 41 3A 29 20 C
      00 C
DD0E 46 6C 6F 70 70 79 C i_fduB_m db 'Floppy (B) ',NUL
      20 28 42 3A 29 20 C
      00 C
DD1B 20 4E 6F 74 C i_fdu_not_m db ' Not'
DD1F 20 52 65 61 64 79 C i_fdu_rdy_m db ' Ready',CR,LF,NUL ; purposely no NUL!!!!
      0D 0A 00 C
DD28 46 69 78 65 64 20 C i_hdu_m db 'Fixed Disk ',NUL ; Pass/Fail:xx
      44 69 73 6B 20 20 C
      00 C
DD35 53 65 6C 65 63 74 C i_alt_select_m db 'Select Alternate CPU (y/n)?',NUL
      20 41 6C 74 65 72 C
      6E 61 74 65 20 43 C
      50 55 20 28 79 2F C
      6E 29 3F 00 C
      C
      C ; db 'Disk Diagnoston xxxxx'
      C ; db 'Loop Diagnoston xxxxx'
      C ; db 'Primary BootStrap Floppy (A:) Not Ready'
      C ; db 'Insert system disk and type any key.'
      C ; db 'Primary BootStrap Floppy (A:) Fail:xx'
      C ; db 'Primary BootStrap Floppy (B:) Fail:xx'
      C ; db 'Primary BootStrap Fixed Disk Fail:xx'
      C ; db 'Select Operating System?'
      C ; db 'Serial BootStrap'
      C
DD51 0F C i_onl_val db 0Fh ; port 074h = units of minutes (0-9)
DD52 07 C db 07h ; port 075h = tens of minutes (0-5)
DD53 0F C db 0Fh ; port 076h = units of hours (0-9)
DD54 03 C db 03h ; port 077h = tens of hours (0-2)
DD55 0F C db 0Fh ; port 078h = units of days (0-9)
DD56 03 C db 03h ; port 079h = tens of days (0-3)
DD57 07 C db 07h ; port 07Ah = day of week (0-7)
DD58 0F C db 0Fh ; port 07Bh = tens of months (0-9)
DD59 01 C db 01h ; port 07Ch = units of months (0-1)
      C
DD5A C pi_data1 endp
      C
      C ; =====
DD5A C diagnostics_1 proc near
      C assume cs:code, ds:nothing, es:nothing, ss:nothing
      C
      C cli ; disable interrupts
      C mov ax,40h ; Check Point #0
      C mov dx,378h ; parallel port data port address
      C out dx,al ; output "Running-Checkpoint 0"
      C cld ; clear string direction flag
      C
      C ; -----
      C ; 8086 CPU Test
      C ; -----
DD62 C i_opu:
      C ; Flags Test (All Set): SF, ZF, AF, PF, CF & OF.
      C ; (Exercises flags and accumulator only.)
      C
      C mov ax,0FF00h ; ah = all 1's; al = all 0's
      C shlf ; set SF, ZF, AF, PF, & CF
      C jns i_opu_err ; SF set? if not, abort
      C jnz i_opu_err ; ZF set? if not, abort
      C jmp i_opu_err ; PF set? if not, abort
      C jnb i_opu_err ; CF set? if not, abort
      C
      C ; to test if AF is set, al must be <= 9
      C ; if AF set, then: (ah +=1) == 0;
      C ; al = ((al+6) & 0Fh) == 6; CF = AF == 1

```

# ROM BIOS Listing

```

DD6F 73 1C      C      jnb     i_cpu_err      ; CF = AF set?  if not, abort
DD71 0A E4      C      or      ah,ah        ; ah = 0?  if not, abort
DD73 75 18      C      jnz     i_cpu_err
C
C
DD75 80 80      C      mov     al,40h        ; ah = 0
DD77 02 C0      C      add     al,al         ; al = 40h + 40h = 80h = -128
DD79 71 12      C      jno     i_cpu_err      ; OF set?  if not, abort
C
C ; Flags Test (All Reset): SF, ZF, AF, PF, CF & OF.
C ; (Exercises flags and accumulator only.)
C
DD7B 33 C0      C      xor     ax,ax         ; ax = 0
DD7D 9E          C      aahf                    ; reset SF, ZF, AF, PF, & CF
DD7E 78 0D      C      ja     i_cpu_err      ; SF reset?  if not, abort
DD80 76 0B      C      jbe     i_cpu_err      ; ZF or CF reset?  if not, abort
DD82 7A 09      C      jp      i_cpu_err      ; PF reset?  if not, abort
C
DD84 37          C      aaa                    ; to test if AF reset, al must be <= 9
C ; if AF reset, then: ah unchanged;
C ; al = (al & 0Fh) == 0; CF = AF == 0
C ; CF = AF reset?  if not, abort
C ; ax = 0?  if not, abort
DD85 72 06      C      jb     i_cpu_err
DD87 03 C0      C      add     ax,ax
DD89 75 02      C      jnz     i_cpu_err
C ; ax = 0 + 0 = 0, so should be no OF.
C ; OF reset?  if not, abort
DD8B 71 11      C      jno     i_cpu_ok
C
C      assume cs:code, ds:code, es:abs0, ss:code
C
C      i_cpu_err:
DD8D          C      mov     ax,os        ; satisfy assumptions
DD8E 8C C8      C      mov     ds,ax
DD8F 8E D8      C      mov     es,ax        ; use ROM 'stack'
DD91 8E D0      C      mov     sp,os:(offset stack_rom)
DD93 8C DB7E R  C
C
DD96 BE DCAB R  C      mov     si,os:(offset i_cpu_m)
DD98 32 E4      C      xor     ah,ah        ; clear ah (no error number to report)
DD99 E9 E0E9 R  C      jmp     i_fatal      ; i_fatal will 'ret' to i_rom
C
C      i_cpu_ok:
DD9E          C      mov     ax,os        ; satisfy assumptions
DD9F 8E D8      C      mov     ds,ax
DDA2 8E D0      C      mov     es,ax        ; use ROM 'stack'
DDA4 8C DB7E R  C      mov     sp,os:(offset stack_rom)
C
DDA7 80 41      C      mov     al,41h        ; Check Point #1
DDA9 BA 0378   C      mov     dx,378h      ; parallel port data port address
DDAC EE        C      out     dx,al        ; output "Running- Checkpoint 1"
C ; Reset the keyboard
C
DDAD 80 00      C      mov     al,0
DDAF 86 61      C      out     p_kotrl,al
C      ret                    ; will 'ret' to i_rom
C
C ;-----
C ; ROM Module Test
C ;-----
C
C      assume cs:code, ds:code, es:abs0, ss:code
C
C      i_rom:
C
C ; Calculate Checksum of ROM.
C
C      mov     si,0E000h      ; ROM starts at ds:si = F000:E000
C      jmp     rom_checksum   ; 'call' rom_checksum
C      i_rom_ret:            ; will 'ret' here
C      jz      i_rom_ok
C
C      i_rom_err:
C      mov     si,cs:(offset i_rom_m)
C      jmp     i_fatal      ; ah has illegal checksum
C ; i_fatal will 'ret' to i_dmat
C
C      i_rom_ok:
C      mov     al,42h        ; Check Point #2
C      mov     dx,378h      ; parallel port data port address
C      out     dx,al        ; output "Running- Checkpoint 2"
C      ret                    ; will 'ret' to i_dmat
C
C ;-----
C ; 8253 p_dma p_timer Test
C ;-----
C
C      assume cs:code, ds:code, es:abs0, ss:code
C
C      i_dmat:
C
C ; Disable 8237A p_dma Controller before the testing of the 8253 p_dma p_timer channel.
C
C      mov     al,dma_cmd_disable ; disable p_dma controller command
C      out     dma_command,al
C
C ; Proceed with the testing of the 8253 p_dma p_timer channel (i)p_8253_1.
C
C      mov     al,074h        ; 01 11 010 0 -> p_8253_1, 1st 1st, mode 2, no BCD
C      mov     dx,p_8253_1    ; select p_dma refresh counter
C      jmp     rtc_ohk        ; 'call' rtc_ohk
C      i_dmat_ret:          ; will 'ret' here
C      jz      i_dmat_ok

```

# ROM BIOS Listing

```

C
C
DD05          C      i_dmat_err:
DD05 BE DC65 R      mov     si,cs:(offset i_dmat_m)
DD08 E9 E0E9 R      jmp     i_fatal          ; ah has error code to report.
C                                     ; i_fatal will 'ret' to i_dmae
C
C
DDDB          C      i_dmat_ok:
DDDB B0 43          mov     al,43h          ; Check Point #3
DDDD BA 0378        mov     dx,378h        ; parallel port data port address
DD00 E2           out     dx,al          ; output "Running-Checkpoint 3"
DDE1 C3           ret
C                                     ; will 'ret' to i_dmae
C
C-----
C      ;
C      ;      8237 p_dma Controller Test -- Test Chip's Operation & Channel Registers
C      ;
C      ;      The 8237A p_dma Controller was disabled before the testing of the
C      ;      8253 p_dma p_timer channel.
C-----
C
C      assume cs:code, ds:code, es:abs0, ss:code
C
DDE2          C      i_dmae:
C      ; Send a 'master clear' to 8237 p_dma Controller.
DDE2 B6 0D          out     dma_master_clr,al      ; send master clear to port
C
C      ; The dma_command, dma_status, dma_requost, dma_temp, and dma_ff registers
C      ; are cleared, and the dma_mask register is set (all off).
C      ; Test readable control registers: dma_status & dma_temp
C
DDE4 B4 01          mov     ah,1            ; TEMP Error #1
DDE6 B4 0D          in     al,dma_temp
DDE8 DA C0          or     al,al           ; al = 0?
DDEA 75 72          jnz    i_dmae_err      ; if not, abort
C
C      ; Test all 8 16-bit readable/writeable channel registers (address and count
C      ; registers for all 4 channels, i.e., ports 0 through 7) with register bit test:
C      ; (dma_addr_x & dma_count_x are tested with 0FFFFh and then 0h for x = 0 to 3.)
C
DDEC BB FFFF        mov     bx,0FFFFh      ; bx = 0 all bits reset
DDEF          C      i_dmae_pass2:
C      ; outer loop
C      ; if 1st pass, bx = 0FFFFh
C      ; if 2nd pass, bx = 0h
C      ; loop counter and port address!!!
DDEF BA 0007        mov     dx,7
C
C      i_dmae_lp:
C      ; inner loop
C      ; get bit test pattern
C      ; write low byte of address/count
C      ; write high byte of address/count
C      ; read low byte of address/count
C      ; save low byte in ah
C      ; read high byte of address/count
DDF2          C      mov     ax,bx
DDF4 BE           out     dx,al
DDF6 E2           out     dx,al
DDF8 EC           in     al,dx
DDFA EC           mov     sb,al
DDFC EA E0       in     al,dx
DDFE EC           in     al,dx
C
C      ; does what's been read = test pattern?
C      ; TEMP Error #2
C      ; if not, abort
DDFA B3 C3        cmp     ax,bx
DDFC B4 02        mov     ah,2
DDFE 75 5E        jnz    i_dmae_err
C
DDE0 41           dec     dx              ; did we decrement past port address 0?
DDE1 79 EF        jns    i_dmae_lp      ; if not, continue same pass for all 8.
C
C      ; 1st pass? if so, bx = 0FFFFh & loop
C      ; 2nd pass? if so, bx = 0 & continue
DDE3 43           ino    bx
DDE4 74 E9        jz     i_dmae_pass2
C
C      ; We are done testing all 8 16-bit readable/writeable channel registers (address
C      ; and count registers for all 4 channels) with the following results: All the
C      ; address registers (dma_addr_x) and count registers (dma_count_x) have been
C      ; initialized to zero.
C
C      ; Load 64k (0FFFFh-1) count for RAM refresh p_dma controller channel.
C
DDE6 B0 FF        mov     al,0FFh
DDE8 B6 01        out     dma_count_0,al      ; low byte of count for 64k RAM refresh
DDEA B6 01        out     dma_count_0,al      ; high byte of count for 64k RAM refresh
C
C      ; Load mode for RAM refresh p_dma controller channel: channel 0, read, auto-
C      ; initialize, increment, single mode.
DDE0 B0 58        mov     al,dma_mode_0
DDE2 B6 0B        out     dma_mode,al
C
C      ; Enable p_dma controller: memory-to-I/O, controller enable, normal, fixed
C      ; priority, late write, and DREQ/DACK.
DDE0 B0 00        mov     al,dma_cmd_enable
DDE2 B6 08        out     dma_command,al
C
C      ; The master clear command above has masked off all channels. Now, we 'unmask'
C      ; the RAM refresh dma_mask bit. p_dma RAM refresh begins for the first time!
C
DDE4 B0 00        mov     al,dma_unmask_0
DDE6 B6 0A        out     dma_mask_bit,al      ; turn on RAM refresh channel 0
C
C      ; Program p_8253_1 of 18253 p_timer to proper value for RAM refresh.
C
DDE8 B0 74        mov     al,t1cmd
DDEA B6 43        out     p_8253_ctrl,al

```

# ROM BIOS Listing

```

DE1C B8 0013      C          mov     ax,ticount          ; load p_dma refresh count
DE1F B6 41        C          out     p_8253_1,al
DE21 8A C4        C          mov     al,ah
DE23 B6 41        C          out     p_8253_1,al
C          ; Check dma_status for 'hot' p_dma request from p_8253_1.
C
DE25 B4 03        C          mov     ah,3              ; TEMP Error #3
DE27 B4 08        C          in     al,dma_status      ; test for RAM refresh request in status
DE29 A3 10        C          test    al,010h          ; bit #4 -> channel 0 request
DE2B 75 31        C          jnz    i_dmao_err        ; if 'hot' p_dma request is there, abort
C          ; Initialize other p_dma counters and modes.
C
DE2D BA 00B0      C          mov     dx,dma_mode
C          ; Initialize p_dma channel 1 not used.
C
DE30 B0 41        C          mov     al,dma_mode_1     ; mode for not used
DE32 BE          C          out     dx,al
C          ; Initialize p_dma channel 2 PDU.
C
DE33 B0 56        C          mov     al,dma_mode_2     ; mode for PDU
DE35 BE          C          out     dx,al
C          ; Initialize p_dma channel 3 display.
C
DE36 B0 43        C          mov     al,dma_mode_3     ; mode for display
DE38 BE          C          out     dx,al
C          ; Initialize p_dma Segment Nibble Latches to zero.
C          ; (dma_seg_x for x = 0 to 3 is port addresses 80h to 83h).
C
DE39 32 C0        C          xor     al,al             ; al = 0
DE3B BA 0083      C          mov     dx,083h          ; loop counter and port address!
C          ; dx = dma_seg_3 = 083h
C
DE3E             C          i_dmao_nib:
DE3E BE          C          out     dx,al
DE3F FE CA        C          dec     dl                ; when dl goes from 80h (-128) to
DE41 78 FB        C          ja     i_dmao_nib        ; 07fh (+127) we will exit
C          ;-----
C          ; 8237 p_dma Controller Test -- Test Lowest 64k bank of RAM
C          ;-----
C          assume cs:code, ds:data, es:abs0, ss:code
C
DE43 2E: 8E 1E E5F2 R      C          mov     ds,word ptr es:[set_ds_word] ; satisfy assumptions
DE48 B8 36 0072 R      C          mov     si,word ptr ds:[reset_flag] ; save reset_flag
C
DE4C 33 D2        C          xor     dx,dx
DE4E E9 E266 R      C          jmp     wstat            ; dx = 0; test 0000:0 to 0000:FFFF
DE51             C          i_dmao_ret:
C          ; call wstat
C          ; will 'ret' here
C
DE51 2E: 8E 1E E5F2 R      C          mov     ds,word ptr es:[set_ds_word] ; satisfy assumptions
DE56 89 36 0072 R      C          mov     word ptr ds:[reset_flag],si ; restore reset_flag
C
DE5A B4 04        C          mov     ah,4
DE5C 74 06        C          jz     i_dmao_ok
C
DE5E             C          i_dmao_err:
DE5E BE DC72 R      C          mov     si,cs:(offset i_dmao_m)
DE61 E9 E029 R      C          jmp     i_fatal          ; ah has error code to report.
C          ; i_fatal will 'ret' to i_pic
C
DE64             C          i_dmao_ok:
DE64 B0 44        C          mov     al,44h           ; Check Point #4
DE66 BA 0378      C          mov     dx,378h          ; parallel port data port address
DE69 BE          C          out     dx,al
DE6A C3            C          ret                     ; output "Running- Checkpoint 4"
C          ; will 'ret' to_pic
C          ;-----
C          ; 8259A Programmable Interrupt Controller Test.
C          ;-----
C          assume cs:code, ds:data, es:abs0, ss:stack_ram
C
DE6B             C          i_pic:
DE6B B8 0030      C          mov     ax,stack_seg     ; Initialize RAM Stack
DE6E BE D0        C          mov     es,ax            ; on lower tested memory
DE70 BC 0100      C          mov     sp,100h
C
DE73 E8 E1DC R      C          call    i_pic_init
C          ; Initialize & Disable 8259A Programmable Interrupt Controller.
C
C          ; Install Interrupt Vectors for diagnostics.
C
C          ; Install unexpected diagnostic interrupt vectors.
C
DE75 33 F6        C          xor     si,si
DE76 B8 FE        C          mov     di,si
DE7A B9 01FE      C          mov     cx,(0400h-000hh)/2 ; es:di = abs0_seg:int0000h
C          ; words from 0:000hh to 0:0400h
C
DE7D B8 EDCD R      C          mov     ax,cs:(offset i_pic_err) ; store offset i_pic_err
DE80 AB          C          stcsw
DE81 8C C8        C          mov     ax,cs            ; store segment address

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# ROM BIOS Listing

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DE83 AB          C          stow          word ptr es:0000h,word ptr es:0000h ; es:di = abs0_seg:int00loca + 4
DE84 F3/ 26: A5 C          rep          movs          word ptr es:0000h ; replicate vector
C
C
C          ; Install software diagnostic interrupt vectors.
C
DE87 B8 DEA9 R  C          mov          ax,es:(offset i_pic_0_ok) ; ax = offset i_pic_0_ok
DE8A 33 FF          C          xor          di,di ; es:di = abs0_seg:int00loca
DE8C B1 05          C          mov          cl,5 ; load INT's 0h through 4h.
C
DE8E          C          i_pic_soft: ; ax = (4*x)-(i_pic_0_ok)
DE8E AB          C          stow          ; es:di gets offset i_pic_x_ok
DE8F 47          C          inc          di ; skip segment (already = es)
DE90 47          C          inc          di ; skip segment (already = es)
DE91 05 0004      C          add          ax,4 ; i_pic_x_ok are 4 bytes apart
DE94 E2 F8          C          loop         i_pic_soft ; until cx = 0.
C
C          ; Install hardware diagnostic interrupt vectors.
C
DE96 B8 FF23 R   C          mov          ax,es:(offset ill_int) ; ax = offset ill_int
DE99 BF 0020 R   C          mov          di,es:(offset int08loca) ; es:di = abs0_seg:int08loca
DE9C B1 08          C          mov          cl,8 ; load INT's 8h through Fh.
C
DE9E          C          i_pic_hard: ; es:di gets offset ill_int
DE9E AB          C          stow          ; skip segment (already = es)
DE9F 47          C          inc          di ; skip segment (already = es)
DEA0 47          C          inc          di ; skip segment (already = es)
DEA1 E2 FB          C          loop         i_pic_hard ; until cx = 0.
C
C          ; Test software interrupts first (cl = 0 if error).
C
DEA3 B7 09          C          mov          bh,09h ; bx has its 8th and 11th bits set.
C
C          ; cx = 0 from loop above.
C          ; generate a divide-by-zero INT 00h
DEA5 F6 F5          C          div          oh ; generate a divide-by-zero INT 00h
DEA7 BF 33          C          jmp          short i_pic_err
DEA9          C          i_pic_0_ok: ; bh = 09h, set trap & OF flags in bx
C          ; (bits 8 and 11 of flags).
C          ; put trap flags on stack
DEA9 53          C          push         bx ; generate a single-step trap INT 01h
DEAA 9D          C          popf          ; must be 4 bytes long!
DEAB EB 2F          C          jmp          short i_pic_err
DEAD          C          i_pic_1_ok: ; generate a software interrupt INT 02h
C          ; must be 4 bytes long!
DEAD CD 02          C          INT          02h ; generate a software interrupt INT 02h
DEAF EB 2B          C          jmp          short i_pic_err ; must be 4 bytes long!
DEB1          C          i_pic_2_ok: ; generate a 1-byte break-point INT 03h
C          ; must be 4 bytes long!
DEB1 CC          C          INT          03h ; generate a 1-byte break-point INT 03h
DEB2 90          C          nop          ; must be 4 bytes long!
DEB3 EB 27          C          jmp          short i_pic_err ; must be 4 bytes long!
DEB5          C          i_pic_3_ok: ; OF overflow flag is still set.
C          ; generate an overflow interrupt INT 04h
DEB5 CE          C          INTO         ; must be 4 bytes long!
DEB6 90          C          nop          ; must be 4 bytes long!
DEB7 EB 23          C          jmp          short i_pic_err ; must be 4 bytes long!
DEB9          C          i_pic_4_ok: ; OF overflow flag is still set.
C          ; generate an overflow interrupt INT 04h
C          ; must be 4 bytes long!
C          ; Test hardware interrupts second.
C          ; Test 8259A PIC interrupt mask with test patterns (cl = 0 if error).
DEB9 B0 01          C          mov          al,1 ; initialize mask value = 1
C
DEBB          C          i_pic_test: ; output pattern, test input
C          ; if not same pattern, abort
DEBB EB E1ED R   C          call         i_out_mask ; output pattern, test input
DEBE 75 1C          C          jne         i_pic_err ; if not same pattern, abort
DEC0 D0 D0          C          cpl         al,1 ; rotate test pattern
DEC2 73 F7          C          jnc         i_pic_test ; test again, if not finished
C
DEC4 B0 FF          C          mov          al,0FFh ; test pattern of all ones
DEC6 EB E1ED R   C          call         i_out_mask ; output pattern, test input
DEC9 75 11          C          jne         i_pic_err ; if not same pattern, abort
C
C          ; Look for 'hot' (active though masked off) PIC interrupts (cl = IR# if error).
C          ; Enable Interrupts for the very first time!
DEC9          C          i_pic_hot: ; delay awhile, waiting for
C          ; a 'hot' interrupt.
DEC9 FB          C          sti          ; enable interrupts
DECC 33 C9          C          xor          cx,cx ; delay awhile, waiting for
DECE E2 FE          C          loop        $ ; a 'hot' interrupt.
C
DEDD 40 006B R   C          mov          al,byte ptr ds:[intr_flag] ; get the flag from ill_int
DEDD 04 C0          C          or          al,al ; intr_flag = 0?
DEDD 74 34          C          jz          i_pic_ok ; if so, we're all done.
C
C          ; Convert 'hot' interrupt mask (bit pattern) to IR# (1 to 8 error code).
C
DEDD          C          i_pic_hot: ; cx = 0 from loop above.
DEDD 41          C          inc          cx ; increment cx (IR#-1).
DEDD D0 D8          C          rer          al,1 ; mask's least significant bit.
DEDA 73 FB          C          jnb         i_pic_hot ; if not set, continue.
C          ; (exit with cl = 1 to 8.)
C
DEDC          C          i_pic_err: ; cl = 0 or failing PIC 'hot' active IR#
DEDC BC 0100      C          mov          sp,100h ; re-initialize stack
C
DEDF 51          C          push         cx ; save error code.
C
C          ; Install Vector Table. ; set int10loca = code_seg:v_10, and

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# ROM BIOS Listing

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DEE0 EB E1A0 R      C      call    i_vector          ; set int1Dloen = code_seg:v_parms.
C
C      ; Initialize Video.
C
DEE3 EB E148 R      C      call    i_d_init
C
C      ; Display error message.
C
DEE6 BE DC7F R      C      mov     si,cs:(offset i_pic_m)
DEE9 EB E5FA R      C      call    DRomString        ; display failing test message.
C
DEEC BE DC45 R      C      mov     si,cs:(offset fail_m)
DEEF EB E5FA R      C      call    DRomString        ; display fail message.
C
DEF2 59             C      pop     cx                ; restore error code.
DEF3 0A C9          C      or     cl,cl              ; cl = 0?
DEF5 74 0E          C      jz     i_pic_no_hot      ; if so, we're done.
C
C      ; Display 'hot' interrupt number :Hx. (where x is the IR# from 0 to 7)
C
DEF7 EB E626 R      C      call    DColon           ; display a colon.
DEFA BB 0E48          C      mov     ax,(0Eh*100h)+'H' ; display 'hot' interrupt symbol.
DEFD CD 10            C      int    10h
DEFF 8A C1          C      mov     al,al            ; transfer error code.
DF01 48             C      dec     ax                ; error code (1 to 8) to (0 to 7) IR#.
DF02 EB E650 R      C      call    DHexNib         ; display lowest nibble.
C
DF05             C      i_pic_no_hot:
DF05 EB E619 R      C      call    DCrLf
DF08 EB 07          C      jmp     short i_pic_end
C
DF0A F4            C      hlt
C
DF0B             C      i_pic_ok:
DF0B B0 45            C      mov     al,45h           ; Check Point #5
DF0D BA 0378       C      mov     dx,378h         ; parallel port data port address
DF10 EB             C      out     dx,al           ; output "Running- Checkpoint 5"
C
DF11             C      i_pic_end:
C
C      ;-----
C      ;      Install Vector Table.
C      ;-----
DF11 BC 0100       C      mov     sp,100h        ; re-initialize stack
DF14 EB E1A0 R      C      call    i_vector
C
C      ;-----
C      ;      Determine System Configuration from Switches and Initialize Video.
C      ;-----
DF17 EB E148 R      C      call    i_d_init
C
C      ;-----
C      ;      Display Passing Error Messages
C      ;-----
DF1A             C      disp_pass:
DF1A BE DB8C R      C      mov     si,cs:(offset banner_m)
DF1D EB E5FA R      C      call    DRomString
C
DF20 BE DC4B R      C      mov     si,cs:(offset i_opu_m)
DF23 EB E5FA R      C      call    DRomString
DF26 BE DC3D R      C      mov     si,cs:(offset pass_m)
DF29 EB E5FA R      C      call    DRomString
C
DF2C BE DC58 R      C      mov     si,cs:(offset i_rom_m)
DF2F EB E5FA R      C      call    DRomString
DF32 BE DC3D R      C      mov     si,cs:(offset pass_m)
DF35 EB E5FA R      C      call    DRomString
C
DF38 BE DC65 R      C      mov     si,cs:(offset i_dmat_m)
DF3B EB E5FA R      C      call    DRomString
DF3E BE DC3D R      C      mov     si,cs:(offset pass_m)
DF41 EB E5FA R      C      call    DRomString
C
DF44 BE DC72 R      C      mov     si,cs:(offset i_dmatc_m)
DF47 EB E5FA R      C      call    DRomString
DF4A BE DC3D R      C      mov     si,cs:(offset pass_m)
DF4D EB E5FA R      C      call    DRomString
C
DF50 BE DC7F R      C      mov     si,cs:(offset i_pic_m)
DF53 EB E5FA R      C      call    DRomString
DF56 BE DC3D R      C      mov     si,cs:(offset pass_m)
DF59 EB E5FA R      C      call    DRomString
C
C      ;-----
C      ;      Size & clear RAM at every 64k byte bank past the lowest 64k.
C      ;-----
DF5C             C      RAM_size_tst:
DF5C             C      assume cs:code, ds:data, es:abs0, ss:stack_ram
DF5C BD 0040       C      mov     bp,64          ; initialize memory count
C
DF5F 8B 36 0072 R   C      mov     si,word ptr ds:[reset_flag] ; get warm bootflag
DF63 81 EE 1234   C      sub     si,01234h       ; si=0 iff CTL ALT DEL sequence.
DF67 33 FF        C      xor     di,di           ; offset = 0000h
C

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# ROM BIOS Listing

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DF69 BA 1000      C      mov     dx,1000h      ; start at 1000:0000 (dx keeps segment)
DF6C              C      RAM_size_1p:
DF6C 8E C2        C      mov     es,dx          ; got segment
C
DF6E 26: 8B 05    C      mov     ax,word ptr es:[di] ; read existing ram value
DF71 F7 D0        C      not     ax             ; complement it
DF73 26: 89 05    C      mov     word ptr es:[di],ax ; write complement back to RAM
C
DF76 26: 8B 1D    C      mov     bx,word ptr es:[di] ; read back from RAM
C
DF79 3B C3        C      cmp     ax,bx          ; verify to test for end of RAM
DF7B F7 D0        C      not     ax             ; recreate original value
DF7D 75 2C        C      jne    RAM_size_end    ; if verify fails, at end of RAM
C
DF7F 26: 89 05    C      mov     word ptr es:[di],ax ; restore original value back to RAM
DF82 0B F6        C      or     si,si           ; test warm boot flag
DF84 74 1D        C      jz     RAM_size_next   ; if CTL ALT DEL sequence,
C                          ; don't clear memory
DF86 E8 E266 R    C      call   testat          ; test and clear memory
DF89 75 3E        C      jnz    RAM_error       ; test flag from storage test
C
DF8B 83 C5 40     C      add     bp,6h          ; increment size
DF8E 56           C      push   si             ; save Warm Boot Flag
DF91 E8 0E0D      C      mov     ax,0E0Dh       ; put out a CR
DF92 CD 10        C      int    10h
C
DF94 8B C5        C      mov     ax,bp          ; display tested RAM
DF96 EB 0003      C      mov     bx,3           ;
DF99 E8 E66D R    C      call   DHnum          ;
DF9C BE DCEA R    C      mov     si,cs:[offset i_RAM_m]
DF9F BE E5FA R    C      call   DRomString     ;
C
DFA2 5E           C      pop     si             ; retrieve Warm Boot Flag
C
DFA3              C      RAM_size_next:
DFA3 86 C6 10     C      add     dh,10h        ; maximum RAM = 640k = 10 * 64k
DFA5 80 FE 40     C      cmp     dh,0A0h       ; next segment
DFA9 72 C1        C      jb     RAM_size_1p    ; top of RAM yet (A000:0000)?
C                          ; if not, continue.
C
DFAB              C      RAM_size_end:
DFAB 0B F6        C      or     si,si           ; test warm boot flag
DFAE 74 06        C      jz     RAM_size_end_1 ; if CTL ALT DEL sequence,
DFAF BE DC3D R    C      mov     si,cs:[offset pass_m] ; Display OK
DFB2 E8 E5FA R    C      call   DRomString     ;
C
DFB5              C      RAM_size_end_1:
DFB5 33 C0        C      xor     ax,ax          ; bx = RAM size/16
DFB7 BE C0        C      mov     es,ax          ; ax = 0
DFB9 BA C6        C      mov     al,dh          ; satisfy assumptions es = 0 = abs0_seg
DFBB D1 E0        C      shl     ax,1           ; ax = (RAM size/16)/256 = RAM size/4k
DFBD D1 E0        C      shl     ax,1           ; ax = (RAM size/4k) * 2 = RAM size/2k
DFBF D1 E0        C      shl     ax,1           ; ax = (RAM size/2k) * 2 = RAM size/1k
C
DFBF 2E: BE 1E E5F2 R C      mov     ds,word ptr es:[set_ds_word] ; restore data segment pointer
DFC4 A3 0013 R    C      mov     word ptr ds:[memory_size],ax
C
C
C      ;      GoTo Display Passing Messages
C
DFC7 EB 30        C      jmp     short i_oal    ;Go check clock calendar
C
DFC9              C      RAM_error:
DFC9              ;      Error message looks like: Fail:cc:y000:zzzz:www:rrrr
DFC9              ;      where: cc = RAM configuration number
DFC9              ;      y000 = Segment of failure      = dx = es
DFC9              ;      zzzz = Offset of failure      = di
DFC9              ;      wwww = Data that was written   = ax
DFC9              ;      rrrr = Data that was read     = bx
C
DFC9 52           C      push   dx             ;save failing segment
DFCA 1E          C      push   ds             ;save ds
DFCB 50           C      push   ax             ;save failing test pattern.
C
DFCC EB E619 R    C      call   DCrLf          ;Carriage Return, Line Feed
DFCD E8 DC55 R    C      mov     si,cs:[offset fail_m]
DFD2 E8 E5FA R    C      call   DRomString     ; display fail message.
C
DFD5 E8 E626 R    C      call   DColon         ; display a colon
C
DFD8 EA 66        C      in     al,sysd_conf_m ; get RAM configuration.
DFDA 24 0F        C      and    al,0Fh         ; mask valid bits.
DFDC EB E643 R    C      call   DHexByte       ; display RAM configuration.
C
DFD9 E8 E626 R    C      call   DColon         ; display a colon
C
DFE2 E8 DA        C      mov     ds,dx          ; ds = failing segment = dx
DFE4 EB C7        C      mov     ax,di          ; ax = failing segment = di
DFE6 E8 E632 R    C      call   DHexLong       ; display ds:ax
C
DFE9 E8 E626 R    C      call   DColon         ; display a colon
C
DFEC 1F          C      pop     ds            ; ds = failing test pattern = on stack
DFED EB C3        C      mov     ax,bx          ; ax = what was read = bx
DFEF E8 E632 R    C      call   DHexLong       ; display ds:ax
DFF2 E8 E619 R    C      call   DCrLf
C
DFF5 1F          C      pop     ds            ;restore ds
DFF6 5A          C      pop     dx            ;restore failing segment
DFF7 EB BC        C      jmp     short RAM_size_end_1
C

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# ROM BIOS Listing

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C :-----
C :
C :             MMS8174 Clock Calendar Device Test
C :-----
C
C             assume cs:code, ds:data, es:abs0, ss:stack_ram
C
DFF9          i_cal:
C
C             ; Read Clock Calendar Device.
C             ; bx = day (from 1-1 of leap year)
C             ; ch = hour
DFF9 B4 FE     mov     ah,-2
C             ; cl = minutes
DFFB CD 1A     int     1Ah
C             ; dh = seconds
C             ; dl = hundredths of seconds
C
C             ; Check time & date read.
C             ; Hundredths of Seconds.
C
DFFD B8 000A   mov     ax,10
E000 B6 C2     xchg   al,dl
E002 F6 F2     div     dl
C             ; ax = 10; dl = hundredths
C             ; ax = hundredths; dl = 10
C             ; ah = remainder, al = quotient
C             ; (can only read tenths of seconds.)
E004 3D 000A   cmp     ax,10
E007 73 15     jae    i_cal_1_1_80
C             ; if not, test chip & write 1-1-80.
C
C             ; Seconds.
E009 80 FE 3C   cmp     dh,60
E00C 73 10     jae    i_cal_1_1_80
C             ; dh = seconds should be < 60.
C             ; if not, test chip & write 1-1-80.
C
C             ; Minutes.
E00E 80 F9 3C   cmp     cl,60
E011 73 0B     jae    i_cal_1_1_80
C             ; cl = minutes should be < 60.
C             ; if not, test chip & write 1-1-80.
C
C             ; Hours.
E013 80 FD 18   cmp     ch,24
E016 73 06     jae    i_cal_1_1_80
C             ; ch = hour should be < 24.
C             ; if not, test chip & write 1-1-80.
C
C             ; Days.
E018 81 FB 0B6A  cmp     bx,(2*366)+(6*365)
E01C 72 5D     jb     i_cal_end
C             ; bx = day from leap year mod 8 should
C             ; be < (0-292) = (0-0B69h)
C             ; if no, valid time & day, skip test.
E01E          i_cal_1_1_80:
C             ; else invalid time & day, write 1-1-80.
C
C             ; Initialize and Stop Clock.
C
E01E 33 C0       xor     ax,ax
E020 B6 70     out    70h,al
E022 B6 7E     out    7Eh,al
C             ; test only port = out of test mode
C             ; stop/start port = stop clock
C
C             ; Output test pattern of maximum value with all bits set to read/writable ports.
C
E024 BE DD51 R  mov     si,cs:(offset i_cal_val)
E027 B9 0009   mov     cx,9
E02A BA 0074   mov     dx,0074h
C             ; ch keeps 0; cx = 9
C             ; dh keeps 0; dx = 74h
C
C             i_cal_max:
C
E02D 2E AC     lods   byte ptr cs:[si]
E02F 8A E0     mov     ah,al
E031 EE     out    dx,al
C             ; al get cs:si (ds overridden).
C             ; save maximum value.
C             ; ports 74 through 7C (units of minutes
C             ; to tens of months) get max value.
E032 EC     in     al,dx
E033 22 C4     and    al,ah
E035 3A C4     cmp    al,ah
E037 75 28     jnz   i_cal_err
C             ; read it back.
C             ; mask valid bits.
C             ; is it equal to the value written?
C             ; if not, abort.
E039 42     inc   dx
E03A E2 F1     loop  i_cal_max
C             ; increment to next port
C
E03C B0 07     mov     al,07h
E03E B2 7F     mov     dl,7Fh
E040 EE     out    dx,al
E041 EC     in     al,dx
E042 EC     in     al,dx
E043 EC     in     al,dx
E044 24 07     and    al,07h
E046 2C 07     cmp    al,07h
E048 75 17     jnz   i_cal_err
C             ; if not, abort.
C
C             ; Write out 0h (bits of lower nibble read) test pattern to read/writable ports.
C
E04A B1 09     mov     cl,9
E04C B2 74     mov     dl,74h
E04E          i_cal_0:
E04E EE     out    dx,al
C             ; al kept 0h.
C             ; ch kept 0; cx = 9
C             ; dh kept 0; dx = 74h
C             ; ports 74 through 7C (units of minutes
C             ; to tens of months) get 0h.
E04F EC     in     al,dx
E050 24 0F     and    al,0Fh
E052 75 0D     jnz   i_cal_err
C             ; read it back.
C             ; mask valid bits (lower nibble) = 0h?
C             ; if not, abort.
E054 42     inc   dx
E055 E2 F7     loop  i_cal_0
C             ; increment to next port
C
E057 B2 7F     mov     dl,7Fh
E059 EE     out    dx,al
C             ; dh kept 0; dx = 7Fh
C             ; interrupt (year mod 8) gets 0Fh.

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# ROM BIOS Listing

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E05A EC          C      in      al,dx          ; must do 'in' from this port 3 times.
E05B EC          C      in      al,dx
E05C EC          C      in      al,dx
E05D 28 0F      C      and     al,0Fh          ; mask valid bits (lower nibble) = 0h?
E05F 74 12      C      jz     i_cal_ok          ; if so, we're all done.
                                     ; else, abort.
E061            C      i_cal_err:
E061 BE DCA6 R   C      mov     si,cs:(offset i_rtc_m)
E064 E8 E5FA R   C      call  DROMString
E067 BE DCA5 R   C      mov     si,cs:(offset fail_m)
E06A E8 E5FA R   C      call  DROMString          ; display fail message.
E06D E8 E619 R   C      call  DCrLf
E070 EB 01       C      jmp     short i_cal_ok      ; try to write 1-1-80, regardless...
E072 F8         C      bit
E073            C      i_cal_ok:
E073 33 DB        C      xor     bx,bx          ; 1-1-80 is day 0.
E075 33 C9        C      xor     cx,cx          ; hours & minutes = 0.
                                     ; Write & Start Clock Calendar Device.
E077 B4 FF        C      mov     ah,-1          ; bx = day (from 1-1 of leap year)
E079 CD 1A        C      int    1Ah          ; ah = hour
                                     ; cl = minutes
                                     ; Output: ah = -1 implies date/time err.
                                     ;         ah = 0 implies date/time OK.
E07B            C      i_cal_end:
                                     ;-----
                                     ; 18253 Real-Time Time Clock Test (p_8253_1 tested in i_dmat)
                                     ;-----
                                     ; assume cs:code, ds:data, es:ah=0, ss:stack_ram
E07B            C      i_rtc:
                                     ; String to be displayed regardless of results.
E07B BE DCA6 R   C      mov     si,cs:(offset i_rtc_m)
E07E E8 E5FA R   C      call  DROMString
                                     ; Test 18253 real-time clock interrupt p_timer counter (p_8253_0).
E081 B0 34        C      mov     al,034h          ; 00 11 010 0 -> p_8253_0, lsb 1st, mode 2, no BCD
E083 B4 0040      C      mov     dx,p_8253_0      ; select real-time clock counter
E086 E8 E1F6 R   C      call  rtc_chk
E089 75 2E        C      jnz     i_rtc_err          ; if nz, ah has error code to report.
                                     ; Test 18253 tone generator p_timer counter (p_8253_2).
E08B B0 01        C      mov     al,1            ; clear kb interrupts, reset kb, disable parity
E08D B6 61        C      out    p_kotrl,al       ; turn off speaker data -- bit #1
                                     ; turn on speaker gate to p_8253_2 -- bit #0
E08F B0 B4        C      mov     al,0B4h         ; 10 11 010 0 -> p_8253_2, lsb 1st, mode 2, no BCD
E091 B4 0042      C      mov     dx,p_8253_2      ; select tone generator counter
E094 E8 E1F6 R   C      call  rtc_chk
E097 B0 00        C      mov     al,0            ; clear kb interrupts, reset kb, disable parity
E099 E6 61        C      out    p_kotrl,al       ; turn off speaker data & gate -- bits #1 & #0
E09B 75 1C        C      jnz     i_rtc_err          ; if nz, ah has error code to report.
                                     ; Initialize 18253 real-time clock interrupt p_timer counter (p_8253_0).
E09D B0 36        C      mov     al,t00md        ; select real time clock counter
E09F E6 43        C      out    p_8253_ctr1,al
E0A1 B8 0000      C      mov     ax,t0count      ; load real time clock count
E0A4 E6 40        C      out    p_8253_0,al
E0A6 B4 C8        C      mov     al,ah
E0A8 E6 40        C      out    p_8253_0,al
                                     ; Initialize 18253 tone generator p_timer counter (p_8253_2).
E0AA B0 B6        C      mov     al,t2emd        ; select tone generator counter
E0AC E6 43        C      out    p_8253_ctr1,al
E0AE B8 0266      C      mov     ax,t2count      ; load tone generator count
E0B1 E6 42        C      out    p_8253_2,al
E0B3 B4 C8        C      mov     al,ah
E0B5 E6 42        C      out    p_8253_2,al
E0B7 EB 1C        C      jmp     short i_rtc_ok
E0B9            C      i_rtc_err:
E0B9 BE DCA5 R   C      mov     si,cs:(offset fail_m)
E0BC E8 E5FA R   C      call  DROMString          ; display fail message.
E0BF BE DCA5 R   C      mov     si,cs:(offset i_rtc_lo_m-(*))
E0C2 B4 C4        C      mov     al,ah          ; al = error code = (1, 2 or, 3)
E0C4 32 E4        C      xor     ah,ah          ; ah = error code = (1, 2 or, 3)
E0C6 D1 E0        C      shl     ax,1           ; ax = 2*(error code) = (2, 4, or 6)
E0C8 D1 E0        C      shl     ax,1           ; ax = 4*(error code) = (4, 8; or 12)
E0CA C3 F0        C      add     si,ax          ; index to L0, H1, or NR message.)
E0CC E8 E5FA R   C      call  DROMString
E0CF E8 E619 R   C      call  DCrLf

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# ROM BIOS Listing

```

E0D2 EB 0D          C          jmp     short i_rtc_end
E0D4 F4            C          bit
E0D5 BE DC3D R     C          i_rtc_ok:
E0D8 E8 E5FA R     C          mov     si,cs:(offset pass_m)
E0DB B0 48         C          oall   DRomString
E0DD BA 0378       C          mov     al,48h          ; Check Point #8
E0E0 EE           C          mov     dx,378h        ; parallel port data port address
E0E1              C          out     dx,al          ; output "Running- Checkpoint 8"
E0E2 B8 E0E7       C          i_rtc_end:
E0E4 CD 10         C          mov     ax,(0Eh*100h)+BEL ; beep keyboard
E0E6 E9 E224 R     C          int     10h
E0E9              C          assume cs:code, ds:nothing, es:nothing, ss:atack_ram
E0E6 E9 E224 R     C          jmp     point
E0E9              C          diagnostics_1 endp
E0E9              C          -----
E0E9              C          ; Fatal Error Routine.
E0E9              C          ; Input:  cs:si = points to offset of failing error message
E0E9              C          ;         if ah < 0, do DHexByte of ah.
E0E9              C          ;         if ah = 0, do nothing (just print error).
E0E9              C          ; Output: None.
E0E9              C          ; Trash:  al, dx, & si destroyed.
E0E9              C          -----
E0E9              C          i_fatal proc    near
E0E9              C          assume cs:code, ds:nothing, es:nothing, ss:nothing
E0E9              C          ; Disable 8237A p_dma Controller.
E0E9 B0 04          C          mov     al,dma_cmd_disable ; disable p_dma controller command
E0EB E6 08         C          out     dma_command,al
E0ED E6 0D         C          ; Send a 'master clear' to 8237 p_dma Controller.
E0ED              C          dma_master_clr,al ; send master clear port any garbage
E0ED              C          ; Load 64k (0FFFFh+1) count for RAM refresh p_dma controller channel.
E0EF B0 FF         C          mov     al,0FFh
E0F1 E6 01         C          out     dma_count_0,al    ; low byte of count for 64k RAM refresh
E0F3 E6 01         C          out     dma_count_0,al    ; high byte of count for 64k RAM refresh
E0F5              C          ; Load mode for RAM refresh p_dma controller channel: channel 0, read, auto-
E0F5              C          ; initialize, increment, single mode.
E0F5 B0 58         C          mov     al,dma_mode_0     ; mode for RAM refresh
E0F7 E6 08         C          out     dma_mode,al
E0F9              C          ; Enable p_dma controller: memory-to-I/O, controller enable, normal, fixed
E0F9              C          ; priority, late write, and DREQ/~DACK.
E0F9 B0 00         C          mov     al,dma_cmd_enable ; enable p_dma controller
E0FB E6 08         C          out     dma_command,al
E0FD              C          ; The master clear command above has masked off all channels. Now, we 'unmask'
E0FD              C          ; the RAM refresh dma_mask bit. p_dma RAM refresh begins for the first time!
E0FD B0 00         C          mov     al,dma_unmask_0   ; turn on RAM refresh channel 0
E0FF E6 0A         C          out     dma_mask_bit,al
E101              C          ; Program p_8253_1 of 8253 p_timer to proper value for RAM refresh.
E101 B0 78         C          mov     al,tlowd         ; select p_dma refresh counter
E103 E6 43         C          out     p_8253_ctr1,al
E105 B0 13         C          mov     al,tlocount      ; load p_dma refresh count
E107 E6 41         C          out     p_8253_1,al
E109 E2 C0         C          mov     al,al
E10B E6 41         C          out     p_8253_1,al
E10D              C          assume cs:code, ds:nothing, es:nothing, ss:atack_ram
E10D 8C D7         C          mov     di,es            ; save stack pointer
E10F 8B EC         C          mov     bp,sp
E111 BA 0D30        C          mov     dx,stack_seg
E114 E2 D2         C          mov     ss,dx
E116 BC 0100       C          mov     sp,100h
E119 50           C          push    ax                ; save error code
E11A              C          ; Initialize & Disable 8259A Programmable Interrupt Controller.
E11A E8 E1DC R     C          call   i_plc_init
E11B              C          ; Install Vector Table.
E11B              C          ; set int10locn = code_seg:v_10, and
E11B              C          ; set int1Dlocn = code_seg:v_parms.
E11D E8 E1A0 R     C          call   i_vector
E11E              C          ; Initialize Video.
E11E              C          ;

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# ROM BIOS Listing

```

E120 E8 E148 R      C      call    i_d_init
C      ; Display error message.
E123 58            C      pop     ax                ; restore error code
E124 E8 E5FA R      C      call    DROMString       ; display string at cs:al.
E127 BE DC45 R      C      mov     si,cs:(offset fail_m)
E12A E8 E5FA R      C      call    DROMString       ; display fail message.
E12D 0A E4          C      or     ah,ah             ; ah = 0?
E12F 74 08          C      jz     i_fatal_ret       ; if so, no arguments
E131 E8 E626 R      C      call    DColon           ; display a colon
E134 8A C4          C      mov     al,ah            ; display error code
E136 E8 E643 R      C      call    DHexByte
E139 E8 E619 R      C      i_fatal_ret:
C      call    DCrLf
C      ;Output fatal error status for manufacturing tests
E13C BA 0378        C      mov     dx,378h          ; parallel port address
E13F EC            C      in     al,dx             ; read last checkpoint value
E140 34 3F          C      xor     al,03fh          ; extract checkpoint number from status
E142 EE            C      out    dx,al            ; output "Not OK - number"
C      assume cs:code, ds:nothing, es:nothing, ss:nothing
E143 8E D7          C      mov     ss,di            ; restore stack pointer
E145 8B E5          C      mov     sp,bp
C      ;
E147 F4            C      hlt
E148              C      i_fatal endp
C      ;-----
C      ; Determine System Configuration from Switches and Enable Video.
C      ; Input: None.
C      ; Output: None.
C      ; Trash: ax & cx destroyed.
C      ;-----
E148              C      i_d_init      proc    near
C      assume cs:code, ds:nothing, es:nothing, ss:stack_ram
E148 1E            C      push    ds                ; save registers
C      ; Initialize both boards.
C      assume cs:code, ds:data, es:nothing, ss:stack_ram
E149 B8 0040        C      mov     ax,data_seg       ; ds = ax = data_seg = 0040h.
E14C 8E D8          C      mov     ds,ax             ; (ah = 0.)
C      ; Initialize monochrome board.
C      mov     al,30h          ; switch_bits for monochrome.
E14E 80 30          C      mov     word ptr ds:[switch_bits],ax ; set data for monochrome.
E150 A3 0010 R      C      INT     10h              ; ah = 0 = v_set_mode.
E153 CD 10          C      ; Initialize color board.
C      mov     ax,0003h        ; switch_bits for not monochrome.
E155 B8 0003        C      mov     word ptr ds:[switch_bits],ax ; set data for color.
E158 A3 0010 R      C      INT     10h              ; ah = 0 = v_set_mode.
E15B CD 10          C      ; Determine system configuration from switches (low byte of switch_bits).
C      in     al,sys_conf_b    ; read high nibble of
C      ; system configuration switches.
E15D E4 67          C      and    al,0F0h           ; bits #7 - #6: (number of FDU's)-1
C      ; bits #5 - #4: monitor type
E15F 24 F0          C      and    al,0F0h           ; mask off low nibble (keep high nibble)
C      ; of low byte; clear high bytes.
E161 0C 0D          C      or     al,00Dh          ; ALWAYS 64k planar RAM and >= 1 FDU!
E163 8A C3          C      mov     cl,al            ; cl is ok, excepts bits #5 & #4.
E165 B5 03          C      mov     oh,03h          ; initialize display to mode #3 (default).
E167 24 30          C      and    al,030h          ; isolate display switches (bits #5 & #4).
E169 74 1C          C      js     i_d_80x25         ; if zero, default to 80x25 color.
E16B 3C 30          C      cmp     al,030h         ; is it the monochrome board?
E16D 75 1E          C      jnz    i_d_ok            ; if not, 40x25 or 80x25 color ok.
C      assume cs:code, ds:v_ram, es:nothing, ss:stack_ram
E16F 1E            C      push    ds                ; save ds = data_seg = 0040h.
E170 B8 B000        C      mov     ax,para_mono     ; satisfy assumptions
E173 8E D8          C      mov     ds,ax
E175 B0 A5          C      mov     al,0A5h         ; test pattern
E177 A2 0000        C      mov     byte ptr ds:[0000h],al
E17A 8A 26 0000    C      mov     ah,byte ptr ds:[0000h] ; read monochrome RAM
E17E 1F            C      pop     ds                ; restore 'ds = data_seg = 0040h.

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# ROM BIOS Listing

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C                                     assume es:code, ds:data, es:nothing, ss:stack_ram
C
E17F 3A C4      cmp     al,ah          ; if monochrome RAM is there,
E181 75 04      jnz     i_d_80x25     ; then the board must be there!
C                                     ; if not, default to 80x25 color?
E183 B5 07      mov     ch,07h        ; if there, we believe switches,
E185 EB 06      jmp     short i_d_ok   ; initialize display to mode #7.
C
E187           i_d_80x25:
E187 80 E1 EF      and     ol,0EFh       ; reset bit #8 for 80x25 color.
E18A 80 C9 20      or      ol,020h       ; set bit #5 for 80x25 color.
C
E18D           i_d_ok:
C                                     ; Set system configuration (switch_bits) from switches.
C
E18D 32 E4      xor     ah,ah          ; ah = 0.
E18F 8A C1      mov     al,ol          ; get data from switches.
E191 A3 0010 R   mov     word ptr ds:[switch_bits],ax ; save data from switches
C
C                                     ; Determine mode to initialize display monitor (from switches).
C
E194 A8 20      test    al,020h        ; does user want 40x25 color?
E196 75 02      jnz     i_d_mode       ; if so, initialize mode #1.
E198 B5 01      mov     ch,01h
E19A           i_d_mode:
C                                     ; Initialize desire board (from switches).
C
E19A 8A C5      mov     al,ah          ; transfer display mode to al.
E19C CD 10      INT     10h           ; ah = 0 = v_set_mode.
C
E19E 1F        pop     ds              ; restore registers
E19F C3        ret
C
E1A0           i_d_init     endp
C
C-----
C                                     Install Vector Table
C
C                                     Input: None.
C                                     Output: None.
C
C                                     Trash: ax = cx = 0 destroyed.
C-----
C
E1A0           i_vector     proc     near
C                                     assume es:code, ds:nothing, es:nothing, ss:stack_ram
C
E1A0 1E        push    ds              ; save registers
E1A1 06        push    es
E1A2 57        push    di
E1A3 56        push    si
C
C                                     ; Initialize Interrupt Vectors 00h through 07h to known routines.
C
C                                     assume es:code, ds:code, es:aba0, ss:stack_ram
C
E1A4 33 FF      xor     di,di           ; satisfy assumptions
E1A6 8E DF      mov     ds,di           ; ds = es = ax = aba0_seg = 0
E1A8 8E C7      mov     es,di           ; es:di = aba0_seg:int00locc
E1AA B6 FF23 R  mov     ax,es:(offset ill_int) ; ax = offset ill_int
E1AD B9 0008    mov     cx,(07h-00h)+1 ; load INT's 00h through 07h.
C
E1B0 AB        i_vec0: stoww          ; es:di++ gets offset ill_int
E1B1 8C 0D      mov     word ptr ds:[di],cs ; es:di gets cs
E1B3 47        inc     di              ; di++
E1B4 47        inc     di
E1B5 E2 F9      loop   i_vec0           ; until cx = 0.
C
C                                     ; load INT'n 02h and 05h
E1B7 C7 06 0014 R mov     word ptr ds:[int05locc],es:(offset a_int)
E1BD C7 06 0008 R mov     word ptr ds:[int02locc],es:(offset a_int)
C
C                                     ; Initialize Interrupt Vectors 08h through 1Eh to known routines.
C
C                                     assume es:code, ds:code, es:aba0, ss:stack_ram
C
E1C3 8C C8      mov     ax,es           ; satisfy assumptions
E1C5 8E D8      ds,ax                  ; ds = ax = cs
E1C7 BE FEF3 R  mov     si,cs:(offset i_vec_tbl) ; ds:si = code_seg:i_vec_tbl
C                                     ; es:di = aba0_seg:int08locc
E1CA B1 18      mov     ol,(1Fh-08h)+1 ; load INT's 08h through 1Fh.
C
E1CC A5        i_vec8: mov     ds:si (offset) ; es:di++ gets ds:si (offset)
E1CD AB        stoww          ; es:di++ gets ax = cs (segment)
E1CE E2 FC      loop   i_vec8           ; until cx = 0.
C
C                                     ; Initialize Interrupt Vectors 20h and above to zero.
C
E1D0 33 C0      xor     ax,ax           ; ax = 0
C
E1D2 B9 01B8    mov     cx,((03F0h-0080h)/2) ; es:di = aba0_seg:int20locc
C                                     ; clear 0:0080h to 0:03F0h
E1D5 F3/ AB    rep     stoww          ; don't blow away stack!
C                                     ; es:di++ gets 0
C
E1D7 5E        pop     si              ; restore registers
E1D8 5F        pop     di
E1D9 07        pop     es
E1DA 1F        pop     ds

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```

E1DB C3          C          ret
E1DC            C          i_vector      endp
C
C-----C-----
C          ; Initialize & Disable 8259A Programmable Interrupt Controller.
C          ;
C          ; Input: None.
C          ; Output: None.
C          ;
C          ; Trash: al & dx destroyed.
C-----C-----
E1DC            C          i_pic_init    proc   near
C          ; assume cs:code, ds:nothing, es:nothing, ss:stack_ram
E1DC BA 0020    C          mov     dx,pic_0      ; dx = pic_0 (8259A 'control' port)
E1DF B0 13     C          mov     al,pic_icw1    ; icw4 triggered, single, icw4 to follow
E1E1 EE        C          out     dx,al
C
E1E2 A2       C          inc     dx          ; dx = pic_1 (8259A 'data' port)
E1E3 B0 08    C          mov     al,pic_icw2    ; interrupt vector base address
E1E5 EE        C          out     dx,al
C          ; since we are single mode (no slave), skip icw3
C
C          ; dx = pic_1 (8259A 'data' port)
E1E6 B0 0D    C          mov     al,pic_icw4    ; not special fully nested, buffered,
E1E8 EE        C          out     dx,al      ; master, normal end_of_int, 8086 mode
C
E1E9 B0 FF    C          mov     al,pic_off_mask ; mask all interrupts off for now
E1EB EE        C          out     dx,al      ; dx = pic_1 (8259A 'data' port)
E1EC C3       C          ret
C
E1ED            C          i_pic_init    endp
C
C-----C-----
C          ; Output Mask to 8259A Programmable Interrupt Controller.
C          ;
C          ; Input: AL = mask pattern
C          ;
C          ; Output: Flags
C          ;
C          ; Trash: ah destroyed.
C-----C-----
E1ED            C          i_out_mask   proc   near
C          ; assume cs:code, ds:nothing, es:nothing, ss:stack_ram
E1ED E6 21    C          out     pic_1,al   ;output interrupt mask pattern
E1EF 8A E0    C          mov     ah,al         ;save pattern for compar
E1F1 EA 21    C          in     al,pic_1       ;get mask from 8259
E1F3 3A E0    C          cmp     ah,al         ;the same ?
E1F5 C3       C          ret                ;return flags = result of compare
C
E1F6            C          i_out_mask   endp
C
C-----C-----
C          ; 8253 p_timer test for one p_timer counter channel
C          ;
C          ; Input: al = 8253 p_timer control byte
C          ;          dx = port address of 8253 p_timer data (counter)
C          ;
C          ; Output: zf = set (z status) if no error; reset (nz status) if error
C          ;          ah = Error codes: 0 -> No Error!
C          ;          1 -> Low below time interval window.
C          ;          2 -> High above time interval window.
C          ;          3 -> No Response.
C          ;
C          ; Trash: al, bx & cx destroyed.
C-----C-----
E1F6            C          rtc_chk     proc   near
C          ; assume cs:code, ds:nothing, es:nothing, ss:nothing
E1F6 8A E0    C          mov     ah,al         ; save control byte for later.
E1F8 B9 FFFF  C          mov     cx,0FFFFh     ; time out for both Register Bit Tests.
C          ; Register Bit Test (All Reset): Count down from 100h until all bits reset.
C
E1FB 8B D9    C          mov     bx,cx         ; bx gets all its bits set.
E1FD E6 43    C          out     p_8253_ctrl,al ; send 18253 p_timer control byte.
C
E1FF 32 C0    C          xor     al,al         ; al = 00h
E201 EE        C          out     dx,al         ; load low byte of p_timer count.
E202 FE C0    C          inc     al            ; al = 01h
E204 EE        C          out     dx,al         ; load high byte of p_timer count.
C
E205            C          rtc_chk_reset_lp:
E205 8A C4    C          mov     al,ah         ; get control byte for read.
E207 24 C0    C          and     al,0C0h       ; mask off all but top 2 bits.
E209 E6 43    C          out     p_8253_ctrl,al ; send latching control byte for read.
C
E20B EC        C          in     al,dx         ; get low byte of p_timer count.
E20C 22 D8    C          and     bl,al         ; 'and' low byte.
E20E EC        C          in     al,dx         ; get high byte of p_timer count.
E20F 22 F8    C          and     bh,al         ; 'and' high byte.
C
E211 0B DB    C          or     bx,bx         ; is bx = 0?

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# ROM BIOS Listing

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E213 74 05      C      js      rto_ohk_reset_ok      ; if so, we're done.
E215 E2 EE      C      loop     rto_ohk_reset_lp    ; if not, continue reading.
C              C              ; (Note: loops less than 16 times.)
C
E217           C      rto_ohk_reset_err:      ; time out.
E217 B4 03      C      mov      ah,3              ; Error #3. (No Response.)
E219 C3         C      ret                          ; return nz status (loop leaves zf ok).
C
E21A           C      rto_ohk_reset_ok:
C              C      ; Register Bit Test (All Set): Count down from 0h (FFFFh+1) until all bits set.
E21A 33 DB      C      xor      bx,bx              ; bx gets all its bits reset.
C
E21C 8A C4      C      mov      al,ah              ; get control byte for load.
E21E E6 A3      C      out      p_8253_ctrl,al     ; send i8253 p_timer control byte.
C
E220 32 C0      C      xor      al,al              ; al = 00h
E222 EE        C      out      dx,al              ; load low byte of p_timer count.
E223 EE        C      out      dx,al              ; load high byte of p_timer count.
C
E224           C      rto_ohk_set_lp:
E224 8A C4      C      mov      al,ah              ; get control byte for read.
E226 24 C0      C      and      al,0C0h           ; mask off all but top 2 bits.
E228 E6 A3      C      out      p_8253_ctrl,al     ; send latching control byte for read.
C
E22A EC        C      in      al,dx              ; get low byte of p_timer count.
E22B 0A D6      C      or       bl,al              ; or' low byte.
E22D EC        C      in      al,dx              ; get high byte of p_timer count.
E22E 0A F8      C      or       bh,al              ; or' high byte.
C
E230 81 FB FFFF C      cmp      bx,0FFFFh           ; is bx = 0FFFFh?
E234 74 05      C      js      rto_ohk_set_ok      ; if so, we're done.
E236 E2 EC      C      loop     rto_ohk_set_lp    ; if not, continue reading.
C              C              ; (Note: loops less than 16 times.)
C
E238           C      rto_ohk_set_err:      ; time out.
E238 B4 03      C      mov      ah,3              ; Error #3. (No Response.)
E23A C3         C      ret                          ; return nz status (loop leaves zf ok).
C
E23B           C      rto_ohk_set_ok:
C              C      ; p_timer Time Window Test: Test p_timer versus CPU & see if it falls within spec.
E23B 8A C4      C      mov      al,ah              ; get control byte for read.
E23D 24 C0      C      and      al,0C0h           ; mask off all but top 2 bits.
E23F E6 A3      C      out      p_8253_ctrl,al     ; send latching control byte for read.
C
E241 EC        C      in      al,dx              ; get low byte of p_timer count.
E242 0A D6      C      mov      bl,al              ; save low byte.
E244 EC        C      in      al,dx              ; get high byte of p_timer count.
E245 0A F8      C      mov      bh,al              ; save high byte.
C
E247 8A C4      C      mov      al,ah              ; get control byte for read.
E249 24 C0      C      and      al,0C0h           ; mask off all but top 2 bits.
E24B E6 A3      C      out      p_8253_ctrl,al     ; send latching control byte for read.
C
E24D EC        C      in      al,dx              ; get low byte of p_timer count.
E24E 0A C8      C      mov      cl,al              ; save low byte.
E250 EC        C      in      al,dx              ; get high byte of p_timer count.
E251 0A E8      C      mov      ch,al              ; save high byte.
C
E253 2B D9      C      sub      bx,ox              ; calculate time difference.
C
C              C      ; Do Time Range Cheeking (4 <= bx <= 14).
E255 B4 02      C      mov      ah,2              ; Error #2. (High above time window.)
E257 83 FB 0E   C      cmp      bx,14              ; return nz status. (ja has zf reset.)
E25A 77 09      C      ja      rto_ohk_high
C
E25C FE CC      C      dec      ah                  ; Error #1. (Low below time window.)
E25E 83 FB 04   C      cmp      bx,4                 ; return nz status. (jb has zf reset.)
E261 72 02      C      jb      rto_ohk_low
C
E263 FE CC      C      dec      ah                  ; Error #0. (No Error!) return z status.
C
E265           C      rto_ohk_high:
E265           C      rto_ohk_low:
E265           C      ret
C
E266           C      rto_ohk endp
C
C      -----
C      RAM (64k) Storage Test.
C      ;
C      Input: dx      = segment of RAM to be tested
C      ;
C      Output: zf     = set (z status) if no error; reset (nz status) if error
C      ;
C      ;          = dx:di = failing RAM location if error; else di = 0.
C      ;          = test pattern (what was written).
C      ;          = if error, what was read.
C      ;          = number left to test if error; else cx = 0.
C      ;
C      ;          Trash: None.
C      -----
E266          C      nearat      proc      near
C              assume   es:code, ds:nothing, es:nothing, ss:nothing
E266 B9 8000    C      mov      cx,08000h        ; get word count

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# ROM BIOS Listing

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E269 8E C2      C      mov     es,dx          ;      (64k = 32k * 2 bytes/word)
E26B 33 FF      C      xor     di,di          ; es:di = address
E26D           C      mentat_w1:
E26D 8B C7      C      mov     ax,di          ;data = offset
E26F AB         C      stow   mentat_w1
E270 E2 FB      C      loop   mentat_w1
E272 85 DA      C      mov     dx,dx
E274 33 DB      C      xor     bx,bx          ;dx:bx = address
E276 B9 8000    C      mov     cx,08000h     ; word count
E279           C      mentat_r1:
E279 8B 07      C      mov     ax,[bx]       ;read data
E27B 3B C3      C      cmp     ax,bx         ;verify data
E27D 75 2C      C      jne    mentat_err
E27F 43         C      inc    bx
E280 43         C      inc    bx
E281 E2 F6      C      loop   mentat_r1     ;next address
E283 B9 8000    C      mov     cx,08000h     ; word count
E286           C      mentat_w2:
E286 8B C7      C      mov     ax,di          ; address is already ok
E288 F7 D0      C      cmp     ax,bx         ; data = offset
E28A AB         C      stow   mentat_w2     ;fill memory
E28B E2 F9      C      loop   mentat_w2
E28D B9 8000    C      mov     cx,08000h     ; word count
E290           C      mentat_r2:
E290 8B 07      C      mov     ax,[bx]       ; read data
E292 77 D0      C      not    ax              ; complement
E294 3B C3      C      cmp     ax,bx         ; verify
E296 75 0F      C      jne    mentat_err_0
E298 43         C      inc    bx              ; update address
E299 43         C      inc    bx
E29A E2 F4      C      loop   mentat_r2
E29C B8 0000    C      mov     ax,0           ; to clear memory
E29F B9 8000    C      mov     cx,08000h     ; word count
E2A2 F3 AB      C      rep   stow
E2A4 08 C0      C      or     ax,ax
E2A6 C3         C      ret
E2A7           C      mentat_err_0:
E2A7 F7 D0      C      not    ax              ; error during complemented
E2A9 F7 D3      C      not    bx              ; address test
E2AB           C      mentat_err:
E2AB 93         C      xchg  ax,bx           ;return registers as specified
E2AC C3         C      ret
E2AD           C      mentat     endp
E2AD           C      code     ends
E2AD           C      include pwrup0.asm
E2AD           C      ;=====
E2AD           C      ;      Filename:      pwrup0.src
E2AD           C      ;
E2AD           C      ;      This module includes temporary hardware initialization.
E2AD           C      ;
E2AD           C      ;      includes      Diagnostics
E2AD           C      ;                  Cold Boot
E2AD           C      ;                  Device Drivers
E2AD           C      ;
E2AD           C      ;=====
E2AD           C      code     segment public 'ROM'
E2AD           C      assume  cs:code, ds:nothing, es:nothing, ss:nothing
E2AD           C
E2AD           C      p0_data1  proc     near
E2AD           C
E2AD 4F 70 74 69 6F 6E 8E  ; opt_ROM_m  db  'Optional ROM at ',NUL
E2AD 61 6C 20 52 4F 4D 20  ;
E2AD 20 61 74 20 00        ;
E2AD           C
E2AD           C      p_tbl  dw  prt_data_a  ; printer in port address space
E2AD           C      dw  prt_data_b  ; always on mother board.
E2AD           C      dw  prt_data_c  ; printer in port address space
E2AD           C      dw  0           ; no printer
E2AD           C
E2AD           C      sec_tbl dw  sec_otl_b  ; ra232 SCC channel B
E2AD           C      dw  sec_otl_a  ; ra232 SCC channel A
E2AD           C
E2AD           C      alt_ret dw  i_alt_restart ; 00h 28000 restart sequence offset
E2AD           C      dw  code_seg  ; 00h 28000 restart sequence segment
E2AD           C
E2AD           C      mastab dw  ((mt_end)-(mastab)) ; 00h master table byte length
E2AD           C
E2AD           C      dw  kb_data_table ; 02h kb xlation table offset
E2AD           C      dw  code_seg  ; 02h kb xlation table segment
E2AD           C
E2AD           C      dw  font_lo_8x8 ; 06h 1st 128 char.s 8x8 font offset
E2AD           C      dw  code_seg  ; 08h 1st 128 char.s 8x8 font segment
E2AD           C
E2AD           C      dw  font_lo_8x16 ; 0Ah 1st 128 char.s 8x16 font offset
E2AD           C      dw  code_seg  ; 0Ch 1st 128 char.s 8x16 font segment
E2AD           C
E2AD           C      dw  0           ; 0Eh 2nd 128 char.s 8x16 font offset
E2AD           C

```

# ROM BIOS Listing

```

E2DE 0000      C          dw      0          ; 10h 2nd 128 char.s 8x16 font segment
E2E0 0000      C          dw      0          ; 12h soft font utility offset
E2E2 0000      C          dw      0          ; 14h soft font utility segment
                                C          ; 16h etc...
E2E4          C      st_end label word
E2E4          C      p0_data1      endp
                                C
                                C      -----
                                C      ; Initialize the basic hardware,
                                C      ; Set up the interrupt pointers,
                                C      ; Initialize all RAM variables,
                                C      ; Clear the screen,
                                C      ; Initialize the disk drivers,
                                C      ; and perform the cold boot.
                                C      -----
E2E4          C      point1 proc      near
                                C
                                C          assume cs:code, ds:data, es:data, ss:stack_ram
                                C
                                C          mov     ax,data_seg      ; satisfy assumptions
                                C          mov     ds,ax
                                C          mov     es,ax
                                C
                                C      ; Initialize Keyboard Controller.
                                C
                                C          pushf      ; save flags and
                                C          ori         ; disable interrupts
                                C
                                C          mov     dx,p_kctrl      ; dx = p_kctrl
                                C          mov     al,40h      ; remove keyboard reset
                                C          out     dx,al
                                C
                                C          xor     cx,cx      ; delay
                                C          loop    $
                                C
                                C          mov     bh,1      ; enable self test
                                C          call   kb_cmd_send
                                C          mov     word ptr ds:[reset_flag],cx
                                C
                                C          xor     cx,cx      ; delay
                                C          loop    $
                                C      ; Flush any keyboard scan code and store AAh if we get it.
                                C
                                C      kb_flush:
                                C          in     al,kb_status      ; get 80h status
                                C          test    al,1      ; test output buffer bit
                                C          jz     kb_flush_back    ; jump if no character pending
                                C          in     al,p_kscan      ; get scan code from data port
                                C          cmp     al,0AAh      ; verify keyboard present
                                C          jnc     kb_flush
                                C          mov     word ptr ds:[reset_flag],ax      ; keyboard present
                                C      kb_flush_back:
                                C          loop   kb_flush      ;loop if zero
                                C
                                C          xor     cx,cx      ; delay
                                C          loop   $
                                C
                                C      ; Initialize System Variables.
                                C
                                C          mov     word ptr ds:[master_tbi_ptr+0000h],cs:[offset mastab]
                                C          mov     word ptr ds:[master_tbi_ptr+0002h],cs
                                C
                                C      ; Initialize Keyboard Driver Variables.
                                C
                                C          mov     ax,ds:[offset kb_buffer]      ; pointer to beginning of buffer
                                C          mov     word ptr ds:[buffer_head],ax      ; keyboard output pointer offset
                                C          mov     word ptr ds:[buffer_tail],ax      ; keyboard input pointer offset
                                C          mov     word ptr ds:[buffer_start],ax      ; keeps beginning of buffer
                                C
                                C          mov     word ptr ds:[buffer_end],ds:[offset kb_buffer]+(size kb_buffer)
                                C
                                C          ; Assume first not Deluxe Keyboard
                                C          and     byte ptr ds:[kb_flag],(not num_lock_mode)
                                C          and     byte ptr ds:[kb_flag+1],(not dlx_kb)
                                C
                                C          ; Send command to request ID code from keyboard.
                                C          mov     bh,05h      ; Read keyboard type
                                C          call   kb_cmd_send      ; -- send command.
                                C
                                C          xor     cx,cx      ; set up timeout count
                                C      kb_type_wait:
                                C          in     al,kb_status      ; get port status
                                C          test    al,1      ; data byte available?
                                C          jnz    kb_type_read     ; if so, go read it..
                                C          loop   kb_type_wait    ; else wait awhile longer.
                                C          jmp     kb_not_dlx     ; timeout, default to non-dlx
                                C
                                C      kb_type_read:
                                C          in     al,p_kscan      ; read ID byte..
                                C          test    al,01h      ; deluxe kb's bit set?
                                C          jz     kb_not_dlx
                                C
                                C          ; 01h bit set, so initialize to Deluxe Keyboard.
                                C

```



# ROM BIOS Listing

```

E357 80 0E 0017 R 20      C      or      byte ptr ds:[kb_flag],num_look_mode
E35C 80 0E 0018 R 01      C      or      byte ptr ds:[kb_flag+1],dix_kb
E361                      C      kb_not_dix:
E361 9D                    C      popfd      ; restore interrupt-
                        C      ; enable state.
                        C      ; Initialize Printer & Communication (RS-232) Driver Variables.
E362 80 14                C      mov      al,14h      ; printer default timeout = 20
E364 BF 0078 R            C      mov      di,ds:(offset printer_t_out)
E367 B9 0004              C      mov      cx,4
E36A F3/ AA               C      rep      stosb      ; es:di gets al
                        C      ; printer default timeout = 01
E36C 80 01                C      mov      al,01h
E36E BF 007C R            C      mov      di,ds:(offset serial_t_out)
E371 B9 0004              C      mov      cx,4
E374 F3/ AA               C      rep      stosb      ; es:di gets al
                        C      ; Determine Parallel Port Configuration.
                        C      assume es:code, ds:code, es:data, ss:stack_ram
E376 8C C8                C      mov      ax,cs
E378 8E D8                C      mov      ds,ax      ; satisfy assumptions
E37A 32 DB                C      xor      bl,bl      ; clear high byte of switch_bits
E37C BF 0008 R            C      mov      di,es:(offset printer_addr) ; es:di points at printer_base
E377 BE E2BE R            C      mov      si,ds:(offset p_tbl)      ; addresses of printer ports
E382                      C      i_prt_loop:
E382 AD                    C      lodsb      ; ax gets ds:si port address.
E383 0B C0                C      or      ax,ax      ; valid port address?
E385 74 14                C      jz      i_prt_exit ; exit if invalid port address
                        C      ; transfer to data register
E387 8B D0                C      mov      dx,ax
E389 B0 A5                C      mov      al,0A5h   ; load test pattern
E38B EE                  C      out      dx,al     ; output test pattern.
E38C 86 C4                C      xchg    al,ah     ; mov ah:al; trash al; & delay.
E38E 8C                  C      in      al,dx     ; input test pattern back.
E38F 3A C4                C      cmp     al,ah     ; what we read = test pattern ?
E391 75 EF                C      jnz    i_prt_loop ; if not, loop as port is absent
                        C      ; else, printer port is present
E393 8B C2                C      mov     ax,dx     ; retrieve port address
E395 AB                  C      stosw   ; es:di gets ax.
E396 80 C3 40            C      add     bl,040h   ; add to high byte of switch_bits
E399 EB E7                C      jmp    i_prt_loop ; will go around loop 3 times
E39B                      C      i_prt_exit:
                        C      ; Determine Communication (RS-232) Configuration (SCC 28530 & INS8250's).
E39B BF 0000 R            C      mov     di,es:(offset rs232_addr) ; es:di points at rs232_base
E39E BA 03FA              C      mov     dx,com_id_a ; read interrupt I.D. register
E3A1 EC                  C      in     al,dx      ; for first 8250 port.
E3A2 A8 F8                C      test    al,0F8h   ; bits #3-7 are always low if
E3A4 75 07                C      jnz    i_no_com_a ; installed.
E3A6 B8 03F8              C      mov     ax,com_data_a ; if present, load address of
E3A9 AB                  C      stosw   ; first 8250 data port.
E3AA 80 C3 02            C      add     bl,002h   ; es:di gets ax.
E3AD                      C      i_no_com_a:
                        C      ; es:di points next empty word
E3AD BA 02FA              C      mov     dx,com_id_b ; read interrupt I.D. register
E3B0 EC                  C      in     al,dx      ; for second 8250 port.
E3B1 A8 F8                C      test    al,0F8h   ; bits #3-7 are always low if
E3B3 75 07                C      jnz    i_no_com_b ; installed.
E3B5 B8 02F8              C      mov     ax,com_data_b ; if present, load address of
E3B8 AB                  C      stosw   ; second 8250 data port.
E3B9 80 C3 02            C      add     bl,002h   ; es:di gets ax.
E3BC                      C      i_no_com_b:
                        C      ; read switch settings to test
E3BC EA 66                C      in     al,sys_conf_a ; for SCC 28530 chip
E3BE A8 20                C      test    al,020h   ; bit #5: SCC chip installed
E3C0 74 08                C      jz     i_no_sccos ; if not, don't load SCC table
E3C2 BE E2C6 R            C      mov     si,ds:(offset scc_tbl) ; SCC 28530 control ports
E3C5 A5                    C      movsw   ; always 2 ports
E3C6 A5                    C      movsw   ; es:di gets ds:si (twice)
E3C7 80 C3 04            C      add     bl,2*(002h) ; add to high byte of switch_bits
E3CA                      C      i_no_sccos:
                        C      ; Determine Game Card Configuration.
E3CA BA 0201              C      mov     dx,game_card ; get game card address.
E3CD EC                  C      in     al,dx      ; bits #0-3 are low if installed
E3CE A8 0F                C      test    al,0Fh    ;
E3D0 75 03                C      jnz    i_no_game_card ; skip, if not present
E3D2 80 C3 10            C      add     bl,010h   ; add to high byte of switch_bits

```

# ROM BIOS Listing

```

E3D5          C      i_no_game_card:
C
C      ; Initialize High Byte of switch_bits.
E3D5 26: 88 1E 0011 R      C      mov     byte ptr es:[switch_bits+1],bl ; save high byte of switch_bits
C      ; Initialize 18259A PIC with appropriate interrupt mask and enable interrupts.
C
C      ;
C      ; mov     al,10111100b ; p_timer & kb & dsk at this point
C      ; mov     al,11111100b ; p_timer & kb only at this point.
E3DA 80 FC      C      mov     dx,pic_1
E3DC BA 0021    C      out    dx,al ; now set proper interrupt mask
E3DF EE        C
C
C      ; Send specific end of interrupt (SEOI) to pic 'command' port for keyboard.
C
C      ;
E3E0 80 61      C      mov     al,pic_seoi_1 ; specific end of interrupt
E3E2 BA 0020    C      mov     dx,pic_0 ; to pic 'command' port.
E3E5 EE        C      out    dx,al
E3E6 FB        C      sti     ; enable interrupts
C
C      ; Initialize Parallel Printer Interface.
C
E3E7 B4 01      C      mov     ah,1 ; initialize printer...
E3E9 33 D2      C      xor     dx,dx ; ...port 0
E3EB CD 17      C      int    17h
C
C      ; Initialize all 4 (2) 28530 Serial Communication Controller.
C      ; NOTE: Special function code (FF) for power up ONLY initialization of 8530
E3ED B9 0004    C      mov     ra_init:
E3FO          C      mov     ax,4
E3FO B8 FFF3    C      mov     ax,111111111100011b ; initialize SCC RS-232
C      ; 9600 baud,none,1 stop & 8 data
C      ; port number = loop - 1
E3F3 8B D1      C      mov     dx,ax
E3F5 4A        C      dec    dx ;
E3F6 CD 14      C      int    14h
E3F8 E2 F6      C      loop   ra_init
C
C      -----
C      ;Test for and Initialize optional ROMs
C      -----
C
C      assume es:code, ds:nothing, es:nothing, ss:nothing
E3FA BB C800    C      mov     bx,0C800h ; load starting segment
C
C      rom_scan_loop:
E3FD          C      mov     ds,bx
E3FD 8E DB      C      xor     si,si ; bx has pending segment
E3FF 33 F6      C      ; offset 0000h
C
E401 81 3C AA55  C      cmp     word ptr ds:[si],0AA55h
E405 75 43      C      jne    rom_scan_next
C
E407 BE E2AD R   C      mov     si,es:(offset opt_ROMs) ; indicate ROM detected
E40A E8 E5FA R   C      call  DROMString
C
E40D 33 C0      C      xor     ax,ax
E40F E8 E632 R   C      call  DHexLong ; ds:ax points at ROM
C
E412 B8 E820    C      mov     ax,(0Eh*100h)+' ' ; put out SPACE
E415 CD 10      C      int    10h
C
E417 B8 0040    C      mov     ax,data_seg ; satisfy assumptions
E41A 8E C0      C      mov     es,ax ; for es in rom_check
E41C 33 F6      C      xor     si,si ; ds:si points to ROM to check
C
C      ;
C      ; Now: ds:si = pointer to ROM to be tested
C      ; bx = ds = pending segment of ROM under test
C      ; es: = data segment
C
C      assume es:code, ds:nothing, es:data, ss:nothing
C
E41E 33 C0      C      xor     ax,ax ; clear al
E420 8A 64 02    C      mov     ah,byte ptr ds:[si+2] ; ax = (ROM length/512) * 256
E423 D1 E0      C      shl     ax,1 ; ax = (ROM length/512) * 512
C      ; ax = ROM length in bytes
C      ; save ROM length
E425 50        C      push  ax
E426 B1 04      C      mov     ol,4
E428 D3 E8      C      shr     ax,cl ; advance segment for next ROM
E42A 03 D8      C      add     bx,ax ; by the number of paragraphs
E42C 59        C      pop     ax ; restore ROM length in ax
C
E42D E8 E5E8 R   C      call  rom_checksum_cnt ; get the checksum of the ex-
C      ; byte ROM.
E430 74 03      C      jz     rom_chksum_ok ; OK if the checksum was zero
E432 E9 E5D5 R   C      jmp     rom_err ; error the checksum wasn't zero
C
E435          C      rom_chksum_ok:
E435 53        C      push  bx ; save the segment for next ROM
C
E436 26: C7 06 0067 R 0003 C      mov     word ptr es:[io_rom_init],0003h
E43D 26: 8C 1E 0069 R   C      mov     word ptr es:[io_rom_seg],ds
E442 26: FF 1E 0067 R   C      call  dword ptr es:[io_rom_init] ; initialize the ROM
C
E447 5B        C      pop     bx ; restore segment for next ROM
C
E448 EB 04      C      jmp     short rom_scan_exit
C
E44A          C      rom_scan_next:
E44A 81 C3 0080    C      add     bx,(800h/10h) ; add 2k to the pending segment
C

```

# ROM BIOS Listing

```

E44E                                     C rom_scan_exit:
E44E 81 FB F600                          C     cmp     bx,0PF00h                ; are we done?
E452 7C A9                               C     jnge   rom_scan_loop            ; if not, continue
C
C
C -----
C ; HDU Test
C -----
C
C     assume  cs:code, ds:abs0, es:nothing, ss:stack_ram
E454 33 C0                               C     xor     ax,ax                    ; satisfy assumptions
E456 8E D8                               C     mov     ds,ax
C
C ; Check int 41h to see if any one installed a HDU parameter table pointer.
C
C     mov     ax,word ptr ds:[(4*41h)+0000h]
E458 A1 0104                             C     or     ax,word ptr ds:[(4*41h)+0002h]
E45B 0B 06 0106                          C     jnz     i_hdu_ok                ; if so, let them be...
E45F 75 1C                               C
C ; If not, call HDU initialization routine.
C
C     mov     si,cs:(offset i_hdu_m)
E461 BE DD28 R                            C     call   DROMString              ; print test message
E464 BE E5FA R                            C
C     call   h_init
C
C     assume  cs:code, ds:data, es:nothing, ss:stack_ram
C
C     mov     ds,word ptr cs:[set_da_word] ; satisfy assumptions
E46A 2E: 8E 1E E5F2 R                    C     cmp     byte ptr ds:[hf_num],0   ; number of hard disks.
E46F 80 3E 0075 R 00                     C     jnz     i_hdu_ok                ; if ok, leave everything alone.
E474 75 07                               C
C
C     mov     sp,100h                  ; re-initialize stack
E476 BC 0100                             C     ori     i_vector                 ; disable interrupts
E479 FA                                     C     call   i_vector                 ; re-install old vectors
E47A BE E1A0 R                            C
C
C i_hdu_ok:
C
C ; Clean Up after Option ROM's
C
C     ori     ; disable interrupts
E47D FA                                     C
C
C     mov     dx,ptr_1                ; get current interrupt mask
E47E BA 0021                             C     in     al,dx
E481 EC                                     C     and    al,10111100b
C ; ;                                     C     and    al,11111100b             ; P_timer & kb & dsk at this point.
E482 24 FC                                     C     out   dx,al                     ; P_timer & kb must be on at this point.
E484 8E                                     C
C
C     assume  cs:code, ds:abs0, es:nothing, ss:stack_ram
C
C     xor     ax,ax
E485 33 C0                               C     mov     ds,ax
E487 8E D8                               C     mov     word ptr ds:[int8loc+0000h],cs:(offset bt_int)
E489 CT 06 0060 R P860 R                 C     mov     word ptr ds:[int8loc+0002h],cs ; (ROM BASIC not available)
E48F 8C 0E 0062 R                            C
C
C     sti     ; enable interrupts
E493 FB                                     C
C
C -----
C ; FDU Test
C -----
C
C ; Initialize Floppy Disk Controller and related Driver Variables
C
C     xor     ax,ax                    ; initialize the disk routines
E494 33 C0                               C     xor     bx,bx
E496 33 DB                               C     xor     cx,cx
E498 33 C9                               C     xor     dx,dx
E49A 33 D2                               C     INT    13h
E49C CD 13                               C
C
C ; Dummy Disk Attachment Test to Spin Up Drive for INT 19h (boot-strap).
C
C     mov     si,cs:(offset i_fdu_m)
E49E BE DD01 R                            C     call   DROMString              ; print test message
E4A1 BE E5FA R                            C
C
C     mov     bp,3                      ; loop counter
E4A4 BD 0003                             C
C i_fdu_lp:
E4A7                                     C     mov     ax,0201h                ; read one sector
E4A7 B8 0201                             C
C
C     xor     bx,bx
E4AA 33 DB                               C     mov     ds,bx
E4AC 8E DB                               C     mov     es,bx                    ; xfer_segment
E4AE 8E C3                               C     mov     bx,7C00h                 ; xfer_offset
E4B0 BB 7C00                             C
C
C     mov     cx,0001h                  ; track 0; sector 1
E4B3 B9 0001                             C     xor     dx,dx                    ; head 0; drive 0
E4B6 33 D2                               C
C
C     push   bp                          ; save retry count
E4B8 55                                     C     push   ax                        ; save return registers
E4B9 50                                     C     push   es
E4BA 06                                     C     INT    13h                       ; bx, cx, dx, & ds preserved
E4BB CD 13                               C     pop    es                        ; restore return registers
E4BD 07                                     C     pop    ax
E4BE 58                                     C     pop    bp                        ; restore retry count
E4BF 5D                                     C
C
C     jnc    i_fdu_ok                    ; error during read?
E4C0 73 08                             C     dec    bp                        ; if so, decrement retry count
E4C2 4D                                     C     jnz    i_fdu_lp                  ; and try again
E4C3 75 E2                               C
C
C     mov     si,cs:(offset i_fdu_not_m) ; drive not ready message.
E4C5 BE DD1B R                            C

```

# ROM BIOS Listing

```

E4C8 EB 03          C          jmp      short i_fdu_end
E4CA BE DD1F R     C          i_fdu_ok:
E4CD              C          mov      si,es:(offset i_fdu_rdy_m) ; drive ready message.
E4CD              C          i_fdu_end:
E4CD E8 E5FA R     C          call   DRonString
E4D0              C          ; Initialize & enable NMI's (parity register).
E4D0 BA 0061       C          mov      dx,p_kctrl
E4D3 EC           C          in      al,dx
E4D4 0C 30        C          or      al,030h ; enable bits #5 & #4
E4D6 EE           C          out     dx,al
E4D7              C          ; If alternate processor is available, let user select which one to use.
E4D7              C          i_alt_cpu:
E4D7 9C           C          pushf   ax ; preserve state for int 19h
E4D8 50           C          push   bx
E4D9 53           C          push   cx
E4DA 51           C          push   dx
E4DB 52           C          push   bp
E4DC 55           C          push   di
E4DD 57           C          push   si
E4DE 56           C          push   ds
E4DF 1E           C          push   es
E4E0 06           C          assume cs:code, ds:data, es:nothing, ss:nothing
E4E1 2E: BE 1E E5F2 R C          mov      ds,word ptr es:[set_da_word] ; satisfy assumptions
E4E5 A1 0072 R     C          mov      ax,word ptr ds:[reset_flag] ; get result of keyboard test
E4E9 3C AA        C          cmp     al,0AAh ; is keyboard attached?
E4EB 74 03        C          je      i_alt_cont ; jump if yes (continue)
E4ED EB 7D 90      C          jmp     i_init_end ; jump if no (in mfg)
E4F0              C          i_alt_cont:
E4F0 FA           C          cli ; disable interrupts
E4F1              C          assume cs:code, ds:abs0, es:nothing, ss:nothing
E4F1 33 C0        C          xor     ax,ax ; set up absolute zero address
E4F3 8E D8        C          mov     ds,ax ; for alternate opu semaphore
E4F5 8B 16 0000   C          mov     dx,word ptr ds:0 ; save word at 0:0
E4F9 52           C          push   dx
E4FA A2 0000       C          byte ptr ds:0,al ; request alt cpu id (0:0 = 0)
E4FD BA 80C1h     C          mov     dx,80C1h ; Z8000 liaison port
E500 B0 01        C          mov     al,1 ; AL:1 starts Z8000
E502 EE          C          out     dx,al ; try to boot Z8000
E503 B9 00FF     C          mov     cx,0FFh ; loop counter
E506              C          i_alt_test:
E506 80 3E 0000 01 C          cmp     byte ptr ds:0,01h ; has the semaphore changed?
E508 74 04        C          je      i_alt_found ; jump if yes (Z8000 id = 1)
E50D E2 FF       C          loop   i_alt_test ; wait for Z8000 to gain control
E50F EB 56        C          jmp     short i_alt_end ; jump: no alternate opu
E511              C          i_alt_found:
E511 58           C          pop     ax ; restore word at 0:0
E512 43 0000     C          mov     word ptr ds:0,ax ; reave for future pop
E515 50           C          push   ax
E516 FB          C          sti ; enable interrupts
E517 E8 E619 R   C          call   DCrLr
E51A BE DD35 R   C          mov     si,es:(offset i_alt_select_m) ; ask user if alt. cpu used
E51D E8 E5FA R   C          call   DRonString
E520 33 D2        C          xor     dx,dx ; for int 14h
E522              C          i_alt_inq:
E522 BA 01        C          mov     ah,1 ; has a key been struck?
E524 CD 16        C          INT    16h
E526 74 FA        C          jz     i_alt_inq ; if not, stay in loop
E528 32 E4        C          xor     ah,ah ; if so, get the keystroke
E52A CD 16        C          INT    16h
E52C 0C 20        C          or      al,00100000b ; force lower case
E52E 3C 79        C          cmp     al,'y' ; did user mean "yes"
E530 74 02        C          je      i_alt_echo ; jump if yes
E532 B0 6E        C          mov     al,'n' ; force "no"
E534              C          i_alt_echo:
E534 BA 0E         C          mov     ah,0Eh ; echo "y" or "n"
E536 CD 10        C          INT    10h
E538 3C 79        C          cmp     al,'y' ; was answer "yes"
E53A 75 2B        C          jne    i_alt_end ; jump if no
E53C E8 E619 R   C          call   DCrLr
E53F FA          C          cli ; disable interrupts
E540 C6 06 0000 0F C          mov     byte ptr ds:0,0Fh ; tell Z8000 to take over
E545              C          i_alt_restart:
E545 BA 80C1h     C          mov     dx,80C1h ; Z8000 liaison port
E548 B0 01        C          mov     al,1 ; AL:1 starts Z8000
E54A EE          C          out     dx,al ; pass control to Z8000
E54B B9 00FF     C          mov     cx,0FFh ; loop counter
E54E E2 FE        C          loop   $ ; wait for Z8000 to gain control

```

# ROM BIOS Listing

```

C
E550 33 C0          xor     ax,ax          ; we're here only if 28000 released control
E552 8E D8          mov     ds,ax         ; reset segment register
E554 80 3E 0000 10  cap     byte ptr ds:0,10h ; to absolute zero
E559 72 CC          jb     i_alt_end      ; is a jump requested?
E55B 8C C8          mov     ax,cs         ; no, try to boot (or crash)
E55D 8E C0          mov     es,ax         ; pass return registers so that:
E55F BD E2CA R      mov     bp,offset alt_ret ; restarts 28000 as desired
C                    jmpf   0,0             ;
E562 EA            db     0EAh          ; intersegment direct jmp to 0:0
E563 0000          dw     0
E565 0000          dw     0
C
C ; End of Initialization.
C
E567              i_alt_end:
E567 58            pop     ax             ; restore word at 0:0
E568 A3 0000      mov     word ptr ds:0,ax
E56B FB            sti                     ; enable interrupts
C
E56C              i_init_end:
E56C BA 0378      mov     dx,0378h      ; printer port
E56F B0 80        mov     al,80h        ; OK status
E571 EE            out     dx,al         ; tell arg tester
C
E572 07            pop     es             ; restore state for boot
E573 1F            pop     ds
E574 5E            pop     si
E575 5F            pop     di
E576 5D            pop     bp
E577 5A            pop     dx
E578 59            pop     cx
E579 58            pop     bx
E57A 58            pop     ax
E57B 9D            popf
C
E57C E8 E619 R     call   DCrLf
E57F CD 19        int    19h           ; go to boot-strap routine
C
E581              ppoint endp
C
C ; Send command in AH to keyboard interface processor. AX is used.
C
E581              kb_cmd_send proc near
C
C kb_cmd_wlup:
E581 EN 64        in     al,kb_status   ; get 8041 port status
E583 A8 02        test   al,10b        ; ready to receive?
E585 75 FA        jnz   kb_cmd_wlup
C
E587 8A C4        mov   al,ah          ; ready, send command
E589 B6 60        out   port,al
E58B C3            ret
C
E58C              kb_cmd_send endp
C
E58C              ocode ends
C
C include pwrup2.asm
C
C ;=====
C ; Filename: pwrup2.sro
C ;
C ; This module includes 8259 Interrupt, Video Controller, 8087
C ; NPU, and 8253 & MM58174 Clock tests.
C ;=====
C
E58C              ocode segment public 'ROM'
C                    assume os:ocode, ds:nothing, es:nothing, ss:nothing
C ;=====
C ; Note: We are called from ill_int ONLY (see vector.sro), and
C ; stack looks like this:
C ;
C ; High Address
C ; (10) |-----| return faw flags |<-- sp before ill_int trap
C ; (0E) |-----| return os segment |
C ; (0C) |-----| return ip offset |
C ; (0A) |-----| ax |<-- sp after ill_int trap
C ; (08) |-----| ds |
C ; (06) |-----| near call here |<-- sp after ill_int pushes
C ; (04) |-----| ax |<-- sp after ill_int calls ill_trap
C ; (02) |-----| dx |
C ; (00) |-----| si |<-- sp after ill_trap pushes
C ; Low Address
C ;=====
C                    assume os:ocode, ds:nothing, es:nothing, ss:nothing
C
E58C              ill_trap proc near

```

# ROM BIOS Listing

```

; Turn off floppy disk drives.
C
C
E58C 50          C          push    ax                ; save registers
E58D 52          C          push    dx
E58E 56          C          push    si
C
E58F E8 EF4F R   C          call    stop_disk         ; destroys ax & dx
C
E592 E8 E5C4 R   C          call    ill_ln
E595 BE DC1B R   C          mov     si,cs:(offset ill_m1) ; part 1 of message
E598 E8 E5FA R   C          call    DRomString
C
E59B 8B FA       C          mov     si,sp
E59D 36: 8E 5C 0E C          mov     ds,word ptr ss:[si+0Eh] ; cs past si,dx,ax,ret,ds,ax,ip
E5A1 36: 8B 74 0C C          mov     si,word ptr ss:[si+0Ch] ; ip past si,dx,ax,ret,ds,ax
C
E5A5 4E          C          dec     si                ; si points to interrupt number
E5A6 8A 04       C          mov     al,byte ptr ds:[si]   ; print illegal interrupt number
E5A8 E8 E643 R   C          call    DHexByte
E5AB 4E          C          dec     si                ; si points to interrupt instr.
E5AC 8B C6       C          mov     ax,si              ; save pointer
C
E5AE BE DC34 R   C          mov     si,cs:(offset ill_m2) ; part 2 of message
E5B1 E8 E5FA R   C          call    DRomString
C
E5B4 E8 E632 R   C          call    DHexLong           ; print illegal cs:ip = ds:ax
C
E5B7 BE DC3A R   C          mov     si,cs:(offset ill_m3) ; part 3 of message
E5BA E8 E5FA R   C          call    DRomString
E5BD E8 E5C4 R   C          call    ill_ln
C
E5C0 5E          C          pop     si                ; restore registers
E5C1 5A          C          pop     dx
E5C2 5B          C          pop     ax
E5C3 C3          C          ret
C
E5C4 E8 E619 R   C          ill_ln: call    DCrLf        ; prints a line of '*'s
E5C7 B2 2A       C          mov     dl,42
C
E5C9 BB 0E2A      C          ill_lp: mov     ax,(0Eh*100b)*('')
E5CC CD 10        C          INT     10h
E5CE FE CA       C          dec     dl
E5D0 75 F7       C          jnz    ill_lp
E5D2 EB 45 90     C          jmp     DCrLf
C
E5D5          C          ill_trap    endp
C
E5D5          C          code    ends
C          include pwrup3.asm
C
;=====
C          Filename:      pwrup3.asm
C
;          This module includes 8041 keyboard, communication LSI, RAM, and
C          optional ROM tests.
C
;=====
E5D5          C          code    segment public 'ROM'
C
C          assume cs:code, ds:nothing, es:data, ss:nothing
C
;-----
C          Input:  ds      = segment of ROM under test
C          ;       es      = firmware data segment
C
;          Trash: All other registers except bx destroyed (in general).
C          ;-----
E5D5          C          rom_err    proc    near
C          ;       assume cs:code, ds:nothing, es:data, ss:nothing
C
E5D5 8C D8       C          mov     ax,ds
E5D7 26: 88 26 0015 R C          mov     byte ptr es:[mfg_err_flag],ah ; high byte of ROM address
C
E5DC BE DC45 R   C          mov     si,cs:(offset fail_m) ; indicate ROM failed
E5DF E8 E5FA R   C          call    DRomString
E5E2 EB 35 90     C          jmp     DCrLf
C
E5E5          C          rom_err    endp
C
C
C          assume cs:code, ds:nothing, es:nothing, ss:nothing
C
;-----
C          Input:  ds:si    = pointer to ROM to be tested
C          ;
C          Output: ah      = checksum for the ROM
C          ;       cx      = 0
C          ;       si      = pointer to byte past ROM
C          ;       zf      = state of checksum for the ROM
C
;          Trash:  al destroyed.
C          ;-----
E5E5          C          rom_checksum proc    near
C          ;       assume cs:code, ds:nothing, es:nothing, ss:nothing

```

# ROM BIOS Listing

```

E5E5 B9 2000      C      mov     cx,2000h
E5E8             C      rom_checksum_cnt:
E5E8 33 C0         C      xor     ax,ax           ; clear ah
E5EA             C      rom_checksum_loop:
E5EA AC          C      lodsb                    ; 12 ah gets ds:si
E5EB 02 E0       C      add     ah,al           ; 3
E5ED E2 FB       C      loop   rom_checksum_loop ; 17
E5EF 0A EA       C      or     ah,ah
E5F1 C3          C      ret
E5F2             C      rom_checksum   endp
E5F2             C      code   ends
E5F2             C      include pwrup4.asm
E5F2             C      ;=====
E5F2             C      ;      Filename:      pwrup4.src
E5F2             C      ;
E5F2             C      ;      This module includes disk drive tests, system initialization,
E5F2             C      ;      keyboard boot-strap options, and message routines.
E5F2             C      ;
E5F2             C      ;=====
E5F2             C      code   segment public 'ROM'
E5F2             C      assume cs:code, ds:nothing, es:nothing, ss:nothing
E5F2             C      ;=====
E5F2             C      ;      Utility Routines:
E5F2             C      ;
E5F2             C      ;      DRomString      DString      DCrLf      DColon
E5F2             C      ;      DHexLong       DHexWord    DHexByte   DHexNib
E5F2             C      ;      DNum           DNumW
E5F2             C      ;=====
E5F2             C      pH_data1   proc   near
E5F2             C      even
E5F2 0040         C      set_ds_word dw     data_seg           ; 2 bytes   = 0 olocks
E5F4             C      pH_data1   endp
E5F4             C      set_ds     proc   near           ; set ds to firmware data segment
E5F4             C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E5F4 2E: 8E 1E E5F2 R C      mov     ds,word ptr cs:[set_ds_word] ; 5 bytes 2*9+6 = 17 olocks
E5F9 C3          C      ret                               ; 1 byte   = 8 olocks
E5FA             C      ;-----
E5FA             C      set_ds     endp
E5FA             C      ;=====
E5FA             C      ;      Display ASCII String Utilities
E5FA             C      ;=====
E5FA             C      DRomString proc   near           ; Displays NUL terminated string at ds:si
E5FA             C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E5FA 1E          C      push  ds           ; all registers saved
E5FB 0E          C      push  es           ; ds gets cs
E5FC 1F          C      pop   ds
E5FD E8 E602 R   C      call  DString
E600 1F          C      pop   ds           ; restore ds
E601 C3          C      ret
E602             C      DRomString   endp
E602             C      DString     proc   near           ; Displays NUL terminated string at ds:si
E602             C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E602 50          C      push  ax           ; all registers & flags saved
E603 53          C      push  bx
E604 56          C      push  si
E605 9C          C      pushf
E606 FC          C      old
E607 B3 01       C      mov     bl,1           ; auto increment
E609 AC          C      DS_lp: lodsb                    ; select foreground color for grafix modes
E60A 04 C0       C      or     al,al           ; al gets ds:si and si++
E60C 74 0E       C      je     DS_ret          ; NUL ?
E60E B4 0E       C      mov     ah,0Eh        ; tty emulator
E610 CD 10       C      INT   10h
E612 EB F5       C      jmp     short DS_lp
E614             C      DS_ret:
E614 9D          C      popf                    ; restore registers & flags
E615 5E          C      pop   si
E616 5B          C      pop   bx
E617 58          C      pop   ax
E618 C3          C      ret
E619             C      DString     endp
E619             C      DCrLf      proc   near           ; Displays a CR & LF.
E619             C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E619 50          C      push  ax           ; all registers preserved
E61A B8 0E0D     C      mov     ax,(0Eh*100h)+CR
E61D CD 10       C      INT   10h           ; tty emulator
E61F B8 0E0A     C      mov     ax,(0Eh*100h)+LF
E622 CD 10       C      INT   10h           ; tty emulator
E624 58          C      pop   ax           ; restore ax

```

# ROM BIOS Listing

```

E625 C3      C      DCrLf      ret      endp
E626      C      C
E626      C      DColon     proc      near      ; Displays a ':'.
E626 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E627 53      C      push     bx      ; all registers preserved
E628 B3 01   C      mov      bl,1    ; select foreground color for grafix modes
E62A B8 0E3A C      mov      ax,(0Eh*100h)+';'
E62D CD 10   C      INT     10h     ; tty emulator
E62P 5B     C      pop      bx      ; restore registers
E630 5B     C      pop      ax
E631 C3      C      ret
E632      C      DColon     endp
C
C
;=====
; Display Hexadecimal Number in CII Utilities
;=====
C
E632      C      DHexLong   proc      near      ; Displays ds:ax in ASCII
E632 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E633 8C D8   C      push     ax      ; all registers preserved
E635 B8 E63C R C      mov      ax,ds   ; display segment first
C      call    DHexWord
E638 B8 E626 R C      call    DColon   ; display a colon
C
E63B 5B     C      pop      ax      ; restore ax
C      jmp     short DHexWord ; fall through: display offset second
C
E63C      C      DHexLong   endp
C
E63C      C      DHexWord   proc      near      ; Displays ax in ASCII
E63C 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E63D 8A C4   C      push     al,ah   ; all registers preserved
E63F B8 E643 R C      call    DHexByte  ; display high byte first
E642 5B     C      pop      ax      ; restore ax
C      ; jmp     short DHexByte ; fall through: display low byte second
C
E643      C      DHexWord   endp
C
E643      C      DHexByte   proc      near      ; Displays al in ASCII
E643 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E644 DO C8   C      push     al,1    ; all registers preserved
E646 DO C8   C      ror     al,1
E648 DO C8   C      ror     al,1
E64A DO C8   C      ror     al,1
E64C B8 E650 R C      call    DHexNib   ; move high nibble to low nibble
E64F 5B     C      pop      ax      ; display high nibble in ASCII
C      ; jmp     short DHexNib ; restore ax
C      ; jmp     short DHexNib ; fall through: display low nibble in ASCII
C
E650      C      DHexByte   endp
C
E650      C      DHexNib   proc      near      ; Displays low nibble of al in ASCII
E650 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E651 53      C      push     bx      ; all registers preserved
E652 B3 01   C      mov      bl,1    ; select foreground color for grafix modes
E654 2A 0F   C      and     al,0Fh   ; clear high nibble
E656 0A 30   C      add     al,'0'
E658 3C 39   C      cmp     al,'9'
E65A 76 02   C      jbe     NibOk   ; '0' <= al <= '9' ?
E65C 04 07   C      add     al,'A'-'0'-10
E65E B8 0E   C      NibOk: mov  ah,0Eh ; tty emulator
E660 CD 10   C      INT     10h
E662 5B     C      pop      bx      ; restore registers
E663 5B     C      pop      ax
E664 C3      C      ret
E665      C      DHexNib   endp
C
;=====
; Display Decimal Number in ASCII Utilities
;=====
C
E665      C      DNum      proc      near      ; Displays decimal of ax in ASCII in min width
E665 53      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E666 33 DB   C      push     bx      ; all registers preserved
E668 B8 E66D R C      xor     bx,bx    ; minus width
E66B 5B     C      call    DNumW    ; display ax
E66C 5B     C      pop      bx      ; restore bx
E66D      C      ret
C
E66D      C      DNum      endp
C
E66D      C      DNumW     proc      near      ; Displays decimal of ax in ASCII of width bx
E66D 50      C      assume   cs:code, ds:nothing, es:nothing, ss:nothing
E66D 50      C      push     ax      ; all registers preserved
E66E 53      C      push     bx
E66F 51      C      push     cx
E670 52      C      push     dx
E671 56      C      push     si
C
E672 B8 000A C      mov     si,10    ; decimal modulus
E675 33 C9   C      xor     cx,cx    ; clear digit counter
E677      C      DNumW_loop:
E677 33 D2   C      xor     dx,dx
E679 F7 F6   C      div     si      ; dh = 0
C      ; dl = remainder = (0-9)

```



# ROM BIOS Listing

```

E67B 52          C          push   dx          ; ax = quotient = higher order digits
E67C 41          C          inc     cx          ; save the digit on stack
E67D 0B C0       C          or     ax,ax       ; increment count of what's on stack
E67F 75 F6       C          jnz    DNumW_loop  ; are we done?
E681 2B D9       C          sub    bx,cx       ; subtract digit count from width
E683 76 08       C          jbe    DNumW_skip ; skip spaces if bx is not > cx
E685            C          DNumW_spaces:
E685 B8 0220      C          mov    ax,(02h*100b)-' ' ; display a space
E688 CD 10       C          int   10h         ; INT
E68A 4B          C          dec   bx          ; decrement count of spaces
E68B 75 F8       C          jnz    DNumW_spaces ; keep going
E68D            C          DNumW_skip:
E68D B3 01        C          mov    bl,1       ; foreground color for grafix modes
E68F 58          C          pop   ax          ; remove digit from stack
E690 04 30       C          add   al,'0'      ; convert to ASCII
E692 B4 0E       C          mov   ah,0Eh     ; display the digit
E694 CD 10       C          int   10h         ; INT
E696 E2 F5       C          loop  DNumW_skip
E698 5E          C          pop   si          ; restore registers
E699 5A          C          pop   dx
E69A 59          C          pop   cx
E69B 5B          C          pop   bx
E69C 58          C          pop   ax
E69D C3          C          ret
E69E            C          DNumW   endp
E69E            C          oode   ends
E69E            C          include boot1.asm
E69E            C          ;-----
E69E            C          ;          Filename:      boot1.src
E69E            C          ;
E69E            C          ;          This module includes the ORG'd jump to INT 19h (boot2.src)
E69E            C          ;-----
E69E            C          oode   segment public 'ROM'
E69E            C          assume cs:code, ds:nothing, es:nothing, ss:nothing
E6F2            C          ORG   0E6F2h
E6F2            C          bt_jmp proc near
E6F2 H9 F860 R   C          jmp  bt_int      ; necessary jump for ORG
E6F5            C          bt_jmp endp
E6F5            C          oode ends
E6F5            C          include com1.asm
E6F5            C          ;-----
E6F5            C          ;          Filename:      com1.src
E6F5            C          ;
E6F5            C          ;          This module, com2, and com3 supply INT 14h.
E6F5            C          ;-----
E6F5            C          oode   segment public 'ROM'
E6F5            C          assume cs:code, ds:nothing, es:nothing, ss:nothing
E6F5            C          ;-----
E6F5            C          ;-----
E6F5            C          ;          IN$8250 Compatible Line Status Bits (ah) for Z8530 SCC Re-Mapping
E6F5            C          ;-----
= 0080          C          com_rxd   equ    80h          ; time out error (bit #7)
= 0020          C          com_txd   equ    20h          ; transmit ready (bit #5)
= 0008          C          com_fe    equ    08h          ; framing error (bit #3)
= 0004          C          com_pe    equ    04h          ; parity error (bit #2)
= 0002          C          com_oe    equ    02h          ; overrun error (bit #1)
= 0001          C          com_rxd   equ    01h          ; receive ready (bit #0)
E6F5            C          ;-----
E6F5            C          ;-----
E6F5            C          ;          IN$8250 Compatible Modem Status Bits (al) for Z8530 SCC Re-Mapping
E6F5            C          ;-----
= 0020          C          com_dsr   equ    20h          ; data set ready (bit #5)
= 0010          C          com_ots   equ    10h          ; clear to send (bit #4)
E6F5            C          ;-----
E6F5            C          ;-----
E6F5            C          ;          IN$8250 Compatible Modem Control Bits.
E6F5            C          ;-----
= 0002          C          com_rts   equ    02h          ; request to send (bit #1)
= 0001          C          com_dtr   equ    01h          ; data terminal ready (bit #0)
E6F5            C          ;-----
E6F5            C          ;-----
E6F5            C          ;          Z8530 SCC Status Register (Read Register #0)
E6F5            C          ;-----
= 0004          C          scc_txd   equ    04h          ; transmit ready (bit #2)
= 0001          C          scc_rxd   equ    01h          ; receive ready (bit #0)
E6F5            C          ;-----
E6F5            C          ;-----
E6F5            C          ;          Z8530 SCC Error Register (Read Register #1)
E6F5            C          ;-----

```

# ROM BIOS Listing

```

C ;-----
C
= 0040
= 0020
= 0010
C sec_fe equ 40h ; framing error (bit #6)
C sec_oe equ 20h ; overrun error (bit #5)
C sec_pe equ 10h ; parity error (bit #4)
C
C ;-----
C ; INS8250 Asynchronous Communication Chip Baud Rate Time Constants
C ; (baud rate generator signal is 3.6864 MHz put through a
C ; divide-by-2 circuit.
C ;
C ; Time Constant = ((3,686,400 Hz)/2) = Input Freq.
C ; (16)*(baud rate)
C ;-----
E729
C
C ORG 0E729h
C
E729
C oom_data1 proc
C
C oom_baud dw 1047 ; 110 baud (0)
C dw 768 ; 150 baud (1)
C dw 384 ; 300 baud (2)
C dw 192 ; 600 baud (3)
C dw 96 ; 1200 baud (4)
C dw 48 ; 2400 baud (5)
C dw 24 ; 4800 baud (6)
C dw 12 ; 9600 baud (7)
C
C .list
C
E739
C oom_data1 endp
C
C ;-----
C ; Z8530 Serial Communication Controller Baud Rate Time Constants
C ; (baud rate generator signal is 3.6864 MHz)
C ; (NO divide-by-2 circuit!!!!)
C ;
C ; Time Constant = (3,686,400 Hz) = Input Freq.
C ; (16)*(2)*(baud rate) - 2
C ;
C ; NOTE: These values are the SAME as the above EXCEPT for the - 2!!!!
C ;-----
C
C iscc_baud dw 1045 ; 110 baud (0)
C dw 766 ; 150 baud (1)
C dw 382 ; 300 baud (2)
C dw 190 ; 600 baud (3)
C dw 94 ; 1200 baud (4)
C dw 46 ; 2400 baud (5)
C dw 22 ; 4800 baud (6)
C dw 10 ; 9600 baud (7)
C
C .list
C
C ;-----
C ; INT 14h -- RS-232 Software Interrupt Request Routine
C ;
C ; Assumes: INS8250 port addresses are > 256. That is, the
C ; high byte of the port address is nonzero, if and
C ; only if, the port is a INS8250. (e.g. com_a ports
C ; are 03F8h - 03F9h & com_b ports are 02F8h - 02F9h.)
C ;
C ; Similarly: Z8530 port addresses are < 256. That is, the
C ; high byte of the port address is zero, if and
C ; only if, the port is a Z8530. (e.g. scc_a ports
C ; are 0050h - 0051h & scc_b ports are 0052h - 0053h.)
C ;
C ; Z8530 Note: For the reset during power-up, DTR and RTS must be
C ; set low which is the only difference from a normal
C ; reset (AH=0). This is accomplished by a special
C ; function code (AH=0FFh).
C ;-----
C
C ORG 0E739h
C
E739
C serial_io proc near
C assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C sti ; enable interrupts
E73A 55 push bp ; save register
C
E73B 83 FA 04 cmp dx,4 ; 4 RS-232 channels allowed max
E73E 73 3D jae rs_nop
C
E740 8B E8 mov bp,ax ; save original function code
E742 80 FC FF cmp ah,0FFh ; power-up Reset?
E745 75 02 jne rs_norm ; jump if no
E747 32 E4 xor ah,ah ; same as reset, BP remembers FF
C
C rs_norm:
E749 80 FC 03 cmp ah,03h ; input out of range?
E74C 77 2F ja rs_nop
C
C assume cs:code, ds:data, es:nothing, ss:nothing
C
C push dx ; save registers
E74E 52
C74F 51 push cx
E750 53 push bx
E751 1E push ds ; save ds

```

# ROM BIOS Listing

```

E752 2E: 8E 1E E5F2 R      C      mov     ds,word ptr cs:[set_ds_word]      ; satisfy assumptions
E757 8B DA                  C      mov     bx,dx                            ; get port number (0-3)
E759 33 C9                  C      xor     cx,cx                            ; clear ch
E75B 8A 8F 007C R          C      mov     cl,byte ptr ds:[bx+serial_t_out] ; get RS-232 time-out
E75F D1 E3                  C      shl     bx,1                             ; make word index
E761 8B 97 0000 R          C      mov     dx,word ptr ds:[bx+rs232_addr]   ; get address of RS-232
E765 1F                      C      pop     ds                               ; data port
                                           C      ; restore ds
                                           C      ;
                                           C      assume cs:code, ds:nothing, es:nothing, as:nothing
E766 0B D2                  C      or      dx,dx                            ; RS-232 port present?
E768 74 10                  C      js      ra_ret                           ; if not, leave
E76A 0A F6                  C      or      dh,dh                            ; are we a IN8250 chip?
E76C 75 03                  C      jnz    ra_ok                             ; if so, take jump
E76E 80 C4 04              C      add     ah,4                             ; if SCC Z8530 add 4 to function
                                           C      ;
E771 ra_ok:                   C      mov     bl,ah                            ; bh = function number
E771 8A DC                  C      mov     bl,ah                            ; bh = 2*(function number)
E773 D1 E3                  C      shl     bx,1                             ; perform rs232 function
E775 2E: EF 97 E77F R      C      call   cs:[bx+(offset ra_tbl)]
                                           C      ;
E77A ra_ret:                   C      pop     bx                               ; restore registers
E77A 5B                      C      pop     cx
E77B 59                      C      pop     dx
E77C 5A                      C      ;
E77D ra_nop:                   C      pop     bp
E77D 5D                      C      iret
E77E CF                      C      ;
                                           C      ;-----
                                           C      ; INT 14h Jump Table
                                           C      ;-----
E77F E87F R                  C      ra_tbl dw  com_init      ; ah = 00h for IN8250
E781 EBEC R                  C      dw  com_pb      ; ah = 01h for IN8250
E783 E924 R                  C      dw  com_gb      ; ah = 02h for IN8250
E785 E87F R                  C      dw  com_stat    ; ah = 03h for IN8250
E787 F573 R                  C      dw  sec_init    ; ah = 00h for SCC Z8530
E789 E91B R                  C      dw  sec_pb      ; ah = 01h for SCC Z8530
E78B E93D R                  C      dw  sec_gb      ; ah = 02h for SCC Z8530
E78D E88A R                  C      dw  sec_stat    ; ah = 03h for SCC Z8530
E78F serial_io                C      endp
                                           C      ;-----
                                           C      ; Initialize RS-232 Interface.
                                           C      ;
                                           C      ; Input:  al = input parameters
                                           C      ;         dx = address of RS-232 channel
                                           C      ; Output: ax = RS-232 channel status
                                           C      ;
                                           C      ; al initializes port with: bit # 7 6 5 4 3 2 1 0
                                           C      ;
                                           C      ; -----+-----
                                           C      ; |B|B|B|P|P|P|S|D|D|
                                           C      ; -----+-----
                                           C      ;
                                           C      ; Baud (BBB):          Parity (PP):          Stop Bits (S):  Data Bits (DD):
                                           C      ; 0 = 110 B = 1200      x0 = None          0 = 1           10 = 7
                                           C      ; 1 = 150 B = 2400      01 = Odd           1 = 2           11 = 8
                                           C      ; 2 = 300 B = 4800      11 = Even          1 = 2           (00 = 5?)
                                           C      ; 3 = 600 B = 9600
                                           C      ;
                                           C      ; Assumes:      com_int_x = com_data_x + 1 = dx + 1
                                           C      ;              com_lctl_x = com_data_x + 3 = dx + 3
                                           C      ;-----
E78F com_init                C      proc  near                            ; ah = 00h
                                           C      assume cs:code, ds:nothing, es:nothing, as:nothing
E78F 52                      C      push  dx                               ; save dx = com_data_x
E790 8A E8                  C      mov     ch,al                           ; save input parameters.
E792 80 80                  C      mov     al,080h                          ; access divisor latch of
                                           C      ; baud count register.
E794 83 C2 03              C      add     dx,3                             ; dx = com_lctl_x
E797 EE                    C      out     dx,al                           ; write to line control register
E798 E8 E8E2 R            C      call   ra_dly
                                           C      ;
E79B 8A D4                  C      mov     bl,ch                            ; get input parameters.
E79D 81 E3 00E0            C      and     bx,11100000b                    ; get bits #5, 6, & 7 (clear bh)
ETA1 81 04                  C      mov     cl,b                             ;
ETA3 D2 EB                  C      shr     bl,cl                            ; move to bits #1,2,& 3
                                           C      ; bx is word index
ETA5 2E: 8B 87 E729 R      C      mov     ax,word ptr cs:[bx+com_baud]     ; get 8250 baud count
E7AA 5A                      C      pop     dx                               ; restore dx = com_data_x
E7AB EE                    C      out     dx,al                           ; output low byte of baud rate
E7AC E8 E8E2 R            C      call   ra_dly
                                           C      ;
ETAf 8A C4                  C      mov     al,ah                            ; transfer high byte to low byte
E7B1 42                      C      inc     dx                               ; dx = com_int_x
E7B2 E2                    C      out     dx,al                           ; output high byte of baud rate
E7B3 E8 E8E2 R            C      call   ra_dly
E7B6 8A C5                  C      mov     al,ch                            ; get input parameters.

```

# ROM BIOS Listing

```

E7B8 24 1F      C      and    al,00011111b      ; get bits #0 thru #4
E7BA 42         C      inc    dx
E7BB 42         C      inc    dx
E7BC EE        C      out   dx,al
E7BD E8 E8E2 R  C      call   ra_dly           ; dx = com_lctl_x
                                ; write to line control register
                                ; disable access divisor latch,
                                ; set data & stop bits, & parity
                                ; disable all interrupts!!

E7C0 32 C0      C      xor    al,al
E7C2 4A         C      dec    dx
E7C3 4A         C      dec    dx
E7C4 EE        C      out   dx,al           ; dx = com_int_x
                                ; write to interrupt ID register

E7C5 4A         C      dec    dx
E7C6 E9 E87F R  C      jmp    com_stat        ; dx = com_data_x
                                ; return status

E7C9           C      com_init    endp

E7C9           C      code    ends
E7C9           C      include kb1.asm

C      ;
C      ;      Filename:      kb1.asm
C      ;
C      ;      This module includes INT 09h & 16h.
C      ;
C      ;
E7C9           C      code    segment public 'ROM'
C      ;      assume cs:code, ds:nothing, es:nothing, ss:nothing
C      ;
C      ;      =====
C      ;      INT 16h -- 18041A Keyboard Software Interrupt Request Routine
C      ;      =====
C      ;
C      ;      Input:  ah    = function number (00h <= ah <= 03h)
C      ;      Output: ah    = (ah - 2) if ah >= 2
C      ;
C      ;      Trash: None. (bx & ds if ROM stack)
C      ;
C      ;      Note:  The stack never gets deeper than 6 words!!!
C      ;
C      ;
C      ;
C      ;      High Address
C      ;      |-----| <-- sp (at entry & exit)
C      ;      | return fsw flags |
C      ;      |-----|
C      ;      | return cs segment |
C      ;      |-----|
C      ;      | return ip offset |
C      ;      |-----| <-- sp after kb trap
C      ;      |   ds   |
C      ;      |-----|
C      ;      |   bx   |
C      ;      |-----|
C      ;      |   1 near call | <-- sp (at its deepest!!!)
C      ;      |-----|
C      ;      Low Address
C      ;
C      ;
C      ;      =====
E82E           C      ORG    0882Eh
E82E           C      k_io   proc    near
C      ;      assume cs:code, ds:nothing, es:nothing, ss:nothing
C      ;
E82E  FB        C      sti     ; enable interrupts!!
E82F  1E        C      push  ds      ; save ds
E830  2E: 8E 1E E5F2 R  C      mov   ds,word ptr es:[set_ds_word] ; avoid potential stack problems
E835  53        C      push  bx      ; save bx
C      ;
C      ;      assume cs:code, ds:data, es:nothing, ss:nothing
C      ;
E836  80 FC 01    C      cmp   ah,1      ; ah <= 1 ?
E839  72 0A      C      jb   k_read    ; jump if ah = 0
E83B  74 23      C      je   k_look   ; jump if ah = 1
E83D  80 FC 02    C      cmp   ah,2      ; ah=2 ?
E840  74 27      C      je   k_stat
C      ;
E842  5B        C      k_ret: pop   bx      ; restore registers
E843  1F        C      pop   ds
E844  CF        C      iret
C      ;
E845           C      k_io   endp
C      ;
C      ;      -----
C      ;      Wait for key and extract if from the keyboard buffer.
C      ;
C      ;      Output: ah = raw scan code
C      ;      al = ASCII translated key
C      ;      or
C      ;      ah = translated key
C      ;      al = 00h
C      ;
C      ;      Trash: Ncne.
C      ;
C      ;      -----
E845           C      k_read proc    near
C      ;      assume cs:code, ds:data, es:nothing, ss:nothing
C      ;
E845  FB        C      sti     ; enable interrupts (again)
E846  E8 E854 R  C      call   k_ee     ; is there a character present?

```

# ROM BIOS Listing

```

E849 74 FA          ; interrupts come back disabled!
C          js      k_read          ; loop until something in buffer
E84B E8 E86E R     oall     k_adv_ptr         ; move pointer to next position
E84E 89 1E 001A R  mov     word ptr ds:[buffer_head],bx ; store value in variable
E852 EB EE          jmp     short k_ret

C
C
C          k_see: cll             ; disable interrupts!!
E854 FA          mov     bx,word ptr ds:[buffer_head] ; get pointer to head of buffer
E855 3B 1E 001C R  cmp     bx,word ptr ds:[buffer_tail] ; if equal, then nothing there
E859 8B 07          mov     ax,word ptr ds:[bx]         ; get scan code and ascii code
E85F C3            ret

E860          k_read endp

C
C
C          ;-----
C          ; Checks for key in keyboard buffer, but does not extract it.
C          ;
C          ; Output: if key is in buffer, then:
C          ;         zf = 0 (nz = reset)
C          ;         ah = raw scan code
C          ;         al = ASCII translated key
C          ;         or
C          ;         ah = translated key
C          ;         al = 00h
C          ;
C          ; else:
C          ;         zf = 1 (z = set)
C          ;         ax = 16th previous key
C          ;
C          ; Trash: ax is trashed if keyboard buffer is empty.
C          ;-----
C
E860          k_look proc far      ; must be far!!!!
C          assume cs:code, ds:data, es:nothing, ss:nothing
C
E860 EB E854 R     oall     k_see          ; is there a character present?
C          ; interrupts come back disabled!
E863 FB          sti             ; must return interrupts enabled!
E864 5B          pop     bx             ; restore registers
E865 1F          pop     ds             ; blow away flags returning:
E866 CA 0002     ret     2             ; zf & ax = k_see output, & sti
C
E869          k_look endp

C
C
C          ;-----
C          ; Returns keyboard shift state kb_flag in al.
C          ;
C          ; Output: ah = 0.
C          ;         al = kb_flag
C          ; Trash: None.
C          ;-----
C
E869          k_stat proc near
C          assume cs:code, ds:data, es:nothing, ss:nothing
C
E869 A0 0017 R     mov     al,byte ptr ds:[kb_flag] ; get the shift status flags
E86C EB D4          jmp     short k_ret
C
E86E          k_stat endp

C
C
C          ;-----
C          ; Advances kb_buffer ring buffer pointer.
C          ;
C          ; Input:  bx
C          ; Output: bx
C          ; Trash:  None.
C          ;-----
C
E86E          k_adv_ptr proc near
C          assume cs:code, ds:data, es:nothing, ss:nothing
C
C          inc     bx             ; move to next word in list
E86E 43          inc     bx
E86F 43          cmp     bx,word ptr ds:[buffer_end] ; end of buffer ?
E870 3B 1E 0082 R  jne     k_adv_end         ; no continue
E874 75 04          mov     bx,word ptr ds:[buffer_start] ; yes, buffer to beginning
E876 8B 1E 0080 R  k_adv_end: ret
E87A          ret
C
E87B          k_adv_ptr endp
C
E87B          code ends

C
C          include com2.asm
C
C          ;-----
C          ; Filename: com2.src
C          ;-----
C
E87B          code segment public 'ROM'
C          assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C          ;-----
C          ; Read Status of RS-232 Interface. (rs_stat)
C          ;
C          ; Input:  dx = if dh = 0, then address of Z8530 channel (cc_ctl_x).
C          ;         if dh <> 0, then address of 8250 data port (com_data_x).
C          ; Output: ax = RS-232 (iNS8250-compatible) channel status.
C          ; Trash: None.

```

# ROM BIOS Listing

```

C ;
C ;           Assumes:      com_lstat_x = com_data_x + 5 = dx + 5 (line status)
C ;                       com_mstat_x = com_data_x + 6 = dx + 6 (modem status)
C ;-----
E87B          ra_stat proc   near           ; ah = 03h
C              assume      cs:code, ds:nothing, es:nothing, as:nothing
C              or          dh,dh           ; are we a SCC 28530 chip?
E87D 0A F6    jz          sec_stat        ; if so, take jump
E87F          com_stat:      ; INS8250 read status routine.
C              ; Get Line Status.
C              push       dx              ; save dx = com_data_x
E87F 52          add       dx,5            ; dx = com_lstat_x
E880 83 C2 05   in        al,dx           ; get line status
E883 EC          mov      ah,al           ; line status comes back in high byte
C              ; Get Modem Status.
C              in        dx              ; dx = com_mstat_x
E886 42          in        al,dx           ; get modem status in low byte
E887 5C          pop      dx              ; restore dx = com_data_x
E888 5A          ret
E889 C3
C
C          sec_stat:      ; SCC 28530 read status routine.
C              ; Get Channel Status.
C              xor       ax,ax            ; al = selects 0 ; ah = no errors
E88A 33 C0      out       dx,al           ; dx = sec_ctl_x
E88C EE          call      ra_dly         ; get channel status
E88D E8 E8E2 R  in        al,dx
E890 EC
C              test      al,sec_txd      ; test for transmit ready
E891 A8 04      jz          sec_no_txd    ; if so, set INS8250-compatible bit.
E893 74 03
C              or        ah,com_txd
E895 80 CC 20   sec_no_txd:
E898
C              test      al,sec_rxd      ; test for receive ready
E898 A8 01      jz          sec_no_rxd    ; if so, set INS8250-compatible bit.
E89A 74 03
C              or        ah,com_rxd
E89C 80 CC 01   sec_no_rxd:
E89F
C              ; Get Error Status.
C              mov      al,i              ; get errors
E89F B0 01      out       dx,al           ; dx = sec_ctl_x
E8A1 EE          call      ra_dly         ; get error status
E8A2 E8 E8E2 R  in        al,dx
E8A5 EC
C              test      al,sec_fe       ; test for framing error
E8A6 A8 80      jz          sec_no_fe     ; if so, set INS8250-compatible bit.
E8A8 74 03
C              or        ah,com_fe
E8AA 80 CC 08   sec_no_fe:
E8AD
C              test      al,sec_pe       ; test for parity error
E8AD A8 10      jz          sec_no_pe     ; if so, set INS8250-compatible bit.
E8AF 74 03
C              or        ah,com_pe
E8B1 80 CC 04   sec_no_pe:
E8B4
C              test      al,sec_oe       ; test for overrun error
E8B4 A8 20      jz          sec_no_oe     ; if so, set INS8250-compatible bit.
E8B6 74 03
C              or        ah,com_oe
E8B8 80 CC 02   sec_no_oe:
E8BB
C              ; Set Modem Status.
C              mov      al,(com_dsr+com_cts) ; al = DSR and CTS
E8BB B0 30      ret
E8BD C3
C
C          ra_stat endp
C ;-----
C ;           Wait for Status of RS-232 Interface. (ra_we)
C ;
C ;           Input:  ah = RS-232 channel status for which to wait
C ;                   cx = RS-232 time-out
C ;                   dx = if dh = 0, then address of 28530 channel (sec_ctl_x).
C ;                       if dh <> 0, then address of 8250 data port to poll.
C ;
C ;           Output: AH = Status.
C ;                   ZF = set, if status matches.
C ;                   reset, if time-out.
C ;
C ;           Trash:  al & bx destroyed.
C ;
C ;           Assumes:      com_lstat_x = com_data_x + 5 = dx + 5 (line status)
C ;                       com_mstat_x = com_data_x + 6 = dx + 6 (modem status)
C ;-----

```

# ROM BIOS Listing

```

EBBE          C ra_ws proc near
              C assume cs:code, ds:nothing, es:nothing, ss:nothing
              C
              C
              C push  ox          ; save time-out
EBBF          C xor    bx,bx       ; clear bx
EBD1          C xchg  cx,bx       ; BL now has ra232_time_out.
              C
EBD3          C ra_ws_lp:
EBD3          C or     dh,dh       ; are we an INSR250 chip?
EBD5          C jnz   ra_ws_com    ; if so, take jump
              C
EBD7          C xor    al,al       ; al = selects 0 on SCC 28530
EBD9          C out   dx,al        ; dx = scc_ctl_x
EBDB          C call  ra_dly
              C
EBDD          C ra_ws_com:
EBDD          C in    al,dx        ; get channel status
EBDE          C mov   bh,al        ; save status in BH.
EBE0          C and   al,ah        ; mask bits we're waiting for
EBE2          C cmp   al,ah        ; are they all on?
              C
EBE4          C jz    ra_ws_exit    ; if so, exit with zf set
              C
EBE6          C loop  ra_ws_lp      ; inner loop
EBE8          C dec   bl           ;
EBEA          C jnz   ra_ws_lp      ; outer loop
              C
EBEC          C or     ah,ah       ; time-out, exit with zf reset
EBED          C ra_ws_exit:
EBED          C mov   ah,bh        ; move status to AH.
EBE9          C pop   cx           ; restore time-out
EBE1          C ret
              C
EBE2          C ra_ws endp
              C
EBE2          C ra_dly proc near
              C assume cs:code, ds:nothing, es:nothing, ss:nothing
              C
              C
              C pushf
EBE3          C push  cx
EBE4          C mov   cx,8
EBE7          C ra_lp: loop ra_lp
EBE9          C pop   cx
EBEA          C popf
EBEB          C ret
              C
EBEC          C ra_dly endp
              C
              C assume cs:code, ds:nothing, es:nothing, ss:nothing
              C
              C
              C -----
              C ;
              C ; INSR250 Put Byte (com_pb) & SCC 28530 Put Byte (scc_pb)
              C ;
              C ; Transmit Character to RS-232 Interface.
              C ;
              C ; Input:  al = character to transmit
              C ;         cx = RS-232 time-out
              C ;         dx = if dh = 0, then address of 28530 channel (scc_ctl_x),
              C ;             if dh <> 0, then address of 8250 data port (com_data_x).
              C ;
              C ; Output: ah = line status
              C ;         bh =
              C ;         Trash: bx destroyed.
              C ;
              C ; Assumes: com_ctl_x = com_data_x + 4 = dx + 4
              C ;          com_lstat_x = com_data_x + 5 = dx + 5
              C ;          com_rstat_x = com_data_x + 6 = dx + 6
              C ;          scc_data_x = scc_ctl_x + 1 = dx + 1
              C ;
              C -----
EBEC          C com_pb proc near
              C assume cs:code, ds:nothing, es:nothing, ss:nothing
              C
              C
              C push  dx          ; save dx = com_data_x
EBED          C push  ax          ; save character to output in al
              C
EBEE          C mov   al,(com_rts+com_dtr) ; signal RTS & DTR
EBF0          C add   dx,4         ; dx = com_actl_x
EBF3          C out   dx,al        ; send to modem control register
              C
EBF4          C mov   ah,(com_dsr+com_cts) ; wait for DSR & CTS
EBF5          C inc   dx
EBF7          C dx = com_rstat_x
EBF8          C call  ra_ws        ; wait for modem status register
EBFB          C jnz   ra_pbe       ; if time-out, take jump
              C
EBFD          C mov   ah,com_txd    ; wait for transmit ready
EBFF          C dec   dx            ; dx = com_lstat_x
E900          C call  ra_ws        ; wait for line status register
E903          C jnz   ra_pbe       ; if time-out, take jump
              C
E905          C pop   ax           ; restore character to output in al
E906          C mov   bl,al        ; save character input/output in bl
E908          C call  ra_stat      ; get return status
E90B          C mov   al,bl        ; restore character input/output in al
E90D          C pop   dx           ; restore dx = com_data_x
E90E          C out   dx,al        ; else, output the character
              C
              C ; exit for put and get byte

```

# ROM BIOS Listing

```

E90F          C ra_pb_gb:                ; if SCC Z8530, dx = sec_ctl_x
E90F C3      C ret
E910          C
E910 5B      C ra_pbe:                ; exit for put byte error
E911 5A      C pop bx                ; restore character to output in bl
E911 5A      C pop dx                ; if SCC Z8530, restore dx = sec_ctl_x
E911 5A      C                ; else INS8250, restore dx = com_data_x
E912 88 E87B R C call ra_stat          ; get return status
E915 8A C3   C mov al,bl            ; restore character to output in al
E917 80 CC 80 C or ah,com_te         ; indicate timeout error
E91A C3     C ret
E91B          C oom_pb endp
E91B          C
E91B sec_pb proc near      ; ah = 01h
E91B          C assume cs:code, ds:nothing, es:nothing, ss:nothing
E91B 52      C push dx              ; save dx = sec_ctl_x
E91C 50      C push ax              ; save character to output in al
E91D BA 04   C mov ah,sec_txd       ; wait for transmit ready
E91F E8 E8BE R C call ra_ws           ; restore character to output in al
E922 75 EC   C jnz ra_pbe           ; if time-out, take jump
E924 58      C pop ax               ; restore character to output in al
E925 82      C inc dx               ; dx = sec_data_x
E926 E8      C out dx,al           ; else, output the character
E927 5A      C pop dx               ; restore dx = sec_ctl_x
E928 EB E5   C jmp short ra_pb_gb
E92A          C oom_pb endp
E92A          C
E92A          C -----
E92A          C ;
E92A          C ; INS8250 Get Byte (com_gb) & SCC Z8530 Get Byte (sec_gb)
E92A          C ;
E92A          C ; Receive Character to RS-232 Interface.
E92A          C ;
E92A          C ; Input:  cx = RS-232 time-out
E92A          C ;          dx = if dh = 0, then address of Z8530 channel (sec_ctl_x).
E92A          C ;             if dh <> 0, then address of 8250 data port (com_data_x).
E92A          C ; Output: al = character received
E92A          C ;          ah = line status
E92A          C ;          Traah: bx destroyed.
E92A          C ;
E92A          C ; Assumes:  com_ctl_x = com_data_x + 4 = dx + 4
E92A          C ;           com_lstat_x = com_data_x + 5 = dx + 5
E92A          C ;           com_mstat_x = com_data_x + 6 = dx + 6
E92A          C ;
E92A          C ;           sec_data_x = sec_ctl_x + 1 = dx + 1
E92A          C ; -----
E92A          C
E92A sec_gb proc near      ; ah = 02h
E92A          C assume cs:code, ds:nothing, es:nothing, ss:nothing
E92A 52      C push dx              ; save dx = com_data_x
E92B 80 01   C mov al,com_dtr       ; signal DTR
E92D 83 C2 04 C add dx,4              ; dx = com_ctl_x
E930 E8      C out dx,al            ; send to modem control register
E931 BA 20   C mov ah,com_dsr       ; wait for DSR
E933 82      C inc dx               ;
E934 82      C inc dx               ;
E935 E8 E8BE R C call ra_ws           ; dx = com_mstat_x
E938 75 0E   C jnz ra_gbe          ; wait for modem status register
E938 75 0E   C                ; if time-out, take jump
E93A BA 01   C mov ah,com_rxd       ; wait for receive ready
E93C 4A      C dec dx               ; dx = com_lstat_x
E93D E8 E8BE R C call ra_ws           ; wait for line status register
E940 75 06   C jnz ra_gbe          ; if time-out, take jump
E942 80 E4 0E C and ah,0Eh           ; Only interested on low nibble.
E945 5A      C pop dx               ; restore dx = com_data_x
E946 EC      C in al,dx             ; else get character
E947 C3     C ret
E948          C
E948 ra_gbe:          C
E948 5A      C pop dx               ; exit for get byte error
E949 80 CC 80 C or ah,com_te         ; if SCC Z8530, restore dx = sec_ctl_x
E94C C3     C ret                ; else INS8250, restore dx = com_data_x
E94D          C oom_gb endp
E94D          C
E94D sec_gb proc near      ; ah = 02h
E94D          C assume cs:code, ds:nothing, es:nothing, ss:nothing
E94D 52      C push dx              ; save dx = sec_ctl_x
E94E BA 01   C mov ah,sec_rxd       ; wait for receive ready
E950 E8 E8BE R C call ra_ws           ; restore character to output in al
E953 75 F3   C jnz ra_gbe          ; if time-out, take jump
E955 42      C inc dx               ; dx = sec_data_x

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# ROM BIOS Listing

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E956 EC          C          in     al,dx          ; else get character
E957 5A          C          pop     dx          ; restore dx = scg_otl_x
E958 EB B5       C          jmp     short ra_pb_gb
E95A             C          scg_gb endp
E95A             C          code ends
E95A             C          include kb2.asm
C
C
C ;=====
C ; Filename: kb2.src
C ; This module includes INT 09h & 16h.
C ;=====
E95A             C          code segment public 'ROM'
E95A             C          assume cs:code, ds:nothing, es:nothing, ss:nothing
E987             C          ORG     0E987h
C
C ;=====
C ; INT 09h -- 18041A Keyboard Hardware Interrupt Service Routine
C ; Note: 'make' -> key is depressed -> 00h + key scan code
C ; 'break' -> key is released -> 80h + key scan code
C ;=====
E987             C          k_int proc near
E987             C          assume cs:code, ds:nothing, es:nothing, ss:nothing
E987             C          sti     ; re-enable interrupts
E988             C          old    ; clear direction flag
E989             C          push  ax
E99A             C          push  bx
E98B             C          push  cx
E98C             C          push  dx
E98D             C          push  si
E98E             C          push  di
E98F             C          push  ds
E990             C          mov     ds,word ptr cs:[set_ds_word] ; avoid potential stack problems
E995             C          push  es
E995             C          assume cs:code, ds:data, es:nothing, ss:nothing
E995             C          ; Get the scan code.
E996             C          in     al,p_kscan ; get scan code from data port
E998             C          mov     ah,al ; save scan code in ah
E998             C          ; Reset the keyboard.
E99A             C          mov     dx,p_kctrl ; get control port address
E99D             C          in     al,dx ; get the status
E99E             C          mov     bl,al ; save the status in bl
E9A0             C          or     al,080h ; set bit #7 -- reset
E9A2             C          out    dx,al ; reset keyboard
E9A3             C          mov     al,bl ; retrieve original status
E9A5             C          out    dx,al ; send it back to keyboard
E9A5             C          ; Retrieve the scan code in both al & ah.
E9A6             C          mov     al,ah ; scan code in both registers
E9A6             C          ; Test for overrun scan code from keyboard = 0FFh.
E9A6             C          ; Note: 20 key scan codes can be buffered up by the keyboard.
E9A8             C          cmp     al,0FFh ; an overrun scan code?
E9AA             C          jnz     k_ok ; if not, continue
E9AC             C          call  k_beep ; beep the speaker
E9AF             C          jmp     k_nop
E9B2             C          k_ok:
E9B2             C          ;-----
E9B2             C          ; ah = scan code (make/break) al = scan code (make/break)
E9B2             C          ; bx = ?
E9B2             C          ; cx = ?
E9B2             C          ; dx = ?
E9B2             C          ; es:di = ?
E9B2             C          ;-----
E9B2             C          and     al,07Fh ; al = scan code make
E9B4             C          les     di,dword ptr ds:[master_tbl_ptr] ; es:di points to master table
E9B8             C          les     di,dword ptr es:[di+0002h] ; es:di points to p_kscan table
E9BC             C          xor     bx,bx ; clear bh
E9BE             C          xor     cx,cx ; clear cl
E9C0             C          mov     oh,byte ptr ds:[kb_flag]
E9C4             C          mov     bl,al ; bx = scan code make
E9C6             C          shl     bx,1 ; bx = 2*(scan code make)
E9C8             C          shl     bx,1 ; bx = 4*(scan code make)

```

# ROM BIOS Listing

```

C
C ;-----
C ; ah = scan code (make/break) al = scan code (make)
C ; bx = 4*(scan code make) = 4*al
C ; oh = kb_flag ol = 0
C ; dx = ?
C ; es:di = p_kscan base
C ;-----
E9CA 4B          dec     bx                ; bx = 4*(scan code make)-1
E9CB F6 C5 08    test    oh,alt_shift     ; alt state?
E9CE 75 32       jnz     k_ix             ; if so, has highest priority
E9D0 4B          dec     bx                ; bx = 4*(scan code make)-2
E9D1 F6 C5 04    test    oh,entri_shift   ; control state?
E9D4 75 2C       jnz     k_ix             ; if so, next highest priority
E9D6 4B          dec     bx                ; bx = 4*(scan code make)-3
C
C ; Handle CapLk Case.
E9D7 3C 37       cmp     al,55             ; 0 <= scan code <= (7*8)-1
E9D9 77 0C       ja      k_no_cap        ; test NumLk case.
E9DB F6 C5 40    test    oh,caps_lock_mode ; caplock state?
E9DE 74 1C       jsz     k_no_lock       ; if not, test shift states
E9E0 E8 EB 85 R  call    k_bit            ; get kb_cap_flags bit in of
E9E3 73 17       jnb     k_no_lock       ; (jnc) swap if of set
E9E5 EB 0D       jmp     short k_lock     ; honor caps lock.
E9E7
C k_no_cap:
C ; Handle NumLk Case.
E9E7 3C 47       cmp     al,71            ; scan code >= 71?
E9E9 72 11       jb      k_no_lock       ;
E9EB 3C 53       cmp     al,83            ; scan code <= 83?
E9ED 77 0D       ja      k_no_lock       ;
E9EF F6 C5 20    test    oh,num_lock_mode ; numlock state?
E9F2 74 08       jsz     k_no_lock       ; if not, test shift states
E9F4
C k_lock:
E9F4 F6 C5 03    test    oh,(left_shift+right_shift) ; either caps or num lock.
E9F7 74 09       jsz     k_ix            ; if so, and shift state
C ; also true
E9F9 4B          dec     bx                ; bx = 4*(scan code make)-4
E9FA EB 06       jmp     short k_ix      ; (base case)
E9FC
C k_no_lock:
E9FC F6 C5 03    test    oh,(left_shift+right_shift) ; (shift state)
E9FF 75 01       jnz     k_ix            ;
E9A0 4B          dec     bx                ; bx = 4*(scan code make)-4
C ; (base case) fall through
E9A2
C k_ix:
E9A2 D1 E3       shl     bx,1             ; bx = index into p_kscan table
E9A4 03 FB       add     di,bx           ; bx = p_kscan word index
C ; add p_kscan base & index
E9A6 26: 8B 15    mov     dx,word ptr es:[di] ; get data word from table
E9A9 33 DB       xor     bx,bx           ; clear bh
E9AB 8A DA       mov     bl,dl           ; move translated key to bx
E9AD F6 06 0018 R 01 test    byte ptr ds:[kb_flag_1],dl,x_kb ; are we a deluxe keyboard
E9A2 74 02       jsz     k_xlat          ; key
E9A4 8A DE       mov     bl,dh           ; move translated delux
E9A6
C k_xlat:
C ; key to key
C ; bx has translated byte (bh=0)
C ;-----
C ; ah = scan code (make/break) al = scan code (make)
C ; bx = deluxe keyboard translated byte (bh = 0)
C ; oh = kb_flag ol = 0
C ; dx = es:[di] (could be delux key code)
C ; es:di = p_kscan base + p_kscan scan code word index
C ;-----
C ; Registers are all loaded up. Start going through the cases.
E9A6 0A D2       or      di,dl           ; delux scan codes are
E9A8 74 1C       jsz     k_no_case       ; NEVER special cases!!!!
C
C ; Test for special cases.
E9A8 80 FB C0    cmp     bl,0C0h         ; xlated byte special case?
E9AD 72 17       jb      k_no_case       ; if not, handle unspecial case
E9AF 80 FB D8    cmp     bl,0D8h         ; 0C0h <= xlated byte <= 0D8h
E9A2 77 12       ja      k_no_case       ; if so, do the special function
C
C ; Test for 'break' of special case.
E9A4 80 FB C8    cmp     bl,0C8h         ; is xlated byte a shift key?
E9A7 72 04       jb      k_jmp           ; if so, do 'break' of shift key
E9A9 0A E4       or      ah,ah          ; 0C0h <= xlated byte < 0C8h

```

# ROM BIOS Listing

```

EA2B 78 2E          C          js      k_none          ; nothing for 'break' of others.
EA2D              C          k JMP:          ; jump to special case routine.
EA2D 8B F3          C          mov     si, bx          ; if so, si gets special index
EA2E D1 E6          C          shl     si, 1          ; make it a word index
EA31 2E: FF A4 EA66 R C          jmp     cs:[si+((offset k_case)-(2*0C0h))]
EA36              C          k_no_case:
EA36              C          ; Test for 'break' of non special case.
EA36 0A E4          C          or      ah, ah
EA38 78 21          C          js      k_none          ; do nothing if 'break' of key.
EA38              C          ; Test for 'unpause' case.
EA3A 76 06 0018 R 08 C          test   byte ptr ds:[kb_flag_1], pause_mode ; are we in hold state?
EA3F 74 0B          C          jz      k_no_hold       ; if not, continue.
EA41 3C 45          C          cmp     al, num_lock_key ; don't clear hold state
EA43 74 16          C          je      k_none          ; on num_lock_key (Pause).
EA45 80 26 0018 R F7 C          and    byte ptr ds:[kb_flag_1], not pause_mode ; reset hold state bit &
EA4A EB 0F          C          jmp     short k_none     ; ignore the key.
EA4C              C          k_no_hold:
EA4C              C          ; Test for deluxe scan code.
EA4C 0A D2          C          or      dl, dl
EA4E 75 04          C          jnz     k_no_xcode
EA50 8B C2          C          mov     ax, dx          ; move deluxe key to scan code
EA52 EB 02          C          jmp     short k_buf     ; put ax into the buffer
EA54              C          k_no_xcode:
EA54 8A C3          C          mov     al, bl          ; move translated key to key
EA56              C          k_buf:
EA56              C          ; put ax into kb_buffer.
EA56 EB EBAD R      C          call   k_try           ; try to put ax into kb_buffer.
EA59 74 03          C          jz      k_nop          ; if set (z) if buffer is full
EA5B              C          k_none:
EA5B              C          ; scan code translate to nothing
EA5B              C          ; Send specific end of interrupt (SEOI) to pic 'command' port.
EA5B EB EBA4 R      C          call   k_eoi          ; send specific end of interrupt
EA5E 07          C          k_nop: pop     es          ; restore registers without issuing SEOI
EA5F 1F          C          pop     ds
EA60 5F          C          pop     di
EA61 5E          C          pop     si
EA62 5A          C          pop     dx
EA63 59          C          pop     ox
EA64 5B          C          pop     bx
EA65 58          C          pop     ax
EA66 0F          C          iret
EA67 80 E5 0C      C          k_res: and    oh, (alt_shift+ontrl_shift)
EA6A 80 FD 0C      C          and    oh, (alt_shift+ontrl_shift) ; is it CTL ALT shift?
EA6D 75 EC          C          jne     k_none
EA6F 80 E5 0C      C          ; CTL ALT DEL system reset.
EA6F C7 06 0072 R 1234 C          mov     word ptr ds:[reset_flag], 01234h ; set flag for warm boot
EA75 89 DD5A R      C          jmp     diagnostics_1 ; re-boot
EA78              C          ; Pause waiting for another key. 'make' only.
EA78 80 0E 0018 R 08 C          k_pause: or      byte ptr ds:[kb_flag_1], pause_mode ; set the pause bit.
EA7D EB EBA4 R      C          call   k_eoi          ; send specific end of interrupt
EA80 80 3E 0049 R 07 C          ; Note: Video not disabled during vertical retrace.
EA85 74 0B          C          cmp     byte ptr ds:[v_mode], 7 ; never on a monochrome card
EA87 8B 16 0063 R   C          je      k_hold
EA88 83 C2 04      C          mov     dx, word ptr ds:[v_base6845] ; get 6845 pointer register
EA8E A0 0D65 R     C          add     dx, 4          ; get 6845 mode control register
EA91 EE          C          mov     al, byte ptr ds:[v_3x8] ; get the video mode last sent
EA92 F6 06 0018 R 08 C          out    dx, al          ; enable video
EA97 75 F9          C          k_hold: test   byte ptr ds:[kb_flag_1], pause_mode ; test the pause bit.
EA99 EB C3          C          jnz     k_hold         ; loop until pause bit cleared
EA99 jmp     short k_nop
EA9B EB EBA4 R      C          ; Print Screen sequence. 'make' only.
EA9E CD 05          C          k_prt: call   k_eoi          ; send specific end of interrupt
EAA0 EB BC          C          INT    5h            ; issue print screen interrupt
EAA0 jmp     short k_nop

```

# ROM BIOS Listing

```

C
C
C ;-----
C ; Deluxe code put NUL into kb_buffer. 'make' only.
C ;-----
EAA2 BB 0300 k_nul: mov ax,0300h ; NUL=x03
EAA5 EB AF jmp short k_buf ; put ax into the buffer
C
C ;-----
C ; Four state shifts. 'make' & 'break' in kb_flag_1 plus history in kb_flag.
C ;-----
EAAT B0 80 k_ins: mov al,insert_shift ; INS toggle look
EAA9 E8 EAD4 R call k_2tog ; toggle 4 state
C
C or ah,ah ; is INS toggle 'make' ?
EAAE 78 AB js k_none ; if not, exit
EAB0 EB 5200 mov ax,(insert_key*100h)+00h ; else, ax gets deluxe INS key
EAB3 EB A1 jmp k_buf ; put ax into the buffer
C
C
EAB5 B0 40 k_cap: mov al,caps_lock_shift ; CAPS LOCK toggle look
EAB7 E8 EAD4 R call k_2tog ; toggle 4 state
EABA B1 01 mov mov 01,00000001b ; CAPS LOCK LED is bit #0.
EABC E8 EB63 R call k_LED_asy ; send LED information
EABF EB 9A k_non1: jmp short k_none
C
C
EAC1 B0 20 k_num: mov al,num_lock_shift ; NUM LOCK toggle look
EAC3 E8 EAD4 R call k_2tog ; toggle 4 state
EAC6 B1 02 mov mov 01,00000010b ; NUM LOCK LED is bit #1.
EAC8 E8 EB59 R call k_LED_num ; send LED information
EACB EB F2 jmp short k_non1
C
C
EACD B0 10 k_scr: mov al,scr1_lock_shift ; SCROLL LOCK toggle look
EACF E8 EAD4 R call k_2tog ; toggle 4 state
EAD2 EB EB jmp short k_non1
C
C
EAD4 0A E4 k_2tog: or ah,ah ; is toggle shift 'make' ?
EAD6 78 0F js k_2res ; if 'break' reset kb_flag_1
C
C
EAD8 84 06 0018 R test byte ptr ds:[kb_flag_1],al ; if 'make', test bit.
EADC 75 08 jnz k_2ret ; return if already pressed
C
C
EAD E 08 06 0018 R or byte ptr ds:[kb_flag_1],al ; set the bit.
EA22 30 06 0017 R xor byte ptr ds:[kb_flag],al ; toggle kb_flag history.
EA26 C3 k_2ret: ret
C
C
EA27 F6 D0 k_2res: not al
EA29 20 06 0018 R and byte ptr ds:[kb_flag_1],al ; if 'break', reset bit only.
EA2D C3 ret
C
C
C ;-----
C ; Two state shifts. 'make' & 'break' in kb_flag only.
C ;-----
EAE E B0 08 k_alt: mov al,alt_shift ; ALT set/reset kb_flag
EAF0 E8 EBF0 R call k_2tog ; toggle 2 state
C
C
EAF3 33 C0 xor ax,ax ; scan code of ah = 0.
EAF5 86 06 0019 R shlb al,byte ptr ds:[alt_input] ; alt_input gets 0.
EAF9 0A C0 or al,al ; was alt_input 0?
EAFB 74 C2 je k_non1 ; if so, do nothing.
EAFD E9 EA56 R jmp k_buf ; else, put it into buffer.
C
C
EB00 B0 04 k_ctl: mov al,ctrl_shift ; CTL set/reset kb_flag
EB02 EB 06 jmp short k_2ret ; toggle 2 state and return
C
C
EB04 B0 02 k_lsh: mov al,left_shift ; LEFT SHIFT set/reset kb_flag
EB06 EB 02 jmp short k_2ret ; toggle 2 state and return
C
C
EB08 B0 01 k_rsh: mov al,right_shift ; RIGHT SHIFT set/reset kb_flag
; jmp short k_2ret ; fall through
C
C
EB0A k_2ret: call k_2tog ; toggle 2 state
EB0A E8 EBF0 R call k_2tog
EB0D EB B0 jmp short k_non1
C
C
EB0F 0A E4 k_2tog: or ah,ah ; is set/reset shift 'make' ?
EB11 78 05 js k_2res ; if 'break', reset bit only.
C
C
EB13 08 06 0017 R or byte ptr ds:[kb_flag],al ; if 'make', set bit only.
EB17 C3 ret
C
C
EB18 F6 D0 k_2res: not al
EB1A 20 06 0017 R and byte ptr ds:[kb_flag],al ; if 'break', reset only.
EB1E C3 ret
C
C
C ;-----
C ; Alternate Numeric Keypad. 'make' only.
C ;-----
EB1F 41 k_alt9: inc cx ; Alternate Numeric Keypad #9
EB20 41 k_alt8: inc cx ; Alternate Numeric Keypad #8

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# ROM BIOS Listing

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EB21  A1          C   k_alt7: inc     ex           ; Alternate Numeric Keypad #7
EB22  A1          C   k_alt6: inc     ex           ; Alternate Numeric Keypad #6
EB23  A1          C   k_alt5: inc     ex           ; Alternate Numeric Keypad #5
EB24  A1          C   k_alt4: inc     ex           ; Alternate Numeric Keypad #4
EB25  A1          C   k_alt3: inc     ex           ; Alternate Numeric Keypad #3
EB26  A1          C   k_alt2: inc     ex           ; Alternate Numeric Keypad #2
EB27  A1          C   k_alt1: inc     ex           ; Alternate Numeric Keypad #1
EB28  A1          C   k_alt0: inc     ex           ; Alternate Numeric Keypad #0
EB28  B0 0A      C
EB2A  P6 26 0019 R  C   mov     al,10
EB2E  02 C1      C   mul     byte ptr ds:[alt_input] ; alt_input = (10*alt_input)+cl
EB30  A2 0019 R  C   add     byte ptr ds:[alt_input],al
EB33  EB 8A      C   jmp     short k_nop1
C
C   -----
C   ; Double Zero on Keypad. 'make' only.
C   -----
EB35  B0 30      C   k_00:  mov     al,'0'           ; try to put ax into kb_buffer.
EB37  EB EBAD R  C   call    k_try                 ; zf set (z) if buffer is full
EB3A  74 03      C   js     k_nop1                 ; zf reset (nz) if buffer got ax
EB3C  E9 EA56 R  C   jmp     k_buf                 ; put it into buffer, again.
EB3F  E9 EA5E R  C   k_nop1: jmp    k_nop
C
C   -----
C   ; Break key sequence. 'make' only.
C   -----
EB42  BB 001E R  C   k_brk: mov     bx,ds:[offset kb_buffer] ; reset buffer to empty
EB45  89 1E 001A R  C   mov     word ptr ds:[buffer_head],bx
EB49  89 1E 001C R  C   mov     word ptr ds:[buffer_tail],bx
EB4D  C6 06 0071 R 80 C   mov     byte ptr ds:[bios_break],80h ; turn on bios_break bit
EB52  CD 1B      C   INT     1Bh                  ; break interrupt vector
EB54  33 C0      C   xor     ax,ax                 ; ax gets deluxe 00h
EB56  E9 EA56 R  C   jmp     k_buf                 ; put ax into the buffer
EB59  E9 EA5E R  C   k_int  endp
C
C   -----
C   ; Puts keyboard LED's in correct state after CAPS/NUM LOCK.
C   ;
C   ; Input:  ah = scan code (make or break)
C   ;         al = kb_flag bit for CAPS/NUM LOCK (caps_lock_shift or num_lock_shift)
C   ;         cl = 00000010b for CAPS LOCK LED or 00000100b for NUM LOCK LED.
C   ;
C   ; Output: None.
C   ;
C   ; Trash:  al & cl destroyed.
C   -----
EB59  E9 EA5E R  C   k_LED_num  proc  near
C   assume  cs:code, ds:data, es:nothing, ss:nothing
EB59  P6 06 0018 R 01 C   test    byte ptr ds:[kb_flag_1],dlx_kb ; are we a deluxe keyboard
EB5E  74 03      C   js     k_LED_cap             ; if kb_LED is num_lock
EB60  80 F1 80    C   xor     cl,10000000b         ; if deluxe kb, LED is
C   ; "num_lock
C
C   k_LED_cap:
EB63  0A E4      C   or     ah,ah                 ; is CAPS/NUM LOCK 'make' ?
EB65  78 1D      C   js     k_LED_ret             ; if not, exit
EB67  84 06 0017 R  C   test    byte ptr ds:[kb_flag],al   ; is CAPS/NUM LOCK kb_flag set ?
EB68  74 03      C   js     k_LED_end             ; if not, LED data is ok.
EB6D  80 F1 80    C   xor     cl,10000000b         ; else, flip sense of LED data.
C
C   k_LED_end:
EB70  E4 64      C   in     al,kb_status          ; polling loop to send command.
EB72  A8 02      C   test   al,00000010b         ; get 8041 status
EB74  75 FA      C   jnz    k_LED_end            ; test input buffer bit
C   ; if not ok to write cmd, loop.
C
EB76  80 13      C   mov     al,013h              ; keyboard 'LED' command.
EB78  E6 60      C   out    P_kscan,al           ; send keyboard 'LED' command.
C
C   k_LED_dat:
EB7A  E4 64      C   in     al,kb_status          ; polling loop to send data.
EB7C  A8 02      C   test   al,00000010b         ; get 8041 status
EB7E  75 FA      C   jnz    k_LED_dat            ; test input buffer bit
C   ; if not ok to write data, loop.
C
EB80  8A C1      C   mov     al,cl                ; retrieve keyboard 'LED' data.
EB82  E6 60      C   out    P_kscan,al           ; send keyboard 'LED' data.
EB84  C3          C   k_LED_ret: ret
EB85  E9 EA5E R  C   k_LED_num  endp
C
C   -----
C   ; Get kb_cap_flags bit into the carry flag (cf).
C   ;
C   ; Input:  al = scan code (make)
C   ;         cl = 0
C   ;         es:di = p_kscan base
C   ; Output: cf set if kb_cap_flags bit
C   ;
C   ; Trash:  si destroyed.
C   -----
EB85  E9 EA5E R  C   k_bit  proc  near
C   assume  cs:code, ds:data, es:nothing, ss:nothing

```

# ROM BIOS Listing

```

EB85 8B F3          C          mov     si,bx                ; save bx
EB87 33 DB          C          xor     bx,bx                ; clear bh
EB89 8A D8          C          mov     bl,al                ; bx = scan code (make) index
                               C          ; bx = 00000000 00xxxxyy
EB8B B1 03          C          mov     cl,3                ; rotate right bx 3
EB8D D3 CB          C          ror     bx,cl                ; bx = yyyy0000 00000xxx
EB8F B1 03          C          mov     cl,3                ; rotate left bh 3
EB91 D2 C7          C          rol     bh,cl                ; bh = remainder = (0-7)
                               C          ; bl = quotient = (0-6)
EB93 8A CF          C          mov     cl,bh                ; cl = remainder = (0-7)
EB95 32 FF          C          xor     bh,bh                ; bx = quotient = (0-6)
EB97 26: 8A 59 F9   C          mov     bl,byte ptr es:[di-bx-7] ; bl = proper cap_flags byte
EB9B D2 D3          C          rcl     bl,cl                ; rotate (0-7) times into bit #7
EB9D 32 C9          C          xor     cl,cl                ; cl = 0
EB9F D0 D3          C          ror     bl,1                ; rotate into of bit #7
EBA1 8B DE          C          mov     bx,si                ; restore bx
EBA3 C3             C          ret
EBA4              C          k_bit  endp
                               C          ;-----
                               C          ; Input: None.
                               C          ; Output: None.
                               C          ; Trash: al & dx destroyed.
                               C          ;-----
EBA4              C          k_eoi  proc  near
                               C          ; Send specific end of interrupt (SEOI) to pic 'cosmand' port.
EBA4 FA           C          cli                          ; disable interrupts
EBA5 B0 61          C          mov     al,pic_seoi_1        ; specific end of interrupt
EBA7 BA 0020        C          mov     dx,pio_0            ; cosmand to pic 'cosmand' port.
EBA8 EE           C          out     dx,al
EBA9 FB           C          sti                          ; enable interrupts
EBAE C3             C          ret
EBAD              C          k_eoi  endp
                               C          ;-----
                               C          ; Try to put ax into the kb_buffer.
                               C          ; Input: ax = word to put in kb_buffer.
                               C          ; Output: zf set (z) if buffer is full. (ax trashed)
                               C          ;        zf reset (nz) if buffer got ax. (ax saved)
                               C          ; Trash: bx, cx, dx, & si destroyed (in general).
                               C          ;-----
EBAD              C          k_try  proc  near
                               C          assume cs:code, ds:data, es:nothing, ss:nothing
EBAD 8B 1E 001C R   C          mov     bx,word ptr ds:[buffer_tail] ; get buffer end pointer
EBB1 8B F3          C          mov     si,bx                ; save the value
EBB3 E8 E86E R     C          call    k_adv_ptr            ; advance the tail
EBB6 3B 1E 001A R   C          cmp     bx,word ptr ds:[buffer_head] ; has the buffer wrapped around
EBBA 74 07          C          je     k_bEEP                ; if is reset (nz)
EBBC 89 0A          C          mov     word ptr ds:[si],ax    ; store the value
EBBE 89 1E 001C R   C          mov     word ptr ds:[buffer_tail],bx ; move the pointer up
EBC2 C3             C          ret                          ; return zf reset (nz)
EBC3              C          k_try  endp
                               C          ;-----
                               C          ; Input: None.
                               C          ; Output: zf set (z) always.
                               C          ; Trash: ax, bl, cx, & dx destroyed.
                               C          ;-----
EBC3              C          k_bEEP proc  near
                               C          assume cs:code, ds:data, es:nothing, ss:nothing
EBC3 E8 EBA4 R     C          call    k_eoi                ; send specific end of interrupt
EBC6 BA 0061        C          mov     dx,p_kotrl          ; get kb control port address
EBC9 EC             C          in     al,dx                ; get control data
EBCA 8A E0          C          mov     ah,al                ; save control data
EBCD B3 80          C          mov     bl,80h              ; outer loop counter
EBCF 24 FC          C          k_lp: and     al,0FCh        ; turn off speaker data
EBD0 EE           C          out     dx,al
EBD1 B9 0048        C          mov     cx,48h              ; set up count
EBD4 E2 FE          C          loop   $                    ; delay awhile
                               C

```

# ROM BIOS Listing

```

EBD6 0C 02      C      or      al,02h          ; turn on speaker
EBD8 EE        C      out     dx,al
EBD9 B9 0048    C      mov     cx,48h          ; set up count
EBDC E2 FE      C      loop   $              ; delay awhile
EBDE FE CB      C      dec     bl              ; decrement outer loop counter
EBE0 75 EC      C      jnz     k_lp           ;
EBE2 8A C4      C      mov     al,ah           ; zf is set (z)
EBE4 EE        C      out     dx,al          ; restore control data
EBE5 C3        C      ret                    ; return zf set (z)

EBE6           C      k_beep      endp
EBE5           C      k_data1    proc
EBE5           C      k_oase     dw     k_ins      ; kbina (0C0h)
EBE8 EAB5 R     C      dw     k_cap      ; kboap
EBEA EAC1 R     C      dw     k_num      ; kbnum
EBEC EACD R     C      dw     k_sprt     ; kbsor
EBEE EABE R     C      dw     k_alt      ; kballt 'make' & 'break'
EBF0 EB00 R     C      dw     k_ctl      ; kbotl
EBF2 EB04 R     C      dw     k_lsh      ; kblsh
EBF4 EB08 R     C      dw     k_rsh      ; kbrsh
EBF6 EA67 R     C      dw     k_res      ; kbrea (0C8h)
EBF8 EB42 R     C      dw     k_brk      ; kbrbk
EBFA EA78 R     C      dw     k_pause     ; kbpst
EBFC EA9B R     C      dw     k_sul      ; kbnul
EBFE EA42 R     C      dw     k_none     ; NONE
EC00 EA5B R     C      dw     k_alt9     ; kdeo9
EC02 EB17 R     C      dw     k_alt8     ; kdeo8
EC04 EB20 R     C      dw     k_alt7     ; kdeo7 'make' only
EC08 EB22 R     C      dw     k_alt6     ; kdeo6
EC0A EB23 R     C      dw     k_alt5     ; kdeo5
EC0C EB24 R     C      dw     k_alt4     ; kdeo4
EC0E EB25 R     C      dw     k_alt3     ; kdeo3
EC10 EB26 R     C      dw     k_alt2     ; kdeo2
EC12 EB27 R     C      dw     k_alt1     ; kdeo1
EC14 EB28 R     C      dw     k_alt0     ; kdeo0
EC16 EB35 R     C      dw     k_00      ; kbl0 (0D8h)
EC18           C      k_data1    endp
EC18           C      oode     ends
EC18           C      include  fdul.asm
EC18           C      oode     segment public 'ROM'
EC18           C      assume  cs:code, ds:data, es:nothing, ss:nothing
EC18           C      f_neo_reset proc near
EC18 BA 03F4 90 C      mov     dx,f_neo_status ; NEC status port
EC1C EC        C      in     al,dx
EC1D 3C 10      C      cmp     al,10h         ; NEC busy.
EC1F 75 0E      C      jne     f_neo_reset_ret ; no.
EC21 A0 0041 R  C      mov     al,diskette_status ; save from previous operation.
EC24 50        C      push  ax
EC25 33 C0      C      xor     ax,ax
EC27 8B D0      C      mov     dx,ax
EC29 CD 13      C      int 13h
EC2B 58        C      pop   ax
EC2C A2 0041 R  C      mov     dx,diskette_status,al ; restore from previous op.
EC2F           C      f_neo_reset_ret:
EC2F C3        C      ret
EC30           C      f_neo_reset endp
EC30           C      oode     ends
EC30           C      include  fdul.asm
EC30           C      EQUATES
EC30           C      Controller constants
= 000C          equ 1100h ; 48TPI Step Rate Time (6 ms @ 4 Mhz)
= 000E          equ 1110h ; 96TPI Step Rate Time (4 ms @ 4 Mhz)
= 000F          equ 1111b ; Head Unload Time (480 ms @ 4 Mhz)
= 0001          equ 1 ; Head Load Time (4 ms @ 4 Mhz)
= 0000          equ 0 ; Not DMA bit (0 = dma on)
= 0025          equ 37 ; no. of RTC ticks before turning
                  ; motor off. (f_motor_wait x 55ms)
=              equ [bp-0] ; byte pointer.
=              equ [bp-1] ; byte pointer.
=              equ [bp-2] ; byte pointer.
=              equ [bp-3] ; byte pointer.
=              equ [bp-4] ; word pointer.
=              equ [bp-6] ; byte pointer.
=              equ [bp-7] ; byte pointer.
=              equ [bp-8] ; byte pointer.

```

# ROM BIOS Listing

```

C ; Floppy Disk port addresses
C
= 03F2 C f_motor_port equ 03F2h ; drive select port
= 03F4 C f_nec_status equ 03F4h ; disk controller status port
= 03F5 C f_nec_data equ 03F5h ; disk controller data port
C
C ; Floppy Disk commands
C
= 00E6 C f_read_cmd equ 0E6h ; read data
= 00C5 C f_write_cmd equ 0C5h ; write data
= 004D C f_format_cmd equ 04Dh ; format
= 0007 C f_recal_cmd equ 007h ; recalibrate
= 0008 C f_senseint_cmd equ 008h ; sense interrupt
= 0004 C f_sensdrv_cmd equ 004h ; sense drive
= 0003 C f_specify_cmd equ 003h ; specify
= 000F C f_seek_cmd equ 00Fh ; seek
C
C ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C
EC30 C code segment public 'ROM'
C assume cs:code, ds:data, es:nothing, ss:nothing
C
C ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C
EC59 C ORG 0EC59h
EC59 C fd_io proc far
C
EC59 FB C sti ; enable interrupts
EC5A 55 C push bp
EC5B 1E C push ds
EC5C 56 C push si
EC5D 57 C push di
EC5E 52 C push dx ; head & drive#
EC5F 51 C push cx ; cyl. & sec#
EC60 53 C push bx ; buffer offset
EC61 50 C push ax ; command & #secs
EC62 52 C push dx ; this one gets modified(96 TPI)
EC63 8B EC C mov bp,sp ; BP preserves SP throughout
C
C ; test command code & use jump table to jump to appropriate routine
C
EC65 2E: 8E 1E E5F2 R C mov ds,word ptr cs:[set_ds_word] ; DS = data_seg (40h)
EC6A 80 26 003F R 0F C and motor_status,0Fh ; preserve motor on bits.
EC6F 80 FA 01 C cmp dl,1 ; max. drives
EC72 77 05 C jnz ja f_io1 ; drive out of range.
EC74 80 FC 05 C cmp ah,5 ; max. command.
EC77 76 07 C jbe diskette_io1 ; command in range
C
EC79 C f_io1:
EC79 C6 06 0041 R 01 C mov diskette_status,cmd_error ; 01h
EC7E EB 1B C jmp short f_io_ret ; quick return
C
EC80 C diskette_io1:
EC80 FC C old
EC81 EB EFAD R C call f_check_valid ; Autoincrement for strings.
EC84 32 FF C xor bh,bh ; Will not return if error.
EC86 8A DC C mov bl,ah ; clear high byte
EC88 D1 E3 C shl bx,1 ; move selection into low byte
EC8A 2E: FF A7 EC6F R C jmp cs:[f_table.bx] ; multiply by 2
C
C ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C
EC8F C f_table label word
C
EC8F ECBF R C dw f_reset ; AH = 0 (reset)
EC91 EC9B R C dw f_io_ret ; AH = 1 (status)
EC93 ED65 R C dw f_r_data ; AH = 2 (read)
EC95 ED39 R C dw f_w_data ; AH = 3 (write)
EC97 ED65 R C dw f_r_data ; AH = 4 (verify)
EC99 ED39 R C dw f_w_data ; AH = 5 (format)
C
C ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C
EC9B C f_io_ret:
EC9B EB EC18 R C ; f_nec_reset is located in the module called special.arc.
EC9E EB 0002 C call f_nec_reset ; reset if necessary.
ECA1 EB E8FF R C mov bx,2 ; motor_wait parameter.
ECA4 A2 0040 R C call f_get_var ; Returns 0 in AH.
C mov motor_count,al ; motor shut off value.
C
ECAT 32 C0 C xor al,al ; zero AL.
ECA9 8A 26 0041 R C mov ah,diskette_status
C
ECAD 80 FC 01 C omp ah,1
ECB0 F5 C oac
C
ECB1 8B E5 C mov sp,bp ; for safety sake.
ECB3 5B C pop bx
ECB4 5B C pop bx ; discard DI.
ECB5 5B C pop bx ; discard AX.
ECB6 59 C pop cx
ECB7 5A C pop dx
ECB8 5F C pop di
ECB9 5E C pop si
ECBA 1F C pop ds
ECBB 5D C pop bp
C
ECBC CA 0002 C ret 2
C
ECBF C fd_io endp

```





# ROM BIOS Listing

```

ED39      C      f_motor_on      endp
C
C
C      f_wdata proc      near
C
ED39      E8 ED14 R      call      f_motor_on      ; sets carry if motor was off.
ED3C      73 1E          jnc       f_vdi          ; motor was on, skip delay.
C
ED3E      EA 67          in        al,sys_conf_b  ; read switch.
ED40      F6 D0          not       al              ; toggle the sense.
ED42      24 02          and       al,2           ; isolate slow motor bit.
ED44      8A C8          mov      al,al          ;
ED46      BA 007D        mov      dx,125         ; 125 ms delay to start with.
ED48      D3 E2          shl      dx,cl          ; 125 x 4
ED4B      BB 000A        mov      bx,10          ; motor start delay parameter.
ED4E      E8 EDFF R      call     f_get_var       ; returns param. in AL.
ED51      32 84          xor      ah,ah          ; for good measure.
ED53      F7 E2          mul      dx              ; AX has total delay
ED55      8B C8          mov      cx,ax
C
C      f_wd_loop:
ED57      E8 EF47 R      call     f_wait_one_ms   ;
ED5A      E2 FB          loop    f_wd_loop
C
C      f_vdi:
ED5C      80 0E 003F R 80 or        motor_status,080h ; set high bit, indicate write.
ED61      80 4A          mov      al,08Ah        ; DMA mode byte: channel 2,
C
C      ED63      EB 22          jnp      short f_rw_common ; single mode, read transfer
ED65      C
C      f_wdata endp
C
C
C      f_rdata proc      near
C
ED65      C
C      ED65      80 26 003F R 7F      and       motor_status,07Fh ; clear high bit, indicate read
ED6A      E8 ED14 R      call     f_motor_on      ;
ED6D      73 0K          jnc       f_rdi          ; motor was on, no delay.
C
C      ; slow motor delay loop
C
ED6F      EA 67          in        al,sys_conf_b  ; read configuration switch(7W)
ED71      18 02          test     al,2           ; bit 1 = slow drive bit
ED73      75 08          jnz      f_rdi          ; 1 = 250 ms motors, no delay
ED75      B9 01F4        mov      cx,500         ; approx. 500 ms delay for
C
C      ; slow motors
C
C      f_rdi_loop:
ED78      E8 EF47 R      call     f_wait_one_ms   ;
ED7B      E2 FB          loop    f_rdi_loop
C
C      f_rdi:
ED7D      80 46          mov      al,046h        ; DMA mode byte: channel 2,
ED7D      C
C      ED7D      80 78 03 04        cmp      byte ptr f_command,4 ; Is it a verify command?
ED83      75 02          jne      f_rw_common    ; No, must have been a read.
ED85      80 42          mov      al,042h        ; DMA mode byte: channel 2,
C
C      ; single mode, verify transfer.
C
C      f_rdata endp
C
C
C      ;
C      ;
C      ; Common (f_rw_common)
C      ;
C      ; INPUT:      AL      dma mode byte.
C      ;
C      ; OUTPUT:
C      ;
C      ; DESTROYS:
C      ;
C
C
C      f_rw_common      proc      near
C
ED87      C
C      ED87      C6 06 0040 R FF      mov      motor_count,0FFh ; long wait.
ED8C      E8 E873 R      call     f_set_dma       ; pass mode byte on through.
C
C      ; Clear out status from previous operation.
C
ED8F      06          push    es
ED90      1E          push    ds
ED91      07          pop     es
ED92      32 C0       xor     al,al
ED94      B9 0007        mov     cx,7
ED97      BF 0042 R      mov     di,offset nec_status
ED9A      F3 / AA       rep    stosb
ED9C      07          pop     es
C
ED9D      E8 E8CD R      call     f_seek          ; On return, f_drive has
C
C      ; head bit or'd in.
C
EDA0      8A 56 03       mov     di,byte ptr f_command ; get command
EDA3      84 C5          mov     ah,f_write_cmd
EDA5      80 FA 03       cmp     di,3             ; Is it a write command?
EDA8      74 09          jbe     f_rw1           ; yes
EDA9      84 4D          mov     ah,f_format_cmd
EDAC      80 FA 05       cmp     di,5             ; Is it a format command?

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# ROM BIOS Listing

```

EDAF 74 02          C          je      f_rw1          ; yes
EDB1 B4 E6          C          mov     ab,f_read_omd      ; must be read or verify.
EDB3               C          f_rw1:
EDB3 E8 E8C R       C          call   f_put_byte         ; send command.
EDB6 8A E6 00       C          mov     ab,f_drive        ; has head and drive bits.
EDB9 E8 E8C R       C          call   f_put_byte         ;
EDBC 80 7E 03 05   C          cmp     byte ptr f_command,5 ; was it a format command?
EDC0 74 15          C          je      f_rw_skip        ; yes, skip next 3 params.
EDC2 8A E6 07       C          mov     ab,f_yl1
EDC5 E8 E8C R       C          call   f_put_byte         ;
EDC8 8A E6 01       C          mov     ab,f_head        ; blow off high 7 bits.
EDCB 80 B4 01       C          and    ab,1
EDCE E8 E8C R       C          call   f_put_byte         ;
EDD1 8A E6 06       C          mov     ah,f_seenum
EDD4 E8 E8C R       C          call   f_put_byte
C          ; Get bytes 3,4,5,6 from table.
C          ; If we are formatting then we need bytes 3,4,7,8 from table.
C
EDD7               C          f_rw_skip:
EDD7 B9 0004        C          mov     cx,4
EDDA B9 0003        C          mov     bx,3          ; no. bytes per sector.
EDDD               C          f_rw2:
EDDD E8 EDF R       C          call   f_get_var
EDE0 8A 80          C          mov     ab,al
EDE2 E8 E8C R       C          call   f_put_byte
EDE5 43             C          inc    bx
EDE6 83 FB 05       C          cmp     bx,5          ; time to check for format?
EDF9 75 09          C          jne    f_rw3          ; No.
EDDB 80 7E 03 05   C          cmp     byte ptr f_command,5 ; was it a format command?
EDDF 75 03          C          jne    f_rw3          ; no.
EDF1 B8 0007        C          mov     bx,7          ; 7th parameter in table.
EDF4               C          f_rw3:
EDF4 E2 E7          C          loop   f_rw2
EDF6 E8 EF8 R       C          call   f_wait_for_nec
EDF9 E8 E29 R       C          call   f_get_byte      ; get the results.
C
EDFC               C          f_rw_ret:
EDFC E9 EC9 B R     C          jmp    f_io_ret
C
EDFF               C          f_rw_comon  endp
C
C          ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C          ;          Get specified byte from fdu parameter table (f_get_var)
C          ;
C          ;          INPUT:      BX      parameter number (0 - 10)
C          ;
C          ;          OUTPUT:     AL      The requested byte.
C          ;
C          ;          DESTROYS:   AH
C          ;
C          ;          ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
EDFF               C          f_get_var   proc  near
C
EDFF 1E             C          push   ds
EE00 33 C0           C          xor    ax,ax
EE02 8E D8           C          mov     ds,ax          ; segment 0
C
C          assume ds:abs0          ; tell assembler seg 0:
EE04 C5 36 0078 R   C          lda    si,dword ptr [int1E:00h] ; DS:SI points to table
EE08 84 00           C          mov     al,[bx-si]
EE0A 1F             C          pop    ds
C
C          assume ds:data          ; tell assembler seg 40:
EE0B C3             C          ret
C
EE0C               C          f_get_var   endp
C
C          ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
C          ;          Send a byte to the NEC controller (f_put_byte)
C          ;
C          ;          INPUT:      AH      byte to output.
C          ;
C          ;          OUTPUT:
C          ;
C          ;          ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
EE0C               C          f_put_byte  proc  near
C
EE0C E8 EF6 B R     C          call   f_nec_rdy        ; returns MSR byte in AL.
EE0F A8 40           C          test   al,40h         ; direction bit.
C          .list
EE11 75 05          C          jnz    f_pb_orret      ; wrong direction.
EE13 42             C          inc    dx
EE14 84 C4          C          mov     al,ah
EE16 EE             C          out    dx,al
C
EE17               C          f_pb_ret:
EE17 C3             C          ret
C
EE18               C          f_pb_orret:
EE18 C6 06 0041 R 20 C          mov     diskette_status,fdc_error
EE1D E9 EC9 B R     C          jmp    f_io_ret
C
EE20               C          f_put_byte  endp

```



# ROM BIOS Listing

```

EE81 B1 04      C      mov     cl,4           ; shift count
EE83 D3 C0      C      rol     ax,cl         ; move high nib around.
EE85 8A 56      C      mov     ch,al         ; save high nib.
EE87 80 E5 0F   C      and     ch,0Fh        ; isolate high nib
EE8A 24 F0      C      and     al,0F0h      ; prepare for offset calculation
EE8C 03 D8      C      add     bx,ax         ; 20 bit calculation.
EE8E 73 02      C      jnc     f_sd1        ; high nib
EE90 FE 05      C      inc     ch
EE92           C      f_sd1:
EE92 8A C5      C      mov     al,ah        ; high nib. to latch
EE94 E6 51      C      out     dma_seg2_2,al
EE96 B0 06      C      mov     al,6         ; disable channel 2.
EE98 E6 0A      C      out     dma_mask_bit,al
EE9A 8A C3      C      mov     al,bh        ; low byte of address.
EE9C E6 04      C      out     dma_addr_2,al
EE9E 8A C7      C      mov     al,bh        ; high byte of address.
EEA0 E6 04      C      out     dma_addr_2,al
EEA2 8B D3      C      mov     dx,bx        ; save buffer offset.
EEA4 B8 00 03   C      mov     bx,3         ; bytes/sector param
EEA7 E8 E9 FF R C      call    f_get_var    ; get param from table
EEAA 8A C8      C      mov     cl,al        ; save for shift count
EEAC 8A 66 02   C      mov     ah,f_numsecs ; get #sectors.
EEAF 32 C0      C      xor     al,al        ; AX = #sectors x 256
EB01 D1 E8      C      shr     ax,1         ; AX = #sectors x 128
EB03 D3 20      C      shl     ax,cl        ; multiply by bytes/sector.
EB05 48         C      dec     ax           ; DMAC counts zero.
EB06 03 D0      C      add     dx,ax        ; add count to offset
EB08 73 03      C      jnc     f_sd2        ; exit boundary crossing.
EB0A E9 E9 C9 R C      jmp     f_sd2:
EB0C           C      f_sd2:
EB0C E6 05      C      out     dma_count_2,al ; low byte of count.
EB0E 8A C4      C      mov     al,ah        ; high byte of count.
EB10 E6 05      C      out     dma_count_2,al
EB12 B0 02      C      mov     al,2         ; enable channel 2
EB14 E6 0A      C      out     dma_mask_bit,al
EB16 C6 06 00 41 R 00 C      mov     diskette_status,0
EB18           C      f_sd_ret:      ret
EB1A C3         C      f_set_dma      endp
EB1C           C      ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
EB1D           C      ;
EB1E           C      ; Seek (f_seek)
EB1F           C      ;
EB20           C      ; INPUT:
EB21           C      ;
EB22           C      ; OUTPUT:
EB23           C      ;
EB24           C      ; DESTROYS:
EB25           C      ;
EB26           C      ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
EB27           C      ;
EB28           C      f_seek proc      near
EB29           C      ;
EB2A 8A E2 00   C      mov     cl,f_drive   ; get drive# as shift count.
EB2C B0 01      C      mov     al,1
EB2E D2 E0      C      shl     al,cl        ; mask for recal.
EB30 84 06 00 3E R C      test    seek_status,al
EB32 75 28      C      jnz     f_s1         ; no recal. required.
EB34 08 06 00 3E R C      or      seek_status,al ; set the corresponding bit.
EB36           C      ; Two recalibrate commands required in the case of 96 TPI drives.
EB37           C      ;
EB38 B9 00 02   C      mov     cx,2         ; loop count for 96 TPI
EB3A           C      f_a_recal:
EB3B B4 07      C      mov     ah,f_recal_cmd ; recal. command
EB3D 51         C      push    cx          ; save it.
EB3E E8 E9 C0 R C      call    f_put_byte   ; drive bit.
EB40 8A 66 00   C      mov     ah,f_drive   ; drive bit.
EB42 E8 E9 C0 R C      call    f_put_byte   ; end of command phase.
EB44 E8 EF 82 R C      call    f_sis        ; Sense Interrupt Status
EB46 59         C      pop     cx          ; restore it.
EB47           C      ; possibly test bit 4 as well (equipment check...track 0 not reached)
EB48 F6 06 00 42 R C0 C      test    nec_status,0C0h
EB4A 74 0A      C      jz     f_s1         ; equipment OK so restore.
EB4C E2 27      C      loop   f_a_recal
EB4E C6 06 00 41 R 40 C      mov     diskette_status,seek_error
EB50 EF E9 C9 R C      jmp     f_io_ret
EB52           C      ;
EB53           C      f_s1:
EB54 B4 0F      C      mov     ah,f_seek_cmd
EB56 E8 E9 C0 R C      call    f_put_byte   ;
EB58           C      ; prepare second byte of seek command.
EB59 8A 46 01   C      mov     al,f_head
EB5B 24 01      C      and     al,1         ; blow off high 7 bits.
EB5D D0 D0      C      shl     al,1         ; move head to bit 2.
EB5F D0 D0      C      shl     al,1
EB61 D0 D0      C      shl     al,1
EB63 8A 46 00   C      or      al,f_drive   ; combine drive bit with head
EB65 88 46 00   C      mov     f_drive,al  ; and save it.
EB67 8A E0      C      mov     ah,al
EB69 E8 E9 C0 R C      call    f_put_byte   ;
EB6B 8A 66 07   C      mov     ah,f_cyl    ;
EB6D F6 46 01 80 C      test    byte ptr f_head,80h ; test 80 track bit.
EB6F 74 02      C      jz     f_cont       ;
EB71 D4 E4      C      shl     ah,1         ; cyl x 2
EB73           C      f_cont:
EB74 E8 E9 C0 R C      call    f_put_byte   ; end of seek command.
EB76 E8 EF 82 R C      call    f_sis        ; Sense Interrupt Status
EB78           C      ;
EB79           C      ;

```

# ROM BIOS Listing

```

EF2C F6 06 0042 R C0      C          test    nec_status,0C0h          ; test for seek end.
C
C
EF31 75 13                C          jnz     f_s_ret
EF33 BB 0009                C          mov     bx,9
C
EF36 E8 EDFF R            C          call   f_get_var
EF39 0A C0                C          or     al,al
EF3B 74 09                C          jz     f_s_ret          ; head settle = 0.
EF3D 8A C6                C          mov     cl,al          ; use settle parm. al loop index
EF3F 32 ED                C          xor     oh,oh
C
EF41                      C f_head_settle:
EF41 E8 EF47 R            C          call   f_wait_one_ms
EF44 E2 FB                C          loop  f_head_settle
C
EF46                      C f_s_ret:
EF46 C3                    C          ret
C
EF47                      C f_seek  endp
C
C
C ;
C ;
C ; One millisecond delay loop (approximately)
C ;
C ; The CALL is 19 clocks.
C ; The callers LOOP statement is 17 clocks.
C ; No flags affected.
C ;
C ;
C ;
C
EF47                      C f_wait_one_ms proc near
EF47 51                    C          push  cx          ; 11 clocks
EF48 B9 0176                C          mov   cx,374        ; 4 clocks
EF4B E2 FE                C          w_one: loop w_one ; (17 x CX) + 5 clocks
EF4D 59                    C          pop  cx          ; 8 clocks
EF4E C3                    C          ret             ; 16 clocks
EF4F                      C f_wait_one_ms endp
C
C
C ;
C ;
C ; This routine is called by the timer_int routine when motor_count = 0
C ;
C ;
C ;
C
EF4F                      C stop_disk proc near
C
EF4F B0 0C                C          mov   al,0Ch
EF51 BA 03F2                C          mov   dx,f_motor_port
EF54 EE                    C          out  dx,al
EF55 C3                    C          ret
EF56                      C stop_disk endp
C
C
C include fdu2.asm
C
C ;
C ;
C ;
C ; INPUT: none
C ;
C ; OUTPUT: MSB of seek_status is set if NEC interrupts.
C ;
C ; DESTROYS: nothing
C ;
C ;
C ;

```







# ROM BIOS Listing

```

C ;          al      preserved
C ;
C ;          Input: ah = 2  read the printer status
C ;                   dx = printer port number (0,1,2,3)
C ;          Output: ah =  status of printer
C ;
C ;          Trash: ah =  (ah - 2) if ah > 2
C ;                   al      preserved
C ;
C ;          Assumes:  prt_stat_x = prt_data_x + 1 = dx + 1
C ;                   prt_cmd_x = prt_data_x + 2 = dx + 2
C ;
C ;          Printer Status Byte from prt_stat_x:
C ;
C ;          bit #0 =  time-out on printing character (p_out).
C ;                   set by software; no hardware significance.
C ;          bits #1-2 = no significance (always cleared).
C ;          bit #3 =  hardware: I/O error.
C ;          bit #4 =  hardware: selected.
C ;          bit #5 =  hardware: out of paper.
C ;          bit #6 =  hardware: acknowledge.
C ;          bit #7 =  hardware: not busy.
C ;
C ;          "Good" Statuses are: 90h & 10h if a printer is connected.
C ;                               30h if printer is disconnected.
C ;
C ;          =====
EFD2          ORG      0EFD2h
EFD2          p_io    proc  near
C ;                   assume cs:code, ds:nothing, es:nothing, ss:nothing
EFD2          FB      ati                      ; enable interrupts
EFD3          83 FA 04  cmp      dx,a                      ; 4 printers allowed max
EFD6          73 32   jae      p_nop
C ;
C ;                   assume cs:code, ds:data, es:nothing, ss:nothing
EFD8          51     push     cx                      ; save registers
EFD9          52     push     dx
EFDA          57     push     di
EFDB          86 C4  xchg    al,ah                    ; reverse al & ah
EFDD          1E     push     ds                      ; ah saves al throughout
EFDE          2E: 8E 1E E5F2 R mov     ds,word ptr cs:[set_ds_word] ; satisfy assumptions
EFEE          8B FA  mov     di,dx                    ; get port number (0-3)
EFES          33 C9  xor     cx,cx                      ; clear cx
EFET          8A BD 0078 R mov     cl,byte ptr ds:[di+printer_t_out] ; get printer time-out
EFEB          D1 E1  sal     cx,1                      ; double it 2 faster epu
EFED          03 FF  add     di,di                    ; make word index
EFEF          8B 95 0008 R mov     dx,word ptr ds:[di+printer_addr] ; get address of printer
EFF3          1F     pop      ds                      ; data port
C ;                   restore ds
C ;
C ;                   assume cs:code, ds:nothing, es:nothing, ss:nothing
EFF4          0B D2  or      dx,dx                    ; is a printer there?
EFF6          74 0D  jz      p_ret
C ;
EFF8          33 FF  xor     di,di                    ; clear di
EFAA          0A C0  or      al,al                    ; al = 0?
EFAE          74 0D  jz      p_out                    ; dx = prt_data_x
EFBE          42     inc     dx                      ; dx = prt_stat_x
EFFF          2C 02  sub     al,2                    ; al = 1 < 2?
F001          72 24  jb      p_init                    ; dx = prt_stat_x
F003          74 2F  je      p_stat                    ; al = 2?
C ;                   dx = prt_stat_x
F005          86 C4  p_ret: xchg    al,ah                    ; reverse al & ah back
C ;                   ; ah saved al throughout
F007          5F     pop      di                    ; restore registers
F008          5A     pop      dx
F009          59     pop      cx
F00A          CF     p_nop:  iret
C ;
C ;          -----
C ;          Print Character to Parallel Printer Interface.
C ;
C ;          Input:  ah =  character to print
C ;                   cx =  printer time-out
C ;                   dx =  address of printer data port (prt_data_x).
C ;                   di =  0
C ;          Output: ah =  character to print
C ;                   al =  status of printer: bit #0 set if time out
C ;                   dx =  address of printer status port (prt_stat_x).
C ;          Trash:  cx & di destroyed.
C ;
C ;          Assumes:  prt_stat_x = prt_data_x + 1 = dx + 1
C ;                   prt_cmd_x = prt_data_x + 2 = dx + 2
C ;          -----
C ;
C ;                   assume cs:code, ds:nothing, es:nothing, ss:nothing
F00B          8A C4  p_out:  mov     al,ah                    ; get character to print
F00D          EE     out     dx,al                    ; output character

```

# ROM BIOS Listing

```

F00E 42          C          inc     dx                      ; dx = prt_stat_x
F00F EC          C          p_lp:  in     al,dx                ; get printer status
F010 24 F8       C          and     al,0F8h              ; clear bogus printer bits
F012 34 49       C          xor     al,049h            ; flip acknowledge & I/O err bit
F014 78 07       C          js     p_ok                ; & set printer time-out bit #0
F016 4F          C          dec     di                      ; inner loop counter
F017 75 F6       C          jnz    p_lp                ; inner loop
F019 E2 F4       C          loop   p_lp                ; outer loop
F01B EB E8       C          jmp     short p_ret          ; return status with time-out

F01D 42          C          p_ok:  inc     dx                      ; dx = prt_cmd_x
F01E B0 0D       C          mov     al,0Dh              ; set strobe high (al = 0Dh)
F020 EE          C          out     dx,al
F021 90          C          nop
F022 48          C          dec     ax                      ; set strobe low (al = 0Ch)
F023 EE          C          out     dx,al
F024 4A          C          dec     dx                      ; dx = prt_stat_x

F025 EB 0D       C          jmp     short p_stat

;-----
; Initialize Parallel Printer Interface.
;
; Input:  ah =   byte to return in al.
;         dx =   address of printer status port (prt_stat_x).
; Output: al =   status of printer
;         dx =   address of printer status port (prt_stat_x).
; Trash:  cx =   0 destroyed.
;
; Assumes:  prt_stat_x = prt_data_x + 1 = dx + 1
;           prt_cmd_x = prt_data_x + 2 = dx + 2
;-----
          assume cs:code, ds:nothing, es:nothing, ss:nothing

F027 B0 08       C          p_init: mov  al,08h                ; request init (hold line low)
F029 42          C          inc     dx                      ; dx = prt_cmd_x
F02A EE          C          out     dx,al

F02B B5 05       C          mov     ch,05h                ; delay awhile (cx = 0577h)
F02D E2 FE       C          loop   $

F02F B0 0C       C          mov     al,0Ch                ; disable interrupts, manual lf
F031 EE          C          out     dx,al                ; (init done - line set high)
F032 90          C          nop

F033 4A          C          dec     dx                      ; dx = prt_stat_x
;          jmp     short p_stat          ; fall through

;-----
; Read Status of Parallel Printer Interface.
;
; Input:  dx =   address of printer status port (prt_stat_x).
; Output: al =   status of printer
;         dx =   address of printer status port (prt_stat_x).
;
; Assumes:  prt_stat_x = prt_data_x + 1 = dx + 1
;-----
          assume cs:code, ds:nothing, es:nothing, ss:nothing

F034 EC          C          p_stat: in  al,dx                ; get printer status
F035 24 F8       C          and     al,0F8h              ; clear bogus printer bits
F037 34 48       C          xor     al,048h              ; flip acknowledge & I/O err bit
F039 EB CA       C          jmp     short p_ret          ; exit

F03B          C          p_io  endp

F03B          C          code  ends
          include vid.asm

;=====
;          Filename:      vid.src
;
;          This module includes INT 10h, the display routines.
;=====
; These constants must be defined (amount to scroll/clear during vert retrace):
; V_KSCROLL equ 4 ; 4 rows, plus
; V_KCLEAR  equ 7

F03B          C          code  segment public 'ROM'
          assume cs:code, ds:nothing, es:nothing, ss:nothing

;-----
;          ROM data
;-----

F045          C          ORG     0F045h

F045          C          v_data1 proc  near

F045 F0FC R       C          v_tbl  dw     v_set_mode          ; ah = 00h
F047 F1E9 R       C          dw     v_ours_type             ; ah = 01h

```

# ROM BIOS Listing

```

F049 F1F7 R      C      dw      v_curs_pos      ; ah = 02h
F04B F215 R      C      dw      v_r_curs_pos     ; ah = 03h
F04D DTCD R      C      dw      grf_light_pen    ; ah = 04b      (see graph.src)
F04F F22C R      C      dw      v_page       ; ah = 05h
F051 F27F R      C      dw      v_scrll_up     ; ah = 06h
F053 F35B R      C      dw      v_scrll_dn     ; ah = 07h
F055 F37C R      C      dw      v_rac        ; ah = 08h
F057 F3A6 R      C      dw      v_wac        ; ah = 09h
F059 F3DF R      C      dw      v_wc         ; ah = 0Ah
F05B F41A R      C      dw      v_col        ; ah = 0Bh
F05D D7EA R      C      dw      grf_write_dot   ; ah = 0Ch      (see graph.src)
F05F D7D0 R      C      dw      grf_read_dot    ; ah = 0Dh      (see graph.src)
F061 F446 R      C      dw      v_terminal    ; ah = 0Eh
F063 F4CF R      C      dw      v_stat       ; ah = 0Fh

F065
C      v_data1 endp
C
C ;=====
C ; INT 10h -- Video Interrupt Service Routine.
C ;=====
C ; -- Set CPU flags.
C ; -- Segment registers properly loaded.
C ; -- CALLs routines with: -- al, bx, cx, dx intact
C ; -- ah = v_mode
C ; -- si = 2 * (function that was in ah)
C ; -- di = bits #4 & 5 of switch_bits
C ; -- bp = value of ax to be returned
C ;
C ; Input: ah = function number (00h <= ah <= 0Fh)
C ;
C ; Trash: None. (bp, si, di, ds, & es if ROM stack)
C ;=====
F065
C      ORG      0F065h
F065
C      v_io   proc   near
C
C      assume  cs:code, ds:nothing, es:nothing, ss:nothing
C
C      stl     esp                ; enable interrupts
C      mov     ah,0Fh            ; input out of range?
C      ja     v_nop
C
C      push   es                 ; save 'trashable' registers
C      push   ds
C      mov     ds,word ptr cs:[set_ds_word] ; avoid potential stack problems
C      push   di
C      push   si
C      push   bp
C
C      assume  cs:code, ds:data, es:nothing, ss:nothing
C
C      push   ax                 ; save ax
C
C      mov     al,ah              ; al = function number
C      add     al,ah              ; # 2
C      cbw
C      push   ax                 ; save for CALL later.
C
C      mov     di,para_graph      ; get screen segment ..
C      mov     al,byte ptr ds:[switch_bits] ; .. check switch bits ..
C      test    al,20h
C      jz     v_colour            ; .. if either is 0, it's
C      test    al,10h            ; .. color display board
C      jz     v_colour
C      add     di,para_mono-para_graph ; .. it's a monochrome board
C      v_colour:
C      mov     es,di              ; set es = video ram
C
C      pop     di                 ; Get index to call table.
C
C      pop     ax                 ; restore ax
C      mov     ah,byte ptr ds:[v_mode] ; get display driver mode
C      mov     bp,ax              ; bp saves ax throughout
C      ; (return ah = v_mode
C      ; unless specific ret. value)
C
C      cld
C      call    cs:[di+(offset v_tbl)] ; String ops move UP, mostly.
C      ; perform display function
C
C      pop     bp                 ; restore 'trashed' registers
C      pop     si                 ; (destroyed if ROM stack)
C      pop     di
C      pop     ds
C      pop     es
C
C      v_nop:  ired
C
C      v_io   endp
C
C ;=====
C
C      ORG      0F0A4h
F0A4
C      v_data2 proc   near
F0A8
C      v_parms label   byte
C      ; 6845 Parameters except register 3h (Horizontal Synch Width).
C

```

# ROM BIOS Listing

```

FOA4 38 28 2D 06      C v_md_40      db      38h,28h,2Dh,06h ; text 40 x 25
FOA8 1F 06 19 1C      C              db      1Fh,06h,19h,1Ch ; mode 0 -> monochrome
FOAC 02 07 06 07      C              db      02h,07h,06h,07h ; mode 1 -> color
FOB0 00 00 00 00      C              db      00h,00h,00h,00h
FOB4 71 50 5A 0C      C v_md_80      db      71h,50h,5Ah,0Ch ; text 80 x 25
FOB8 1F 06 19 1C      C              db      1Fh,06h,19h,1Ch ; mode 2 -> monochrome
FOBC 02 07 06 07      C              db      02h,07h,06h,07h ; mode 3 -> color
FOC0 00 00 00 00      C              db      00h,00h,00h,00h
FOC4 38 28 2D 06      C v_md_graph   db      38h,28h,2Dh,06h ; graphics
FOC8 7F 06 64 70      C              db      7Fh,06h,64h,70h ; mode 4 -> 320 x 200 color
FOCC 02 01 06 07      C              db      02h,01h,06h,07h ; mode 5 -> 320 x 200 monochrome
FOD0 00 00 00 00      C              db      00h,00h,00h,00h ; mode 6 -> 640 x 200 monochrome
FOD4 61 50 52 0F      C v_md_mono    db      61h,50h,52h,0Fh ; monochrome card 80 x 25
FOD8 19 06 19 19      C              db      19h,06h,19h,19h ; mode 7 -> monochrome card
FODC 02 0D 0B 0C      C              db      02h,0Dh,0Bh,0Ch
FOE0 00 00 00 00      C .list
FOE4 0800              C v_md_len     dw      2048          ; 40x25      modes 0 & 1
FOE6 1000              C              dw      4096          ; 80x25      modes 2 & 3
FOE8 4000              C              dw      16384         ; graphics   modes 4 & 5
FOEA 4000              C              dw      16384         ;             mode 6
FOEC 28                C v_md_wid     db      40            ; 0 -> text   40x 25 monochrome
FOED 28                C              db      40            ; 1 -> text   40x 25 color
FOEE 50                C              db      80            ; 2 -> text   80x 25 monochrome
FOEF 50                C              db      80            ; 3 -> text   80x 25 color
FOF0 28                C              db      40            ; 4 -> graphics 320x200 color
FOF1 28                C              db      40            ; 5 -> graphics 320x200 monochrome
FOF2 50                C              db      80            ; 6 -> graphics 640x200 monochrome
FOF3 50                C              db      80            ; 7 -> text   80x 25 monochrome card
FOF4 2C                C .list
FOF5 28                C v_md_enable  db      2Ch           ; 0 -> text   40x 25 monochrome
FOF6 2D                C              db      28h           ; 1 -> text   40x 25 color
FOF7 29                C              db      2Dh           ; 2 -> text   80x 25 monochrome
FOF8 2A                C              db      29h           ; 3 -> text   80x 25 color
FOF9 2E                C              db      2Ah           ; 4 -> graphics 320x200 color
FOFA 1E                C              db      2Eh           ; 5 -> graphics 320x200 monochrome
FOFB 29                C              db      1Eh           ; 6 -> graphics 640x200 monochrome
FOFC 29                C              db      29h           ; 7 -> text   80x 25 monochrome card
FOFC                C .list
FOFC                C v_data2_endp
FOFC                C ;-----
FOFC                C ; Set Mode & Clear Screen      ah = 00h
FOFC                C ;
FOFC                C ; Input: al      = mode
FOFC                C ;              = 0 -> text   40x 25 monochrome
FOFC                C ;              = 1 -> text   40x 25 color
FOFC                C ;              = 2 -> text   80x 25 monochrome
FOFC                C ;              = 3 -> text   80x 25 color
FOFC                C ;              = 4 -> graphics 320x200 color
FOFC                C ;              = 5 -> graphics 320x200 monochrome
FOFC                C ;              = 6 -> graphics 640x200 monochrome
FOFC                C ;              = 7 -> text   80x 25 monochrome card
FOFC                C ;              = 8 -> graphics 640x400 monochrome
FOFC                C ;              = 72 -> graphics 640x400 monochrome tinytext
FOFC                C ;
FOFC                C ; Output: ah     = 00h
FOFC                C ;           al     = v_colorpal
FOFC                C ;
FOFC                C ; Assume: contents of v_base6845 = pointer register      (3D4h)
FOFC                C ;         (contents of v_base6845)+1 = data register      (3D5h)
FOFC                C ;         (contents of v_base6845)+4 = mode control register (3D8h)
FOFC                C ;         (contents of v_base6845)+5 = overscan register   (3D9h)
FOFC                C ;         (contents of v_base6845)+6 = status register     (3DAh)
FOFC                C ;         (contents of v_base6845)+10 = mode control register #2 (3DEh)
FOFC                C ;
FOFC                C ; Trash: si & di destroyed.
FOFC                C ;-----
FOFC                C v_set_mode     proc  near
FOFC                C ; assume cs:code, ds:data, es:v_ram, ss:nothing
FOFC 52            C          push  dx          ; save dx
FOFC 51            C          push  cx          ; save cx
FOFC                C ; Get Color/Monochrome dependent stuff.
FOFC                C ;
FOFC 32 E4        C          xor   ah,ah          ; AH = mode ctrl., color board
FOFC BA 03D4      C          mov   dx,color_pointer ; color 6845 pointer register.
FOFC                C ;
FOFC F6 06 0010 R 10 C          test  byte ptr ds:[switch_bits],10h ; monochrome board?
FOFC 74 0D        C          jz   v_set_mode_color ; if not, skip monochrome stuff.
FOFC F6 06 0010 R 20 C          test  byte ptr ds:[switch_bits],20h
FOFC 74 06        C          jz   v_set_mode_color
FOFC                C ;
FOFC 11 B8 0107   C          mov  ax,0107h          ; It's a monochrome board, so..
FOFC                C ;         ; (AH,AL) = (overwrite mode
FOFC 1114 83 C2 E0 C          add  dx,v_pointer-color_pointer; for monochrome, mono. mode)
FOFC                C ;         ; monochrome pointer register.
FOFC                C v_set_mode_color:
FOFC                C ; Save CRT Mode & 6845 address, and reset display monitor with mode control.

```

# ROM BIOS Listing

```

C
F117 A2 00A9 R      ; save mode
C      mov     byte ptr ds:[v_mode],al
C      mov     word ptr ds:[v_base6845],dx      ; save 6845 pointer register.
C      xchg   ah,al      ; AH=mode, AL=mode ctrl.
C      add    dx,4      ; get 6845 mode control register
C      out    dx,al      ; reset display
C      sub    dx,4      ; restore 6845 address.
C      mov    al,ah      ; restore mode in al
C
C      ; Get pointer to display parameters.
C
F129 1E             ; save ds = data_seg
C      push  ds
C      assume cs:code, ds:abs0, es:v_ram, ss:nothing
C
F12A 33 F6         xor     si,si
C      mov    ds,si      ; satisfy assumptions
C      lds   si,dword ptr ds:[int1Dloc]      ; display parameter pointer
C
C      ; ds:si in effect points to cs:v_params.
C
C      assume cs:code, ds:code, es:v_ram, ss:nothing
C
C      ; Determine which set of parameters to use from mode.
C
F132 B9 0010      mov     cx,16      ; count of parameters
C      cmp    al,2      ; 40x25 mode? (0 & 1?)
C      jb    v_set_mode_lp      ; if so, we're done
C      add    si,cx      ; next set of parameters
C      cmp    al,4      ; 80x25 mode? (2 & 3?)
C      jb    v_set_mode_lp      ; if so, we're done
C      add    si,cx      ; next set of parameters
C      cmp    al,7      ; graphics mode? (4,5,6,64,7?)
C      jne   v_set_mode_lp      ; if so, we're done
C      add    si,cx      ; else, monochrome card (7)
C
C      ; Loop through 6845 initialization table outputting register number and data
C      v_set_mode_lp:
C
F147             mov     al,16      ; get 6845 register number =
C                                     ; = (16 - cl) (unscrambled)
C
F149 2A C1         sub    al,cl
C      out    dx,al      ; output to register port
C      inc    dx      ; point to 6845 data register
C      lodsb      ; get parm value: al gets ds:si
C      out    dx,al      ; output to data port
C      dec    dx      ; point back to pointer register
C      loop  v_set_mode_lp      ; next register
C                                     ; dx = pointer register
C
C      assume cs:code, ds:data, es:v_ram, ss:nothing
C
F152 1F             pop    ds      ; restore ds = data_seg
C
F153 8A C4         mov    al,ah      ; save mode in ah & al
C      xor    ah,ah      ; ax = mode
C      mov    si,ax      ; si = mode hence...
C
C      ; Clear the screen.
C
F159 B9 2000      mov     cx,2000h      ; assume 8k words to clear
C
F15C 3C 04         cmp    al,4      ; 40x25 or 80x25 text modes 0-3?
C      jb    v_md_clr_8k      ; if so, clear 8k words.
C      cmp    al,7      ; monochrome card mode 7?
C      je    v_md_clr_2k      ; if so, clear 2k words.
C      jb    v_md_clr_graphics      ; graphics mode 4-6 clear 8k wds
C      shl    cx,1      ; mode 64 & 72 clear 16k wds
C      v_md_clr_graphics:
C      xor    ax,ax      ; graphics mode
C      jmp   short v_md_clr      ; clear screen with zeroes
C
C      v_md_clr_2k:
C      mov    ch,08h      ; cx = 0800h
C      v_md_clr_8k:
C      mov    ax,(7*100h),(' ')      ; clear with attribute & space
C      v_md_clr:
C      xor    di,di
C      rep   stosw      ; es:di gets ax
C
C      ; Set mode control register #2
C
C      ; Handle underline on shades-of-gray monitor.
C
F175 83 C2 06      add    dx,6      ; dx = pointer register
C      in    al,dx      ; get 6845 status register
C      and   al,010h      ; get CRT status
C      shl  al,1      ; isolate color/shades bit #4
C      shl  al,1      ; move it to underline bit #6
C
C      ; Handle double scan line modes 64 & 72.
C
F17F 83 FE 40      cmp    si,64      ; dx = 6845 status register
C      jb    v_md_dbl      ; modes 0 through 7?
C      inc   ax      ; if so, single scan line mode
C      mov   si,6      ; else mode 64 or 72, set bit #0
C                                     ; modes 64 & 72 look like mode 6
C                                     ; from now on
C
F188             v_md_dbl:
C                                     ; double scan line mode.

```

# ROM BIOS Listing

```

F188 83 C2 04      C      add    dx,8          ; get mode control register #2
F18B EE           C      out    dx,al
C
C      ; Enable display monitor with mode control.
C
F18C 2E: 8A 84 F0F4 R  C      mov    al,byte ptr cs:[si-v_md_enable]
F191 A2 0065 R      C      mov    byte ptr ds:[v_3x8],al      ; save the value for later
C
F194 83 EA 06      C      sub    dx,6          ; get 6845 mode control register
F197 EE           C      out    dx,al      ; enable display
C
C      ; Determine width & length of screen.
C
F198 33 C0        C      xor    ax,ax         ; clear ah
F19A 2E: 8A 84 F0E4 R  C      mov    al,byte ptr cs:[si-v_md_wid]
F19F A3 004A R      C      mov    word ptr ds:[v_width],ax
C
F1A2 81 E6 000E    C      and    si,0Eh        ; make word index divided by 2
F1A6 2E: 8B 84 F0E4 R  C      mov    ax,word ptr cs:[si-v_md_len]
F1AB A3 004C R      C      mov    word ptr ds:[v_height],ax
C
C      ; Set up overscan register & v_colorpal.
C
F1AE B0 30        C      mov    al,030h       ; v_colorpal for modes 0-5 & 7
F1B0 8A 26 0049 R  C      mov    ah,byte ptr ds:[v_mode] ; retrieve v_mode
F1B4 80 FC 06      C      cmp    ah,6          ; modes 0-5 ?
F1B7 72 0D        C      jb    v_ovr_ok       ; if so, we're ok.
C
F1B9 74 09        C      je    v_ovr_not_ok   ; 640x200 graphics mode 6 ?
C                        ; if so, change v_colorpal
C
F1BB 80 FC 40      C      cmp    ah,64         ; 640x400 graphics mode 64, 72 ?
F1BE 72 06        C      jb    v_ovr_ok       ; if not, we're ok.
C
F1C0 D1 26 004C R  C      shl    word ptr ds:[v_height],1 ; if so we set v_height wrong,
C                        ; double v_height from 16k to 32k
C
F1C4             C      v_ovr_not_ok:
F1C4 B0 3F        C      mov    al,03Fh       ; v_colorpal for modes 6,64,72
C
F1C6             C      v_ovr_ok:
F1C6 A2 0066 R      C      mov    byte ptr ds:[v_colorpal],al ; dx = 6845 mode control register
F1C9 42           C      inc   dx             ; save the value for later
F1CA EE           C      out    dx,al      ; get 6845 overscan register
C
C      ; Clear all cursor positions.
C
C      assume cs:code, ds:data, es:data, ss:nothing
C
F1CB 1E           C      push  da            ; set es = firmware data area
F1CC 07           C      pop   es
C
F1CD BF 0050 R      C      mov    di,ds:[offset v_cursor] ; get address [defined by DB]
F1D0 B9 0008      C      mov    cx,8
F1D3 33 C0        C      xor    ax,ax         ; ax = 0
F1D5 F3/ AB       C      rep   stoaw          ; es:di gets ax = 0
C
C      ; Clear other firmware data variables (ax = 0).
C
F1D7 A3 004E R      C      mov    word ptr ds:[v_top],ax ; set starting offset to 0
F1DA A2 0062 R      C      mov    byte ptr ds:[v_page],al ; set current active page to 0
F1DD C7 06 0060 R 0607 C      mov    word ptr ds:[v_cursor],0607h ; set cursor mode
C
C      ; Clean up.
C
F1E3 A0 0066 R      C      mov    al,byte ptr ds:[v_colorpal]
F1E5 59           C      pop   cx            ; restore cx
F1E7 5A           C      pop   dx            ; restore dx
F1E8 C3           C      ret
C
F1E9             C      v_set_mode      endp
C
C      ;-----
C      ; Set Cursor Value
C      ; ah = 01h
C      ; Input:  ch = bits #0-4 = starting line for cursor
C      ;         cl = bits #0-4 = ending line for cursor
C      ; Output: ah = 10
C      ;         al = cl
C      ; Trash: si & di destroyed. (si = dx; di = cx)
C      ;-----
C
F1E9             C      v_curs_type    proc  near
C                        assume cs:code, ds:data, es:v_ram, ss:nothing
C
F1E9 89 0E 0060 R  C      mov    word ptr ds:[v_cursorize],cx ; save the cursor value
F1ED 8B F9        C      mov    di,cx
C
F1EF B4 0A        C      mov    ah,10         ; 6845 cursor set register = 10
F1F1 E8 F262 R      C      call  v_6845        ; set cursor; ah 6845 gets cx
C                        ; si = dx destroyed
C                        ; ah = preserved = 10; al = cl
C                        ; di restores cx
C                        ; restore al with original cl
C
F1F4 8A C1        C      mov    al,cl
F1F6 C3           C      ret
F1F7             C      v_curs_type    endp
C      ;-----

```

# ROM BIOS Listing

```

C ; Set Cursor Position          ah = 02h
C ;
C ; Input: bh = page number (0-7)
C ;         (dh,dl) = (row,col) of current cursor from (0,0)
C ; Output: if bh = v_apage,    ah = 14
C ;         al = low byte of cursor position
C ;         else,              ah = v_mode
C ;         al = preserved
C ;
C ; Trash: al & dl destroyed. (al = dx, dl = cx)
C -----
F1F7          v_cura_pos      proc  near
C ;
C ; assume cs:code, ds:data, es:v_ram, ss:nothing
C ;
C ; mov     di,cx                ; save cx
C ;
C ; mov     cl,bh                ;
C ; mov     si,cx                ;
C ; and     si,7                 ; mask to 8 pages
C ; add     si,si                 ; *2 => word index
C ;
C ; mov     word ptr ds:[si+v_curpos],dx  ; save the cursor position
C ;
C ; cmp     bh,byte ptr ds:[v_apage]     ; if active page, put the cursor
C ; jne     v_set_cura                    ; on the screen.
C ;
C ; mov     cx,di                    ; not active page, so just
C ; ret                                     ; restore cx
C ;                                     ; and exit
C ;
C ; v_set_cura:                    ; active page, so set cursor..
C ; mov     ax,dx                    ; ax gets cursor position
C ; jmp     v_set_cur_pos              ; set cursor; ah 6845 gets cx
C ;                                     ; si = dx destroyed
C ;                                     ; ah = preserved = 14
C ;                                     ; al = low byte of cursor posn
C ;
C ; v_cura_pos      endp
C -----
C ; Read Cursor          ah = 03h
C ;
C ; Input: bh = page number (0-7)
C ; Output: (dh,dl) = (row,col) of current cursor from (0,0)
C ;         (ch,cl) = current cursor mode setting
C ;         ax = dx
C ;
C ; Trash: None.
C -----
F215          v_r_cura_pos    proc  near
C ;
C ; assume cs:code, ds:data, es:v_ram, ss:nothing
C ;
C ; mov     ax,dx                ;
C ; mov     cx,bx                ; save bx
C ; mov     bl,bh                ;
C ; and     bx,07h               ; page number mod 8
C ; shl     bx,1                 ; page number mod 8 word index
C ; mov     dx,word ptr ds:[bx+v_curpos]
C ; mov     bx,cx                ; restore bx
C ; mov     cx,word ptr ds:[v_cursize]
C ; ret
C ;
C ; v_r_cura_pos      endp
C -----
C ; Read Light Pen (see graph.src) ah = 04h
C ;
C ;
C ; Set Active Display Page          ah = 05h
C ;
C ; Input: al = new page number (0-7 for modes 0-1; 0-3 for 2-3)
C ; Output: 6845 is reset to display the new active page
C ;         ah = 14
C ;         al = low byte of cursor position
C ;
C ; Trash: bp, si & di destroyed. (si = dx, di = cx)
C -----
F22C          v_page         proc  near
C ;
C ; assume cs:code, ds:data, es:v_ram, ss:nothing
C ;
C ; and     ax,07h               ; page number mod 8
C ; mov     bp,ax                ; save ax = page number mod 8
C ;
C ; mov     byte ptr ds:[v_apage],al  ; save active page number (0-7)
C ; mov     v_page_0,al          ; page number = 07
C ;
C ; mov     di,dx                ; save dx
C ; mul     word ptr ds:[v_height]    ; dx:ax = (page number)*v_height
C ; mov     dx,di                ; restore dx
C ;
C ; v_page_0:                    ;
C ; mov     word ptr ds:[v_top],ax    ; save starting address of page
C ; mov     ax,1                 ; divide by 2 for byte count

```





# ROM BIOS Listing

```

C
F287 52          C          push  dx          ; save registers
F288 51          C          push  cx
F289 53          C          push  bx
C
F28A 8A D8      C          mov    bl,al        ; save line count
F28C BB C1      C          mov    ax,cx        ; pass upper left coordinates...
F28E E8 F4DE R  C          call   v_serl_pos   ; to common scroll positioning routine
F291 74 62      C          jz     v_clr_bot   ; clear rows if nothing to move
C
; Scroll cl rows up.
C
F293 03 F0      C          iv_mv_up: add    si,ax        ; add (bytes/row)*(rows to scroll) to
C                                     ; 'from' address for scroll
C
; Scroll cl rows up/down (based on bp & direction flag DF).
C
F295          C          v_mv:
F295 8A E1      C          mov    ah,cl        ; ah gets number of rows to move = cl
C
F297 80 3E 0049 R 07 C          cmp    byte ptr ds:[v_mode],7
F29C 74 49      C          je     v_mv_flp    ; jump to fast loop
C
F29E 8A CA      C          mov    cl,dl        ; no. of columns to move up/down per row
C
F2A0          C          v_mv_lp:
F2A0 52          C          push  dx          ; save dx
F2A1 8B 16 0063 R  C          mov    dx,word ptr ds:[v_base6845] ; get 6845 pointer register
F2A5 83 C2 06      C          add    dx,6        ; get 6845 status register
C
; assume es:code, ds:v_ram, es:v_ram, ss:nothing
C
F2A8 06          C          push  es          ; satisfy assumptions
F2A9 1F          C          pop   ds          ; ds gets es
C
; Wait for horizontal retrace...
C
F2AA          C          v_mv_hi:
F2AA EC          C          in    al,dx        ; get CRT status
F2AB D0 DB      C          ror   al,1        ; test display enable (bit #0)
F2AD 72 FB      C          jc    v_mv_hi     ; wait for display enable low (cr)
C                                     ; interrupts are disabled...
C
F2AF FA          C          cli            ; disable now
C
F2B0          C          v_mv_lo:
F2B0 EC          C          in    al,dx        ; 08 get CRT status
F2B1 D0 DB      C          ror   al,1        ; 02 test display enable (bit #0)
F2B3 73 FB      C          jnc   v_mv_lo     ; 16/04 wait for display enable hi (cr)
C
; .list
C
F2B5 A5          C          movsw        ; 18 move word (es:di gets ds:si)
C
; Worst case: (8*2+16)+(8*2+4)+(18) = 58 cycles = 72.5% of 80 cycles
C
F2B6 EC          C          in    al,dx        ; 08 get CRT status (vert synch slow)
C
; assume es:code, ds:data, es:v_ram, ss:nothing
C
F2B7 BA 0040     C          mov    dx,data_seg ; 04 satisfy assumptions
F2BA BE DA      C          mov    ds,dx       ; 02
F2BC 5A          C          pop   dx          ; 08 restore dx
C
F2BD 49          C          dec    cx          ; 03 decrement columns to move
F2BE 75 0A      C          jnz   v_mv_next   ; 04/16 did we move the last column?
C
F2C0 03 F5      C          add    si,bp       ; 03 add/subtract number of bytes
C                                     ; to skip in row to/from 'from'
C                                     ; address for scroll up/down
C
F2C2 03 FD      C          add    di,bp       ; 03 add/subtract number of bytes
C                                     ; to skip in row to/from 'to'
C                                     ; address for scroll up/down
C
F2C4 FE CC      C          dec    ah          ; 03 decrement rows to move
F2C6 74 2C      C          jz     v_mv_end    ; 4/16 did we move the last row?
C
F2C8 8A CA      C          mov    cl,dl        ; 02 number of columns to move
C                                     ; up/down per row
C
; Worst case: [58]+(8*4+2*8)+(3*4)+(3*3)+(3*4+2) = 102 cycles = 12.75% usec
C
F2CA          C          v_mv_next:
C
F2CA FB          C          sti            ; enable interrupts immediately
F2CB AB 08      C          test   al,08h     ; 04 check for vertical retrace
F2CD 74 16      C          jz     v_mv_past   ; 16/04 jump past vertical retrace code
C
; We get here if vertical retrace has started...
C
F2CF 80 04      C          mov    al,V_KSCROLL ; NOTE: interrupts disabled for 1.1ms!
C                                     ; 04 at most V_KSCROLL rows per
C                                     ; vertical retrace...
C
F2D1          C          v_mv_row:
F2D1 1E          C          push  ds
F2D2 06          C          push  es
F2D3 1F          C          pop   ds
F2D4 F3/ A5     C          rep  movsw        ; 11*17*80 move row (es:di gets es:si)
F2D6 1F          C          pop   ds
C
F2D7 03 F5      C          add    si,bp       ; 03 add/subtract number of bytes

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# ROM BIOS Listing

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C                                     ; to skip in row to/from 'from'
C                                     ; address for scroll up/down
F2D9 03 FD          add     di, bp      ; 03
C                                     ; add/subtract number of bytes
C                                     ; to skip in row to/from 'to'
C                                     ; address for scroll up/down

F2DB FE CC          dec     ah        ; 03 decrease rows to move
F2DD 74 15          jz      v_mv_end    ; 04/16 did we move the last row
C                                     ;
C                                     ;
F2DF 8A CA          mov     cl, di     ; 02 number of columns to move
C                                     ; up/down per row
F2E1 FE C8          dec     al        ; 03
F2E3 75 EC          jnz     v_mv_row   ; 04/16

C                                     ; Worst case: [98]*(4+4+4)+[6*(1369+3+3+4+2+3)]+[5*16]*(4)
C                                     ; = 98*12+8322+80*4 = 8516 cycles = 88.71% * 9600 cycles = 1.065ms < 1.2ms
C                                     ;
F2E5 EB B9          jmp     short v_mv_lp
C                                     ;
C                                     ; -----
C                                     ;
F2E7 8A CA          mov     cl, di     ; ah has number of rows to move
F2E9 F3 26: A5      rep     movs  word ptr es:[di], word ptr es:[si] ; number of columns to move
C                                     ;
C                                     ; move the row (es:di gets es:si)
F2EC 03 F5          add     si, bp      ; add number of bytes to skip in row to
C                                     ; 'from' address for scroll
F2EE 03 FD          add     di, bp      ; add number of bytes to skip in row to
C                                     ; 'to' address for scroll
F2F0 FE CC          dec     ah        ;
F2F2 75 F3          jnz     v_mv_flip

C                                     ; -----
C                                     ;
F2F4 EB FB          jmp     short v_mv_end
C                                     ;
C                                     ; enable interrupts immediately
C                                     ;
C                                     ; Clear bl rows below.
F2F5                v_clr_bot:
C                                     ; Clear bl rows below/above if scroll up/down (based on bp & direction flag DF).
C                                     ;
F2F5                v_clr:
C                                     ;
F2F5 8A E7          mov     ah, bh
F2F7 80 3E 0049 R 07 cmp     byte ptr ds:[v_mode], 7
F2FC 74 41          je      v_clr_fast    ; jump to fast loop
C                                     ;
C                                     ;
F2FE 8A CA          mov     cl, di     ; cl = no. of columns to clear per row
C                                     ; (bl = number of rows to clear)
F300 B7 20          mov     bh, ' '     ; bh = blanking character
C                                     ;
C                                     ;
F302 52          push  dx           ; save dx
F303 8B 16 0063 R  mov     dx, word ptr ds:[v_base6845] ; get 6845 pointer register
F307 83 C2 06      add     dx, 6       ; get 6845 status register
C                                     ;
C                                     ; Wait for horizontal retrace...
C                                     ;
F30A                v_clr_hi:
C                                     ; wait till we're in a scanline
F30A EC          in     al, dx      ; get CRT status
F30B D0 D8          rcr    al, 1       ; test display enable (bit #0)
F30D 72 FB          jc     v_clr_hi     ; wait for display enable low (cf)
F30F FA          cli
C                                     ; disable ints first.
C                                     ;
C                                     ;
F310                v_clr_lo:
C                                     ; wait till start of horiz. blanking
F310 EC          in     al, dx      ; 08 get CRT status
F311 D0 D8          rcr    al, 1       ; 02 test display enable (bit #0)
F313 73 FB          jnc   v_clr_lo     ; 16/04 wait for display enable hi (cf)
C                                     ;
C                                     ;
F315 8A C7          mov     al, bh     ; 02 al= bh= ' ' = blanking character
C                                     ;
F317 AB          .list  atow      ; 11 clear word (es:di gets ax)
C                                     ;
C                                     ; Worst case: (8+2*16)+(8+2*4)+(2+11) = 53 cycles = 66.25% of 80 cycles
C                                     ;
F318 EC          in     al, dx      ; 08 get CRT status (vert synch slow)
F319 5A          pop     dx         ; 08 restore dx
C                                     ;
C                                     ;
F31A 49          dec     cx         ; 03 decrease columns to clear
F31B 75 08          jnz   v_clr_nxt    ; 04/16 did we move the last column?
C                                     ;
C                                     ;
F31D 03 FD          add     di, bp     ; 03 add/subtract number of bytes
C                                     ; to skip in row to/from 'to'
C                                     ; address for clear for up/down
C                                     ;
C                                     ;
F31F FE C8          dec     bl        ; 03 decrease rows to clear
F321 74 28          jz     v_scri_ret  ; 04/16 did we clear the last row?
C                                     ;
C                                     ;
F323 8A CA          mov     cl, di     ; 02 number of columns to clear
C                                     ; per row
C                                     ;
C                                     ; Worst case: [53]+(8+8)+(3+4)+(3)+(3+4+2) = 88 cycles = 11.00 usec
C                                     ;
F325                v_clr_nxt:
C                                     ;
F325 FB          sti
F326 A8 08          test   al, 08h     ; 04 check for vertical retrace

```

# ROM BIOS Listing

```

F328 74 12      C          jz      v_clr_past      ; 16/08 jump past vertical retrace code
C              ; We get here if vertical retrace has started...
C              ; NOTE: interrupts disabled for 1.1ms!
F32A 8A C7      C          mov     al,bh          ; 02  al= bh= ' ' = blanking character
F32C B7 07      C          mov     bh,V_KCLEAR      ; 04  at most 7 (not 10) rows per pass
C              v_clr_row:
F32E F3/ AB      C          rep     stow          ; 09*10*80 clear the row (es:di gets ax)
F330 03 FD      C          add     di,bp          ; 03  add/subtract number of bytes
C              ; to skip in row to/from 'to'
C              ; address for clear for up/down
F332 FE CB      C          dec     bl          ; 03  decrement rows to clear
F334 74 15      C          jz      v_scri_ret      ; 04/16 did we clear the last row?
C              mov     cl,di          ; 02  number of columns to clear
F336 8A CA      C          mov     cl,di          ; up/down per row
F338 FE CF      C          dec     bh          ; 03  still working on 10 scan lines??
F33A 75 F2      C          jnz     v_clr_row          ; 04/16
C              ; Worst case:[88]*(4+4+2+4)+[10*(809+3+3+4+2+3)]+[9*16]*(4)
C              ; = 88*14+8240+144*4 = 8490 cycles = 88.44% * 9600 cycles = 1.06ms < 1.2ms
C              v_clr_past:
F33C          C          sti          ; enable interrupts immediately
F33E FB C1      C          jmp     short v_clr_lp
C              ;-----
F33F          C          v_clr_fast:
F341          C          mov     al,' '          ; ah has attribute for blank line(s)
C              ; al = blanking character
C              ; (bl = number of rows to clear)
F343          C          v_clr_flp:
F345          C          mov     cl,di          ; number of columns to clear
F347          C          rep     stow          ; clear the row (es:di gets ax)
F349          C          add     di,bp          ; add number of bytes to skip in row to
C              ; 'to' address for scroll
F34B          C          dec     bl
F34D          C          jnz     v_clr_flp
C              ;-----
F348          C          v_scri_ret:
F34A          C          sti          ; common clean up routine
C              ; enable interrupts immediately
F34C          C          cmp     byte ptr ds:[v_mode],7
F34E          C          je      v_scri_mode_7
F350          C          mov     al,byte ptr ds:[v_3x8]
F352          C          v_scri_mode_7:
C              ; We didn't disable display during vertical retrace...
C              ; Clean up.
F354          C          cld          ; in case we are 'call'ed & scroll down
F356          C          pop     bx          ; restore registers
F358          C          pop     cx
F35A          C          pop     dx
F35C          C          ret
F35B          C          v_scri_up      endp
C              ;-----
C              ; Scroll Active Page Down      ah = 07h
C              ; Input:  if al = 0, then clear entire window with attribute in bh
C              ; else,  al = number of rows to 'scroll' down
C              ;          = number of rows to clear at top of window
C              ;          bh = attribute to be used on blank row(s)
C              ;          (ch,cl) = (row,col) of upper left corner of window from (0,0)
C              ;          (dh,dl) = (row,col) of lower right corner of window from (0,0)
C              ; Output: ah = attribute to be used on blank row(s)
C              ;          if v_mode = 7,  al = 20h = space
C              ;          else          al = v_3x8
C              ; Assume: (contents of v_base6845)+6 = status register
C              ; Traah:  bp, si, & di destroyed. (bx thru dx destroyed if ROM stack)
C              ;-----
F35B          C          v_scri_dn      proc  near
C              assume  cs:code, ds:data, es:v_ram, ss:nothing
F35D          C          std          ; NOTE: scroll down everything backwards
C              oall     v_txt_md      ; all registers preserved
F35F          C          jb      v_txt_dn
F361          C          jmp     grf_graphics_down      ; jump if graphics
F363          C          v_txt_dn:
F365          C          push     dx          ; save registers
F367          C          push     cx
F369          C          push     bx

```

# ROM BIOS Listing

```

F367 8A D6          C      mov     bl,al          ; save line count
F369 8B C2          C      mov     ax,dx          ; pass lower right coordinates...
F36B E8 F4DE R     C      call    v_scri_pos     ; to common scroll positioning routine
F36E 74 07          C      jz      v_clr_top     ; clear rows if nothing to move
C
C      ; Scroll cl rows down.
C
F370              C      v_mv_dn:
F370 2B F0          C      sub     si,ax          ; subtract (bytes/row)*(rows to scroll)
C
F372 F7 DD          C      neg     bp            ; negate number of bytes to skip per row
F374 E9 F295 R     C      jmp     v_mv          ; now identical to scroll up!
C
C      ; Clear bl rows above.
C
F377              C      v_clr_top:
F377 F7 DD          C      neg     bp            ; negate number of bytes to skip per row
F379 E9 F2F5 R     C      jmp     v_clr        ; now identical to v_clr_bot!
C
F37C              C      v_scri_dn  endp
C
C      ;-----
C      ; Read Attribute & Character at Cursor  ah = 08h
C      ;
C      ; Input:  bh = current active display page (0-7)
C      ; Output: al = character read
C      ;        ah = attribute of character read
C      ;
C      ; Assume: (contents of v_base6845)+6 = status register
C      ; Trash: si & di destroyed. (si = dx; di = bx)
C      ;-----
F37C              C      v_rac  proc  near
C
C      assume  cs:code, ds:data, es:v_ram, ss:nothing
C
C      call    v_txt_md   ; all registers preserved
C      jb     v_txt_rac   ; v_txt_rac
C      jmp     grf_graphics_read ; jump if graphics
C      v_txt_rac:
C
C      mov     di,bx      ; save bx
C      call    v_fpos     ; ax & si destroyed.
C                        ; bx = offset into current page
C
C      mov     si,dx      ; save dx
C      mov     dx,6       ; get 6845 status reg. offset
C      add     dx,word ptr ds:[v_base6845] ; add 6845 pointer
C
C      ; Wait for horizontal retrace... we can't read the screen during a trace
C      ; without disturbing the screen image.
C
F392              C      v_rac_inlne:
F392 EC          C      in     al,dx          ; make sure we're in a scanline
F393 D0 D8          C      rcr     al,1         ; get horiz. retrace blanking status
F395 72 FB          C      jc     v_rac_inlne  ; test for horiz. retrace
F397 FA          C      cld                    ; wait for display enable low (cf)
C                        ; disable ints FIRST
C
C                        ; wait for blanking:
C
F398              C      v_rac_inblank:
F398 EC          C      in     al,dx          ; get retrace blanking status
F399 D0 D8          C      rcr     al,1         ; test display enable (bit #0)
F39B 73 FB          C      jnc   v_rac_inblank ; try again if still in scanline.
C
F39D 26: 8B 07     C      mov     ax,es:[bx]    ; chr. and attr. now in AX
F3A0 FB          C      sti                    ; enable interrupts immediately
C
F3A1 8B D6          C      mov     dx,si         ; restore dx
F3A3 8B DF          C      mov     bx,di         ; restore bx
F3A5 C3          C      ret
C
F3A6              C      v_rac  endp
C
C      ;-----
C      ; Write Attribute & Character at Cursor  ah = 09h
C      ;
C      ; Input:  al = character to write
C      ;        bh = current active display page (0-7)
C      ;        bl = attribute of character to write
C      ;        cx = counter of characters to write
C      ;        bp = value to return in ax
C      ; Output: al = character to write
C      ;        ah = attribute of character to write
C      ;
C      ; Assume: (contents of v_base6845)+6 = status register
C      ; Trash: bp, si & di destroyed. (si = cx; dx if 80H stack)
C      ;-----
F3A6              C      v_wac  proc  near
C
C      assume  cs:code, ds:data, es:v_ram, ss:nothing
C
C      call    v_txt_md   ; all registers preserved
C      jb     v_txt_wac   ; v_txt_wac
C      jmp     grf_graphics_write ; jump if graphics
C      v_txt_wac:

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# ROM BIOS Listing

```

F3A E 8B FB      C      mov     di,bx                ; save bx
F3B0 E8 F50D R   C      call    v_fpos                ; ax & si destroyed.
F3B3 87 DF       C      xchg   bx,di                ; bx = offset into current page
F3B5 88 C5       C      mov     ax,bp                ; restore ax
F3B7 8A E3       C      mov     ah,bl                ; transfer attribute byte to ah
F3B9 8B E8       C      mov     bp,ax                ; save attribute & character in bp
F3BB 8B F1       C      mov     si,cx                ; save cx
F3BD 52           C      push   dx                    ; save dx
F3BE 8B 16 0063 R C      mov     dx,word ptr ds:[v_base6845] ; get 6845 pointer register
F3C2 83 C2 06     C      add     dx,6                  ; get 6845 status register
C      ; Wait for horizontal retrace blank interval ...
C      v_wac_hi:
F3C5           C      in     al,dx                ; wait till we're in a scanline..
F3C6 00 DB       C      rcr    al,1                  ; get CRT status
F3C8 72 FB       C      jc     v_wac_hi              ; test display enable (bit #0)
F3CA FA         C      cll                    ; wait for display enable low (cr)
C      ; disable ints FIRST
F3CB           C      v_wac_lo:
F3CB EC         C      in     al,dx                ; now wait till start of blanking..
F3CC D0 D8       C      rcr    al,1                  ; 08 get CRT status
F3CE 73 FB       C      jnc   v_wac_lo              ; 02 test display enable (bit #0)
C      ; 16/04 wait for display enable hi (cr)
F3D0 8B C5       C      mov     ax,bp                ; 02 restore ax
F3D2 AB         C      stosw                    ; 11 es:di gets ax (attribute & char)
F3D3 49          C      dec     cx                    ; 02
F3D4 74 04       C      jz     v_wac_end            ; 04/16
F3D6 AB         C      stosw                    ; 11 es:di gets ax (attribute & char)
C      ; Worst case: (8*2+16)+(8*2+4)+(2*11)+(2*4+11) = 70 cycles = 87.5% of 80 cycles
F3D7 FB         C      sti                    ; enable interrupts immediately
F3D8 E7 EB       C      loop   v_wac_hi             ; do it cx times
F3DA           C      v_wac_end:
F3DA FB         C      sti                    ; enable interrupts immediately
F3DB 5A         C      pop     dx                    ; restore dx
F3DC 8B CE       C      mov     cx,si                ; restore cx
F3DE C3         C      ret
F3DF           C      v_wac  endp
C      -----
C      ; Write Character at Cursor Position  ah = 0Ah
C      ; Input:  al = character to write
C      ;         bh = current active display page (0-7)
C      ;         cx = counter of characters to write
C      ;         bp = value to return in ax
C      ; Output: al = character to write
C      ;         ah = top byte of offset of character in page 0
C      ; Assume: (contents of v_base6845)+6 = status register
C      ; Trash: si & di destroyed. (si = cx; dx if ROM stack)
C      -----
F3DF           C      v_wc  proc  near
C      ; assume  cs:code, ds:data, es:v_ram, ss:nothing
F3DF E8 F53C R   C      call    v_txt_md            ; all registers preserved
F3E2 72 03       C      jb     v_txt_wc            ; v_txt_wc
F3E4 E9 DA59 R   C      jmp     grf_graphics_write ; jump if graphics
F3E7           C      v_txt_wc:
F3E7 8B FB       C      mov     di,bx                ; save bx
F3E9 E8 F50D R   C      call    v_fpos                ; si destroyed.
C      ; ax = offset into page 0
C      ; bx = offset into current page
C      ; restore bx; di = transfer offset
F3EC 87 DF       C      xchg   bx,di
F3EE 8B F1       C      mov     si,cx                ; save cx
F3F0 52           C      push   dx                    ; save dx
F3F1 8B D5       C      mov     dx,bp                ; retrieve character in di
F3F3 8A C2       C      mov     al,di                ; get char in al (ah = attr.)
F3F5 8B E8       C      mov     bp,ax                ; bp = (attr. char)
F3F7 BA 0006     C      mov     dx,6                  ; get 6845 status register
F3FA 03 16 0063 R C      mov     dx,word ptr ds:[v_base6845] ; get 6845 pointer register
C      ; Wait for horizontal retrace...
F3FE           C      v_wc_next:
F3FE           C      v_wc_hi:
F3FE EC         C      in     al,dx                ; get CRT status
F3FF 00 DB       C      rcr    al,1                  ; test display enable (bit #0)

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# ROM BIOS Listing

```

F401 72 FB      C      jc      v_wc_hi      ; wait for display enable low (cf)
F403 FA        C      di      ; disable inta FIRST
C
C
F404          C      v_wc_lo:
F404 EC        C      in      al,dx      ; 08 get CRT status
F405 D0 DB      C      rcr      al,1      ; 02 test display enable (bit #0)
F407 73 FB      C      jnc     v_wc_lo      ; 16/04 wait for display enable hi (cf)
C
C
F409 8B C5      C      mov     ax,bp      ; 02 restore ax = (attr, char)
F40B AA        C      stob   ; 11 es:di gets al (character)
C
C
F40C 49        C      dec     cx      ; 02
C
C
F40D 74 06      C      .list
F40F 47        C      js     v_wc_end      ; 08/16
C      inc     di      ; 02 skip past attribute byte
F410 AA        C      stob   ; 11 es:di gets al (character)
C
C      ; Worst case: (8+2+16)*(8+2+4)+(2+11)-(2+4+2+11) = 72 cycles = 90% of 80 cycles
C
F411 FB        C      sti      ; enable interrupts immediately
F412 47        C      inc     di      ; skip past attribute byte
F413 E2 E9      C      loop   v_wc_next    ; do it cx times
C
C
F415          C      v_wc_end:
F415 FB        C      sti      ; enable interrupts immediately
C
C
F416 5A        C      pop     dx      ; restore dx
F417 8B CE      C      mov     cx,si      ; restore cx
F419 C3        C      ret
C
C
F41A          C      v_wc     endp
C
C
C      ;-----
C      ; Set Overscan, Back, & Foreground Colors ah = 0Bh
C      ;-----
C      ; Input: bh = palette color ID to set (0-127)
C      ;        bl = color value to be used with that color ID
C      ; Output: ah = v_mode
C      ;         al = new v_colorpal
C      ;-----
C      ; Assume: (contents of v_base6845)*5 = overscan register
C      ;-----
C      ; Trash: si & di destroyed. (si = bx; di = dx)
C      ;-----
F41A          C      v_col   proc   near
C
C      assume cs:code, ds:data, es:v_ram, ss:nothing
C
F41A A0 0066 R   C      mov     al,byte ptr ds:[v_colorpal] ; get current palette
C
F41D 8B FA      C      mov     di,dx      ; save dx
F41F 8B F3      C      mov     si,bx      ; save bx
C
C
F421 0A FF      C      or      bh,bh      ; palette color ID = 0?
F423 74 0A      C      jz      v_col_0      ; handle color ID 0
C
C
F425 24 DF      C      and     al,0DFh     ; clear palette select bit #5
F427 D0 DB      C      rcr     bl,1      ; test new color (bit #0)
F429 73 0B      C      jnb     v_col_1      ; if bit #0 set, all done
F42B 0C 20      C      or      al,20h     ; else set palette select bit #5
F42D EB 07      C      jmp     short v_col_1
C
C
F42F          C      v_col_0:
F42F 80 E3 1F    C      and     bl,01Fh     ; save bits #0-4 of new color
F432 24 E0      C      and     al,020h     ; clear bits #0-4 of old color
F434 0A C3      C      or      al,bl      ; and combine the two.
C
C
F436          C      v_col_1:
F436 BA 0005     C      mov     dx,5        ; get 6845 overscan reg. offset
F439 03 16 0063 R C      add     dx,word ptr ds:[v_base6845] ; add 6845 pointer register
F43D EE        C      out     dx,al      ; output selection
C
C
F43E 8B DE      C      mov     bx,si      ; restore bx
F440 8B D7      C      mov     dx,di      ; restore dx
C
C
F442 A2 0066 R   C      mov     byte ptr ds:[v_colorpal],al ; save the value for later
F445 C3        C      ret
C
C
F446          C      v_col   endp
C
C
C      ;-----
C      ; Write Dot (see graph.src) ah = 0Ch
C      ;-----
C
C      ;-----
C      ; Read Dot (see graph.src) ah = 0Dh
C      ;-----
C
C      ;-----
C      ; Terminal Emulator to active page ah = 0Eh
C      ;-----
C      ; Input: al = character to write
C      ;        bl = foreground color in graphics mode
C      ;        bp = value to return in ax
C      ; Output: All registers saved.
C      ;-----
C      ; Trash: si & di destroyed. (si = cx; di = bx; dx if ROM stack)
C      ;-----

```

# ROM BIOS Listing

```

C
C v_terminal proc near
C
C assume cs:code, ds:data, es:v_ram, ss:nothing
C
F446 3C 07      C      cmp     al,BEL                ; is it bell character?
F448 75 03      C      jne     v_term_nobell
C
C
C      jmp     v_bell
C
F44D          C      v_term_nobell:
F44D 52          C      push  dx                ; save dx
F44E 8B F1      C      mov   si, cx              ; save cx
F450 8B FB      C      mov   di, bx              ; save bx
C
C ; Get cursor position in active page.
C
F452 87 07      C      mov   bh, 07h             ;mask for page number, MOD 8
F454 22 3E 0062 R C      and   bh, byte ptr ds:[v_apage] ; get active page number (0-7)
C
C
C      mov   ah, 03h          ; call v_r_curs_pos
F458 B4 03      C      INT   10h                ; (dh,dl) = (row,col) of cursor
F45A CD 10      C      ; (ch,cl) = cursor mode setting
C
C
C      mov   ax, bp           ; restore ax
F45C 8B C5      C      mov   cx, 1              ; character count for write char
F45E B9 0001    C      mov   ah, 0Ah            ; function code for write char
F461 B4 0A      C
C
C ; Handle special cases: dx has (row,col) of current cursor position.
C
C
C      cmp   al, LF          ; is it a line feed?
F463 3C 0A      C
C      je    v_if           ; is it a carriage return?
F465 74 14      C
C      cmp   al, CR          ; is it a carriage return?
F467 3C 0D      C
C      je    v_cr           ; is it a carriage return?
F469 74 60      C
C      cmp   al, BS          ; is it a backspace?
F46B 3C 08      C
C      je    v_bs           ; is it a backspace?
F46D 74 54      C
C
C ; Normal Case: write the character
C
C
C      INT   10h            ; to write the character
F46F CD 10      C
C
C      inc   dl              ; increment the column
F471 FE C2      C
C      cmp   dl, byte ptr ds:[v_width] ; column overflow?
F473 3A 16 004A R C
C      jb   v_set_new_cur    ; set new cursor position
F477 72 13      C
C
C      xor   dl, dl          ; carriage return cursor
F479 32 D2      C
C
C      v_if: cmp   byte ptr ds:[v_mode], 72 ; is this mode 72 ?
F47B 80 3E 0049 R 8B C
C      mov   ah, 49          ; mode 72 has 50 rows
F480 B4 31      C
C      mov   v_lrow, ah      ; mode 72 has 50 rows
F482 74 02      C
C      je    v_lrow         ; mode 4,5,6,64 have 25 rows
F484 B4 18      C
C      mov   ah, 24          ; are we at last row yet?
F486 3A F4      C
C      cmp   dh, ah          ; if yes, go scroll the screen
F488 74 07      C
C      je    v_scroll_tty   ; otherwise, inc to next row
F48A FE C6      C
C      inc   dh              ; otherwise, inc to next row
F48C 74 02      C
C      cmp   v_set_new_cur: ; call v_curs_pos to set new
F48E B4 02      C      mov   ah, 02h          ; cursor position
F490 8B C6      C      jmp   v_term_ret
C
C
C      v_scroll_tty: ; (dh,dl) = (row,col) = (24,0) or (49,0)
F491 B4 02      C      mov   ah, 02h          ; call v_curs_pos to set cursor
F493 CD 10      C      INT   10h            ; and so that we can read back
C
C ; the proper attribute byte
C
C
C      xor   ah, ah         ; ah = 0 for graphics
F495 32 E4      C
C      call  v_txt_md       ; are we text mode?
F497 E8 F53C R  C
C      jnb  v_scroll_tty_graphics ; jump if graphics
F49A 73 04      C
C
C      mov   ah, 08h        ; call v_rac
F49C B4 08      C
C      INT   10h            ; to get attribute byte in ah
F49E CD 10      C
C
C      v_scroll_tty_graphics:
F4A0          C
F4A0 33 C9      C      xor   cx, cx            ; (ch,cl) = upper left (row,col)
C
C ; = (0,0)
C
C      mov   bh, ah         ; store attribute in bh
F4A2 8A FC      C
C      mov   ax, 0601h      ; call v_scroll_up to scroll
F4A4 B8 0601    C
C
C ; one line with attribute bh
C
C      mov   dl, byte ptr ds:[v_width] ; (dh,dl) = lower right (row,col)
F4A7 8A 16 004A R C
C      sub   dl, 1          ; column = v_width-1
F4AB 80 EA 01    C
C      cmp   byte ptr ds:[v_mode], 72 ; is this mode 72 ?
F4AD 80 3E 0049 R 8B C
C      mov   dh, 49         ; is this mode 72 ?
F4AF 80 3E 0049 R 8B C
C      je    v_term_ret     ; if yes then row = 49
F4B1 86 31      C
C      mov   v_term_ret     ; jump if mode = 72
F4B3 B6 31      C
C      mov   dh, 24         ; if not mode 72 then row = 24
F4B5 74 02      C
C
C
C      v_term_ret:
F4B9          C
F4B9 CD 10      C      INT   10h
F4BB          C
C
C      v_term_nop:
F4BD          C
C
C ; Clean up.
C
C
C      mov   ax, bp         ; restore ax
F4BB 8B C5      C
C      mov   bx, di         ; restore bx
F4BD 8B DF      C
C      mov   cx, si         ; restore cx
F4BF 8B CE      C
C      pop   dx             ; restore dx
F4C1 5A          C
C      ret
F4C2 C3          C
C
C
C      v_bs: or    dl, dl          ; back space -- column = 0 ?
F4C3 0A D2      C
C      js   v_term_nop     ; don't change cursor position
F4C5 74 FA      C
C      dec  dl              ; don't change cursor position
F4C7 FE CA      C
C      jmp  v_set_new_cur  ; don't change cursor position
F4C9 EB C1      C

```







# ROM BIOS Listing

```

C
C
C      assume cs:code, ds:data, es:v_ram, ss:nothing
F53C 80 3E 0049 R 04      cmp     byte ptr ds:[v_model],4
F541 72 09                jb     v_txt_ok
C
C
C      cmp     byte ptr ds:[v_model],7
F543 80 3E 0049 R 07      je     v_txt_ok
F544 FB                cld
F54B C3                ret
C
C
C      v_txt_ok:
F54C                stc
F54C F9                ; graphics mode (CF = 0)
F54D C3                ret
C
C
C      v_txt_md      endp
C
C
C      -----
C      Handle BEL character: Beeps the speaker.
C
C      No parameters.
C
C      -----
F54E                v_bell proc near
C
C      assume cs:code, ds:data, es:v_ram, ss:nothing
C
C      push     ax
F54E 50
C
C      mov     al,t2end
F54F 80 86                ; p_8253_2, lsb 1st, mode 3,no BCD
F551 E6 43              out     p_8253_ctrl,al
C
C      mov     al,00h
F553 80 00                ; p_timer count
F555 E6 42              out     p_8253_2,al
C
C      mov     al,06h
F557 80 06                ; least significant byte
F559 E6 42              out     p_8253_2,al
C
C
C      in     al,p_ketrl
F55B E4 61              ; get control data
F55D 8A E0              mov     ah,al
C
C      or     al,03h
F55F 0C 03              ; save control status
F561 E6 61              out     p_ketrl,al
C
C
C      push     cx
F563 51
C
C      mov     cx,200
F564 B9 00C8            ;512 msec
C
C      bell_wait:
F567                call    F_wait_one_ms
F567 E8 EF47 R          ;wait for 1 ms
F56A E7 FB              loop   bell_wait
F56C 59                pop    cx
C
C
C      mov     al,ah
F56D 8A C4              ; restore control status
F56F E6 61              out     p_ketrl,al
C
C
C      pop     ax
F571 58
F572 C3                ; return from v_term
C
C
C      v_bell endp
F573
C
C      code ends
F573
C
C      include com3.asm
C
C
C      ;-----
C      ;
C      ;      Filename:      com3.asm
C      ;-----
F573                code segment public 'ROM'
C
C      assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C
C      ;-----
C      ;      INS8250 Asynchronous Communication Chip Baud Rate Time Constants
C      ;      (baud rate generator signal is 3.6864 MHz put through a
C      ;      divide-by-2 circuit).
C      ;
C      ;      Time Constant = ((3,686,400 Hz)/2) = Input Freq.
C      ;
C      ;      (16)*(baud rate)
C      ;-----
C
C
C      sec_init      proc near
C
C      assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C      mov     cb,al
F573 8A E8                ; save input parameters.
C
C
C      xor     al,al
F575 32 C0
C
C      out     dx,al
F577 EE                ; dummy read on sec_ctl_x
C
C      call    rs_dly
F578 EB E8E2 R          ; insures proper register addr.
C
C      in     al,dx
F57B EC
C
C      call    rs_dly
F57C E8 E8E2 R
C
C
C      mov     al,9
F57F BD 09              ; select write register #9
C
C      out     dx,al
F581 EE                ; reset and disable int
C
C      call    rs_dly
F582 EB E8E2 R
C
C      mov     al,11000001b
F585 B0 C1              ; hw reset, st=0, mledia, nval
C
C      out     dx,al
F587 EE
C
C      call    rs_dly
F588 EB E8E2 R
C
C
C      mov     al,4
F58B B0 04              ; select write register #4
F58D EE                ; transfer parameters

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# ROM BIOS Listing

```

F58E E8 E8E2 R      C      call    rs_dly
F591 B0 44          C      mov     al,01000100b      ; 16x, 8-bit synch, 1 or 2 stop
F593 8A E5          C      mov     ah,ch            ; get input parameters.
F595 80 E4 04       C      and    ah,00000100b     ; get bit #2
F598 D0 E4          C      shl    ah,1             ; move to bit #3
F59A 0A C4          C      or     al,ah            ; 'or' the bit
F59C 8A E5          C      mov     ah,ch            ; get input parameters.
F59E 80 E4 18       C      and    ah,00011000b     ; get bits #3 & 4
F5A1 B1 03          C      mov     cl,3             ;
F5A3 D2 EC          C      shr    ah,cl            ; move to bits #0 & 1
F5A5 0A C4          C      or     al,ah            ; 'or' the bits
F5A7 EE            C      out    dx,al            ;
F5A8 E8 E8E2 R      C      call    rs_dly          ; all done!!!
F5AB B0 0B          C      mov     al,11           ; select write register #11
F5AD EE            C      out    dx,al            ; clock mode control
F5AE E8 E8E2 R      C      call    rs_dly          ;
F5B1 B0 55          C      mov     al,01010101b     ; no x,rsbr,t=br,txc o,tx ck
F5B3 EE            C      out    dx,al            ;
F5B4 E8 E8E2 R      C      call    rs_dly          ;
F5B7 B0 0C          C      mov     al,12           ; select write register #12
F5B9 EE            C      out    dx,al            ; low byte of baud rate const
F5BA E8 E8E2 R      C      call    rs_dly          ;
F5BD 8A DD          C      mov     bl,ch            ; get input parameters.
F5BF B1 E3 00E0     C      and    bx,11100000b     ; get bits #5, 6, & 7 (clear bh)
F5C3 B1 04          C      mov     cl,4             ;
F5C5 D2 EB          C      shr    bl,cl            ; move to bits #1,2,& 3
; bx is word index
; NOTE: These values are the SAME as the com_baud EXCEPT for the - 21111
;
;      mov     ax,word ptr cs:[bx+sec_baud]      ; get 8530 baud count
F5C7 2E: 8B 87 E729 R  C      mov     ax,word ptr cs:[bx+com_baud]         ; get 8250 baud count
F5CC 48              C      dec     ax                ; and subtract 21111!
F5CD 48              C      dec     ax                ;
F5CE EE            C      out    dx,al            ; output low byte of baud rate
F5CF E8 E8E2 R      C      call    rs_dly          ;
F5D2 B0 0D          C      mov     al,13           ; select write register #13
F5D4 EE            C      out    dx,al            ; high byte of baud rate const
F5D5 E8 E8E2 R      C      call    rs_dly          ;
F5D8 8A C4          C      mov     al,ah            ; output high byte of baud rate
F5DA EE            C      out    dx,al            ;
F5DB E8 E8E2 R      C      call    rs_dly          ;
F5DE B0 0E          C      mov     al,14           ; select write register #14
F5E0 EE            C      out    dx,al            ; baud rate generator enable
F5E1 E8 E8E2 R      C      call    rs_dly          ;
F5E3 B0 03          C      mov     al,00000011b     ;
F5E5 EE            C      out    dx,al            ; baud generator enable & source
F5E7 E8 E8E2 R      C      call    rs_dly          ;
F5EA B0 01          C      mov     al,1             ; select write register #1
F5EC EE            C      out    dx,al            ; data xfer mode definition
F5ED E8 E8E2 R      C      call    rs_dly          ;
F5F0 32 C0          C      xor     al,al            ; rx dis, pty no spec, tx dis
F5F2 EE            C      out    dx,al            ; ext dis
F5F3 E8 E8E2 R      C      call    rs_dly          ;
F5F6 B0 03          C      mov     al,3             ; select write register #3
F5F8 EE            C      out    dx,al            ; RxD parameters and control
F5F9 E8 E8E2 R      C      call    rs_dly          ;
F5FC B0 01          C      mov     al,00000001b     ; RxD enable
F5FE 8A DD          C      mov     bl,ch            ; get input parameters.
F600 81 E3 0003     C      and    bx,00000011b     ; get bits #0 & 1 (clear bh)
F604 2E: 8A A7 F62E R  C      mov     ah,byte ptr cs:[bx+sec_dbit]
F609 B1 06          C      mov     cl,6             ;
F60B D2 E4          C      shl    ah,cl            ; move data bits to #6 & 7
F60D 0A C4          C      or     al,ah            ; 'or' the data bits
F60F EE            C      out    dx,al            ;
F610 E8 E8E2 R      C      call    rs_dly          ;
F613 B0 05          C      mov     al,5             ; select write register #5
F615 EE            C      out    dx,al            ; TxD parameters and control
F616 E8 E8E2 R      C      call    rs_dly          ;
F619 B0 08          C      mov     al,00001000b     ; TxD enabled. (power-up value)
F61B 95              C      xchg   ax,bp            ; get original function code
F61C 0A E4          C      or     ah,ah            ; is it 0 or FF?
F61E 95              C      xchg   ax,bp            ; restore AX
F61F 75 02          C      jnz    sec_pwrup        ; jump if original AH=0FFh
F621 B0 8A          C      mov     al,10001010b     ; TxD,DTR,RTS enabled. (normal)
F623                C      sec_pwrup:
F623 D0 EC          C      shr     ah,1             ; move bits #6 & 7 to #5 & 6
F625 0A C4          C      or     al,ah            ; 'or' the bits
F627 EE            C      out    dx,al            ;
F628 E8 E8E2 R      C      call    rs_dly

```

# ROM BIOS Listing

```

C
C
F62B E9 E88A R      C           jmp     sec_stat           ; return status
C
C
C -----
C ;           Z8530 Compatible Data-Bit Definitions for Mapping bits
C -----
C
F62E 00      C sec_dbit   db     00b   ;   5 data bits (0) (non- )
F62F 02      C           db     10b   ;   6 data bits (1) (non- )
F630 01      C           db     01b   ;   7 data bits (2)
F631 03      C           db     11b   ;   8 data bits (3)
C
F632          C sec_init   endp
C
F632          C code     ends
C
C include mem.asm
C
C ;-----
C ;           Filename:      mem.src
C ;
C ;           This module includes INT 12h, 11h, & 15h.
C ;-----
C
F632          C code     segment public 'ROM'
C           assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C -----
C ;           INT 12h -- memory size detect
C -----
C
F841          C           ORG     0F841h
F841          C m_size   proc   near
C           assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C           sti
C           push ds
C           mov  ax,data_seg
C           mov  ds,ax
C
C           assume cs:code, ds:data, es:nothing, ss:nothing
C
C           mov  ax,word ptr ds:[memory_size]
C           pop  ds
C           iret
C
F84D          C m_size   endp
C
C -----
C ;           INT 11h -- equipment check
C -----
C
F84D          C           ORG     0F84Dh
F84D          C m equip  proc   near
C           assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C           sti
C           push ds
C           mov  ax,data_seg
C           mov  ds,ax
C
C           assume cs:code, ds:data, es:nothing, ss:nothing
C
C           mov  ax,word ptr ds:[switch_bits]
C           pop  ds
C           iret
C
F859          C m equip  endp
C
C -----
C ;           INT 15h -- cassette I/O
C -----
C
F859          C           ORG     0F859h
F859          C m_cass   proc   near
C           assume cs:code, ds:nothing, es:nothing, ss:nothing
C
C           stc
C           mov  ah,86h
C           ret  2
C           iret
C
C m_cass   endp
C
F85F          C code     ends
F85F          C include nmi.asm
C
C ;-----
C ;           Filename:      nmi.src
C ;
C ;           This module includes INT 02h.
C ;-----
C

```

# ROM BIOS Listing

```

F85F      C code segment public 'ROM'
          C assume cs:code, ds:nothing, es:nothing, ss:nothing
          C ;
          C -----
          C INT 02h
          C -----
          C
F85F      C ORG OF85Fh
F85F      C n_int proc near
          C assume cs:code, ds:nothing, es:nothing, ss:nothing
          C ;
          C iret
F85F CF   C
F860      C n_int endp
F860      C code ends

C include boot2.asm
C ;
C ;-----
C ; Filename: boot.src
C ;
C ; This module includes INT 19h.
C ;
C ;-----
F860      C code segment public 'ROM'
          C assume cs:code, ds:nothing, es:nothing, ss:nothing
          C ;
          C INT 19h -- Cold boot routine:
          C ;
          C This code reads Track 0, Side 0, Sector 0 into memory at
          C 0000:7C00 and iret's into the secondary boot-strap loader
          C ;-----
          C Note: The stack looks like this at exit!!!!
          C ;
          C ;-----
          C ; High Address
          C ; |-----|
          C ; | return fsw flags | <-- sp (at entry & exit)
          C ; |-----|
          C ; | return cs segment |
          C ; |-----|
          C ; | return ip offset |
          C ; |-----| <-- sp after INT 19h trap
          C ; | saved si, bp |
          C ; |-----| <-- sp at loading of return address
          C ; Low Address
          C ;
          C ;
          C Output:
          C (DL) = Driver Number [ 00h -> Floppy Drive (A:);
          C 01h -> Floppy Drive (B:);
          C 80h -> Fixed Disk (C:). ]
          C ;
          C (DH) = Head Number [ These three parameters will
          C (CH) = Cylinder Number specify the booted partition
          C (CL) = Sector Number in the case of the fixed disk. ]
          C ;
          C (AH) = Successful status = 0.
          C (AL) = Number of Sectors read [in order to read 512 bytes. ]
          C ;
          C (ES:BX) = Address of the transfer [0000:7C00]
          C (SS:BX)
          C ;
          C (CS:IP) = Address of entry point [0000:7C00]
          C ;
          C (SS:SP) = Stack Segment and Pointer are left intact from the INT
          C 19h invocation for multi-tasking environments.
          C ;
          C (IF) = The interrupt enable flag is left intact from the INT
          C 19h invocation for multi-tasking environments.
          C ;
          C ;
          C ; Trash: bp destroyed. (si, di, & bp preserved.)
          C ;-----
F860      C bt_int proc near
          C assume cs:code, ds:nothing, es:nothing, ss:nothing
          C ;
          C F860 FB ati bp ; enable interrupts
          C F861 55 push bp ; save BP & SI
          C F862 56 push si
          C ;
          C assume ds:data ; reset master table ptr to ROM
          C mov ds,word ptr cs:[set_da_word] ; satisfy assumption
          C F863 CT 06 00B4 R E2CE R mov word ptr ds:[master_tbl_ptr-0000h],cs:[offset mastab]
          C F862 8C 0E 0086 R mov word ptr ds:[master_tbl_ptr-0002h],cs
          C ;
          C F872 BE DBB7 R mov si,cs:[offset bt_m] ; boot strap message
          C F875 E6 E5FA R call DROMString ; print banner
          C ;
          C F878 32 DB xor bi,bl ; disable error message blinking
          C F87A 53 push bx ; save blink status
          C ;
          C assume ds:abs0, es:abs0
          C bt_o:
          C F87B xor ax,ax ; boot strap outer loop
          C F87D 8E D8 mov ds,ax ; AX = abs0_seg.
          C F87F 8E C0 mov es,ax ; satisfy assumptions
          C

```

# ROM BIOS Listing

```

C ; Reset fd_parms table vector.
F881 C7 06 0078 R EFC7 R      mov     word ptr ds:[int1Elocn=0],cs:(offset fd_parms)
F887 8C 0E 007A R            mov     word ptr ds:[int1Elocn=2],cs
C ; Initialize retry loop.
F88B BD 0003                mov     bp,3 ; retry counter
F88E                        bt_1:    ; boot retry inner loop
C ; Initialize the driver.
F88E 33 C0                  xor     ax,ax ; AX = 0.
F890 8B DB                mov     bx,ax ; BX = 0.
F892 8B CB                mov     cx,ax ; CX = 0.
F894 8B D0                mov     dx,ax ; DX = 0.
F896 CD 13                INT     13h
F898 72 04                  jc     bt_next ; try again, if error
C ; Read the boot sector.
F89A B8 0201                mov     ax,0201h ; read one sector
F89D B7 7C                  mov     bh,7Ch ; bh = 0.
F89F 41                      inc     cx ; xfer address = ES:BX = 0:7C00
C ; ; cx = 0.
C ; ; track 0; sector 1
C ; ; dx = 0.
C ; ; head 0; drive 0
F8A4 06                      push    es ; save return registers
F8A1 CD 13                INT     13h ; BX,CX,DX,SI,DI,BP, & DS saved
F8A3 07                      pop     es ; restore return registers
C ;
F8A4                        bt_next:
F8A4 73 1E                  jnc     bt_ok ; jump if no error during read
C ;
F8A6 5B                      pop     bx ; get blink status
F8A7 0A DB                or      bl,bl ; have 3 retries been completed?
F8A9 74 0E                  jz     bt_dec ; jump if no
C ;
F8AB BE DBD1 R            mov     si,cs:(offset bt_merr) ; blink error message on
F8AE 78 03                js     bt_blink ; blink state from BL above
F8B0 BE DBF5 R            mov     si,cs:(offset bt_spaces) ; blink error message off
C ;
F8B3                        bt_blink:
F8B3 E8 E5FA R            call   DRomString ; blink error message
F8B6 80 F3 80            xor     bl,10000000b ; toggle blink state
C ;
F8B9                        bt_dec:
F8B9 53                      push    bx ; resave blink status
F8BA 4D                      dec     bp ; decrement retry count
F8BB 75 D1                  jnz    bt_1 ; and, try again
C ;
F8BD 5B                      pop     bx ; get blink status
F8BE 80 CB 01            or      bl,1 ; enable error message blinking
F8C1 53                      push    bx ; save new status
C ;
F8C2 EB B7                  jmp     bt_o ; and try again, for now.
C ;
F8C4                        bt_ok:
F8C4 BE DBF5 R            mov     si,cs:(offset bt_spaces) ; blink error message off
F8C7 E8 E5FA R            call   DRomString
F8CA 5E                      pop     si ; discard blink status
F8CB 5E                      pop     si ; restore SI
F8CC 8B EC                mov     bp,sp
F8CE 89 E2 02            mov     word ptr es:[bp+2],bx ; return IP = BX = 7C00h
F8D1 8C A6 04            mov     word ptr es:[bp+4],es ; return CS = ES = 0000h
F8D4 5D                      pop     bp ; restore BP
F8D5 CF                      iret ; return flags
C ;
F8D6                        bt_int endp
C ;
F8D6                        code ends
C ; include calendar.asm
C ;
C ; =====
C ; ; Filename: cal.src
C ; ;
C ; ; This module includes c_read and c_write of INT 1Ah.
C ; ;
C ; =====
F8D6                        code segment public 'ROM'
C ; ; assume cs:code, ds:nothing, es:nothing, ss:nothing
F8D6                        c_data1 proc
C ; ; Days per year.
C ;
F8DE 0000                c_dy_yr dw (0*366)+(0*365) ; year 0 = leap year + 0
F8E0 015E                dw (1*366)+(0*365) ; year 1 = leap year + 1
F8E4 02DB                dw (1*366)+(1*365) ; year 2 = leap year + 2
F8E8 0448                dw (1*366)+(2*365) ; year 3 = leap year + 3
F8EC 05B5                dw (1*366)+(3*365) ; year 4 = leap year + 0
F8F0 0723                dw (2*366)+(3*365) ; year 5 = leap year + 1
F8F4 0890                dw (2*366)+(4*365) ; year 6 = leap year + 2
F8F8 09FD                dw (2*366)+(5*365) ; year 7 = leap year + 3
C ; ; Days per month.

```

# ROM BIOS Listing

```

F8E6 1F      C  c_dy_mo db 31          ; month 0 = Jan
F8E7 1C      C          db 28          ; month 1 = Feb
F8E8 1F      C          db 31          ; month 2 = Mar
F8E9 1E      C          db 30          ; month 3 = Apr
F8EA 1F      C          db 31          ; month 4 = May
F8EB 1E      C          db 30          ; month 5 = Jun
F8EC 1F      C          db 31          ; month 6 = Jul
F8ED 1F      C          db 31          ; month 7 = Aug
F8EE 1E      C          db 30          ; month 8 = Sep
F8EF 1F      C          db 31          ; month 9 = Oct
F8F0 1E      C          db 30          ; month A = Nov
F8F1 1F      C          db 31          ; month B = Dec

F8F2                C  c_data1 endp
C
C ;=====
C ; Read or Write Clock Calendar Device (c_read)
C ;
C ;
C ; Input: ah = -1 Write Clock Calendar Device, then:
C ;         bx = day (from 1-1 of leap year up to 12-31 of leap year+7)
C ;         cx = (0-2921) = (0-869h)
C ;         ch = hour (0-23)
C ;         cl = minutes (0-59)
C ; Output: ah = -1 implies date/time error
C ;         ah = 0 implies date/time OK
C ;
C ; Input: ah = -2 Read Clock Calendar Device, then:
C ; Output: bx = day (from 1-1 of leap year up to 12-31 of leap year+7)
C ;         ch = hour
C ;         cl = minutes
C ;         dh = seconds
C ;         dl = hundredths of seconds
C ;
C ; Trash: None.
C ;=====
F8F2                C  c_read proc near
C ; assume cs:code, ds:nothing, es:nothing, as:nothing
C ; Save registers.
C ;
F8F2 50                C          push ax
C ; Years.
C ;
F8F3 BA 007F          C          mov dx,7Fh          ; interrupts (years mod 8)
F8F6 EC              C          in al,dx
F8F7 EC              C          in al,dx
F8F8 E8 F945 R        C          call c_rBCD          ; al = years
F8FB 8A EB            C          mov ch,al          ; ch = saves year mod 8
C ; Months.
C ;
F8FD B2 7C            C          mov d1,07Ch          ; d1 = tens of months port = 7Ch
F8FF E8 F958 R        C          call c_rhex          ; Input: d1 = tens of months port = 7Ch
C ; Output: ax = hex of months (1-12)
C ;         dx = day of week port = 7Ah
C ;         ax = map month (1-12) to month (0-11)
F902 48              C          dec ax
F903 8B D8            C          mov bx,ax          ; bx = saves month (0-11)
C ; Days.
C ;
F905 4A              C          dec dx
F906 E8 F958 R        C          call c_rhex          ; Input: dx = tens of days port = 79h
C ; Output: ax = hex of days (1-7)
C ;         dx = tens of hours port = 77h
C ;         ax = map days (1-7) to days (0-7)
F909 48              C          dec ax
C ; Calculate Day (ax has day).
C ;
F90A 8B D0            C          mov dx,ax          ; dx = day
C ; Calculate Month (bx has month).
C ;
F90C 4B              C          dec bx
F90D 78 08            C          js c_rm0          ; jump if it was zero
F90F                C  c_rmlp:
F90F E8 F9FD R        C          call c_gdays          ; get days per month
F912 03 D0            C          add dx,ax
F914 4B              C          dec bx
F915 79 F8            C          jns c_rmlp          ; previous month
F917                C  c_rm0:
C ; zero case
C ; dx = day + month
C ; Calculate Year (ch has month).
C ;
F917 33 DB            C          xor bx,bx          ; clear bh
F919 8A DD            C          mov bl,ch          ; get year mod 8
F91B D1 E3            C          shl bx,1          ; make word index
F91D 2E 03 97 F8D6 R  C          add dx,word ptr cs:[bx+c_dy_yr]
F922 8B DA            C          mov bx,dx          ; bx = day + month + year
C ; Hours.
C ;
F924 B2 77            C          mov d1,077h          ; d1 = tens of hours port = 77h

```

# ROM BIOS Listing

```

F926 E8 F958 R      C      call   c_rhex          ; Input:  dl = tens of hours port = 77h
C                      ; Output: ax = hexadecimal of hours
C                      ;          dx = tens of min.s port = 75h
C                      ;          ch = hours
F929 8A E8          C      mov    ch,al
C
C      ; Minutes.
C                      ; dl = tens of minutes port = 75h
F92B EB F958 R      C      call   c_rhex          ; Input:  dl = tens of min.s port = 75h
C                      ; Output: ax = hexadecimal of minutes
C                      ;          dx = tens of sec.s port = 73h
F92E 8A C8          C      mov    cl,al
C                      ; cl = minutes
C
C      ; Seconds.
C                      ; dl = tens of seconds port = 73h
F930 E8 F958 R      C      call   c_rhex          ; Input:  dl = tens of sec.s port = 73h
C                      ; Output: ax = hexadecimal of seconds
C                      ;          dx = tenths of secs port = 71h
F933 8A F0          C      mov    dh,al
C                      ; dh = seconds
F935 52              C      push   dx
C                      ; save seconds (dh)
C
C      ; Hundredths of Seconds.
C                      ; dl = tenths of seconds port = 71h
F936 EB F945 R      C      call   c_rBCD         ; dl = tenths of seconds
F939 8A E0          C      mov    ah,al         ; ah = tenths of seconds
F93B 32 C0          C      xor    al,al         ; move tenths of seconds to high byte
F93D E8 F962 R      C      call   c_BCD2hex      ; ax = BCD of hundredths of seconds
C                      ; ax = hex of hundredths of seconds
F940 5A              C      pop    dx
C                      ; restore seconds (dh)
F941 8A D0          C      mov    dl,al
C                      ; dl = hex of hundredths of seconds
C
C      ; Restore registers.
C
F943 58              C      pop    ax
F944 C3              C      ret
C
F945 51              C      c_rBCD: push   cx      ; save cx
F946 B9 0003        C      mov    cx,3          ; try 3 times only!!!
F949 32 F6          C      xor    dh,dh        ; clear dh
C
F94B EC            C      c_rB1p: in    al,dx      ; get the byte
F94C 24 0F          C      and    al,'h        ; clear high nibble
F94E 3C 0A          C      cmp    al,0          ; is it less than 10?
F950 72 04          C      jb    c_rBret       ; if so, return
C
F952 E2 F7          C      loop  c_rB1p       ; else, try again
F954 B0 01          C      mov    al,1        ; if timeout, return one.
C
F956              C      c_rBret:
F956 59              C      pop    cx           ; restore cx
F957 C3              C      ret
C
F958              C      c_read  endp
C
C      -----
C      ;
C      ; Convert to Hex (c_rhex)
C      ;
C      ; Inputs both BCD bytes and converts to hexadecimal word.
C      ;
C      ; Input:  dl = pointer to tens of whatever port
C      ; Output: ax = hexadecimal word (ah = 0)
C      ;          dx = pointer to tens of previous port (dh = 0)
C      ;
C      ; Trash: None.
C      ;
C      -----
F958              C      c_rhex  proc  near
C                      assume  cs:code, ds:nothing, es:nothing, ss:nothing
C
F958 EB F945 R      C      call   c_rBCD         ; in from tens of whatever
F95B 8A E0          C      mov    ah,al         ; move tens of whatever to high byte
F95D 74 A          C      dec    dx            ; dx points to units of whatever port
F95E E8 F945 R      C      call   c_rBCD         ; in from units of whatever
F961 74 A          C      dec    dx            ; dx points to tens of previous port
C
C      ; jmp    short c_BCD2hex      ; fall through
F962              C      c_rhex  endp
C
C      -----
C      ;
C      ; BCD to Hexadecimal (c_BCD2hex)
C      ;
C      ; Input:  ah = high BCD digit
C      ;          al = low BCD digit
C      ; Output: ax = hexadecimal byte (ah = 0)
C      ;          dh = 0
C      ;
C      ; Trash: None.
C      ;
C      -----
F962              C      c_BCD2hex  proc  near
C                      assume  cs:code, ds:nothing, es:nothing, ss:nothing
C
F962 8A F4          C      mov    dh,ah        ; dh = hi BCD digit
F964 D0 E6          C      shl    dh,1          ; dh = 2*(hi BCD digit)
F966 D0 E6          C      shl    dh,1          ; dh = 4*(hi BCD digit)
F968 02 F4          C      add    dh,ah        ; dh = 5*(hi BCD digit)
F96A D0 E6          C      shl    dh,1          ; dh = 10*(hi BCD digit)

```



# ROM BIOS Listing

```

F96C 02 C6          C      add     al,dh          ; al = 10*(hi BCD digit)+(low BCD digit)
F96E 32 BA          C      xor     ah,ah          ; ax = 10*(hi BCD digit)+(low BCD digit)
F970 32 F6          C      xor     dh,dh          ; dh = 0
F972 C3              C      ret
F973              C      o_BCD2hex      endp
-----
; Write Clock Calendar Device (c_write)
; Input: ah = -1
;        bx = day (from 1-1 of leap year up to 12-31 of leap year+7)
;        cx = (0-2921) = (0-869h)
;        dx = hour (0-23)
;        dx = hour (0-23)
;        cx = minutes (0-59)
; Output: ah = -1 implies date/time error
;        ah = 0 implies date/time OK
; Trash: None.
-----
F973              C      o_write proc   near
; assume cs:code, ds:nothing, es:nothing, as:nothing
; Check for errors.
C      cmp     cl,60          ; cl = minutes (0-59)
C      jae    c_werr        ;
C      cmp     ch,24        ; ch = hour (0-23)
C      jae    c_werr        ;
C      cmp     bx,(2*366)+(6*365) ; bx = day from leap year mod 8
C      jae    c_werr        ; = (0-2921) = (0-0B69h)
; Save registers.
C      push  ax
C      push  bx
C      push  cx
C      push  dx
; Initialize and Stop Clock.
C      xor   ax,ax          ; ax = 0
C      out  70h,al         ; test only port = out of test mode
C      out  7Eh,al         ; stop/start port = stop clock
; Minutes.
C      mov  d1,07Ah        ; d1 = units of minutes port = 7Ah
C      mov  al,cl          ; al = minutes (0-59)
C      call c_whex        ; Input: al = hexadecimal of minutes
C      ; Output: ax = trash
C      ; dx = units of hours port = 76h
; Hours.
C      mov  al,ch          ; d1 = units of hours port = 76h
C      call c_whex        ; Input: al = hexadecimal of hours
C      ; Output: ax = trash
C      ; dx = units of days port = 78h
; Calculate Year.
C      mov  dx,bx          ; dx = day from leap year mod 8
C      mov  bx,(8*2)      ; word index of year
C      o_wy1p:
C      dec  bx
C      dec  bx
C      cmp  dx,word ptr cs:[bx+c_dy_yr]
C      jb  c_wy1p
C      sub  dx,word ptr cs:[bx+c_dy_yr] ; dx = saves day of year
C      shr  bx,1          ; bl = year mod 8
C      mov  ch,bl        ; ch = saves year mod 8
; Calculate Days & Months.
C      mov  bx,-1         ; start at January
C      o_wm1p:
C      inc  bx            ; next month
C      call c_gdays      ; get days per month
C      sub  dx,ax
C      jae  c_wm1p
C      ; bx = month (0-11)
C      add  ax,dx         ; ax = day (0-7)
; Days.
C      mov  d1,078h       ; d1 = units of days port = 78h
C      inc  ax            ; al = map days (0-7) to days (1-7)
C      call c_whex        ; Input: al = hexadecimal of days
C      ; Output: ax = trash
C      ; dx = day of week port = 7Ah
; Months.
C      inc  dx            ; d1 = units of months port = 78h
C      mov  ax,bx         ; al = month (0-11)
C      inc  ax            ; al = map month (0-11) to month (1-12)
C      ; Input: al = hexadecimal of months
C      call c_whex        ; Output: d1 = units of mon.a port = 78h

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# ROM BIOS Listing

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; Output: ax = trash
;          dx = leap year port = 7Dh
; Leap Years.
C
C
F9C4 80 08 C      mov     al,08h
F9CC 8A CD C      mov     cl,ch
F9CE 80 E1 03 C     and     cl,03h
F9D1 D2 E8 C     shr     al,cl
F9D3 E2 C      out     dx,al
C
C
; Years.
C
F9D4 42 C      inc     dx
F9D5 42 C      inc     dx
F9D6 8A C5 C     mov     al,ch
F9D8 0C 08 C     or      al,08h
F9DA EE C      out     dx,al
F9DB 90 C      nop
F9DC EC C      in     al,dx
F9DD 90 C      nop
F9DE EC C      in     al,dx
F9DF 90 C      nop
F9E0 EC C      in     al,dx
C
C
; Start Clock.
C
F9E1 80 FF C     mov     al,0FFh
F9E3 44 C      dec     dx
F9E4 EE C      out     dx,al
; al = 0FFh
; dx = stop/start = 7Eh
; start clock
C
C
; Restore registers.
C
F9E5 5A C      pop     dx
F9E6 59 C      pop     cx
F9E7 5B C      pop     bx
F9E8 58 C      pop     ax
F9E9 32 E4 C     xor     ah,ah
; ah = 0 no error
C
F9EB C      e_werr: ret
; ah = -1 error
F9EC C      e_write endp
C
C
-----
; Converts hexadecimal byte to BCD and outputs both bytes. (c_whex)
;
; Input:  al = hexadecimal byte
;         dl = pointer to units of whatever port
; Output: dx = pointer to units of next port (dh = 0)
;
; Trash:  ax destroyed.
-----
F9EC C      c_whex proc near
C          assume cs:code, ds:nothing, es:nothing, as:nothing
C
C          xor     ah,ah
; ax = hexadecimal byte
C          mov     dh,10
; dh = divisor
C          div     dh
; ah = remainder = low BCD digit (0-9)
; al = quotient = high BCD digit
C          xchg    al,ah
; ah = quotient = high BCD digit
; al = remainder = low BCD digit (0-9)
C
C          xor     dh,dh
; dx points to units of whatever port
C          out     dx,al
; out to units of whatever
C          mov     al,ah
; move tens of whatever to low byte
C          inc     dx
; dx points to tens of whatever port
C          out     dx,al
; out to tens of whatever
C          inc     dx
; dx points to units of next port
C          ret
C
F9FD C      c_whex endp
C
C
-----
; Get Days per Month. (c_gdays)
;
; This routine calculates the number of days
; per month based on the year without checking validity of month.
;
; Input:  bx = month (assumes bx < 12)
;         ch = year
; Output: ax = days in month, if month valid; else garbage
;
; Trash:  None.
-----
F9FD C      c_gdays proc near
C          assume cs:code, ds:nothing, es:nothing, as:nothing
C
C          xor     ax,ax
; clear ah
C          mov     al,es:[bx+c_dy_mo]
C
C          cmp     bl,1
; is is February?
C          jnz     c_gret
; if not February, return
C
C          test    ah,03h
; if year = 0 mod 4, leap year
C          jnz     c_gret
; if not leap year, ax = 28th, so return
C
C          inc     ax
; load ax with February 29th

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# ROM BIOS Listing

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FA0F C3          C c_gret: ret
FA10           C c_gdays endp
FA10           C code ends
FA10           C -----
FA10           C ; ORG'd Font Tables
FA10           C -----
FA10           C code segment public 'ROM'
FA10           C assume cs:code, ds:nothing, es:nothing, ss:nothing
FA10           C
FA10           C ORG OFA6Eh
FA10           C font_lo_8x8 label byte
FA10           C include fontlo8.asm
FA10           C
FA10           C fontlo8 proc near ; System Font Table for M24
FA10           C
FA10           C DB 00h,00h,00h,00h
FA10           C DB 00h,00h,00h,00h ; 0
FA10           C DB 07eh,081h,0e5h,081h ; 1
FA10           C DB 0bdh,099h,081h,07eh ; 2
FA10           C DB 07eh,07fh,0d0h,07fh ; 3
FA10           C DB 0c3h,0e7h,07fh,07eh ; 4
FA10           C DB 03eh,07fh,07fh,07fh ; 5
FA10           C DB 03eh,01ch,08h,00h ; 6
FA10           C DB 08h,01ch,03eh,07fh ; 7
FA10           C DB 03eh,01ch,08h,00h ; 8
FA10           C DB 018h,03ch,0e7h,0e7h ; 9
FA10           C DB 066h,018h,018h,03ch ; a
FA10           C DB 018h,03ch,07eh,07fh ; b
FA10           C DB 07fh,07eh,018h,03ch ; c
FA10           C DB 00h,00h,018h,03ch ; d
FA10           C DB 03ch,018h,00h,00h ; e
FA10           C DB 07fh,07fh,0e7h,0c3h ; f
FA10           C DB 0c3h,0e7h,07fh,07fh ; 10
FA10           C DB 00h,03ch,0e2h,0e2h ; 11
FA10           C DB 042h,024h,03ch,00h ; 12
FA10           C DB 07fh,0c3h,099h,0bdh ; a
FA10           C DB 0bdh,099h,0c3h,07fh ; b
FA10           C DB 01fh,07h,0e7h,019h ; c
FA10           C DB 078h,0e7h,0e7h,078h ; d
FA10           C DB 03ch,066h,066h,03ch ; e
FA10           C DB 018h,07eh,018h,018h ; f
FA10           C DB 018h,014h,012h,012h ; 10
FA10           C DB 014h,070h,070h,060h ; a
FA10           C DB 01fh,011h,01fh,011h ; b
FA10           C DB 013h,037h,072h,020h ; c
FA10           C DB 018h,04bh,03ch,0e7h ; d
FA10           C DB 03ch,0e7h,018h,00h ; e
FA10           C DB 040h,070h,07ch,07fh ; f
FA10           C DB 07ch,070h,040h,00h ; 10
FA10           C DB 01h,07h,01fh,07fh ; a
FA10           C DB 01fh,07h,01h,00h ; b
FA10           C DB 018h,03ch,07eh,018h ; c
FA10           C DB 018h,07eh,03ch,018h ; d
FA10           C DB 00h,033h,033h,033h ; e
FA10           C DB 033h,00h,033h,00h ; f
FA10           C DB 07fh,04bh,0e7h,07bh ; 13
FA10           C DB 01bh,01bh,01bh,00h ; a
FA10           C DB 03eh,061h,03ch,066h ; b
FA10           C DB 066h,03ch,086h,07ch ; c
FA10           C DB 00h,00h,00h,00h ; d
FA10           C DB 07eh,07eh,07eh,00h ; e
FA10           C DB 018h,03ch,07eh,018h ; f
FA10           C DB 07eh,03ch,018h,07eh ; 17
FA10           C DB 018h,03ch,07eh,018h ; a
FA10           C DB 018h,018h,018h,018h ; b
FA10           C DB 018h,018h,018h,018h ; c
FA10           C DB 018h,07eh,03ch,018h ; d
FA10           C DB 0ch,0e7h,07fh,06h ; e
FA10           C DB 0ch,00h,00h,00h ; f
FA10           C DB 018h,030h,07fh,030h ; 1a
FA10           C DB 018h,00h,00h,00h ; 1b
FA10           C DB 00h,00h,060h,060h ; 1c
FA10           C DB 060h,07fh,07fh,00h ; 1d
FA10           C DB 00h,024h,066h,07fh ; 1e
FA10           C DB 066h,024h,00h,00h ; 1f
FA10           C DB 00h,00h,018h,03ch ; 20
FA10           C DB 07eh,07fh,00h,00h ; 21
FA10           C DB 00h,07fh,07eh,03ch ; 22
FA10           C DB 018h,00h,00h,00h ; 23
FA10           C DB 00h,00h,00h,00h ; 24
FA10           C DB 00h,00h,00h,00h ; 25
FA10           C DB 00h,00h,00h,00h ; 26
FA10           C DB 018h,018h,030h,00h ; 27
FA10           C DB 00h,00h,00h,00h ; 28
FA10           C DB 0ch,018h,030h,030h ; 29
FA10           C DB 030h,030h,018h,0ch ; 2a

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# ROM BIOS Listing

FB86	30 18 0C 0C	C	DB 030h,018h,0eh,0eh	;' 29
FB8A	0C 0C 18 30	C	DB 0eh,0eh,018h,030h	;' 29
FB8E	00 66 3C FF	C	DB 00h,066h,03eh,07fh	;' 2a
FB92	3C 48 30 00	C	DB 03h,066h,00h,00h	;' 2a
FB96	00 18 18 7E	C	DB 00h,018h,018h,07eh	;' 2a
FB9A	18 18 00 00	C	DB 018h,018h,00h,00h	;' 2a
FB9E	00 00 00 00	C	DB 00h,00h,00h,00h	;' 2a
FB02	00 18 18 30	C	DB 00h,018h,018h,030h	;' 2e
FB06	00 00 0E 7E	C	DB 00h,00h,00h,07eh	;' 2d
FB0A	00 00 00 00	C	DB 00h,00h,00h,00h	;' 2d
FB0E	00 00 00 00	C	DB 00h,00h,00h,00h	;' 2d
FB12	00 18 18 00	C	DB 00h,018h,018h,00h	;' 2e
FB16	03 06 0C 18	C	DB 03h,06h,0eh,018h	;' 2e
FB1A	30 60 40 00	C	DB 030h,060h,040h,00h	;' 2f
FB1E	3E 63 67 6F	C	DB 03eh,063h,067h,06fh	;' 30
FB22	7B 73 3E 00	C	DB 07bh,073h,03eh,00h	;' 30
FB26	0C 1C 0C 0C	C	DB 0eh,01eh,0eh,0eh	;' 31
FB2A	0C 0C 3F 00	C	DB 0eh,0eh,03fh,00h	;' 31
FB2E	1F 33 03 0E	C	DB 01fh,033h,03h,0eh	;' 31
FC02	18 33 3F 00	C	DB 018h,033h,03fh,00h	;' 32
FC06	1E 33 03 0E	C	DB 01eh,033h,03h,0eh	;' 32
FC0A	03 33 1E 00	C	DB 03h,033h,01eh,00h	;' 33
FC0E	0E 1E 3E 66	C	DB 0eh,01eh,03eh,066h	;' 33
FC12	7F 06 0F 00	C	DB 07fh,06h,07h,00h	;' 34
FC16	3F 30 3E 03	C	DB 03fh,030h,03eh,03h	;' 34
FC1A	03 33 1E 00	C	DB 03h,033h,01eh,00h	;' 35
FC1E	0E 1E 3E 7E	C	DB 0eh,01eh,03eh,07eh	;' 35
FC22	33 33 1E 00	C	DB 033h,033h,01eh,00h	;' 36
FC26	3F 33 03 0E	C	DB 03fh,033h,03h,0eh	;' 36
FC2A	0C 0C 0C 00	C	DB 0eh,0eh,0eh,00h	;' 37
FC2E	1E 33 33 1E	C	DB 01eh,033h,033h,01eh	;' 37
FC32	33 33 1E 00	C	DB 033h,033h,01eh,00h	;' 38
FC36	1E 33 31 1F	C	DB 01eh,033h,031h,01fh	;' 38
FC3A	03 06 1C 00	C	DB 03h,06h,01eh,00h	;' 39
FC3E	00 18 3E 00	C	DB 00h,018h,018h,00h	;' 3a
FC42	00 18 18 00	C	DB 00h,018h,018h,00h	;' 3a
FC46	00 18 18 00	C	DB 00h,018h,018h,00h	;' 3a
FC4A	00 18 18 30	C	DB 00h,018h,018h,030h	;' 3b
FC4E	06 0C 1E 30	C	DB 06h,0eh,01eh,030h	;' 3c
FC52	1B 0C 06 00	C	DB 018h,0eh,06h,00h	;' 3c
FC56	00 00 7E 00	C	DB 00h,00h,07eh,00h	;' 3d
FC5A	00 7E 00 00	C	DB 00h,07eh,00h,00h	;' 3d
FC5E	30 18 0C 06	C	DB 030h,018h,0eh,06h	;' 3e
FC62	0C 18 3E 00	C	DB 0eh,018h,030h,00h	;' 3e
FC66	3E 63 03 0E	C	DB 03eh,063h,03h,0eh	;' 3f
FC6A	0C 0C 0C 00	C	DB 0eh,0eh,0eh,00h	;' 3f
FC6E	3E 63 6F 6F	C	DB 03eh,063h,06fh,06fh	;' 40
FC72	6E 60 3E 00	C	DB 06eh,060h,03eh,00h	;' 40
FC76	0B 1C 3E 63	C	DB 0bh,01eh,03eh,063h	;' 41
FC7A	7F 63 63 00	C	DB 07fh,063h,063h,00h	;' 41
FC7E	7E 33 33 3E	C	DB 07eh,033h,033h,03eh	;' 42
FC82	33 33 7E 00	C	DB 033h,033h,07eh,00h	;' 42
FC86	1E 33 60 00	C	DB 01eh,033h,060h,00h	;' 43
FC8A	61 33 1E 00	C	DB 061h,033h,01eh,00h	;' 43
FC8E	7C 3E 33 33	C	DB 07eh,03eh,033h,033h	;' 43
FC92	33 3E 7C 00	C	DB 033h,03eh,07eh,00h	;' 43
FC96	7F 31 3A 3C	C	DB 07fh,031h,03ah,03eh	;' 45
FC9A	3A 31 7F 00	C	DB 03ah,031h,07fh,00h	;' 45
FC9E	7F 31 3A 3C	C	DB 07fh,031h,03ah,03eh	;' 46
FC0A	3A 30 78 00	C	DB 03ah,030h,078h,00h	;' 46
FC0E	1E 33 60 60	C	DB 01eh,033h,060h,060h	;' 47
FC1A	67 33 1B 00	C	DB 067h,033h,01bh,00h	;' 47
FC1E	63 63 63 7F	C	DB 063h,063h,063h,07fh	;' 48
FC22	63 63 63 00	C	DB 063h,063h,063h,00h	;' 48
FC26	3C 18 18 18	C	DB 03eh,018h,018h,018h	;' 49
FC2A	18 18 3C 00	C	DB 018h,018h,03eh,00h	;' 49
FC2E	0F 06 06 06	C	DB 0fh,06h,06h,06h	;' 4a
FC32	66 66 3C 00	C	DB 066h,066h,03eh,00h	;' 4a
FC36	73 36 3C 3E	C	DB 073h,036h,03eh,03eh	;' 4b
FC3A	3C 36 73 00	C	DB 03eh,036h,073h,00h	;' 4b
FC3E	7E 30 30 30	C	DB 07eh,030h,030h,030h	;' 4c
FC42	30 33 7F 00	C	DB 030h,033h,07fh,00h	;' 4c
FC46	63 77 7F 6B	C	DB 063h,077h,07fh,06bh	;' 4d
FC4A	63 63 63 00	C	DB 063h,063h,063h,00h	;' 4d
FC4E	63 73 7B 6F	C	DB 063h,073h,07bh,06fh	;' 4e
FC52	67 63 63 00	C	DB 067h,063h,063h,00h	;' 4e
FC56	1C 36 63 63	C	DB 01eh,03eh,063h,063h	;' 4f
FC5A	63 36 1C 00	C	DB 063h,03eh,01eh,00h	;' 4f
FC5E	7E 33 33 3E	C	DB 07eh,033h,033h,03eh	;' 50
FC62	30 30 7E 00	C	DB 030h,030h,07eh,00h	;' 50
FC66	1C 36 63 63	C	DB 01eh,03eh,063h,063h	;' 51
FC6A	63 36 1C 07	C	DB 063h,03eh,01eh,07h	;' 51
FC6E	7E 33 33 3E	C	DB 07eh,033h,033h,03eh	;' 52
FC72	36 33 33 00	C	DB 03eh,033h,033h,00h	;' 52
FD06	3E 63 30 18	C	DB 03eh,063h,030h,018h	;' 53
FD0A	06 63 3E 00	C	DB 06h,063h,03eh,00h	;' 53
FD0E	7E 5A 18 18	C	DB 07eh,05ah,018h,018h	;' 54
FD12	18 18 3C 00	C	DB 018h,018h,03eh,00h	;' 54
FD16	63 63 63 63	C	DB 063h,063h,063h,063h	;' 55
FD1A	63 63 3E 00	C	DB 063h,063h,03eh,00h	;' 55
FD1E	63 63 63 63	C	DB 063h,063h,063h,063h	;' 56
FD22	36 1C 0B 00	C	DB 036h,01eh,00h,00h	;' 56
FD26	63 63 63 6B	C	DB 063h,063h,063h,06bh	;' 57
FD2A	6B 7F 36 00	C	DB 06bh,07fh,036h,00h	;' 57
FD2E	63 63 36 1C	C	DB 063h,063h,036h,01eh	;' 58
FD32	36 63 63 00	C	DB 036h,063h,063h,00h	;' 58
FD36	66 66 66 3C	C	DB 066h,066h,066h,03eh	;' 59
FD3A	18 18 3C 00	C	DB 018h,018h,03eh,00h	;' 59
FD3E	7F 63 06 0C	C	DB 07fh,063h,06h,0eh	;' 5a
FD42	18 33 7F 00	C	DB 018h,033h,07fh,00h	;' 5a

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FD46 3C 30 30 30      C      DB 03ch,030h,030h,030h
FD4A 30 30 3C 00      C      DB 030h,030h,03ch,00h ;'l' 5b
FD4E 20 30 18 0C      C      DB 020h,030h,018h,0ch
FD52 06 03 01 00      C      DB 06h,03h,01h,00h ;'\ ' 5c
FD56 3C 0C 0E 0C      C      DB 03ch,0ch,0ch,0ch
FD5A 0C 0C 3C 00      C      DB 0ch,0ch,03ch,00h ;']' 5d
FD5E 08 1C 36 63      C      DB 08h,01ch,036h,063h
FD62 00 00 00 00      C      DB 00h,00h,00h,00h ;' ' 5e
FD66 00 00 00 00      C      DB 00h,00' 00h,00h
FD6A 00 00 7F 00      C      DB 00h,001 7Fh,00h ;'_ ' 5f
FD6E 18 18 0C 00      C      DB 018h,01h,0ch,00h
FD72 00 00 00 00      C      DB 00h,00h,00h,00h ;'' 60
FD76 00 00 3C 06      C      DB 00h,00h,03ch,06h
FD7A 3E 66 3B 00      C      DB 03eh,066h,03bh,00h ;'a' 61
FD7E 70 30 3E 33      C      DB 070h,030h,03eh,033h
FD82 33 33 6E 00      C      DB 033h,033h,06eh,00h ;'b' 62
FD86 00 00 3E 61      C      DB 00h,00h,03eh,061h
FD8A 60 61 3E 00      C      DB 060h,061h,03eh,00h ;'o' 63
FD8E 0E 06 3E 66      C      DB 0eh,06h,03eh,066h
FD92 66 66 3B 00      C      DB 066h,066h,03bh,00h ;'d' 64
FD96 00 00 3E 63      C      DB 00h,00h,03eh,063h
FD9A 7F 60 3F 00      C      DB 07fh,060h,03fh,00h ;'e' 65
FD9E 1E 33 30 7C      C      DB 01eh,033h,030h,07ch
FDA2 30 30 78 00      C      DB 030h,030h,078h,00h ;'f' 66
FDA6 00 00 3B 66      C      DB 00h,00h,03bh,066h
FDAA 66 3E 46 3C      C      DB 066h,03eh,046h,03ch ;'g' 67
FDAE 70 30 36 3F      C      DB 070h,030h,036h,03fh
FDB2 33 33 73 00      C      DB 033h,033h,073h,00h ;'h' 68
FDB6 0C 00 1C 0C      C      DB 0ch,00h,01ch,0ch
FDBA 0C 0C 1E 00      C      DB 0ch,0ch,01eh,00h ;'i' 69
FDBE 0C 00 1E 0C      C      DB 0ch,00h,01eh,0ch
FDC2 0C 0C 5C 78      C      DB 0ch,0ch,05ch,078h ;'j' 6a
FDC6 70 30 33 36      C      DB 070h,030h,033h,036h
FDCA 3C 36 73 00      C      DB 03ch,036h,073h,00h ;'k' 6b
FDCE 1C 0C 0C 0C      C      DB 01ch,0ch,0ch,0ch
FDD2 0C 0C 1E 00      C      DB 0ch,0ch,01eh,00h ;'l' 6c
FDD6 00 00 66 7F      C      DB 00h,00h,066h,07fh
FDDA 6B 6B 6B 00      C      DB 06bh,06bh,06bh,00h ;'m' 6d
FDDE 00 00 6E 33      C      DB 00h,00h,06eh,033h
FDE2 33 33 33 00      C      DB 033h,033h,033h,00h ;'n' 6e
FDE6 00 00 1E 33      C      DB 00h,00h,01eh,033h
FDEA 33 33 1E 00      C      DB 033h,033h,01eh,00h ;'o' 6f
FDEE 00 00 6E 33      C      DB 00h,00h,06eh,033h
FDF2 33 3E 30 78      C      DB 033h,03eh,030h,078h
FDF6 00 00 3B 66      C      DB 00h,00h,03bh,066h
FDFA 66 3E 06 0F      C      DB 066h,03eh,06h,0fh ;'q' 71
FDFE 00 00 6E 3B      C      DB 00h,00h,06eh,03bh
FE02 30 30 78 00      C      DB 030h,030h,078h,00h ;'r' 72
FE06 00 00 3F 60      C      DB 00h,00h,03fh,060h
FE0A 3C 03 7E 00      C      DB 03ch,03h,07eh,00h ;'a' 73
FE0E 08 18 3E 18      C      DB 08h,018h,03eh,018h
FE12 18 18 0E 00      C      DB 018h,018h,0eh,00h ;'t' 74
FE16 00 00 6E 66      C      DB 00h,00h,06eh,066h
FE1A 66 66 3B 00      C      DB 066h,066h,03bh,00h ;'u' 75
FE1E 00 00 63 63      C      DB 00h,00h,063h,063h
FE22 36 1C 08 00      C      DB 036h,01ch,08h,00h ;'v' 76
FE26 00 00 63 6B      C      DB 00h,00h,063h,06bh
FE2A 6B 7F 36 00      C      DB 06bh,07fh,036h,00h ;'w' 77
FE2E 00 00 63 36      C      DB 00h,00h,063h,036h
FE32 1C 36 63 00      C      DB 01ch,036h,063h,00h ;'x' 78
FE36 00 00 66 66      C      DB 00h,00h,066h,066h
FE3A 66 3E 06 7C      C      DB 066h,03eh,06h,07ch ;'y' 79
FE3E 00 00 7E 4C      C      DB 00h,00h,07eh,04ch
FE42 18 32 7E 00      C      DB 018h,032h,07eh,00h ;'z' 7a
FE46 0E 18 18 70      C      DB 0eh,018h,018h,070h
FE4A 18 18 0E 00      C      DB 018h,018h,0eh,00h ;'[' 7b
FE4E 18 18 18 00      C      DB 018h,018h,018h,00h
FE52 18 18 18 00      C      DB 018h,018h,018h,00h ;'|' 7c
FE56 70 18 18 0E      C      DB 070h,018h,018h,0eh
FE5A 18 18 70 00      C      DB 018h,018h,070h,00h ;']' 7d
FE5E 3B 6E 00 00      C      DB 03bh,06eh,00h,00h
FE62 00 00 00 00      C      DB 00h,00h,00h,00h ;'' 7e
FE66 00 08 1C 36      C      DB 00h,08h,01ch,036h
FE6A 63 63 7F 00      C      DB 063h,063h,07fh,00h ;'' 7f
;End of font matrix
;
PE6E      C      fontlo8 endp
PE6E      C      code      ends

;
;
;      include rtc.asm
;
;      =====
;      ;      Filename:      rtc.arc
;      ;
;      ;      This module includes INT 08h & 1Ah.
;      ;
;      =====
PE6E      C      code      segment public 'ROM'
;
;      ;      assume cs:code, ds:nothing, es:nothing, ss:nothing
;
;      =====
;      ;      INT 1Ah -- Time of Day Software Interrupt Request Routine
;      ;
;      ;      Input:  ah = 0  Read the Clock, then:
;      ;      Output:  cx =  High Portion of Clock (t_hi_order)
;      ;      ;      dx =  Low Portion of Clock (t_low_order)
;      ;      ;      al =  1 if 24 hours have elapsed (t_overflow); 0 otherwise
;

```

# ROM BIOS Listing

```

C ;
C ;
C ;   Input:  ah = 1  Set the Clock, then:
C ;           cx =   High Portion of Clock (t_hi_order)
C ;           dx =   Low Portion of Clock (t_low_order)
C ;
C ;
C ;   Trash:  ah =   (ah - 1) if ah <> 0,-1, or -2
C ;
C ;-----
C ;   Input:  ah = -1 Write Clock Calendar Device, then:
C ;           bx =   day (from 1-1 of leap year up to 12-31 of leap year-7)
C ;           ch =   hour   (0-23)
C ;           cl =   minutes (0-59)
C ;
C ;   Output: ah = -1 implies date/time error
C ;           ah = 0 implies date/time OK
C ;
C ;
C ;   Input:  ah = -2 Read Clock Calendar Device, then:
C ;   Output: bx =   day (from 1-1 of leap year up to 12-31 of leap year-7)
C ;           ch =   hour
C ;           cl =   minutes
C ;           dh =   seconds
C ;           dl =   hundredths of seconds
C ;
C ;
C ;   Trash:  None.
C ;-----
FE6E                ORG     0FE6Eh
FE6E                t_day  proc  near  cs:code, ds:nothing, es:nothing, ss:nothing
FE6F                sti                    ; enable interrupts
FE6F 80 FC FE        cmp     ah,0FEh        ; ZF set if FEh, CF reset if Fh
FE72 75 04           jne     t_nFE         ; ah = -2 = 0FEh ?
FE74 E8 F8F2 R      call    c_read        ; read calendar chip
FE77 CF             ired
FE78                t_nFE:
FE78 72 04           jb     t_nFF          ; ah = -1 = 0FFh > 0FEh ?
FE7A E8 F973 R      call    c_write       ; set calendar chip
FE7D CF             ired
FE7E                t_nFF:
FE7E                assume cs:code, ds:data, es:nothing, ss:nothing
FE7E 1E             push   ds             ; save registers
FE7F E8 E5F4 R      call    set_ds        ; satisfy assumptions
FE82 FA             cli                    ; interrupts off!
FE82 FA             ; (shared variables)
FE83 80 EC 01       sub     ah,1          ; DON'T DECREMENT (CF needed!)
FE86 73 0D          jae     t_set         ; ah = 0 < 1?
FE86                ; Read Time of Day.
FE88 32 E4          xor     ah,ah         ; ah = 0 & ZF set!
FE8A 8B 0E 006E R   mov     cx,word ptr ds:[t_hi_order]
FE8E 8B 16 006C R   mov     dx,word ptr ds:[t_low_order]
FE92 AD 0070 R      mov     al,byte ptr ds:[t_overflow] ; t_overflow = 0 by setting time!
FE92 AD 0070 R      ; fall through (ah = 0 & ZF set)
FE95 75 0C          t_set: jnz     t_end      ; was ah = 1? (is ah = 0 now)?
FE95                ; Set Time of Day.
FE97 89 0E 006E R   mov     word ptr ds:[t_hi_order],cx ; it's ok, if we fell through.
FE9B 89 16 006C R   mov     word ptr ds:[t_low_order],dx ; (a bit slower, but smaller!)
FE9F 88 26 0070 R   mov     byte ptr ds:[t_overflow],ah ; ah = 0 (in all cases...)
FEA3 1F            pop     ds             ; restore registers
FEA4 CF             ired
FEA5                t_day  endp
FEA5                ORG     0FEA5h
FEA5                t_int  proc  near  cs:code, ds:nothing, es:nothing, ss:nothing
FEA5                ; interrupts off!
FEA5                ; (shared variables)
FEA5 50             push   ax             ; preserve registers
FEA6 52             push   dx
FEA7 1E             push   ds
FEA7                assume cs:code, ds:data, es:nothing, ss:nothing
FEA8 2E 8E 1E E5F2 R  mov     ds,word ptr cs:[set_ds_word] ; satisfy assumption
FEA8                ; Handle turning off floppy disk drive motor.
FEAD FE 0E 0040 R   dec     byte ptr ds:[motor_count] ; decrement motor on count

```

# ROM BIOS Listing

```

FEB1 75 08          C          jnz     t_inc           ; should we turn off drive?
FEB3 E8 EF4F R     C          call    stop_disk        ; if so, stop disk motor
FEB6 80 26 003F R  C          and     byte ptr ds:[motor_status],0F0h ; clear low nibble of status
FEBB              C          t_inc:
C          ; increment long p_timer count
FEBB FF 06 006C R  C          inc     word ptr ds:[t_low_order] ; increment low byte of counter
FEBF 75 04          C          jnz     t_hi           ; skip t_hi_order
FEC1 FF 06 006E R  C          inc     word ptr ds:[t_hi_order] ; increment high byte of counter
FEC5              C          t_hi:
C          ; Handle 24 hour overflow situation
FEC5 81 3E 006C R  C          cmp     word ptr ds:[t_low_order],00B0h ; has 24 hours elapsed?
FECB 75 14          C          jne     t_of1         ; if not, skip t_overflow
FECD 83 3E 006E R  C          cmp     word ptr ds:[t_hi_order],24    ; has 24 hours elapsed?
FED2 75 0D          C          jne     t_of1         ; if not, skip t_overflow
FED4 C6 06 0070 R  C          mov     byte ptr ds:[t_overflow],01h
FED9 33 C0         C          xor     ax,ax
FEDB A3 006C R     C          mov     word ptr ds:[t_low_order],ax
FEDE A3 006E R     C          mov     word ptr ds:[t_hi_order],ax
FEE1              C          t_of1:
FEE1 FB           C          sti     ; enable interrupts
C          ; Invoke any user p_timer break routine.
FEE2 CD 1C         C          INT     1Ch
C          ; Send specific end of interrupt (SEOI) to pic 'command' port AFTER p_timer
C          ; break, because user may be out-to-lunch for quite awhile...
FEE4 B0 60         C          mov     al,pic_seoi_0    ; specific end of interrupt command
FEE6 E6 20         C          out     pic_0,al        ; to pic 'command' port.
FEE8 1F           C          pop     ds              ; restore registers
FEE9 5A           C          pop     dx
FEEA 5B           C          pop     ax
FEEB CF           C          iret
FECC              C          t_int endp
FECC              C          code ends
FECC              C          include vector.asm
C          ;=====
C          ;          Filename:      vector.asm
C          ;
C          ;          This module includes the table of ROM interrupt vectors & ill_int
C          ;          hardware diagnostic & illegal software interrupt service routine.
C          ;=====
C          ;          05-11-84
FECC              C          code segment public 'ROM'
FECC              C          assume cs:code, ds:nothing, es:nothing, ss:nothing
FEF3              C          ORG     0FEF3h
FEF3              C          i_vec_tbl proc near
C          dw     t_int           ; int0810cch see rtc.asm
FEF3 F8A5 R       C          dw     k_int           ; int0910cch see kb.asm
FEF5 F84D R       C          dw     ill_int        ; int0A10cch
FEF7 FF23 R       C          dw     ill_int        ; int0B10cch
FEF9 FF23 R       C          dw     ill_int        ; int0C10cch
FEFB FF23 R       C          dw     ill_int        ; int0D10cch
FEFD FF23 R       C          dw     fd_int         ; int0E10cch
FEFF EF57 R       C          dw     fd_int         ; int0E10cch see dsk.asm
FF01 FF23 R       C          dw     ill_int        ; int0F10cch
FF03 F065 R       C          dw     v_io           ; int1010cch see vid.asm
FF05 F84D R       C          dw     m equip        ; int1110cch see mem.asm
FF07 FB41 R       C          dw     m_size         ; int1210cch see mem.asm
FF09 EC59 R       C          dw     fd_io          ; int1310cch see dsk.asm
FF0B E739 R       C          dw     serial_io      ; int1410cch see con.asm
FF0D F859 R       C          dw     m_casa         ; int1510cch see mem.asm
FF0F B82B R       C          dw     k_io           ; int1610cch see kb.asm
FF11 EFD2 R       C          dw     p_io           ; int1710cch see prn.asm
FF13 F860 R       C          dw     bt_int         ; int1810cch (We Don't Have BASIC!)
FF15 F860 R       C          dw     bt_int         ; int1910cch see mem.asm
FF17 FE6E R       C          dw     t_day          ; int1A10cch see rtc.asm
FF19 FF4B R       C          dw     dummy_iret     ; int1B10cch see kb.asm
FF1B FF4B R       C          dw     dummy_iret     ; int1C10cch see rtc.asm
FF1D F0A8 R       C          dw     v_parms        ; int1D10cch see vid.asm
FF1F EFC7 R       C          dw     fd_parms       ; int1E10cch see dsk.asm
FF21 C860 R       C          dw     font_hi_8x8    ; int1F10cch see graph.asm
FF23              C          i_vec_tbl endp
C          ;-----
C          ;          Interrupt Routine for Unused Hardware & Illegal Software Interrupts

```

# ROM BIOS Listing

```

-----
C |-----
C |
C |         assume cs:code, ds:nothing, es:nothing, ss:nothing
FF23 |
C |         ORG     0FF23h
FF23 |
C | 11l_int proc  near
C |                                     ; trap for illegal interrupts
FF23 | 50
C |         push   ax
C |                                     ; save registers
FF24 | B8 FF0B      ; ah = -1; illegal software trap
FF27 | E6 20        ; al = OCW3 -- read PIC's
C |         out    pic_0,al
C |                                     ; in-service register
FF29 | 1E
C |         push   ds
C |                                     ; save registers & delay
C |
C | ; Determine whether it is a hardware or software interrupt.
FF2A | EA 20
C |         in     al,pic_0
C |                                     ; get active PIC IR#
FF2C | 0A C0
C |         or     al,al
C |                                     ; are any active?
FF2E | 74 0E
C |         jz     11l_sw
C |                                     ; if not, illegal software trap.
C |
C | ; If hardware interrupt, disable the 8259 PIC from further interrupts.
FF30 | 8A E0
C |         mov    ah,al
C |                                     ; return active PIC IR#
FF32 | E4 21
C |         in     al,pic_1
C |                                     ; OCW1 -- get PIC interrupt mask
FF34 | 0A C4
C |         or     al,ah
C |                                     ; shut off (set) IR# bit.
FF36 | E6 21
C |         out    pic_1,al
C |                                     ; send PIC new mask.
FF38 | B0 20
C |         mov    al,pic_neoi
C |                                     ; OCW2 -- send PIC a
FF3A | E6 20
C |         out    pic_0,al
C |                                     ; nonspecific end_of_int
C |
C | ; Return ah = active PIC Interrupt Number in intr_flag.
FF3C | EB 03
C |         jmp    short 11l_flg
FF3E |
C | 11l_sw:
C |                                     ; illegal software trap; ah = -1
C |
C | ; Turn off floppy disk drives and notify user
FF3E | EB E50C R
C |         call   11l_trap
C |                                     ; every register but ds saved!
C |
C |         assume cs:code, ds:nothing, es:nothing, ss:nothing
FF41 |
C | 11l_flg:
C |                                     ; set illegal trap flag.
C |                                     ; illegal software trap; ah = -1
C |
C |         assume cs:code, ds:data, es:nothing, ss:nothing
FF41 |
C |         call   set_ds
C |                                     ; satisfy assumptions.
FF44 | 8B 26 006B R ; mov    byte ptr ds:[intr_flag],ah ; return interrupt flag.
FF48 | 1F
C |         pop    ds
C |                                     ; restore registers.
FF49 | 58
C |         pop    ax
C |                                     ; give user a second chance
FF4A | CF
C |         ired
C |
C | 11l_int endp
FF4B |
C |         assume cs:code, ds:nothing, es:nothing, ss:nothing
FF4B |
C |         ORG     0FF4Bh
C |                                     ; ORG 0FF4Bh through 0FF53h
FF4B |
C | dummy_ired   proc  near
C |                                     ; 'BREAK' key interrupt (1Bh)
FF4B | CF
C |         ired
C |                                     ; p_timer break interrupt (1Ch)
C |
C |         ired
C |                                     ; 0FF4Ch -- in case someone is
C |         ired
C |                                     ; 0FF4Dh
C |         ired
C |                                     ; 0FF4Eh
C |         ired
C |                                     ; 0FF4Fh
C |         ired
C |                                     ; 0FF50h
C |         ired
C |                                     ; 0FF51h
C |         ired
C |                                     ; 0FF52h
C |         ired
C |                                     ; 0FF53h
FF54 |
C | dummy_ired   endp
FF54 |
C | code ends
C | include prnscr.asm
C |
C | ;-----
C | ;
C | ;         Filename:      prnscr.src
C | ;
C | ;         This module includes INT 05h.
C | ;-----
C |
C | code  segment public 'ROM'
C |         assume cs:code, ds:nothing, es:nothing, ss:nothing
C |
C | ;-----
C | ;
C | ;         INT 05h -- Print Screen
C | ;
C | ;         Input:  None.
C | ;         Output: None.
C | ;         Trash: None. (Uses byte at 50:0 = 40:0100 as monitor lock:
C | ;                   0 indicates monitor not locked.
C | ;                   1 indicates monitor locked.
C | ;                   -1 indicates printer error.
C | ;-----

```



# ROM BIOS Listing

```

FF54          C          ORG      OFF54h
C
C
FF54          C      _a_int  proc  near
C          C      assume  cs:code, ds:nothing, es:nothing, ss:nothing
C
FF54  1E      C          push   ds          ; save ds
C
C          C          assume  cs:code, ds:data, es:nothing, ss:nothing
C
FF55  2E: 8E 1E E5F2 R  C      mov     ds,word ptr cs:[set_da_word] ; satisfy assumptions
C
C          C      push   dx
C          C      mov     di,1
C          C      look  xchg  byte ptr ds:[100h],di ; check monitor lock
C          C      dec   di ; already locked?
C          C      jz    _a_nop ; if set, do nothing
C          C      sti   ; enable interrupts after
C          C          ; monitor lock code!!!!
C
FF57  51      C          push   cx          ; save registers
C          C      push   bx
C          C      push   ax
C
C          C      ; Get Current Video Width.
C
FF5A  BA 0F      C      mov     ah,0Fh ; call v_video_state
C          C      INT    10h ; Output: ah = crt_cols
C          C          ; al = crt_mode
C          C          ; bh = active_page
C
FF5E  8A DC      C      mov     bl,ah ; save ah = crt_cols
C
C          C      ; Get Current Cursor Position.
C
FF70  BA 03      C      mov     sh,03h ; call v_read_cursor
C          C      INT    10h ; Input: bh = active_page
C          C          ; Output:
C          C          ; (dh,dl) = (row,col) of cursor
C          C          ; (ch,cl) = cursor mode setting
C
FF74  8A EB      C      mov     ch,bl ; get crt_cols
C          C      push  dx ; save row, col of cursor
C          C      mov  cl,-1 ; initialize cl = printer error
C
C          C      ; Loop Through the Screen.
C
FF79  BA 0000     C      mov     dx,0 ; (dh,dl) = (row,col) of origin
C
C          C      call  _a_eol ; print a new line
C          C      jnz  _a_err ; any errors?
C
FF7C  EB FFB5 R  C      _a_lp: call  _a_get ; get next character from screen
C          C      ; Map Invalid Characters to Space.
C
FF84  3C 00      C      cmp     al,0 ; check validity of character.
C          C      jne  _a_ok ; if valid, we're ok.
C          C      mov  al,' ' ; if invalid, print a space.
C          C      _a_ok:
C
C          C      ; Print the Character.
C
FF8A  EB FFB8 R  C      call  _a_out
C          C      jnz  _a_err ; any errors?
C
C          C      ; Advance to Next Character.
C
FF8F  FE C2      C      inc   di ; advance column (1-crt_cols)
C          C      cmp  di,oh ; di < ch = crt_cols?
C          C      jl  _a_lp ; if so, continue
C
FF95  EB FFB5 R  C      call  _a_eol ; else print a new line
C          C      jnz  _a_err ; any errors?
C
FF9A  32 D2      C      xor   di,di ; move column back to 0
C          C      FF9C  FE C6      C      inc  dh ; advance row (1-25)
C          C      FF9E  80 FE 19  C      cmp  dh,25 ; dh < 25
C          C      FFA1  7C DE      C      jl  _a_lp ; if so, continue
C
FFA3  33 C9      C      xor   cx,cx ; set cl = printer no error
C          C      ; jnp  short _a_err ; fall through
C
FFA5  5A          C      _a_err: pop  dx ; restore dx=(row,col) of cursor
C          C      FFA6  BA 02      C      mov  ah,02h ; call v_set_pos
C          C      FFA8  CD 10      C      INT  10h ; Input: bh = active_page
C          C          ; dx = (row,col) of cursor
C
FFAA  FB          C      sti   ; disable interrupts during
C          C          ; monitor lock code!!!!
C          C      FFAB  88 0E 0100  C      mov  byte ptr ds:[100h],cl ; reset monitor lock
C
C          C      ; restore registers
C          C      FFAF  58          C      pop  ax
C          C      FFB0  5B          C      pop  bx
C          C      FFB1  59          C      pop  cx
C          C      FFB2  5A          C      _a_nop: pop dx
C          C      FFB3  1F          C      pop  ds
C          C      FFB4  CF          C      iret
C

```

# ROM BIOS Listing

```

FFB5 B0 0A      C a_eol: mov    al,LF          ; print LF & CR
FFB7 E8 FFBC R  C      call   a_out          ;
FFBA B0 0D      C      mov    al,CR          ; print CR
                  C      jmp    short a_out      ; fall through

FFBC           C a_out:          ; prints out byte in al
FFBC 52         C      push   dx           ; save dx
FFBD BA 0000    C      mov    dx,0           ; address printer port 0.
FFCD BA 00      C      mov    ah,0          ; write byte to port 0
FFC2 CD 17      C      INT    17h          ;
FFC4 5A         C      pop    dx           ; restore dx
                  C      test   ah,025h        ; test for any errors?
FFC5 F6 C4 01   C      test   ah,001h        ; test for time out?
FFC8 C3         C      ret                ;
FFC9           C a_get:          ; Set Cursor Position and get character @ curs. position
FFC9 B4 02      C      mov    ah,02h        ; call v_set_cpos
FFCB CD 10      C      INT    10h          ; Input: bh = active_page
                  C      ; dx = (row,col) of cursor
                  C      ; Read Character at Cursor Position.
FFCD B4 08      C      mov    ah,08h        ; call v_read_ac_current
FFCF CD 10      C      INT    10h          ; Input: bh = active_page
                  C      ; Output: al = character read
FFD1 C3         C      ret                ; ah = attribute

FFD2           C a_int endp
FFD2           C code ends

;-----
; CPU System Reset Vector
;-----

FFD2           code segment public 'ROM'
                  assume cs:code, ds:nothing, es:nothing, ss:nothing

FFF0           ORG    0FFF0h          ; F000:FFF0 = FFFF0 = FFFF:0000

FFF0           vector proc near

FFF0 EA         db    0EAh          ; jmp intersegment F000:(offset diagnostics_1)
FFF1 DD5A R     dw    diagnostics_1 ; instruction pointer cs:(offset diagnostics_1)
FFF3 F000       code_seg F000h      ; code segment F000h

FFF5 30 35 2F 30 33 2F db    '05/03/84' ; release marker (exactly 8 bytes!!!!)
      38 34

FFFD 00         chk_h1 db    0          ; space for checksum of F000:E000 to F000:FFFF

FFFE           vector endp near
FFFE           code ends
FFFE           end

Macros:

      Name Length
IMPORT . . . . . 0005
JMFF . . . . . 0001
EXPORT . . . . . 0005

Structures and records:

      Name Width # fields Initial
      Shift Width Mask

CDB__1 . . . . . 0008 0003
ZFP . . . . . 0006 0002 00C0 0000
SRIVENUM . . . . . 0005 0001 0020 0000
HEADNUM . . . . . 0000 0005 001F 0000
H_CMD_STRUC . . . . . 0004 0003
BX_OPCODE . . . . . 0000
H_CMD_SUBR . . . . . 0001
H_CMD_MODE_DNA . . . . . 0003
PARAMETER_TABLE . . . . . 0010 000A
P_CYLS . . . . . 0000
P_HEADS . . . . . 0002
P_WRITE_CUR . . . . . 0003
P_PRECOMP . . . . . 0005
P_ECC_LEN . . . . . 0007
P_CONTROL_BYTE . . . . . 0008
P_TIMEOUT . . . . . 0009
P_FMT_TIMEOUT . . . . . 000A
P_DRVDIAG_TIMEOUT . . . . . 000B
P_ZZJ . . . . . 000C

Segments and groups:

      Name Size align combine class
ABSD . . . . . 0080 PARA PUBLIC 'RAM'
CODE . . . . . FFFE PARA PUBLIC 'ROM'
DATA . . . . . 0088 PARA PUBLIC 'RAM'
STACK_RAM . . . . . 0000 PARA PUBLIC 'RAM'
V_RAM . . . . . 0000 PARA PUBLIC 'RAM'

Symbols:

```

# ROM BIOS Listing

Name	Type	Value	Attr
ABS0_SEG	Number	0000	
ADDR_MARK_ERROR	Number	0002	
ALLOW_DMA3	Number	0003	
ALT_INPUT	L BYTE	0019	DATA
ALT_KEY	Number	0038	
ALT_RET	L WORD	E2CA	CODE
ALT_SHIFT	Number	0008	
AP_FINISH	L NEAR	D530	CODE
ASSIGN_PARAM	N PROC	D504	CODE Length =002E
ASSIGN_PARAM_1	N PROC	D532	CODE Length =006B
ASSIGN_PARAM_BK	Number	000C	
ASSIGN_PARAM_INT	Number	0009	
A_FINISH	L NEAR	D59C	CODE
BADTRACK_ERR	Number	000B	
BANNER_M	L BYTE	D88C	CODE
BEL	Number	0007	
BELL_WAIT	L NEAR	F567	CODE
BIOS_BREAK	L BYTE	0071	DATA
BOOT_A_DISK	N PROC	D12A	CODE Length =0021
BOOT_INDIRECT	L WORD	D126	CODE
BS	Number	0008	
BT_BLK	L NEAR	F8B3	CODE
BT_DEC	L NEAR	F8B9	CODE
BT_I	L NEAR	F88E	CODE
BT_INT	N PROC	F860	CODE Length =0076
BT_JMP	N PROC	E6F2	CODE Length =0003
BT_M	L BYTE	DBB7	CODE
BT_MERR	L BYTE	DBD1	CODE
BT_MIT	L NEAR	F8A8	CODE
BT_O	L NEAR	F87B	CODE
BT_OK	L NEAR	F8C4	CODE
BT_SPACES	L BYTE	DBF6	CODE
BUFFER_BND	L WORD	0082	DATA
BUFFER_HEAD	L WORD	001A	DATA
BUFFER_START	L WORD	0080	DATA
BUFFER_TAIL	L WORD	001C	DATA
BXDIAO_BX	Number	00E4	
BXDIAO_INT	Number	001A	
BX_ERROR_TABLE	L NEAR	D49F	CODE
BX_READY	L NEAR	D438	CODE
B_FAILED	L NEAR	D12A	CODE
B_LOST	L NEAR	D144	CODE
B_LLP	L NEAR	D12A	CODE
B_OK	L NEAR	D11F	CODE
B_TRY_HDU	L NEAR	D10C	CODE
CAPS_LOCK_KEY	Number	003A	
CAPS_LOCK_MODE	Number	0040	
CAPS_LOCK_SHIFT	Number	0040	
CHKTRK_BX	Number	0005	
CHK_HZ	L BYTE	FFFF	CODE
CHK_LO	L BYTE	C000	CODE
CMD_BLOCK	L BYTE	0042	DATA
CMD_ERROR	Number	0001	
CNTRL_KEY	Number	001D	
CNTRL_SHIFT	Number	0004	
CODE_SEG	Number	F000	
COLOR_POINTER	Number	03D4	
COMMAND	N PROC	D3DD	CODE Length =003B
COMMCONTROL	Number	0065	
COM_BAUD	L WORD	E729	CODE
COM_CTS	Number	0010	
COM_DATA1	N PROC	E729	CODE Length =0010
COM_DATA_A	Number	03F8	
COM_DATA_B	Number	02F8	
COM_DSR	Number	0020	
COM_DTR	Number	0001	
COM_FE	Number	0008	
COM_OB	N PROC	E92A	CODE Length =0023
COM_ID_A	Number	03FA	
COM_ID_B	Number	02FA	
COM_INIT	N PROC	E78F	CODE Length =003A
COM_OE	Number	0002	
COM_PE	N PROC	E8EC	CODE Length =002F
COM_PE	Number	0004	
COM_RTS	Number	0002	
COM_RXD	Number	0001	
COM_STAT	L NEAR	E87F	CODE
COM_TE	Number	0080	
COM_TXD	Number	0020	
CONTROL_B	Number	0062	
CONTROL_BYTE	L BYTE	0076	DATA
CR	Number	000D	
CR_C_ERROR	Number	0010	
C_BCD2BEX	N PROC	F962	CODE Length =0011
C_DATA1	N PROC	F8D6	CODE Length =001C
C_DL_NO	L BYTE	F856	CODE
C_DL_TR	L WORD	F8D6	CODE
C_FINISH	L NEAR	D417	CODE
C_GDATS	N PROC	F9FD	CODE Length =0013
C_ORBT	L NEAR	F80F	CODE
C_WBCD	L NEAR	F945	CODE
C_RBLP	L NEAR	F94B	CODE
C_RBRRT	L NEAR	F956	CODE
C_READ	N PROC	F8F2	CODE Length =0066
C_RHEX	N PROC	F958	CODE Length =000A
C_RMO	L NEAR	F917	CODE
C_RMLP	L NEAR	F90F	CODE

# ROM BIOS Listing

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C_WAIT . . . . . L NEAR D404 CODE
C_WERR . . . . . L NEAR F92B CODE
C_WHEX . . . . . N PROC F9EC CODE Length = 0011
C_WMP . . . . . L NEAR F9B3 CODE
C_WRITE . . . . . N PROC F973 CODE Length = 0079
C_WLP . . . . . L NEAR F99E CODE
DATA_OUT . . . . . N PROC D59D CODE Length = 0014
DATA_SEG . . . . . Number 0040
DCOLON . . . . . N PROC E626 CODE Length = 000C
DCRLF . . . . . N PROC E619 CODE Length = 000D
DELETE_KEY . . . . . Number 0053
DHEXBYTE . . . . . N PROC E643 CODE Length = 000D
DHEXLONG . . . . . N PROC E632 CODE Length = 000A
DHEXNB . . . . . N PROC E650 CODE Length = 0015
DHEXWORD . . . . . N PROC E63C CODE Length = 0007
DIAGNOSTICS_1 . . . . . N PROC D05A CODE Length = 039F
DISABLE_DISK_INTERRUPTS . . . . . N PROC D5FA CODE Length = 0035
DISALLOW_DMA3 . . . . . Number 0007
DISKETTE_101 . . . . . L NEAR EC80 CODE
DISKETTE_STATUS . . . . . L BYTE 0041 DATA
DISK_STATUS . . . . . L BYTE 0074 DATA
DISP_PASS . . . . . L NEAR DF1A CODE
DLX_KB . . . . . Number 0001
DMA_ADDR_0 . . . . . Number 0000
DMA_ADDR_1 . . . . . Number 0002
DMA_ADDR_2 . . . . . Number 0004
DMA_ADDR_3 . . . . . Number 0006
DMA_CMD_DISABLE . . . . . Number 0004
DMA_CMD_ENABLE . . . . . Number 0000
DMA_COMMAND . . . . . Number 0008
DMA_COUNT_0 . . . . . Number 0001
DMA_COUNT_1 . . . . . Number 0003
DMA_COUNT_2 . . . . . Number 0005
DMA_COUNT_3 . . . . . Number 0007
DMA_ERROR . . . . . Number 0008
DMA_FF_CLR . . . . . Number 000C
DMA_MASK_BIT . . . . . Number 000A
DMA_MASK_CLR . . . . . Number 000E
DMA_MASK_WRITE . . . . . Number 000F
DMA_MASTER_CLR . . . . . Number 000D
DMA_MODE . . . . . Number 000B
DMA_MODE_0 . . . . . Number 0058
DMA_MODE_1 . . . . . Number 0041
DMA_MODE_2 . . . . . Number 0056
DMA_MODE_3 . . . . . Number 0043
DMA_REQUEST . . . . . Number 0009
DMA_SEG_0 . . . . . Number 0080
DMA_SEG_1 . . . . . Number 0082
DMA_SEG_2 . . . . . Number 0081
DMA_SEG_3 . . . . . Number 0083
DMA_SEQ_ERROR . . . . . Number 0009
DMA_STATUS . . . . . Number 0008
DMA_TEMP . . . . . Number 000D
DMA_UNHASK_0 . . . . . Number 0000
DNUM . . . . . N PROC E665 CODE Length = 0008
DNUMW . . . . . N PROC E66D CODE Length = 0031
DNUMW_LOOP . . . . . L NEAR E677 CODE
DNUMW_SKIP . . . . . L NEAR E68D CODE
DRUHW_SPACES . . . . . L NEAR E685 CODE
DO_READY . . . . . L NEAR D547 CODE
DROMSTRING . . . . . N PROC E5FA CODE Length = 0008
DRVDIAG_BX . . . . . Number 00E3
DSTRING . . . . . N PROC E602 CODE Length = 0017
DS_LP . . . . . L NEAR E609 CODE
DS_RET . . . . . L NEAR E614 CODE
DUMMY_IRET . . . . . N PROC FF4B CODE Length = 0009
ECC_USED_ERR . . . . . Number 0011
E_LOSE . . . . . L NEAR D3D3 CODE
E_READ_SENSE . . . . . L NEAR E566 CODE
FAIL_M . . . . . L BYTE DC05 CODE
FAR_CALLS . . . . . F PROC C004 CODE Length = 005C
FDC_ERROR . . . . . Number 0020
FDU_DATA1 . . . . . N PROC E220 CODE Length = 0009
FDU_DATA2 . . . . . N PROC EF07 CODE Length = 000B
FD_INT . . . . . N PROC EF57 CODE Length = 0014
FD_IO . . . . . F PROC EC59 CODE Length = 0066
FD_PARMS . . . . . L BYTE EF07 CODE
FIRMWARED . . . . . L NEAR D693 CODE
FLAGS_DATA1 . . . . . N PROC C000 CODE Length = 0004
FMTBAD_BX . . . . . Number 0007
FMTDRV_BX . . . . . Number 0004
FMTDRV_INT . . . . . Number 0007
FMTTRK_BX . . . . . Number 0006
FONTHIB . . . . . N PROC C860 CODE Length = 0400
FONTL016 . . . . . N PROC C060 CODE Length = 0800
FONTL08 . . . . . N PROC FA6E CODE Length = 0400
FONT_HI_8X8 . . . . . L BYTE C860 CODE
FONT_LO_8X16 . . . . . L BYTE C060 CODE
FONT_LO_8X8 . . . . . L BYTE FA6E CODE
FORMAT_ERROR . . . . . L NEAR D69F CODE
F_BUFFER . . . . . Text [bp+4]
F_CHECK_VALID . . . . . N PROC EFAD CODE Length = 001A
F_COMMAND . . . . . Text [bp+3]
F_CONT . . . . . L NEAR EF26 CODE
F_CTL_RET . . . . . L NEAR EF05 CODE
F_CYL . . . . . Text [bp+7]
F_DRIVE . . . . . Text [bp+0]
F_FORMAT_CMD . . . . . Number 004D
F_GB_DECODE . . . . . L NEAR E8E5 CODE
F_GB_TMP . . . . . L NEAR E26D CODE

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# ROM BIOS Listing

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F_GB_LOOP . . . . . L NEAR EE34 CODE
F_GB_LOOP1 . . . . . L NEAR EE5E CODE
F_GB_OUT . . . . . L NEAR EE84 CODE
F_GB_RET . . . . . L NEAR EE71 CODE
F_GB_TABLE . . . . . L BYTE E2E0 CODE
F_GST_BYTE . . . . . N PROC EE29 CODE Length=004A
F_GST_VAR . . . . . N PROC EDDF CODE Length=000D
F_HEAD . . . . . Text [bp+1]
F_HEAD_SETTLE . . . . L NEAR EF41 CODE
F_HLT . . . . . Number 0001
F_INT . . . . . Number 000F
F_IO1 . . . . . L NEAR EC79 CODE
F_IO_RET . . . . . L NEAR EC9B CODE
F_MOTOR_ON . . . . . N PROC ED14 CODE Length=0025
F_MOTOR_PORT . . . . Number 03F2
F_MOTOR_WAIT . . . . Number 0025
F_NO_RET . . . . . L NEAR ED38 CODE
F_DMA . . . . . Number 0000
F_REC_DATA . . . . . Number 03F5
F_REC_RDY . . . . . N PROC EF6B CODE Length=0017
F_REC_RESET . . . . . N PROC EC18 CODE Length=0018
F_REC_RESET_RET . . . L NEAR EC2F CODE
F_REC_STATUS . . . . Number 03F4
F_R1 . . . . . L NEAR EF5C CODE
F_NR_RET . . . . . L NEAR EF80 CODE
F_NUMSECS . . . . . Text [bp+2]
F_PB_ERRRET . . . . . L NEAR EE18 CODE
F_PB_RET . . . . . L NEAR EE17 CODE
F_PUT_BYTE . . . . . N PROC E20C CODE Length=0014
F_R1 . . . . . L NEAR ECDB CODE
F_R2 . . . . . L NEAR EC00 CODE
F_RD1 . . . . . L NEAR ED7D CODE
F_RDATA . . . . . N PROC ED65 CODE Length=0022
F_RD_LOOP . . . . . L NEAR ED78 CODE
F_READ_CMD . . . . . Number 00E6
F_REAL_DRIVE . . . . Text [bp+8]
F_RECAL_CMD . . . . . Number 0007
F_RESET . . . . . N PROC ECBF CODE Length=0055
F_RW1 . . . . . L NEAR EDB3 CODE
F_RW2 . . . . . L NEAR EDDD CODE
F_RW3 . . . . . L NEAR EDF4 CODE
F_RW_COMMON . . . . . N PROC ED87 CODE Length=0078
F_RW_RET . . . . . L NEAR EDFC CODE
F_RW_SKIP . . . . . L NEAR EDD7 CODE
F_S1 . . . . . L NEAR EF02 CODE
F_S01 . . . . . L NEAR EE92 CODE
F_S02 . . . . . L NEAR EEBD CODE
F_S0_RET . . . . . L NEAR EECC CODE
F_SECHUM . . . . . Text [bp+6]
F_SEEK . . . . . N PROC E2CD CODE Length=007A
F_SEEK_CMD . . . . . Number 000F
F_SET_DMA . . . . . N PROC EE73 CODE Length=005A
F_SIS . . . . . N PROC EF82 CODE Length=000B
F_SNSDRV_CMD . . . . Number 0004
F_SNSINT_CMD . . . . Number 0008
F_SPECCIFY_CMD . . . Number 0003
F_SRT_48 . . . . . Number 000C
F_SRT_96 . . . . . Number 000E
F_S_RECAL . . . . . L NEAR EE51 CODE
F_S_RET . . . . . L NEAR EF46 CODE
F_TABLE . . . . . L WORD EC8F CODE
F_WAIT_FOR_REC . . . N PROC EF8D CODE Length=0020
F_WAIT_ONE_MS . . . . N PROC EF47 CODE Length=0008
F_WD1 . . . . . L NEAR EDC5 CODE
F_WDATA . . . . . N PROC ED39 CODE Length=002C
F_WD_LOOP . . . . . L NEAR ED57 CODE
F_WRITE_CMD . . . . . Number 00C5
GAME_CARD . . . . . Number 0201
GET_DRIVE_TYPE_VECTOR . . . N PROC D5C1 CODE Length=0039
GRF_GRAPHICS_DOWN . . . N PROC D909 CODE Length=0063
GRF_GRAPHICS_READ . . . N PROC D96C CODE Length=00ED
GRF_GRAPHICS_UP . . . . N PROC D874 CODE Length=0055
GRF_GRAPHICS_WRITE . . . N PROC DA59 CODE Length=0106
GRF_LIGHT_PEN . . . . . N PROC D7CD CODE Length=0003
GRF_READ_DOT . . . . . N PROC D7D0 CODE Length=001A
GRF_WRITE_DOT . . . . . N PROC D7EA CODE Length=002B
G_T2 . . . . . L NEAR DB6F CODE
G_SIB_2 . . . . . L NEAR D43D CODE
G_SIB_2 . . . . . L NEAR DA7C CODE
G_ADDR . . . . . N PROC DB15 CODE Length=005F
G_ADDR_TEST . . . . . L NEAR DA84 CODE
G_ALIGN_DOT . . . . . L NEAR D808 CODE
G_BITMASK . . . . . L NEAR DB62 CODE
G_CHAR_L_P . . . . . L NEAR DB14 CODE
G_CMP_MOD . . . . . L NEAR D92F CODE
G_COLOR_TABLE . . . . L BYTE D85B CODE
G_CURS_OFF . . . . . N PROC DB5F CODE Length=001E
G_DETMODE . . . . . L NEAR DAA7 CODE
G_RIP_BIT . . . . . L NEAR DB26 CODE
G_FILDER . . . . . N PROC DB8B CODE Length=001E
G_F_COMT . . . . . L NEAR DA15 CODE
G_F_EXIT . . . . . L NEAR DA53 CODE
G_F_L_LP . . . . . L NEAR DBED CODE
G_F_MACH . . . . . L NEAR DA1A CODE
G_F_T_LP . . . . . L NEAR DBEF CODE
G_H_LP . . . . . L NEAR DACB CODE
G_I_LP . . . . . L NEAR DB1F CODE
G_L_LP . . . . . L NEAR DABD CODE
G_JSPT_DOT . . . . . L NEAR D7E5 CODE
G_DS_R . . . . . L NEAR D98C CODE

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# ROM BIOS Listing

G_LDS_W . . . . .	L NEAR DA9F	CODE	
G_LINELP . . . . .	L NEAR DAD7	CODE	
G_MASK . . . . .	L NEAR D5E2	CODE	
G_MATCH . . . . .	L NEAR DA6F	CODE	
G_MDEET . . . . .	L NEAR D9DC	CODE	
G_MED_BIT . . . . .	L NEAR D9F5	CODE	
G_MED_IA . . . . .	L NEAR D9E1	CODE	
G_MED_STORE . . . . .	L NEAR DB3B	CODE	
G_MED_WR . . . . .	L NEAR DB03	CODE	
G_M_AREA . . . . .	L NEAR DBCC	CODE	
G_RDLOOP . . . . .	L NEAR D9AC	CODE	
G_RD_IA . . . . .	L NEAR D9B0	CODE	
G_RD_MED . . . . .	L NEAR D9DA	CODE	
G_REPCHAR . . . . .	L NEAR DAB0	CODE	
G_RETURN . . . . .	L NEAR DB57	CODE	
G_SCAN_LP . . . . .	L NEAR DB1A	CODE	
G_SCROLLER . . . . .	N PROC DBC9	CODE	Length =0022
G_SEL_FONT . . . . .	L NEAR DA91	CODE	
G_SETDOWN . . . . .	L NEAR D93D	CODE	
G_SET_UP . . . . .	L NEAR D8A9	CODE	
G_SKP_1 . . . . .	L NEAR D826	CODE	
G_SKP_2 . . . . .	L NEAR D82C	CODE	
G_SKP_3 . . . . .	L NEAR D832	CODE	
G_SKP_4 . . . . .	L NEAR D855	CODE	
G_SKP_5 . . . . .	L NEAR D873	CODE	
G_SUPER_WR . . . . .	L NEAR DAC7	CODE	
G_TEST_ADDR . . . . .	L NEAR DA49	CODE	
G_TINTTEXT . . . . .	L NEAR DAC3	CODE	
G_TST_MOD . . . . .	L NEAR D89A	CODE	
G_T_XOR . . . . .	L NEAR DAE3	CODE	
G_UNREVERSE_VIDEO_LOOP . . . . .	L NEAR D9D3	CODE	
G_V_BYTE . . . . .	L NEAR DAE4	CODE	
G_XORBIT . . . . .	L NEAR D7FF	CODE	
HARD_DISK_INT13 . . . . .	L NEAR D185	CODE	
HDU_BST . . . . .	Number 0008		
HDU_CD . . . . .	Number 0004		
HDU_DMA_SEG . . . . .	Number 0082		
HDU_IO . . . . .	Number 0002		
HDU_IRQ5 . . . . .	Number 0020		
HDU_PARH_TBL . . . . .	L NEAR D1AB	CODE	
HDU_REQ . . . . .	Number 0001		
HD_ERROR . . . . .	L BYTE 0042	DATA	
HF_NUM . . . . .	L BYTE 0075	DATA	
H_ABS_M . . . . .	L BYTE D0AE	CODE	
H_BAD_COMMAND . . . . .	L NEAR D25A	CODE	
H_BAD_M . . . . .	L BYTE D0A2	CODE	
H_BOOT . . . . .	F PROC D0E9	CODE	Length =0041
H_CMD_TABLE . . . . .	L NEAR D26D	CODE	
H_CMD_WAIT . . . . .	N PROC D43B	CODE	Length =0064
H_C_ERR . . . . .	Number 0002		
H_DATA1 . . . . .	N PROC D49F	CODE	Length =0040
H_DATA2 . . . . .	N PROC D6AC	CODE	Length =0121
H_DMA . . . . .	N PROC D2C1	CODE	Length =007D
H_DMA_BUFF . . . . .	L NEAR D32C	CODE	
H_DMA_ERR . . . . .	L NEAR D336	CODE	
H_DMA_LEN . . . . .	L NEAR D304	CODE	
H_DMA_LONG . . . . .	L NEAR D322	CODE	
H_ERR_CHK . . . . .	N PROC D34A	CODE	Length =0093
H_ERR_M . . . . .	L BYTE D7BT	CODE	
H_ERR_RET . . . . .	L NEAR D3D2	CODE	
H_FINISH . . . . .	L NEAR D242	CODE	
H_FMT . . . . .	N PROC D640	CODE	Length =006C
H_FMT_M . . . . .	L BYTE D733	CODE	
H_GOOD_M . . . . .	L BYTE D0A6	CODE	
H_HAD_ERR . . . . .	L NEAR D352	CODE	
H_INIT . . . . .	N PROC CF9F	CODE	Length =011C
H_INT . . . . .	N PROC D62F	CODE	Length =0011
H_INTRO_M . . . . .	L BYTE D6AC	CODE	
H_IO . . . . .	F PROC D1AB	CODE	Length =0116
H_MAKE_CDB . . . . .	L NEAR D1DE	CODE	
H_MDMA . . . . .	N PROC D33E	CODE	Length =000C
H_NON_E_M . . . . .	L BYTE D784	CODE	
H_PASS_M . . . . .	L BYTE D750	CODE	
H_SAVE_REGS . . . . .	L NEAR D1C4	CODE	
ILL_FLG . . . . .	L NEAR FF91	CODE	
ILL_INT . . . . .	N PROC FF23	CODE	Length =0028
ILL_LN . . . . .	L NEAR E5C4	CODE	
ILL_LP . . . . .	L NEAR E5C9	CODE	
ILL_M1 . . . . .	L BYTE DC1B	CODE	
ILL_M2 . . . . .	L BYTE DC34	CODE	
ILL_M3 . . . . .	L BYTE DC3A	CODE	
ILL_SW . . . . .	L NEAR FF3E	CODE	
ILL_TRAP . . . . .	N PROC E58C	CODE	Length =0039
INIT_CONTROLLER_LP . . . . .	L NEAR CFED	CODE	
INIT_DRIVE_LP . . . . .	L NEAR D022	CODE	
INIT_DRIVE_WIN . . . . .	L NEAR D047	CODE	
INIT_ERR . . . . .	Number 0007		
INIT_START_TIMER . . . . .	L NEAR D028	CODE	
INIT_TRY_DRIVE . . . . .	L NEAR D036	CODE	
INSERT_KEY . . . . .	Number 0052		
INSERT_MODE . . . . .	Number 0080		
INSERT_SHIFT . . . . .	Number 0080		
INT01LOCN . . . . .	L DWORD 0000	AB50	
INT01LOCN . . . . .	L DWORD 0004	AB50	
INT02LOCN . . . . .	L DWORD 0008	AB50	
INT03LOCN . . . . .	L DWORD 000C	AB50	
INT04LOCN . . . . .	L DWORD 0010	AB50	
INT05LOCN . . . . .	L DWORD 0014	AB50	
INT06LOCN . . . . .	L DWORD 0018	AB50	
INT07LOCN . . . . .	L DWORD 001C	AB50	

# ROM BIOS Listing

INT08LOC.	L	DWORD	0020	AB50	
INT09LOC.	L	DWORD	0024	AB50	
INT0ALOC.	L	DWORD	0028	AB50	
INT0BLOC.	L	DWORD	002C	AB50	
INT0CLOC.	L	DWORD	0030	AB50	
INT0DLOC.	L	DWORD	0034	AB50	
INT0ELOC.	L	DWORD	0038	AB50	
INT0FLOC.	L	DWORD	003C	AB50	
INT10LOC.	L	DWORD	0040	AB50	
INT11LOC.	L	DWORD	0044	AB50	
INT12LOC.	L	DWORD	0048	AB50	
INT13LOC.	L	DWORD	004C	AB50	
INT14LOC.	L	DWORD	0050	AB50	
INT15LOC.	L	DWORD	0054	AB50	
INT16LOC.	L	DWORD	0058	AB50	
INT17LOC.	L	DWORD	005C	AB50	
INT18LOC.	L	DWORD	0060	AB50	
INT19LOC.	L	DWORD	0064	AB50	
INT1ALOC.	L	DWORD	0068	AB50	
INT1BLOC.	L	DWORD	006C	AB50	
INT1CLOC.	L	DWORD	0070	AB50	
INT1DLOC.	L	DWORD	0074	AB50	
INT1ELOC.	L	DWORD	0078	AB50	
INT1FLOC.	L	DWORD	007C	AB50	
INTR_FLAG.	L	BYTE	006B	DATA	
IO_ROM_INIT.	L	WORD	0067	DATA	
IO_ROM_SEG.	L	WORD	0069	DATA	
_AL_T_COMT.	L	NEAR	E4F0	CODE	
_AL_T_CPD.	L	NEAR	E4D7	CODE	
_AL_T_ECHO.	L	NEAR	E534	CODE	
_AL_T_END.	L	NEAR	E567	CODE	
_AL_T_F00ND.	L	NEAR	E511	CODE	
_AL_T_IRQ.	L	NEAR	E522	CODE	
_AL_T_RESTART.	L	NEAR	E545	CODE	
_AL_T_SELECT_M.	L	BYTE	DD35	CODE	
_AL_T_TBST.	L	NEAR	E506	CODE	
_CAL.	L	NEAR	DF99	CODE	
_CAL_O.	L	NEAR	E04E	CODE	
_CAL_1_80.	L	NEAR	E01E	CODE	
_CAL_END.	L	NEAR	E07B	CODE	
_CAL_ERR.	L	NEAR	E061	CODE	
_CAL_MAX.	L	NEAR	E02D	CODE	
_CAL_OK.	L	NEAR	E073	CODE	
_CAL_VAL.	L	BYTE	DD51	CODE	
_COM_M.	L	BYTE	DCDD	CODE	
_CPD.	L	NEAR	DD62	CODE	
_CPD_ERR.	L	NEAR	DD8D	CODE	
_CPD_M.	L	BYTE	DC4B	CODE	
_DMAC.	L	NEAR	DD9E	CODE	
_DMAC_ERR.	L	NEAR	DDE2	CODE	
_DMAC_LP.	L	NEAR	DDF2	CODE	
_DMAC_M.	L	BYTE	DC72	CODE	
_DMAC_NIB.	L	NEAR	DE3E	CODE	
_DMAC_OK.	L	NEAR	DE64	CODE	
_DMAC_PASS2.	L	NEAR	DDEF	CODE	
_DMAC_RET.	L	NEAR	DE51	CODE	
_DMAT.	L	NEAR	DDCT	CODE	
_DMAT_ERR.	L	NEAR	DD95	CODE	
_DMAT_M.	L	BYTE	DC65	CODE	
_DMAT_OK.	L	NEAR	DDDB	CODE	
_DMAT_RET.	L	NEAR	DDD3	CODE	
_D_ROOTS.	L	NEAR	E187	CODE	
_D_INIT.	N	PROC	E148	CODE	Length =0058
_D_M.	L	BYTE	DC8C	CODE	
_D_MODE.	L	NEAR	E19A	CODE	
_D_OK.	L	NEAR	E18D	CODE	
_FATAL.	N	PROC	E0E9	CODE	Length =005F
_FATAL_RET.	L	NEAR	E139	CODE	
_FDDA_M.	L	BYTE	DD01	CODE	
_FDDB_M.	L	BYTE	DD0E	CODE	
_FDD_END.	L	NEAR	E4CD	CODE	
_FDD_LP.	L	NEAR	E4A7	CODE	
_FDD_NOT_M.	L	BYTE	DD1B	CODE	
_FDD_OK.	L	NEAR	E4CA	CODE	
_FDD_RD_M.	L	BYTE	DD1F	CODE	
_HDD_M.	L	BYTE	DD28	CODE	
_HDD_OK.	L	NEAR	E47D	CODE	
_INIT_END.	L	NEAR	E56C	CODE	
_IB_M.	L	BYTE	DCBF	CODE	
_IB_ST_M.	L	BYTE	DCCC	CODE	
_IO_COM_A.	L	NEAR	E3AD	CODE	
_IO_COM_B.	L	NEAR	E3BC	CODE	
_IO_GAME_CARD.	L	NEAR	E3D5	CODE	
_IO_SCC.	L	NEAR	E3CA	CODE	
_NPU_M.	L	BYTE	DC99	CODE	
_OPTROM_M.	L	BYTE	DCF4	CODE	
_OUT_MASK.	N	PROC	E1ED	CODE	Length =0009
_PIC.	L	NEAR	E65B	CODE	
_PIC_0_OK.	L	NEAR	DEA9	CODE	
_PIC_1_OK.	L	NEAR	DEAD	CODE	
_PIC_2_OK.	L	NEAR	DEB1	CODE	
_PIC_3_OK.	L	NEAR	DEB5	CODE	
_PIC_4_OK.	L	NEAR	DEB9	CODE	
_PIC_END.	L	NEAR	DF11	CODE	
_PIC_ERR.	L	NEAR	DEDC	CODE	
_PIC_HARD.	L	NEAR	DE9E	CODE	
_PIC_HOT.	L	NEAR	DED7	CODE	
_PIC_INIT.	N	PROC	E1DC	CODE	Length =0011
_PIC_M.	L	BYTE	DC7F	CODE	

# ROM BIOS Listing

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I_PIC_NO_HOT . . . . . L NEAR DF05 CODE
I_PIC_OK . . . . . L NEAR DF08 CODE
I_PIC_SOFT . . . . . L NEAR DE8E CODE
I_PIC_TEST . . . . . L NEAR DEBB CODE
I_PRT_EXIT . . . . . L NEAR E398 CODE
I_PRT_LOOP . . . . . L NEAR E382 CODE
I_PRT_M . . . . . L BYTE DCD0 CODE
I_RAM_M . . . . . L BYTE DCEA CODE
I_ROM . . . . . L NEAR DBB2 CODE
I_ROM_ERR . . . . . L NEAR DBB4 CODE
I_ROM_M . . . . . L BYTE DC58 CODE
I_ROM_OK . . . . . L NEAR DDC0 CODE
I_ROM_RET . . . . . L NEAR DBB8 CODE
I_RTC . . . . . L NEAR E07B CODE
I_RTC_END . . . . . L NEAR E0E1 CODE
I_RTC_ERR . . . . . L NEAR E0B9 CODE
I_RTC_HI_M . . . . . L BYTE DCB7 CODE
I_RTC_LO_M . . . . . L BYTE DCA5 CODE
I_RTC_M . . . . . L BYTE DCA5 CODE
I_RTC_NR_M . . . . . L BYTE DCBB CODE
I_RTC_OK . . . . . L NEAR E0D5 CODE
I_VECO . . . . . L NEAR E1B0 CODE
I_VECO8 . . . . . L NEAR E1CC CODE
I_VECTOR . . . . . N PROC E1A0 CODE
I_VEC_TBL . . . . . N PROC FEF3 CODE
KBALT . . . . . Number 00C4
KBBRK . . . . . Number 00C9
KBCAP . . . . . Number 00C1
KBCTL . . . . . Number 00C5
KBINS . . . . . Number 00C0
KBLSH . . . . . Number 00C6
KBNUL . . . . . Number 00CC
KBNUM . . . . . Number 00C2
KBPR1 . . . . . Number 00C8
KBRES . . . . . Number 00C8
KBRSR . . . . . Number 00C7
KBSCB . . . . . Number 00C3
KB_BUFFER . . . . . L WORD 001E DATA
KB_CAP_FLAGS . . . . . L BYTE CC60 CODE
KB_CHD_SEND . . . . . N PROC E581 CODE
KB_CHD_WLUP . . . . . L NEAR E581 CODE
KB_DATA1 . . . . . N PROC CC60 CODE
KB_DATA_TABLE . . . . . L BYTE CC67 CODE
KB_FLAG . . . . . L BYTE 0017 DATA
KB_FLAG_1 . . . . . L BYTE 0018 DATA
KB_FLUSH . . . . . L NEAR E304 CODE
KB_FLUSH_BACK . . . . . L NEAR E313 CODE
KB_NOT_DLX . . . . . L NEAR E361 CODE
KB_STATUS . . . . . Number 0064
KB_TYPE_READ . . . . . L NEAR E351 CODE
KB_TYPE_WAIT . . . . . L NEAR E346 CODE
XDBLO . . . . . Number 00D8
KDECO . . . . . Number 00D7
KDEC1 . . . . . Number 00D6
KDEC2 . . . . . Number 00D5
KDEC3 . . . . . Number 00D4
KDEC4 . . . . . Number 00D3
KDEC5 . . . . . Number 00D2
KDEC6 . . . . . Number 00D1
KDEC7 . . . . . Number 00D0
KDEC8 . . . . . Number 00CF
KDEC9 . . . . . Number 00CE
KNONE . . . . . Number 00CD
K_00 . . . . . L NEAR EB35 CODE
K_2_RES . . . . . L NEAR EB18 CODE
K_2RET . . . . . L NEAR EBOA CODE
K_2TOG . . . . . L NEAR EB0F CODE
K_3RES . . . . . L NEAR EAET CODE
K_3RET . . . . . L NEAR EA26 CODE
K_3TOG . . . . . L NEAR EAD4 CODE
K_ADV_END . . . . . L NEAR EB7A CODE
K_ADV_PTR . . . . . N PROC EB6E CODE
K_ALT1 . . . . . L NEAR EA2E CODE
K_ALT0 . . . . . L NEAR EB28 CODE
K_ALT1 . . . . . L NEAR EB27 CODE
K_ALT2 . . . . . L NEAR EB26 CODE
K_ALT3 . . . . . L NEAR EB25 CODE
K_ALT4 . . . . . L NEAR EB24 CODE
K_ALT5 . . . . . L NEAR EB23 CODE
K_ALT6 . . . . . L NEAR EB22 CODE
K_ALT7 . . . . . L NEAR EB21 CODE
K_ALT8 . . . . . L NEAR EB20 CODE
K_ALT9 . . . . . L NEAR EB1F CODE
K_BEEP . . . . . N PROC EBC3 CODE
K_BIT . . . . . N PROC EB85 CODE
K_BRK . . . . . L NEAR EB42 CODE
K_BUF . . . . . L NEAR EA56 CODE
K_CAP . . . . . L NEAR EAB5 CODE
K_CASE . . . . . L WORD EB6E CODE
K_CTL . . . . . L NEAR EB00 CODE
K_DATA1 . . . . . N PROC EB26 CODE
K_EOI . . . . . N PROC EBA4 CODE
K_HOLD . . . . . L NEAR EA92 CODE
K_INS . . . . . L NEAR EAAT CODE
K_INT . . . . . N PROC E987 CODE
K_IO . . . . . N PROC EB2E CODE
K_IX . . . . . L NEAR EA02 CODE
K_JMP . . . . . L NEAR EA2D CODE
K_LED_CAP . . . . . L NEAR EB63 CODE
K_LED_CHD . . . . . L NEAR EB70 CODE
Length =003C
Length =0030
Length =0010
Length =000B
Length =0033F
Length =000D
Length =0023
Length =001F
Length =0032
Length =0009
Length =01D2
Length =0017

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# ROM BIOS Listing

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K_LED_DAT . . . . . L NEAR EB7A CODE
K_LED_NUM . . . . . N PROC EB59 CODE Length =002C
K_LED_RET . . . . . L NEAR EB84 CODE
K_LOCK . . . . . L NEAR E9F4 CODE
K_LOOK . . . . . F PROC EB60 CODE Length =0009
K_LF . . . . . L NEAR EBCE CODE
K_LSH . . . . . L NEAR EBO4 CODE
K_NOM1 . . . . . L NEAR EABF CODE
K_NONE . . . . . L NEAR EA5B CODE
K_NOP . . . . . L NEAR EA5E CODE
K_NOP1 . . . . . L NEAR EB3F CODE
K_NO_CAP . . . . . L NEAR E9E7 CODE
K_NO_CASE . . . . . L NEAR EA36 CODE
K_NO_HOLD . . . . . L NEAR EA4C CODE
K_NO_LOCK . . . . . L NEAR E9FC CODE
K_NO_ICODE . . . . . L NEAR EA54 CODE
K_NULL . . . . . L NEAR EAA2 CODE
K_NUM . . . . . L NEAR EAC1 CODE
K_OK . . . . . L NEAR E9B2 CODE
K_PAUSE . . . . . L NEAR EA78 CODE
K_PRT . . . . . L NEAR EA9B CODE
K_READ . . . . . N PROC EB45 CODE Length =001B
K_RES . . . . . L NEAR EA67 CODE
K_RET . . . . . L NEAR EB42 CODE
K_RSH . . . . . L NEAR EB08 CODE
K_SCR . . . . . L NEAR EACD CODE
K_SEE . . . . . L NEAR EB54 CODE
K_STAT . . . . . N PROC EB69 CODE Length =0005
K_TRY . . . . . N PROC EBAD CODE Length =0016
K_XLAT . . . . . L NEAR EA16 CODE
LEFT_SHIFT . . . . . Number 0002
LEFT_SHIFT_KEY . . . . . Number 0024
LF . . . . . Number 000A
MASK_PORT . . . . . Number 0323
MASK_PORT_DMAE . . . . . Number 0001
MASK_PORT_INTE . . . . . Number 0002
MASTAB . . . . . L WORD E2CE CODE
MASTER_TBL_PTR . . . . . L DWORD 008A DATA
MAX_INT . . . . . Number 0014
MAX_INT_SHOW_SENSE . . . . . N PROC D0CE CODE Length =001B
MEMORY_SIZE . . . . . L WORD 0013 DATA
MEMTST . . . . . N PROC E266 CODE Length =0047
MEMTST_ERR . . . . . L NEAR E2AB CODE
MEMTST_ERR_C . . . . . L NEAR E247 CODE
MEMTST_R1 . . . . . L NEAR E279 CODE
MEMTST_R2 . . . . . L NEAR E290 CODE
MEMTST_W1 . . . . . L NEAR E26D CODE
MEMTST_W2 . . . . . L NEAR E286 CODE
MFG_ERR_FLAG . . . . . L BYTE 0015 DATA Length =0002
MFG_TST . . . . . L BYTE 0012 DATA
MOTOR_COUNT . . . . . L BYTE 0040 DATA
MOTOR_STATUS . . . . . L BYTE 003F DATA
MT_END . . . . . L WORD E2E4 CODE
M_CBS . . . . . N PROC F859 CODE Length =0006
M_EQUIP . . . . . N PROC F84D CODE Length =000C
M_EXIT . . . . . L NEAR D0E7 CODE
M_SIZE . . . . . N PROC F841 CODE Length =000C
MFC_STATUS . . . . . L BYTE 0042 DATA Length =0007
NIBOK . . . . . L NEAR E65E CODE
NO_HARD_DISK . . . . . L NEAR D697 CODE
NULL . . . . . Number 0000
NUM_LOCK_KEY . . . . . Number 0045
NUM_LOCK_MODE . . . . . Number 0020
NUM_LOCK_SHIFT . . . . . Number 0020
N_INT . . . . . N PROC F85F CODE Length =0001
OPT_ROM_M . . . . . L BYTE E24D CODE
P0_DATA1 . . . . . N PROC E24D CODE Length =0037
P1_DATA1 . . . . . N PROC DB7D CODE Length =01DD
P4_DATA1 . . . . . N PROC E5F2 CODE Length =0002
PARA_GRAPH . . . . . Number 8B00
PARA_MONO . . . . . Number 8000
PASS_M . . . . . L BYTE DC3D CODE
PAUSE . . . . . Number 00CA
PAUSE_MODE . . . . . Number 0008
PCINIT . . . . . N PROC E2E4 CODE Length =629D
PIC_0 . . . . . Number 0020
PIC_1 . . . . . Number 0021
PIC_ICW1 . . . . . Number 0013
PIC_ICM2 . . . . . Number 0008
PIC_ICM3 . . . . . Number 0008
PIC_ICM4 . . . . . Number 000D
PIC_NB01 . . . . . Number 0020
PIC_OFF_MSK . . . . . Number 00FF
PIC_SEOI_0 . . . . . Number 0060
PIC_SEOI_1 . . . . . Number 0061
PIC_SEOI_6 . . . . . Number 0066
PORT_OFF . . . . . L BYTE 0077 DATA
POST_LOSE . . . . . L NEAR D071 CODE
POST_NO_MORE_DRIVES . . . . . L NEAR D06A CODE
POST_WIN . . . . . L NEAR D083 CODE
PRINTER_ADDR . . . . . L WORD 0008 DATA Length =0004
PRINTER_OUT . . . . . L BYTE 0078 DATA Length =0004
PRT_DATA_A . . . . . Number 03BC
PRT_DATA_B . . . . . Number 0378
PRT_DATA_C . . . . . Number 0278
P_8253_0 . . . . . Number 0040
P_8253_1 . . . . . Number 0041
P_8253_2 . . . . . Number 0042
P_8253_CTRL . . . . . Number 0043
P_DISP . . . . . L NEAR D09B CODE

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# ROM BIOS Listing

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P_INIT . . . . .
P_IO . . . . .
P_CTRL . . . . .
P_KSCAN . . . . .
P_LP . . . . .
P_NOP . . . . .
P_OK . . . . .
P_OUT . . . . .
P_RET . . . . .
P_SOME . . . . .
P_STAT . . . . .
P_TBL . . . . .
RAMDIAG_BX . . . . .
RAMDIAG_INT . . . . .
RAM_ERROR . . . . .
RAM_SIZE_END . . . . .
RAM_SIZE_END_1 . . . . .
RAM_SIZE_LP . . . . .
RAM_SIZE_WT . . . . .
RAM_SIZE_TST . . . . .
RBUF_BX . . . . .
READ_BX . . . . .
READ_ECC_BX . . . . .
READ_INT . . . . .
READ_MODE . . . . .
READ_PARAM . . . . .
READ_PORT . . . . .
RECAL_BX . . . . .
RECAL_INT . . . . .
RESET_BX . . . . .
RESET_FLAG . . . . .
RESET_INT . . . . .
RESET_PORT . . . . .
RET_FROM_NO . . . . .
RIGHT_SHIFT . . . . .
RIGHT_SHIFT_KEY . . . . .
R_LONG_BX . . . . .
ROM_CHECKSUM . . . . .
ROM_CHECKSUM_CNT . . . . .
ROM_CHECKSUM_LOOP . . . . .
ROM_CHECKSUM_OK . . . . .
ROM_ERR . . . . .
ROM_ID . . . . .
ROM_MT . . . . .
ROM_SCAN_EXIT . . . . .
ROM_SCAN_LOOP . . . . .
ROM_SCAN_NEXT . . . . .
RS232_ADDR . . . . .
RS_DLY . . . . .
RS_OB . . . . .
RS_INIT . . . . .
RS_LP . . . . .
RS_NOP . . . . .
RS_NORM . . . . .
RS_OK . . . . .
RS_PBE . . . . .
RS_PB_GB . . . . .
RS_RET . . . . .
RS_STAT . . . . .
RS_TBL . . . . .
RS_WS . . . . .
RS_WS_COM . . . . .
RS_WS_EXIT . . . . .
RS_WS_LP . . . . .
RTC_CHK . . . . .
RTC_CHK_HIGH . . . . .
RTC_CHK_LOW . . . . .
RTC_CHK_RESET_ERR . . . . .
RTC_CHK_RESET_LP . . . . .
RTC_CHK_RESET_OK . . . . .
RTC_CHK_SET_ERR . . . . .
RTC_CHK_SET_LP . . . . .
RTC_CHK_SET_OK . . . . .
R_FINISH . . . . .
R_WAITING . . . . .
SCC_CTL_A . . . . .
SCC_CTL_B . . . . .
SCC_DBIT . . . . .
SCC_FE . . . . .
SCC_GB . . . . .
SCC_INIT . . . . .
SCC_NO_FE . . . . .
SCC_NO_OE . . . . .
SCC_NO_PE . . . . .
SCC_NO_RXD . . . . .
SCC_NO_TXD . . . . .
SCC_OE . . . . .
SCC_PB . . . . .
SCC_PE . . . . .
SCC_PWRUP . . . . .
SCC_RXD . . . . .
SCC_STAT . . . . .
SCC_TBL . . . . .
SCC_TID . . . . .
SCRL_LOCK_KEY . . . . .
SCRL_LOCK_MODE . . . . .
SCRL_LOCK_SHIFT . . . . .
SECTORS_PER_TRACK . . . . .
SECT_NOT_FOUND . . . . .
SREK_BX . . . . .
L HEAR F027 CODE
N PROC EFD2 CODE Length =0Q69
Number 0051
Number 0050
L HEAR F00F CODE
L HEAR F00A CODE
L HEAR F01D CODE
L HEAR F00B CODE
L HEAR F005 CODE
L HEAR D092 CODE
L HEAR F034 CODE
L WORD E2BE CODE
Number 0080
Number 0012
L HEAR DFC9 CODE
L HEAR DFAB CODE
L HEAR DF85 CODE
L HEAR DF6C CODE
L HEAR DF43 CODE
L HEAR DF5C CODE
Number 000E
Number 0008
Number 000D
Number 0002
Number 0047
N PROC D4DF CODE Length =0025
Number 0320
Number 0001
Number 0011
N PROC D5B1 CODE Length =0010
L WORD 0072 DATA
Number 0000
Number 0321
L NEAR D1B2 CODE
Number 0001
Number 0036
Number 00E5
N PROC E5E5 CODE Length =000D
L HEAR E5E8 CODE
L HEAR E5EA CODE
L HEAR E335 CODE
N PROC E5D5 CODE Length =0010
L BYTE C001 CODE
L WORD C002 CODE
L HEAR E24E CODE
L HEAR E3FD CODE
L HEAR E24A CODE
L WORD 0000 DATA Length =0004
N PROC E8E2 CODE Length =000A
L HEAR E948 CODE
L HEAR E3F0 CODE
L HEAR E8E7 CODE
L HEAR E77D CODE
L HEAR E749 CODE
L HEAR E771 CODE
L HEAR E910 CODE
L HEAR E90F CODE
L HEAR E77A CODE
N PROC E87B CODE Length =0043
L WORD E77F CODE
N PROC E8BE CODE Length =0024
L HEAR E8CD CODE
L HEAR E8BE CODE
L HEAR E8C3 CODE
N PROC E1F6 CODE Length =0070
L HEAR E265 CODE
L HEAR E265 CODE
L HEAR E217 CODE
L HEAR E205 CODE
L HEAR E21A CODE
L HEAR E238 CODE
L HEAR E224 CODE
L HEAR E23B CODE
L HEAR D435 CODE
L NEAR D41D CODE
Number 0050
Number 0052
L BYTE F62E CODE
Number 0040
N PROC E94D CODE Length =000D
N PROC F573 CODE Length =00BF
L HEAR E84D CODE
L HEAR E8BB CODE
L HEAR E884 CODE
L HEAR E89F CODE
L HEAR E838 CODE
Number 0020
N PROC E91B CODE Length =000F
Number 0010
L HEAR F623 CODE
Number 0001
L HEAR E88A CODE
L WORD E2C6 CODE
Number 000A
Number 0046
Number 0010
Number 0010
Number 0011
Number 0004
Number 000B

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# ROM BIOS Listing

SBBF_ERROR . . . . .	Number 0040		
SBBF_STATUS . . . . .	L BYTE 003E	DATA	
SREACT_PORT . . . . .	Number 0322		
SEND_CDB_BYTE . . . . .	L NEAR D3F8	CODE	
SENSBO_MSI . . . . .	Number 003F		
SENSE_BX . . . . .	Number 0003		
SENSE_ERR . . . . .	Number 00FF		
SERIAL_IO . . . . .	N PROC E739	CODE	Length =0056
SERIAL_T_OUT . . . . .	L BYTE 007C	DATA	Length =0004
SET_DS . . . . .	N PROC E5F4	CODE	Length =0006
SET_DS_WORD . . . . .	L WORD E5F2	CODE	
SROM_SENSE . . . . .	N PROC D0BB	CODE	Length =0013
STACK_ROM . . . . .	L WORD DB7E	CODE	
STACK_SEG . . . . .	Number 0030		
STATUS . . . . .	L NEAR D283	CODE	
STATUS_INT . . . . .	Number 0001		
STATUS_PORT . . . . .	Number 0321		
STOP_DISK . . . . .	N PROC EFAF	CODE	Length =0007
SWITCH_BITS . . . . .	L WORD 0010	DATA	
SWITCH_PORT . . . . .	Number 0322		
SYS_CONF_A . . . . .	Number 0066		
SYS_CONF_B . . . . .	Number 0067		
S_EOL . . . . .	L NEAR FFB5	CODE	
S_ERR . . . . .	L NEAR FFA5	CODE	
S_GET . . . . .	L NEAR FFC9	CODE	
S_INT . . . . .	N PROC FFS4	CODE	Length =007E
S_LP . . . . .	L NEAR FF81	CODE	
S_NOP . . . . .	L NEAR FF82	CODE	
S_OK . . . . .	L NEAR FFB4	CODE	
S_OUT . . . . .	L NEAR FFB8	CODE	
TOCMD . . . . .	Number 0036		
TOCOUNT . . . . .	Number 0000		
TICMD . . . . .	Number 0074		
TICOUNT . . . . .	Number 0013		
T2CMD . . . . .	Number 00B6		
T2COUNT . . . . .	Number 0266		
TIME_OUT . . . . .	Number 0080		
TST_DRV_RDY_BK . . . . .	Number 0000		
TST_DRV_RDY_INT . . . . .	Number 0010		
T_DAY . . . . .	N PROC FE6E	CODE	Length =0037
T_END . . . . .	L NEAR FE43	CODE	
T_HI . . . . .	L NEAR FEC5	CODE	
T_HI_ORDER . . . . .	L WORD 006E	DATA	
T_INC . . . . .	L NEAR FEBB	CODE	
T_INT . . . . .	N PROC FE45	CODE	Length =0047
T_LO_ORDER . . . . .	L WORD 006C	DATA	
T_NFE . . . . .	L NEAR FET8	CODE	
T_NFF . . . . .	L NEAR FETE	CODE	
T_OFI . . . . .	L NEAR FEB1	CODE	
T_OVERFLOW . . . . .	L BYTE 0070	DATA	
T_SET . . . . .	L NEAR FE95	CODE	
VECTOR . . . . .	N PROC FFF0	CODE	Length =000E
V_3X8 . . . . .	L BYTE 0065	DATA	
V_6845 . . . . .	L NEAR F262	CODE	
V_APAGE . . . . .	L BYTE 0062	DATA	
V_BAS6845 . . . . .	L WORD 0063	DATA	
V_BELL . . . . .	N PROC F54E	CODE	Length =0025
V_BS . . . . .	L NEAR F4C3	CODE	
V_CLR . . . . .	L NEAR F2F5	CODE	
V_CLR_BOT . . . . .	L NEAR F2F5	CODE	
V_CLR_FAST . . . . .	L NEAR F33F	CODE	
V_CLR_FLP . . . . .	L NEAR F341	CODE	
V_CLR_HI . . . . .	L NEAR F30A	CODE	
V_CLR_LO . . . . .	L NEAR F310	CODE	
V_CLR_LFP . . . . .	L NEAR F300	CODE	
V_CLR_MIT . . . . .	L NEAR F325	CODE	
V_CLR_PAST . . . . .	L NEAR F33C	CODE	
V_CLR_ROM . . . . .	L NEAR F32E	CODE	
V_CLR_TOP . . . . .	L NEAR F377	CODE	
V_COL . . . . .	N PROC F41A	CODE	Length =002C
V_COLORPAL . . . . .	L BYTE 0066	DATA	
V_COLOUR . . . . .	L NEAR F08E	CODE	
V_COL_0 . . . . .	L NEAR F42F	CODE	
V_COL_1 . . . . .	L NEAR F436	CODE	
V_CR . . . . .	L NEAR F4CB	CODE	
V_CURPOS . . . . .	L WORD 0050	DATA	Length =0008
V_CURSIZE . . . . .	L WORD 0060	DATA	
V_CURS_POS . . . . .	N PROC F1F7	CODE	Length =001E
V_CURS_TYPE . . . . .	N PROC F1E9	CODE	Length =000E
V_DATA1 . . . . .	N PROC F045	CODE	Length =0020
V_DATA2 . . . . .	N PROC F04A	CODE	Length =0058
V_DHALLOW . . . . .	L NEAR D626	CODE	
V_FPOS . . . . .	N PROC F50D	CODE	Length =001E
V_FPOS_0 . . . . .	L NEAR F51F	CODE	
V_FPOS_LP . . . . .	L NEAR F518	CODE	
V_HEIGHT . . . . .	L WORD 000C	DATA	
V_IO . . . . .	N PROC F065	CODE	Length =003F
V_ECLEAR . . . . .	Number 0007		
V_ESCROLL . . . . .	Number 0004		
V_LFP . . . . .	L NEAR F47B	CODE	
V_LROW . . . . .	L NEAR F486	CODE	
V_MD_NO . . . . .	L BYTE F0A8	CODE	
V_MD_80 . . . . .	L BYTE F0B8	CODE	
V_MD_CLR . . . . .	L NEAR F171	CODE	
V_MD_CLR_2K . . . . .	L NEAR F16C	CODE	
V_MD_CLR_8K . . . . .	L NEAR F16E	CODE	
V_MD_CLR_GRAPHICS . . . . .	L NEAR F168	CODE	
V_MD_DBL . . . . .	L NEAR F169	CODE	
V_MD_ENABLE . . . . .	L BYTE F0F4	CODE	
V_MD_GRAPH . . . . .	L BYTE F0C4	CODE	

# ROM BIOS Listing

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V_MD_LEN . . . . . L WORD F0E4 CODE
V_MD_MONO . . . . . L BYTE F0D4 CODE
V_MD_WID . . . . . L BYTE F0EC CODE
V_MODE . . . . . L BYTE 0049 DATA
V_MV . . . . . L NEAR F295 CODE
V_MV_DM . . . . . L NEAR F370 CODE
V_MV_END . . . . . L NEAR F2F4 CODE
V_MV_FLP . . . . . L NEAR F2E7 CODE
V_MV_HI . . . . . L NEAR F2AA CODE
V_MV_LO . . . . . L NEAR F2B0 CODE
V_MV_LP . . . . . L NEAR F2A0 CODE
V_MV_NXT . . . . . L NEAR F2CA CODE
V_MV_PAST . . . . . L NEAR F2E5 CODE
V_MV_ROW . . . . . L NEAR F2D1 CODE
V_MV_SF . . . . . L NEAR F0A3 CODE
V_OVR_BITE . . . . . N PROC F273 CODE Length =000C
V_OVR_NOT_OK . . . . . L NEAR F1C4 CODE
V_OVR_OK . . . . . L NEAR F1C6 CODE
V_PAGE . . . . . N PROC F22C CODE Length =0047
V_PAGE_0 . . . . . L NEAR F23E CODE
V_PARMS . . . . . L BYTE F0A4 CODE
V_POINTER . . . . . Number 03B4
V_POSN . . . . . N PROC F52B CODE Length =0011
V_RAC . . . . . N PROC F37C CODE Length =002A
V_RAC_INBLANK . . . . . L NEAR F398 CODE
V_RAC_INLINE . . . . . L NEAR F392 CODE
V_RESET_BX . . . . . L NEAR D616 CODE
V_R_CURS_POS . . . . . N PROC F215 CODE Length =0017
V_SCRL_DM . . . . . N PROC F358 CODE Length =0021
V_SCRL_MODE_7 . . . . . L NEAR F356 CODE
V_SCRL_MV_AND_CLR . . . . . L NEAR F50C CODE
V_SCRL_POS . . . . . N PROC F4DE CODE Length =002F
V_SCRL_RET . . . . . L NEAR F34B CODE
V_SCRL_TTY . . . . . L NEAR F491 CODE
V_SCRL_TTY_GRAPHICS . . . . . L NEAR F4A0 CODE
V_SCRL_UP . . . . . N PROC P27F CODE Length =00DC
V_SET_CURS . . . . . L NEAR F210 CODE
V_SET_CUR_POS . . . . . L NEAR F256 CODE
V_SET_MODE . . . . . N PROC F0FC CODE Length =00ED
V_SET_MODE_COLOR . . . . . L NEAR F117 CODE
V_SET_MODE_LP . . . . . L NEAR F147 CODE
V_SET_NEW_CBR . . . . . L NEAR F48C CODE
V_STAT . . . . . N PROC F4CF CODE Length =000F
V_TBL . . . . . L WORD F045 CODE
V_TERMINAL . . . . . N PROC F446 CODE Length =0089
V_TERM_NOBELL . . . . . L NEAR F44D CODE
V_TERM_NOP . . . . . L NEAR F4BB CODE
V_TERM_RET . . . . . L NEAR F4B9 CODE
V_TOP . . . . . L WORD 004E DATA
V_TYT_DM . . . . . L NEAR F364 CODE
V_TYT_MD . . . . . N PROC F53C CODE Length =0012
V_TYT_OK . . . . . L NEAR F54C CODE
V_TYT_RAC . . . . . L NEAR F38A CODE
V_TYT_UP . . . . . L NEAR F287 CODE
V_TYT_WAC . . . . . L NEAR F3AE CODE
V_TYT_WC . . . . . L NEAR F3E7 CODE
V_WAC . . . . . N PROC F3A6 CODE Length =0039
V_WAC_END . . . . . L NEAR F3DA CODE
V_WAC_HI . . . . . L NEAR F3C5 CODE
V_WAC_LO . . . . . L NEAR F3CB CODE
V_WC . . . . . N PROC F3DF CODE Length =0038
V_WC_END . . . . . L NEAR F415 CODE
V_WC_HI . . . . . L NEAR F3FE CODE
V_WC_LO . . . . . L NEAR F404 CODE
V_WC_NEXT . . . . . L NEAR F3FE CODE
V_WIDTH . . . . . L WORD 004A DATA
W1 . . . . . L NEAR D460 CODE
W2 . . . . . L NEAR D46B CODE
WAIT_FOR_IRQS . . . . . N PROC D418 CODE Length =0023
WBUF_BX . . . . . Number 000F
WBUF_INT . . . . . Number 000F
WLONG_BX . . . . . Number 00E5
WRITE_BX . . . . . Number 000A
WRITE_MODE . . . . . Number 004B
WRITE_PORT . . . . . Number 0320
WRITE_PROTECT . . . . . Number 0003
W_FINISH . . . . . L NEAR D494 CODE
W ITS_DONE . . . . . L NEAR D486 CODE
W_REC . . . . . L NEAR E992 CODE
W_REC_BET . . . . . L NEAR EFA6 CODE
W_OWE . . . . . L NEAR EFA8 CODE

```

```

Warning Severe
Errors Errors
0 0

```

## ROM BIOS Change List

---

ROM Rev 1.1 August 10, 1984

Aug 8 16:40 1984 fdul.src:

Fix random value in DX during reset causing  
problem

```
Line 73  Add
        push  es
        cmp   ah, 0           ;Is it a reset command?
        jz    diskette_i01    ;Yes, so ignore drive
                                ;param.
```

```
Line 123 Add
        pop   es
```

Aug 8 16:40 1984 fdul.src:

Allow verify operation without valid buffer pointer  
(buffer not required)

```
        xor   bx,bx           ;Fool the DMAC into
        mov   es,bx           ;thinking there is a full
                                ;segment to play with.
```

Do not range check head number

Change

```
        and   ah,1           ;blow off high 7 bits.
to
        and   ah,07Fh       ;blow off bit 7.
```

Aug 8 16:41 1984 flags.src:

Change date of release in ROM

```
        db   '05/03/84'     ;release marker (exactly
                                ;8 bytes!!!!)
to
        db   '08/10/84'     ;release marker (exactly
                                ;8 bytes!!!!)
```

Aug 8 16:43 1984 fontl08.src:

Change 8 X 8 font to improve italics as displayed  
by 3rd party software

ROM BIOS  
Change List

---

Changed

DB	00h,00h,00h,00h		
DB	00h,00h,00h,00h	;	0
DB	07eh,081h,0a5h,081h		
DB	0bdh,099h,081h,07eh	;	1
DB	07eh,0ffh,0dbh,0ffh		
DB	0c3h,0e7h,0ffh,07eh	;	2
DB	036h,07fh,07fh,07fh		
DB	03eh,01ch,08h,00h	;	3
DB	08h,01ch,03eh,07fh		
DB	03eh,01ch,08h,00h	;	4
DB	018h,03ch,0e7h,0e7h		
DB	066h,018h,018h,03ch	;	5
DB	018h,03ch,07eh,0ffh		
DB	0ffh,07eh,018h,03ch	;	6
DB	00h,00h,018h,03ch		
DB	03ch,018h,00h,00h	;	7
DB	0ffh,0ffh,0e7h,0c3h		
DB	0c3h,0e7h,0ffh,0ffh	;	8
DB	00h,03ch,024h,042h		
DB	042h,024h,03ch,00h	;	9
DB	0ffh,0c3h,099h,0bdh		
DB	0bdh,099h,0c3h,0ffh	;	a
DB	01fh,07h,0dh,019h		
DB	078h,0cch,0cch,078h	;	b
DB	03ch,066h,066h,03ch		
DB	018h,07eh,018h,018h	;	c
DB	018h,014h,012h,012h		
DB	014h,070h,0f0h,060h	;	d
DB	01fh,011h,01fh,011h		
DB	013h,037h,072h,020h	;	e
DB	018h,0dbh,03ch,0e7h		
DB	03ch,0dbh,018h,00h	;	f
DB	040h,070h,07ch,07fh		
DB	07ch,070h,040h,00h	;	10
DB	01h,07h,01fh,07fh		
DB	01fh,07h,01h,00h	;	11
DB	018h,03ch,07eh,018h		
DB	018h,07eh,03ch,018h	;	12

---

DB	00h,033h,033h,033h		
DB	033h,00h,033h,00h	;	13
DB	07fh,0dbh,0dbh,07bh		
DB	01bh,01bh,01bh,00h	;	14
DB	03eh,061h,03ch,066h		
DB	066h,03ch,086h,07ch	;	15
DB	00h,00h,00h,00h		
DB	07eh,07eh,07eh,00h	;	16
DB	018h,03ch,07eh,018h		
DB	07eh,03ch,018h,07eh	;	17
DB	018h,03ch,07eh,018h		
DB	018h,018h,018h,018h	;	18
DB	018h,018h,018h,018h		
DB	018h,07eh,03ch,018h	;	19
DB	0ch,06h,07fh,06h		
DB	0ch,00h,00h,00h	;	1a
DB	018h,030h,07fh,030h		
DB	018h,00h,00h,00h	;	1b
DB	00h,00h,060h,060h		
DB	060h,07fh,07fh,00h	;	1c
DB	00h,024h,066h,0ffh		
DB	066h,024h,00h,00h	;	1d
DB	00h,00h,018h,03ch		
DB	07eh,0ffh,00h,00h	;	1e
DB	00h,0ffh,07eh,03ch		
DB	018h,00h,00h,00h	;	1f
DB	00h,00h,00h,00h		
DB	00h,00h,00h,00h	;	' ' 20
DB	018h,03ch,03ch,018h		
DB	018h,00h,018h,00h	;	'!' 21
DB	036h,036h,014h,00h		
DB	00h,00h,00h,00h	;	'"' 22
DB	036h,036h,07fh,036h		
DB	07fh,036h,036h,00h	;	'#' 23
DB	018h,03eh,060h,03ch		
DB	06h,07ch,018h,00h	;	'\$' 24
DB	00h,063h,066h,0ch		
DB	018h,033h,033h,00h	;	'%' 25

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ROM BIOS  
Change List

---

DB	01ch,036h,01ch,03bh		
DB	06eh,066h,03bh,00h	;	'&' 26
DB	018h,018h,030h,00h		
DB	00h,00h,00h,00h	;	' ' ' 27
DB	0ch,018h,030h,030h		
DB	030h,030h,018h,0ch	;	'(' 28
DB	030h,018h,0ch,0ch		
DB	0ch,0ch,018h,030h	;	'),' 29
DB	00h,066h,03ch,0ffh		
DB	03ch,066h,00h,00h	;	'*' 2a
DB	00h,018h,018h,07eh		
DB	018h,018h,00h,00h	;	'+' 2b
DB	00h,00h,00h,00h		
DB	00h,018h,018h,030h	;	',' 2c
DB	00h,00h,00h,07eh		
DB	00h,00h,00h,00h	;	'_ ' 2d
DB	00h,00h,00h,00h		
DB	00h,018h,018h,00h	;	'-' 2e
DB	03h,06h,0ch,018h		
DB	030h,060h,040h,00h	;	'/' 2f
DB	03eh,063h,067h,06fh		
DB	07bh,073h,03eh,00h	;	'0' 30
DB	0ch,01ch,0ch,0ch		
DB	0ch,0ch,03fh,00h	;	'1' 31
DB	01fh,033h,03h,0eh		
DB	018h,033h,03fh,00h	;	'2' 32
DB	01eh,033h,03h,0eh		
DB	03h,033h,01eh,00h	;	'3' 33
DB	0eh,01eh,036h,066h		
DB	07fh,06h,0fh,00h	;	'4' 34
DB	03fh,030h,03eh,03h		
DB	03h,033h,01eh,00h	;	'5' 35
DB	0eh,018h,030h,03eh		
DB	033h,033h,01eh,00h	;	'6' 36
DB	03fh,033h,03h,06h		
DB	0ch,0ch,0ch,00h	;	'7' 37
DB	01eh,033h,033h,01eh		
DB	033h,033h,01eh,00h	;	'8' 38



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DB	01eh,033h,031h,01fh		
DB	03h,06h,01ch,00h	;	'9' 39
DB	00h,018h,018h,00h		
DB	00h,018h,018h,00h	;	'.' 3a
DB	00h,018h,018h,00h		
DB	00h,018h,018h,030h	;	',' 3b
DB	06h,0ch,018h,030h		
DB	018h,0ch,06h,00h	;	'<' 3c
DB	00h,00h,07eh,00h		
DB	00h,07eh,00h,00h	;	'=' 3d
DB	030h,018h,0ch,06h		
DB	0ch,018h,030h,00h	;	'>' 3e
DB	03eh,063h,03h,06h		
DB	0ch,00h,0ch,00h	;	'?' 3f
DB	03eh,063h,06fh,06fh		
DB	06eh,060h,03eh,00h	;	'@' 40
DB	08h,01ch,036h,063h		
DB	07fh,063h,063h,00h	;	'A' 41
DB	07eh,033h,033h,03eh		
DB	033h,033h,07eh,00h	;	'B' 42
DB	01eh,033h,060h,060h		
DB	061h,033h,01eh,00h	;	'C' 43
DB	07ch,036h,033h,033h		
DB	033h,036h,07ch,00h	;	'D' 44
DB	07fh,031h,034h,03ch		
DB	034h,031h,07fh,00h	;	'E' 45
DB	07fh,031h,034h,03ch		
DB	034h,030h,078h,00h	;	'F' 46
DB	01eh,033h,060h,060h		
DB	067h,033h,01dh,00h	;	'G' 47
DB	063h,063h,063h,07fh		
DB	063h,063h,063h,00h	;	'H' 48
DB	03ch,018h,018h,018h		
DB	018h,018h,03ch,00h	;	'I' 49
DB	0fh,06h,06h,06h		
DB	066h,066h,03ch,00h	;	'J' 4a
DB	073h,036h,03ch,038h		
DB	03ch,036h,073h,00h	;	'K' 4b

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ROM BIOS  
Change List

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DB	078h,030h,030h,030h			
DB	030h,033h,07fh,00h	;	'L'	4c
DB	063h,077h,07fh,06bh			
DB	063h,063h,063h,00h	;	'M'	4d
DB	063h,073h,07bh,06fh			
DB	067h,063h,063h,00h	;	'N'	4e
DB	01ch,036ch,063h,063h			
DB	063h,036h,01ch,00h	;	'O'	4f
DB	07eh,033h,033h,03eh			
DB	030h,030h,078h,00h	;	'P'	50
DB	01ch,036h,063h,063h			
DB	063h,036h,01ch,07h	;	'Q'	51
DB	07eh,033h,033h,03eh			
DB	036h,033h,033h,00h	;	'R'	52
DB	03eh,063h,030h,018h			
DB	06h,063h,03eh,00h	;	'S'	53
DB	07eh,05ah,018h,018h			
DB	018h,018h,03ch,00h	;	'T'	54
DB	063h,063h,063h,063h			
DB	063h,063h,03eh,00h	;	'U'	55
DB	063h,063h,063h,063h			
DB	036h,01ch,08h,00h	;	'V'	56
DB	063h,063h,063h,06bh			
DB	06bh,07fh,036h,00h	;	'W'	57
DB	063h,063h,036h,01ch			
DB	036h,063h,063h,00h	;	'X'	58
DB	066h,066h,066h,03ch			
DB	018h,018h,03ch,00h	;	'Y'	59
DB	07fn,063h,06h,0ch			
DB	018h,033h,07fh,00h	;	'Z'	5a
DB	03ch,030h,030h,030h			
DB	030h,030h,03ch,00h	;	'['	5b
DB	020h,030h,018h,0ch			
DB	06h,03h,01h,00h	;	'\'	5c
DB	03ch,0ch,0ch,0ch			
DB	0ch,0ch,03ch,00h	;	']'	5d
DB	08h,01ch,036h,063h			
DB	00h,00h,00h,00h	;	' '	5e

---

DB	00h,00h,00h,00h		
DB	00h,00h,07fh,00h	;	'_' 5f
DB	018h,018h,0ch,00h		
DB	00h,00h,00h,00h	;	' ' 60
DB	00h,00h,03ch,06h		
DB	03eh,066h,03bh,00h	;	'a' 61
DB	070h,030h,03eh,033h		
DB	033h,033h,06eh,00h	;	'b' 62
DB	00h,00h,03eh,061h		
DB	060h,061h,03eh,00h	;	'c' 63
DB	0eh,06h,03eh,066h		
DB	066h,066h,03bh,00h	;	'd' 64
DB	00h,00h,03eh,063h		
DB	07fh,060h,03fh,00h	;	'e' 65
DB	01eh,033h,030h,07ch		
DB	030h,030h,078h,00h	;	'f' 66
DB	00h,00h,03bh,066h		
DB	066h,03eh,046h,03ch	;	'g' 67
DB	070h,030h,036h,03fh		
DB	033h,033h,073h,00h	;	'h' 68
DB	0ch,00h,01ch,0ch		
DB	0ch,0ch,01eh,00h	;	'i' 69
DB	0ch,00h,01eh,0ch		
DB	0ch,0cch,0cch,078h	;	'j' 6a
DB	070h,030h,033h,036h		
DB	03ch,036h,073h,00h	;	'k' 6b
DB	01ch,0ch,0ch,0ch		
DB	0ch,0ch,01eh,00h	;	'l' 6c
DB	00h,00h,066h,07fh		
DB	06bh,06bh,06bh,00h	;	'm' 6d
DB	00h,00h,06eh,033h		
DB	033h,033h,033h,00h	;	'n' 6e
DB	00h,00h,01eh,033h		
DB	033h,033h,01eh,00h	;	'o' 6f
DB	00h,00h,06eh,033h		
DB	033h,03eh,030h,078h	;	'p' 70
DB	00h,00h,03bh,066h		
DB	066h,03eh,06h,0fh	;	'q' 71
DB	00h,00h,06eh,03bh		

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ROM BIOS  
Change List

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DB	030h,030h,078h,00h	;	'r'	72
DB	00h,00h,03fh,060h			
DB	03ch,03h,07eh,00h	;	's'	73
DB	08h,018h,03eh,018h			
DB	018h,01bh,0eh,00h	;	't'	74
DB	00h,00h,066h,066h			
DB	066h,066h,03bh,00h	;	'u'	75
DB	00h,00h,063h,063h			
DB	036h,01ch,08h,00h	;	'v'	76
DB	00h,00h,063h,06bh			
DB	06bh,07fh,036h,00h	;	'w'	77
DB	00h,00h,063h,036h			
DB	01ch,036h,063h,00h	;	'x'	78
DB	00h,00h,066h,066h			
DB	066h,03eh,06h,07ch	;	'y'	79
DB	00h,00h,07eh,04ch			
DB	018h,032h,07eh,00h	;	'z'	7a
DB	0eh,018h,018h,070h			
DB	018h,018h,0eh,00h	;	'{'	7b
DB	0ch,0ch,00h,00h			
DB	0ch,0ch,0ch,00h	;	' '	7c
DB	070h,018h,018h,0eh			
DB	018h,018h,070h,00h	;	'}'	7d
DB	03bh,06eh,00h,00h			
DB	00h,00h,00h,00h	;	'~'	7e
DB	00h,08h,01ch,036h			
DB	063h,063h,07fh,00h	;		7f

to

DB	00h,00h,00h,00h,00h,00h,00h,00h	;		0
DB	7eh,81h,0a5h,81h,0bdh,99h,81h,7eh	;		1
DB	7eh,0ffh,0dbh,0ffh,0c3h,0e7h,0ffh,7eh	;		2
DB	6ch,0feh,0feh,0feh,7ch,38h,10h,00h	;		3
DB	10h,38h,7ch,0feh,7ch,38h,10h,00h	;		4
DB	38h,7ch,38h,0feh,0feh,7ch,38h,7ch	;		5
DB	10h,10h,38h,7ch,0feh,7ch,38h,7ch	;		6
DB	00h,00h,18h,3ch,3ch,18h,00h,00h	;		7
DB	0ffh,0ffh,0e7h,0c3h,0c3h,0e7h,0ffh,0ffh	;		8
DB	00h,3ch,66h,42h,42h,66h,3ch,00h	;		9
DB	0ffh,0c3h,99h,0bdh,0bdh,99h,0c3h,0ffh	;		a

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DB	0fh,07h,0fh,7dh,0cch,0cch,0cch,78h	;	b
DB	3ch,66h,66h,66h,3ch,18h,7eh,18h	;	c
DB	3fh,33h,3fh,30h,30h,70h,0f0h,0e0h	;	d
DB	7fh,63h,7fh,63h,63h,67h,0e6h,0c0h	;	e
DB	99h,5ah,3ch,0e7h,0e7h,3ch,5ah,99h	;	f
DB	80h,0e0h,0f8h,0feh,0f8h,0e0h,80h,00h	;	10
DB	02h,0eh,3eh,0feh,3eh,0eh,02h,00h	;	11
DB	18h,3ch,7eh,18h,18h,7eh,3ch,18h	;	12
DB	66h,66h,66h,66h,66h,00h,66h,00h	;	13
DB	7fh,0dbh,0dbh,7bh,1bh,1bh,1bh,00h	;	14
DB	3eh,63h,38h,6ch,6ch,38h,0cch,78h	;	15
DB	00h,00h,00h,00h,7eh,7eh,7eh,00h	;	16
DB	18h,3ch,7eh,18h,7eh,3ch,18h,0ffh	;	17
DB	18h,3ch,7eh,18h,18h,18h,18h,00h	;	18
DB	18h,18h,18h,18h,7eh,3ch,18h,00h	;	19
DB	00h,18h,0ch,0feh,0ch,18h,00h,00h	;	1a
DB	00h,30h,60h,0feh,60h,30h,00h,00h	;	1b
DB	00h,00h,0c0h,0c0h,0c0h,0feh,00h,00h	;	1c
DB	00h,24h,66h,0ffh,66h,24h,00h,00h	;	1d
DB	00h,18h,3ch,7eh,0ffh,0ffh,00h,00h	;	1e
DB	00h,0ffh,0ffh,7eh,3ch,18h,00h,00h	;	1f
DB	00h,00h,00h,00h,00h,00h,00h,00h	;,'	20
DB	30h,78h,78h,30h,30h,00h,30h,00h	;,'!	21
DB	6ch,6ch,6ch,00h,00h,00h,00h,00h	;,'"	22
DB	6ch,6ch,0feh,6ch,0feh,6ch,6ch,00h	;,'#'	23
DB	30h,7ch,0c0h,78h,0ch,0f8h,30h,00h	;,'\$'	24
DB	00h,0c6h,0cch,18h,30h,66h,0c6h,00h	;,'%'	25
DB	38h,6ch,38h,76h,0dch,0cch,76h,00h	;,'&'	26
DB	60h,60h,0c0h,00h,00h,00h,00h,00h	;,'"'	27
DB	18h,30h,60h,60h,60h,30h,18h,00h	;,'('	28
DB	60h,30h,18h,18h,18h,30h,60h,00h	;,'.)'	29
DB	00h,66h,3ch,0ffh,3ch,66h,00h,00h	;,'*'	2a
DB	00h,30h,30h,0fch,30h,30h,00h,00h	;,'+'	2b
DB	00h,00h,00h,00h,00h,30h,30h,60h	;,''	2c
DB	00h,00h,00h,0fch,00h,00h,00h,00h	;,'—'	2d
DB	00h,00h,00h,00h,00h,30h,30h,00h	;,'-'	2e
DB	06h,0ch,18h,30h,60h,0c0h,80h,00h	;,'/'	2f
DB	7ch,0c6h,0ceh,0deh,0f6h,0e6h,7ch,00h	;,'0'	30

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ROM BIOS  
Change List

---

DB	30h,70h,30h,30h,30h,30h,0fch,00h	;'1'	31
DB	78h,0cch,0ch,38h,60h,0cch,0fch,00h	;'2'	32
DB	78h,0cch,0ch,38h,0ch,0cch,78h,00h	;'3'	33
DB	1ch,3ch,6ch,0cch,0feh,0ch,1eh,00h	;'4'	34
DB	0fch,0c0h,0f8h,0ch,0ch,0cch,78h,00h	;'5'	35
DB	38h,60h,0c0h,0f8h,0cch,0cch,78h,00h	;'6'	36
DB	0fch,0cch,0ch,18h,30h,30h,30h,00h	;'7'	37
DB	78h,0cch,0cch,78h,0cch,0cch,78h,00h	;'8'	38
DB	78h,0cch,0cch,7ch,0ch,18h,70h,00h	;'9'	39
DB	00h,30h,30h,00h,00h,30h,30h,00h	;'.'	3a
DB	00h,30h,30h,00h,00h,30h,30h,60h	;'.'	3b
DB	18h,30h,60h,0c0h,60h,30h,18h,00h	;'<'	3c
DB	00h,00h,0fch,00h,00h,0fch,00h,00h	;'=''	3d
DB	60h,30h,18h,0ch,18h,30h,60h,00h	;'>'	3e
DB	78h,0cch,0ch,18h,30h,00h,30h,00h	;'?''	3f
DB	7ch,0c6h,0deh,0deh,0deh,0c0h,78h,00h	;'@'	40
DB	30h,78h,0cch,0cch,0fch,0cch,0cch,00h	;'A'	41
DB	0fch,66h,66h,7ch,66h,66h,0fch,00h	;'B'	42
DB	3ch,66h,0c0h,0c0h,0c0h,66h,3ch,00h	;'C'	43
DB	0f8h,6ch,66h,66h,66h,6ch,0f8h,00h	;'D'	44
DB	0feh,62h,68h,78h,68h,62h,0feh,00h	;'E'	45
DB	0feh,62h,68h,78h,68h,60h,0f0h,00h	;'F'	46
DB	3ch,66h,0c0h,0c0h,0ceh,66h,3eh,00h	;'G'	47
DB	0cch,0cch,0cch,0fch,0cch,0cch,0cch,00h	;'H'	48
DB	78h,30h,30h,30h,30h,30h,78h,00h	;'I'	49
DB	1eh,0ch,0ch,0ch,0cch,0cch,78h,00h	;'J'	4a
DB	0e6h,66h,6ch,78h,6ch,66h,0e6h,00h	;'K'	4b
DB	0f0h,60h,60h,60h,62h,66h,0feh,00h	;'L'	4c
DB	0c6h,0eeh,0feh,0feh,0d6h,0c6h,0c6h,00h	;'M'	4d
DB	0c6h,0e6h,0f6h,0deh,0ceh,0c6h,0c6h,00h	;'N'	4e
DB	38h,6ch,0c6h,0c6h,0c6h,6ch,38h,00h	;'O'	4f
DB	0fch,66h,66h,7ch,60h,60h,0f0h,00h	;'P'	50
DB	78h,0cch,0cch,0cch,0dch,78h,1ch,00h	;'Q'	51
DB	0fch,66h,66h,7ch,6ch,66h,0e6h,00h	;'R'	52
DB	78h,0cch,0e0h,70h,1ch,0cch,78h,00h	;'S'	53
DB	0fch,0b4h,30h,30h,30h,30h,78h,00h	;'T'	54
DB	0cch,0cch,0cch,0cch,0cch,0cch,0fch,00h	;'U'	55
DB	0cch,0cch,0cch,0cch,0cch,78h,30h,00h	;'V'	56

---

DB	0c6h,0c6h,0c6h,0d6h,0feh,0eeh,0c6h,00h;	'W'	57
DB	0c6h,0c6h,6ch,38h,38h,6ch,0c6h,00h	;'X'	58
DB	0cch,0cch,0cch,78h,30h,30h,78h,00h	;'Y'	59
DB	0feh,0c6h,8ch,18h,32h,66h,0feh,00h	;'Z'	5a
DB	78h,60h,60h,60h,60h,60h,78h,00h	;'['	5b
DB	0c0h,60h,30h,18h,0ch,06h,02h,00h	;'\'	5c
DB	78h,18h,18h,18h,18h,18h,78h,00h	;'J'	5d
DB	10h,38h,6ch,0c6h,00h,00h,00h,00h	;' '	5e
DB	00h,00h,00h,00h,00h,00h,00h,0ffh	;'—'	5f
DB	30h,30h,18h,00h,00h,00h,00h,00h	;'”	60
DB	00h,00h,78h,0ch,7ch,0cch,76h,00h	;'a'	61
DB	0e0h,60h,60h,7ch,66h,66h,0dch,00h	;'b'	62
DB	00h,00h,78h,0cch,0c0h,0cch,78h,00h	;'c'	63
DB	1ch,0ch,0ch,7ch,0cch,0cch,76h,00h	;'d'	64
DB	00h,00h,78h,0cch,0fch,0c0h,78h,00h	;'e'	65
DB	38h,6ch,60h,0f0h,60h,60h,0f0h,00h	;'f'	66
DB	00h,00h,76h,0cch,0cch,7ch,0ch,0f8h	;'g'	67
DB	0e0h,60h,6ch,76h,66h,66h,0e6h,00h	;'h'	68
DB	30h,00h,70h,30h,30h,30h,78h,00h	;'i'	69
DB	0ch,00h,0ch,0ch,0cch,0cch,78h	;'j'	6a
DB	0e0h,60h,66h,6ch,78h,6ch,0e6h,00h	;'k'	6b
DB	70h,30h,30h,30h,30h,30h,78h,00h	;'l'	6c
DB	00h,00h,0cch,0feh,0feh,0d6h,0c6h,00h	;'m'	6d
DB	00h,00h,0f8h,0cch,0cch,0cch,0cch,00h	;'n'	6e
DB	00h,00h,78h,0cch,0cch,0cch,78h,00h	;'o'	6f
DB	00h,00h,0dch,66h,66h,7ch,60h,0f0h	;'p'	70
DB	00h,00h,76h,0cch,0cch,7ch,0ch,1eh	;'q'	71
DB	00h,00h,0dch,76h,66h,60h,0f0h,00h	;'r'	72
DB	00h,00h,7ch,0c0h,78h,0ch,0f8h,00h	;'s'	73
DB	10h,30h,7ch,30h,30h,34h,18h,00h	;'t'	74
DB	00h,00h,0cch,0cch,0cch,0cch,76h,00h	;'u'	75
DB	00h,00h,0cch,0cch,0cch,78h,30h,00h	;'v'	76
DB	00h,00h,0c6h,0d6h,0feh,0feh,6ch,00h	;'w'	77
DB	00h,00h,0c6h,6ch,38h,6ch,0c6h,00h	;'x'	78
DB	00h,00h,0cch,0cch,0cch,7ch,0ch,0f8h	;'y'	79
DB	00h,00h,0fch,98h,30h,64h,0fch,00h	;'z'	7a
DB	1ch,30h,30h,0e0h,30h,30h,1ch,00h	;'{'	7b
DB	18h,18h,18h,00h,18h,18h,18h,00h	;' '	7c

---

ROM BIOS  
Change List

---

```
DB 0e0h,30h,30h,1ch,30h,30h,0e0h,00h ;'} 7d
DB 76h,0dch,00h,00h,00h,00h,00h,00h ;'~' 7e
DB 00h,10h,38h,6ch,0c6h,0c6h,0feh,00h ;' ' 7f
```

Aug 8 16:44 1984 graph.src:  
Solved 640 X 400 inverse video mode problem

Changed

```
test byte ptr [si],80H ;is upper left bit of
;char = 0 or 1?
```

to

```
test byte ptr ss:[si],80H ;is upper left bit of
;char = 0 or 1?
```

Changed

```
not byte ptr [si] ;reverse the reversed
;byte for matching
```

to

```
not byte ptr ss:[si] ;reverse the reversed
;byte for matching
```

Aug 8 16:48 1984 pwrup1.src:  
Changed release date and display on boot

Changed

```
banner_m db "Resident Diagnostics",CR,LF
db "Rev 1.0 May 1984",CR,LF,LF,
NUL
```

to

```
db "Rev 1.1 Aug 1984",CR,LF,LF
banner_m db "Resident Diagnostics",CR,LF,
LF
db NUL
```



## Notes on Enhancements in ROM BIOS 1.21

---

**Introduction** These notes describe the differences between the 1.0, 1.1 and 1.21 ROM BIOS for the AT&T PC 6300. The notes first describe the differences between the 1.0 and 1.1 ROMs, then describe the differences between the 1.1 and 1.21 ROMs.

**Differences  
Between  
ROM 1.0  
and  
ROM 1.1**

The differences between the 1.0 and 1.1 ROM are:

- In the floppy disk utility, the random value of the DX register is fixed.
- In the floppy disk utility, the verify operation without a valid buffer pointer is allowed.
- In the floppy disk utility, the value checking for head number has been eliminated.
- The ROM release date has been changed to 08/10/84.
- The 8x8 font has been changed to improve italics displayed by some third-party software.
- The 640x400 inverse video mode now works properly.
- The displayed release marker has been changed to "Rev 1.1."
- LOTUS™ Symphony runs on the 1.1 ROM.

These changes are explained in detail in the "System Programmer's Guide" on pages 8-177 to 8-188.

**Differences  
Between  
ROM 1.1  
and  
ROM 1.21**

ROM BIOS 1.21 was introduced to solve problems with the use of external vendor's hard disk expansion boxes, to support the 20 megabyte hard disk drives, and to better initialize the second communications port.

The differences between ROM 1.1 and 1.21 are:

- The code sent to the parallel port during power up diagnostics has been changed from 80H to 3fH.
- In INT 15H, a near return has been changed to a far return.
- INT 18H is enhanced to display a message "ROM BASIC not present, Press RESET to reboot ..." and wait for a key press before re-booting.
- Code has been added to reset the Display Enhancement Board during a warm boot.
- The reset code has been changed to origin at 0E05Bh.
- The floppy disk drive motor delay has been changed from a range of 0-500 milliseconds to 250-750 milliseconds.
- The order of executing HDU code and external ROM code has been reversed to execute the internal HDU code, then check for optional ROMs.

- In order to simplify support for external hard disk drives with controllers other than the DTC controller, a check of DIPSW-1 position 3 on the motherboard (at location 7W) has been added. Position 3 of DIPSW-1 has been defined as:

ON = use indigenous hard disk code  
OFF = use external hard disk code

- A test has been added to check for the presence of the 8530 alternate communications chip.
- The initialization of COM2: has been improved.
- Code has been added in an INT 10H routine that enables the video after scroll up is performed.
- An incompatibility that prevented the Softech P-System from booting has been corrected.
- The high 128 characters of the 8x8 font and the low 128 characters of the 8x16 font have been changed to provide better alignment of the characters within the 8x8 and 8x16 fonts.
- Support for 20 megabyte disk drives has been added to the disk parameter table. Drive type 6 is a Seagate ST225, drive type 7 is a Miniscribe 3425, and drive type 8 is a CMI 6426.

- The disk parameters for the CDC WREN drive have been changed to 697 cylinders to allow for the full capacity of the drive.
- Support in INT 11H was added for 8087 switch setting.
- The ROM release date has been changed to 02/28/85.
- The displayed release marker has been changed to "Rev 1.21."

# ROM Revision 1.1 to ROM Revision 1.21 Source File Differences

---

```
      8/10/84          2/14/85
      < = rom1.1      > = rom1.20

Source Module:      comm2.src

<   call rs_stat          ; get return status
---
> ;; call rs_stat      *E912*   ; get return status

Source Module:      fdul.src

> * mikef      9/18/84      Changed motor delay routine.
> * mikef      01/11/85     If reset cmd don't do check valid.
> * mikef      02/14/85     Made the reset code callable.

<   jz   diskette_io1      ; Yes, so ignore drive parm.
---
>   jz   diskette_io2 *EC73*   ; Yes, so ignore drive parm.

<   cld                      ; Autoincrement for strings.

<   jnz  f_rd1              ; 1 = 250 ms motors, no delay
---
>   mov  cx,250             *ED60*   ;
>   jnz  f_rd_loop *ED63*     ; 1 = 500 ms motors.

Source Module:      flags.src

> * mikef      9/18/84      Changed reset pointer to point to org'ed
> *             location.
> * mikef      10/02/84     Included hdu1.asm

> include pwrupia.asm

> include hdu1.asm
>
>
> include int18.asm
>

<   dw   diagnostics_1    ; instruction pointer cs:(offset diagnostics_1)
---
>   dw   i_hard_reset    ; instruction pointer cs:(offset i_hard_reset)

<   db   '08/10/84'      ; release marker (exactly 8 bytes!!!!)
---
>   db   '02/14/85'      ; release marker (exactly 8 bytes!!!!)
```

# ROM BIOS

## 1.21

Source Module: fonthi8.src

```
<
< * NAME DATE ACTION
< * -----
< * robert 4/30/84 Corrected '^'
< * robert 5/01/84 Corrected char 182
---
> * name date action
> * ----
> * seagrave 12/13/84 new font table
< fonthi8 endp
---
> fonthi8 endp
```

Source Module: fontlo16.src

```
< * NAME DATE ACTION
< * -----
< * robert 4/30/84 corrected 'p'.
< * robert 5/4/84 corrected 'i'
---
> * NAME DATE ACTION
> * ----
> * seagrave 12/14/84 new font table
> * yin 2/5/85 new font table
```

Source Module: graph.src

```
> * mikef 2/13/85 Moved grf_light_pen to vid.src.
```

```
<
<
;=====
< ;
< ; Read Light Pen function code = 04h
< ;
< ; Input: None.
< ; Output: ah = 0 light pen switch not down/not triggered
< ; ah = 1 implies:
< ; (dh,dl) = (row,col) of character light pen
< ; position from (0,0)
< ; ch = raster line (0-199)
< ; bx = pixel column (0-319,0-639)
< ;
< ; Trash: None. ???
< ;
;=====
<
< grf_light_pen proc near
<
< xor ah,ah ; return ah = 0 for now (al intact)...
```

---

```
<   ret
<
<   grf_light_pen      endp

Source Module:      hdu.src

< /*
< *
< * NAME DATE        ACTION
---
> /* NAME DATE        ACTION

> * mikef      10/02/84  Moved h_data2 to hdu1.src to make rom in
> *            low rom for an ORG.
> * mikef      10/23/84  Changed documentation describing dip
> *            switches.
> * mikef      11/02/84  Fixed bug in reset call.
> * mikef      12/06/84  Corrected no. of cyls for CDC drive.
> * mikef      12/18/84  Added type 6 and type 7 drives.
> * mikef      12/20/84  Corrected write precomp for Seagate ST225.
> * mikef      01/08/84  Changed int 19 to jmp bt_int.
> * mikef      01/21/84  Added type 8 in parameter_table and changed
> *            some other parameters per Olivetti memo.

<   int      18h                ; initiate reboot through ROM BASIC INT.
---
>   jmp bt_int      *D124*      ; initiate reboot through floppy.
> ; int      19h                ; initiate reboot through ROM BASIC
INT.

< hdu_parm_tbl:
---
> hdu_parm_tbl proc near

< ; The next six are the supported drives:
---
> ; The next nine are the supported drives:

<   parameter_table <>                ;type 3: 10mb drive
---
>   *D17C*   parameter_table <,,128>    ;type 3: 10mb drive

<   parameter_table <644d,5d,128d,128d> ;type 5: CDC Wren
---
>   parameter_table <697d,5d,697d,0>    ;type 5: CDC Wren
>   parameter_table <612,4,256,256,,3>   ;type 6: Seagate ST225.
>   parameter_table <612,4,128,128,,3>   ;type 7: Miniscribe 3425
>   ; and CMI CM 4426.
>   *D1CC*   parameter_table <640,4,256,256,,3> ;type 8: CMI CM6426.

> hdu_parm_tbl endp
>

<   int 40h                ; if not, pass to the FDU driver
```

---

ROM BIOS  
1.21

```
<
---
> ;; int 40h          ; if not, pass to the FDU driver
>   jmp near ptr fd_io  *D1E1*  ;; rom floppy driver.
>                               ;; will not return.

<   int 40h          ; if so, must reset FDU also
---
> ;; int 40h          ; if so, must reset FDU also
>   pushf            ;; simulate an int because
>                               ;; fd_io simulates an iret.
>   push cs          *D1EE*  ;; Make it look like a far call.
>   call near ptr fd_io *D1EF*  ;; rom floppy driver.

> ; Test to see if the vector at location 0:100 points to me. If it does it
> ; means that an optional rom thinks I'm the floppy driver so I'll just
return.
>

< ; drive 0          0  1      2  3      2  3
< ; drive 1          0  1      2  3      2  3
---
> ;; drive 0          0  1      2  3      2  3
> ;; drive 1          0  1      2  3      2  3

>

<   and al,07fh      ; ignore top switch!
---
> ;; and al,07fh      ; ignore top switch!

< h_data2 proc
<
< h_intro_m         db  'Fixed Disk Formatting Utility',CR,LF
<                   db  'All data on the specified fixed disk will be erased.'
<                   db  CR,LF
<                   db  'Enter fixed disk number (1 to 8) or "Q" to quit: ',NUL
<
< h_fmt_m           db  CR,LF,'Formatting Fixed Disk...',CR,LF,NUL
<
< h_pass_m          db  'Format is complete.',CR,LF
<                   db  'Proceed with FDISK and FORMAT.',NUL
<
< h_none_m          db  'Error: No fixed disk drive exists for this
number.',NUL
<
< h_err_m           db  'Format Error.  Code: ',NUL
<
< h_data2 endp
```



---

Source Module: mem.src

```
< /*
< *
< * NAME DATE ACTION
---
> /* NAME DATE ACTION
```

```
< *
---
> * mikef 9/18/84 Changed m_cass proc to far.
>
< m_cass proc near
---
> m_cass proc far #F8F9*
```

Source Module: nmi.src

```
< /*
< *
< * NAME DATE ACTION
---
> /* NAME DATE ACTION
```

```
> * mikef 12/06/84 Added code to inform user that a parity
> * error happend.
> ; And ENABLE_PARITY
> ;
< assume cs:code, ds:nothing, es:nothing, ss:nothing
>
> push ax #F85F*
> in al,ControlC ; High two bits indicate parity.
> and al,0C0h ; Mask of low 6 bits.
> jz n_out ; It wasn't a parity interrupt!
> mov si,offset parity1_m ; System board message.
> rol al,1
> jc n_1
> mov si,offset parity2_m ; Expansion board message.
> n_1:
> call DRomString
> hlt
> n_out:
> pop ax #F874*
```

Source Module: pwrup0.src

```
<
<
< /*
< *
< * NAME DATE ACTION
---
> /* NAME DATE ACTION
```

```
> * mikef 9/18/84 Changed OK code to parallel port for mfg.
```

# ROM BIOS

## 1.21

---

```
> * mikef      10/02/84  Changed int 18 trap to go to 'basic_trap'.
> * mikef      10/11/84  Added test to see if 8530 is really there.
> * mikef      11/20/84  Now executes internal HDU code before
> *              optional ROM checking.
> * mikef      12/07/84  Changed OK code to '3Fh' for mfg.
> * mikef      12/13/84  Added call to enable parity interrupt.
> * mikef      12/17/84  Added switch reading for indigenous HDU code.
```

```
>
>   mov  al,0Fh                *E2FB*   ;;
>   out  scc_ctl_a,al          ;; read register 15.
>   in   al,scc_ctl_a          ;;
>   test al,1                  ;;
>   jnz  i_no_sccs            *E303*   ;; LSB of rr15 is always 0.
>
```

```
> ; Call internal HDU init code.
```

```
> ;-----
```

```
>
>   assume  cs:code, ds:abs0, es:nothing, ss:stack_ram
>
>   xor  ax,ax                *E33D*   ; satisfy assumptions
>   mov  ds,ax
>
>   in   al,sys_conf_b        ;; port 67h.
>   test al,4                 ;; test switch bit 2
>   jnz  i_hdu_ok             ;; if set, skip init
>
>   mov  si,cs:(offset i_hdu_m)
>   call DRomString           ; print test message
>
>   call h_init
>
>   assume  cs:code, ds:data, es:nothing, ss:stack_ram
>
>   mov  ds,word ptr cs:[set_ds_word] ; satisfy assumptions
>   cmp  byte ptr ds:[hf_num],0       ; number of hard disks.
>   jnz  i_hdu_ok                     ; if ok, leave everything alone.
>
>   mov  sp,100h                   ; re-initialize stack
>   cli                                     ; disable interrupts
>   call i_vector                   ; re-install old vectors
>   sti                 *E363*
> i_hdu_ok:
```

```
> ;-----
```

```
< ;-----
```

```
< ; HDU Test
```

```
< ;-----
```

```
<   assume  cs:code, ds:abs0, es:nothing, ss:stack_ram
```

```
<
<   xor  ax,ax           ; satisfy assumptions
<   mov  ds,ax
<
< ; Check int 41h to see if any one installed a HDU parameter table
pointer.
<
<   mov  ax,word ptr ds:[(4*41h)+0000h]
<   or   ax,word ptr ds:[(4*41h)+0002h]
<   jnz  i_hdu_ok       ; if so, let them be...
<
< ; If not, call HDU initialization routine.
<
<   mov  si,cs:(offset i_hdu_m)
<   call DRomString     ; print test message
<
<   call h_init
<
<   assume  cs:code, ds:data, es:nothing, ss:stack_ram
<
<   mov  ds,word ptr cs:[set_ds_word] ; satisfy assumptions
<   cmp  byte ptr ds:[hf_num],0      ; number of hard disks.
<   jnz  i_hdu_ok                   ; if ok, leave everything alone.
<
<   mov  sp,100h                    ; re-initialize stack
<   cli                                     ; disable interrupts
<   call i_vector                    ; re-install old vectors
<
< i_hdu_ok:
<
>   call DCrLf                       *E3BE*   ;;
<
< ; and al,10111100b                 ; p_timer & kb & dsk at this point.
<
<   assume  cs:code, ds:abs0, es:nothing, ss:stack_ram
<
<   xor  ax,ax
<   mov  ds,ax
<   mov  word ptr ds:[int18locn+0000h],cs:(offset bt_int)
<   mov  word ptr ds:[int18locn+0002h],cs ; (ROM BASIC not
available)
<
< ; Initialize & enable NMI's (parity register).
<
<   mov  dx,p_kctrl
<   in  al,dx
<   or  al,030h                ; enable bits #5 & #4
<   out dx,al
<
```

ROM BIOS  
1.21

```
<   mov  al,80h                ; OK status
---
>   mov  al,3Fh                *E49E*      ; OK status

Source Module:      pwrup1.src

> * mikef      09/18/84  Put in org for reset vector.
> * mikef      12/10/84  Added parity stuff.
> * mikef      01/08/85  Clear the screen before printing messages.

<       db  'Rev 1.1',CR,LF,LF
---
>       db  'Rev 1.20',CR,LF,LF

>   or   cx,cx                *DD68*      ;; if zero then it was a parity error.
>   jnz  i_d_e                ;;
>   mov  si,cs:(offset parity1_m) *DD6C*   ;;
> i_d_e:                ;;

>   mov  ax,3                *DD28*      ; mode co80
>   int  10h                *DD2B*      ; Clear screen.
>

> skip_parity:

<       assume  cs:code, ds:data, es:abs0, ss:stack_ram
<
>   ORG  0E05Bh                ;;
>
> i_hard_reset proc                ;;
>   jmp  diagnostics_1        ;;
> i_hard_reset endp            ;;
>

<   push ds                    ; save registers
---
> ;; Here is the code for putting the DEB in Transparent Mode.

>   push ax                    *E05E*
>   push dx
>   mov  dx,03DDh              ;; DEB I/O Address Register port address
>   mov  al,1                  ;; select Mode Control Register
>   out  dx,al
>
>   inc  dx                    ;; DEB Mode Control Register address
>   inc  dx
>   dec  al                    ;; set DEB Transparent Mode
>   out  dx,al                ;;
>   pop  dx
>   pop  ax                    *E06C*
```

```
> push ds ; save registers
>
< mov al,cl ; get data from switches.
---
> in al,sys_conf_a *E0B4* ; Read port 66h.
> and al,010h ; Keep 80B7 bit only.
> shr al,1 ; Move to bit one.
> shr al,1
> shr al,1
> or al,cl *E0BE* ; get data from switches.
> ; NOTE: If CX is zero and ZF is nz then parity error occurred.
>
> ;; Toggle parity latch
> in al,p_kctrl *E1A1* ;; read B port. (61h)
> or al,30h ;; toggle bits 4 & 5.
> out p_kctrl,al ;;
> and al,0CFh ;;
> out p_kctrl,al *E1A9* ;;
>
```

Source Module: pwrup4.src

```
< /*
< *
< * NAME DATE ACTION
---
> /* NAME DATE ACTION
> * mikef 12/06/84 Added 'enable_parity'
>
>
> enable_parity proc ;;
>
> push ax *E5C5*
> in al,p_kctrl ;; read B port. (61h)
> or al,30h ;; enable bits 4 & 5.
> out p_kctrl,al ;;
> and al,0CFh ;;
> out p_kctrl,al ;;
> mov al,nmi_enable ;; 80h.
> out nmi_enable_port,al ;; defined in sysdata.src (A0h)
> pop ax ;;
> ret ;;
>
> parity1_m db 'Parity error on system board',NUL ;;
> parity2_m db 'Parity error on expansion board',NUL ;;
> *E61C*
> enable_parity endp ;;
```

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---

Source Module: sysdata.src

```
< ControlB equ 062h ; 80B7, etc.
-----
> ControlC equ 062h ; bit #7: Ram parity check.
> ; bit #6: I/O channel parity check.
> ; bit #1: 80B7 installed

< ; bits #3 - #2: reserved for HDU type
-----
> ; bit #3 not defined.
> ; bit #2 - 0 = use indiginous HDU code.
> ; 1 = do not use indiginous HDU code.

> nmi_enable equ 80h
> nmi_enable_port equ 0A0h
```

Source Module: vector.src

```
< dw bt_int ; int18locn (We Don't Have BASIC!)
-----
> dw basic_trap ; int18locn see int18.src
```

Source Module: vid.src

```
< /*
< *
< * NAME DATE ACTION
-----
> /* NAME DATE ACTION

> * mikef 10/25/84 Added code in scroll up to enable video.
> * mikef 02/13/85 Moved grf_light_pen from graph.src to here.

> mov dx,03D8h *F356* ; video enable register.
> out dx,al *F359* ; enable video.

< ; We didn't disable display during vertical retrace...
-----
> ; We didn't disable display during vertical retrace...but enable it
anyway.
>
>
;=====
> ;
> ; Read Light Pen function code = 04h
> ;
> ; Input: None.
> ; Output: ah = 0 light pen switch not down/not triggered
> ; ah = 1 implies:
> ; (dh,dl) = (row,col) of character light pen
> ; position from (0,0)
> ; ch = raster line (0-199)
> ; bx = pixel column (0-319,0-639)
```

---

```
> ;  
> ; Trash:  None.  ???  
> ;  
> ;-----  
>  
> grf_light_pen    proc near  
>     xor  ah,ah          ; return ah = 0 for now (al intact)...  
>     ret  
>  
> grf_light_pen    endp
```