

YAC516

DAC16-L

Delta Sigma Modulation D/A Converter with 8 times Over-sampling Filter

■ OVERVIEW

The YAC516 is a delta sigma D/A converter with 8 times over-sampling filter, designed for use with YAMAHA sound generator chips. Because of the built-in post filter and output buffer, high quality sound system can be designed with a small number of components.

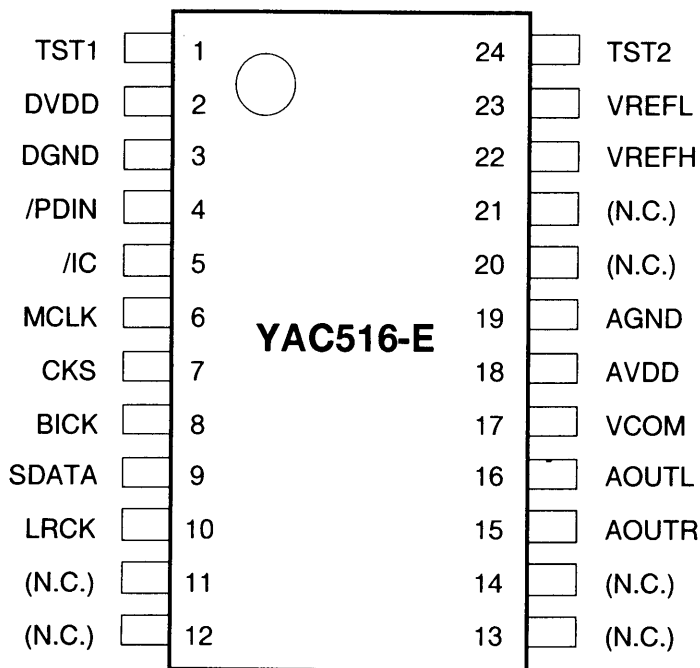
In addition, 3.3V operation and power down mode make the YAC516 most suitable for the sound system of Green PC and Notebook PC.

■ FEATURES

- 1-bit delta sigma DAC.
- Sampling rate ranging from 10kHz to 50kHz.
- On chip 8 times over-sampling filter.
 - Passband: 20 kHz (@ $f_s=44.1$ kHz)
 - Passband ripple: ± 0.02 dB
 - Stopband attenuation: 57 dB
- On chip post filter.
- On chip output buffer.
- High tolerance to clock jitter.
- THD+N: -86 dB.
- Dynamic range: 92 dB.
- Wide voltage operation: 3V ~ 5.25V
- Low power dissipation: 75 mW at 5V.
- 24 pin SSOP (YAC516-E), 28 pin SOP (YAC516-M).

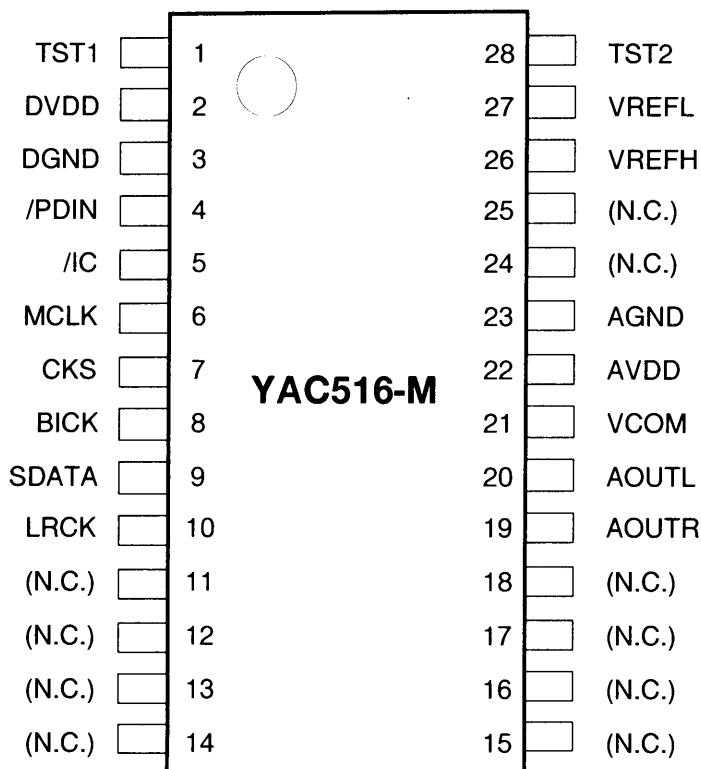
■ PIN LAYOUT

YAC516-E



24pin SSOP Top View

YAC516-M



28pin SOP Top View

■ PIN DESCRIPTION

No		Pin Name	I/O	Function
24SSOP	28SOP			
1	1	TST1	I-	Test Pin Must be left floating or tied DGND
2	2	DVDD	-	Digital power supply pin (+5V)
3	3	DGND	-	Digital ground pin
4	4	/PDIN	I	Power down input pin When this is brought "L" level, the YAC516 is switched to power down mode and is held in reset. The YAC516 should always be reset upon power-up.
5	5	/IC	I	Initial clear input pin This pin has the same function as the /PDIN pin. The /IC pin and /PDIN pin are ANDed internally.
6	6	MCLK	I	Master clock input pin An external CMOS clock should be input on this pin. The input clock frequency is selected by CKS pin.
7	7	CKS	I	Master clock select pin "H": MCLK=384fs "L": MCLK=256fs
8	8	BICK	I	Serial bit input clock pin This clock is used to latch SDATA.
9	9	SDATA	I	Serial data input pin 2's compliment MSB-first data is input on this pin.
10	10	LRCK	I	L/R clock pin This input determines which channel is currently being input on the SDATA pin. "H":Lch, "L":Rch
15	19	AOUTR	OA	Rch analog output pin
16	20	AOUTL	OA	Lch analog output pin
17	21	VCOM	OA	Common voltage pin, AVDD/2 Normally connected to AGND with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic capacitor.
18	22	AVDD	-	Analog power supply pin(+5V)
19	23	AGND	-	Analog ground pin
22	26	VREFH	IA	"H" voltage reference input pin The differential voltage between VREFH and VREFL inputs set the analog output range. The VREFH pin is normally connected to AVDD and the VREFL pin is connected to AGND. A 0.1μF ceramic capacitor should be as near to both pins.
23	27	VREFL	IA	"L" voltage reference input pin
24	28	TST2	O	Test pin Must be left floating.

All pins except the above pins are NC (No Connection) pins. Do not connect externally.

I:-Input pin with pull down resistor IA:Analog input pin OA:Analog output pin

■ BLOCK DIAGRAM

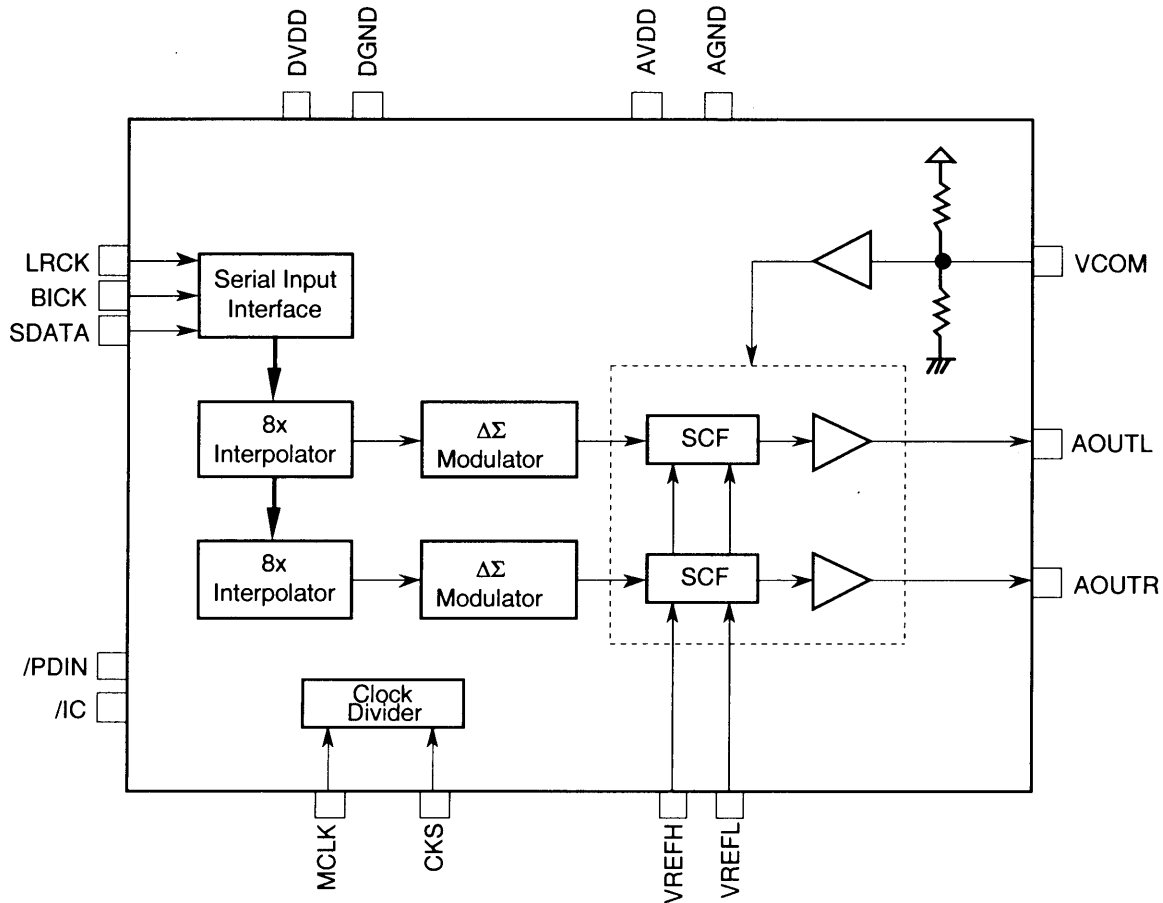


Fig 1. Block diagram

■ FUNCTION

1. System Clock

The external clock which are required to operate the YAC516 are MCLK(256/384fs), LRCK(fs), BICK(32fs~). MCLK should be synchronized with LRCK but the phase is free of care. The frequency of MCLK is determined by the desired Input Word Rate (fs), and the setting of the Clock Select, CKS pins. Setting CKS to "L" level selects an MCLK frequency of 256fs while setting CKS to "H" level selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs x 2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the YAC516.

As the YAC516 includes the phase detect circuit using LRCK, the YAC516 is reset automatically when the synchronization is out of phase by changing the clock frequencies.

Therefore, the reset is not needed except only upon power-up. (Please refer to the "4.System Reset" section.)

All external clock(MCLK, BICK, LRCK) should always be present whenever the YAC516 is in normal operation mode(/PDIN = /RST = "H"). If these clock are not provided, the YAC516 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clock are not present, the YAC516 should be in the power-down mode (/PDIN = "L" or /RST = "L").

Table 1. Example of Master Clock

LRCK(fs) (kHz)	CKS	MCLK (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

2. Serial Data Interface

The YAC516 has three serial input pins(SDATA, BICK, LRCK). Data bits is clocked into the YAC516 via SDATA pin and is latched by LRCK. The data format is MSB-first and 2's compliment.

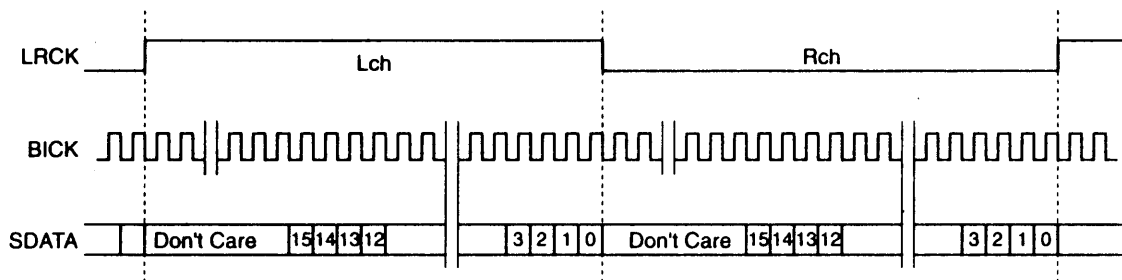


Fig 2. Data Input Format

3. Power-Down Mode

The YAC516 is placed in the power-down mode by setting /PDIN (or /IC) to "L" level. In the power-down mode, the analog output pins go floating.

4. System Reset

The YAC516 should be reset once by bringing /PDIN (or /IC) to "L" level upon power-up. The internal timing starts clocking by the rising edge of LRCK after exiting reset by MCLK. If the phase difference between LRCK and internal control signals is

larger than $+1/16 \sim -1/16$ of word period($1/f_s$), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK. Since RAM address shifts during this synchronization, the correct data would not be output until 18 sampled data input.

5. Grounding and Power Supply Decoupling

The DAC requires careful attention to power supply and grounding arrangement. Figure 3 shows a example of power arrangements which AVDD is supplied from a clean analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitor for high frequency should be as near to the YAC516 as possible, with the low value ceramic capacitor across VREFH and VREFL being the nearest.

6. SYSTEM DESIGN

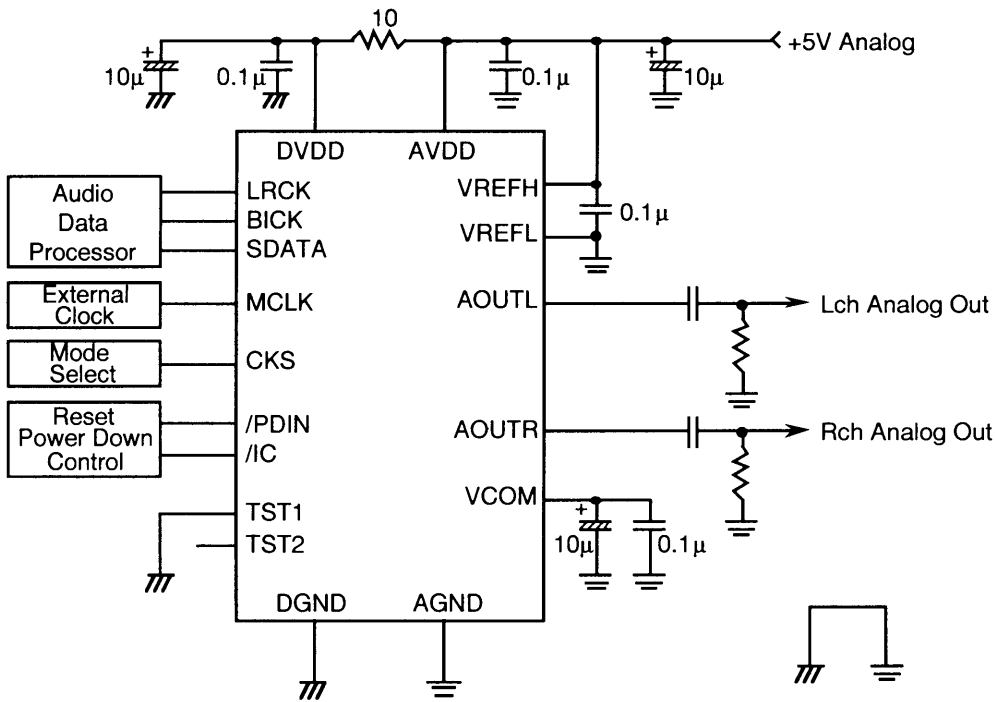


Fig 3. Typical Connection Diagram

■ ELECTRICAL SPECIFICATION

1. ABSOLUTE MAXIMUM RATING

(AGND, DGND=0V; Note 1)

Parameter	Symbol	min	max	units
Power Supplies: Analog (AVDD pin)	AVDD	-0.3	6.0	V
Digital (DVDD pin)	DVDD	-0.3	AVDD+0.3	V
Input Current, Any pin except Supplies	I_{IN}	-	±10	mA
Input Voltage	V_{IND}	-0.3	AVDD+0.3	V
Ambient Operating Temperature	T_{Op}	0	70	°C
Storage Temperature	T_{stg}	-50	125	°C

Note: 1. All voltages with respect to ground.

Warning:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

2. RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V; Note 1)

Parameter	Symbol	min	typ	max	units
Power Supplies: Analog (AVDD pin)	AVDD	3.0	5.0	5.25	V
Digital (DVDD pin)	DVDD	3.0	5.0	AVDD	V
AVDD – DVDD	ΔVDD	0	-	1.0	V
"H" Level Voltage Reference (Note 2)	VREFH	-	AVDD	-	V
"L" Level Voltage Reference	VREFL	-	AGND	-	V
VREFH – VREFL	$\Delta VREF$	2.5	-	AVDD	V

Note: 1. All voltages with respect to ground.

2. AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.

3. Analog output voltage scales with the voltage of (VREFH-VREFL).

$$AOUT(\text{typ. @0dB}) = 2.88 \times (VREFH - VREFL)/5.$$

3. ANALOG CHARACTERISTIC

(Top=25°C; AVDD, DVDD=5.0V; VREFH=AVDD, VREFL=AGND; $f_s=44.1\text{kHz}$; Signal Frequency=1kHz; $R_L \geq 10\text{k}\Omega$; Measurement Bandwidth=10Hz~20kHz; unless otherwise specified)

Parameter	min	typ	max	units
Dynamic Characteristics				
THD+N	-80	-86		dB
(Note 4)	-74	-80		dB
Dynamic Range (A-Weighted)	86	92		dB
(Note 4)	82	88		dB
S/N (A-Weighted)	86	92		dB
(Note 4)	82	88		dB
Cross talk	80	90		dB
DC Accuracy				
Gain Drift		60		ppm/°C
Maximum Output Voltage (Note 5)	2.73	2.88	3.03	V
(Note 4)	1.80	1.90	2.00	V
Power Supplies				
Power Supply Current (Note 6)				
Normal Operation				
AVDD		11	15	mA
DVDD		4	6	mA
Power-Down Mode				
AVDD+DVDD		10	50	μA
Power Dissipation				
Normal Operation		75	105	mW
Power-Down Mode (Note 7)		50	250	μW
Power Supply Rejection		50		dB

Note: 4. AVDD, DVDD = 3.3V

5. Full-scale voltage (0dB). Output voltage scale with the voltage of (VREFH - VREFL)
 $A_{OUT}(\text{typ. @0dB}) = 2.83 \times (VREFH - VREFL)/5$.
6. The typical supply current of DVDD drops to 2.2mA at 3.3V supply voltage.
 The AVDD supply current does not change.
7. External clocks (MCLK, BICK, LRCK) are fixed to "H" level (or "L" level).

4. FILTER CHARACTERISTIC

(Top=25°C; AVDD, DVDD=3.0 ~ 5.25V; $f_s=44.1\text{kHz}$)

Parameter	Symbol	min	typ	max	units
Digital Filter					
Passband	$\pm 0.1\text{dB}$ (Note 8)	PB	0	18.0	kHz
	-3.0dB		0	20.0	kHz
	-6.0dB		0	22.05	kHz
Stopband	(Note 9)	SB	26.0		kHz
Passband Ripple		PR		± 0.02	dB
Stopband Attenuation		SA	57		dB
Group Delay	(Note 9)	GD		$14.2 / f_s$	s
DAC 2nd Order Analog Filter					
Frequency Response	18kHz			-0.1	dB
	20.0kHz			-0.5	dB
	44.1kHz			-6.0	dB

Note: 8. The passband and stopband frequencies scale with f_s .

For example, $PB=0.4535f_s(@-3.0\text{dB})$, $SB=0.5896f_s(@-57\text{dB})$

9. The calculating delay time which occurred by digital filtering. This time is from setting the 16-bit data of both channels to input register to the output of analog signal.

$GD=14.2/f_s @f_s=44.1\text{ kHz}$

5. DIGITAL CHARACTERISTIC

(Top=25°C; AVDD, DVDD=3.0 ~ 5.25V; $f_s=44.1\text{kHz}$)

Parameter	Symbol	min	typ	max	units
"H" Level Input Voltage	V_{IH}	70% DVDD	-	-	V
"L" Level Input Voltage	V_{IL}	-	-	30% DVDD	V
Input Leakage Current	I_{IN}	-	-	± 10	μA

6. SWITCHING CHARACTERISTIC

(Top=25°C; AVDD, DVDD=3.0 ~ 5.25V; CL=20pF)

Parameter	Symbol	min	typ	max	units
Master Clock Frequency					
256fs:	f_{CLK}	2.56	11.2896	12.8	MHz
Pulse Width Low	t_{CLKL}	28			ns
Pulse Width High	t_{CLKH}	28			ns
384fs:	f_{CLK}	3.84	16.9344	19.2	MHz
Pulse Width Low	t_{CLKL}	23			ns
Pulse Width High	t_{CLKH}	23			ns
LRCK Frequency	f_S	5	44.1	50	kHz
Serial Interface Timing (Note 10)					
BICK Period	t_{BCK}	313			ns
BICK Pulse Width Low	t_{BCKL}	100			ns
BICK Pulse Width High	t_{BCKH}	100			ns
LRCK Hold Time (note 11)	t_{LRH}	50		$t_{BCKL}-50$	ns
LRCK Setup Time (note 11)	t_{LRS}	50			ns
SDATA Hold Time	t_{SDH}	50			ns
SDATA Setup Time	t_{SDS}	50			ns
Reset Timing					
/PDIN, /IC pulse Width (Note12)	t_{ICW}	100			ns

Note: 10. Refer to the operating overview section "Serial Data Interface".

11. BICK rising edge must not occur at same time as LRCK edge.

12. The YAC516 can be reset by bringing /PDIN (or /IC) "L" to "H" only upon power up.

7. TIMING CHART

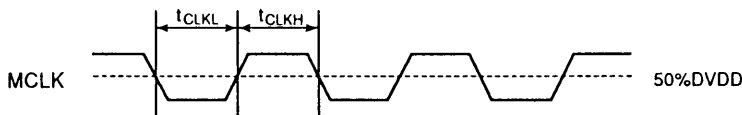


Chart 1. Master Clock Input Timing

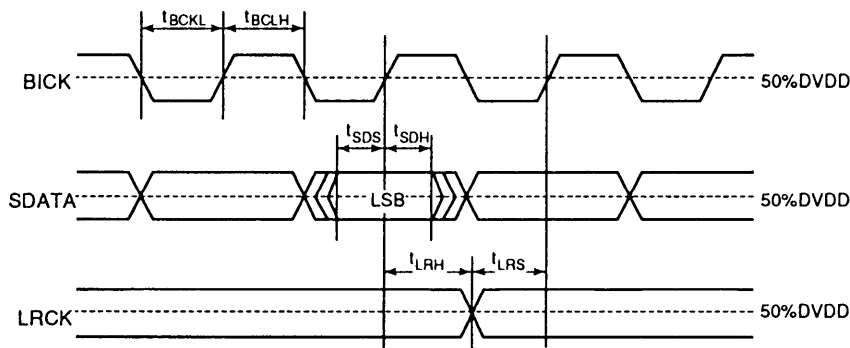


Chart 2. Data Input Timing

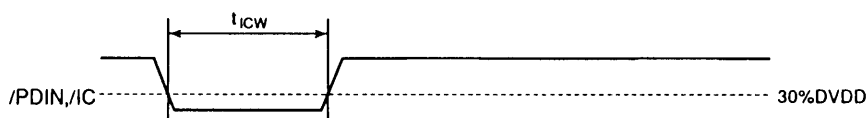
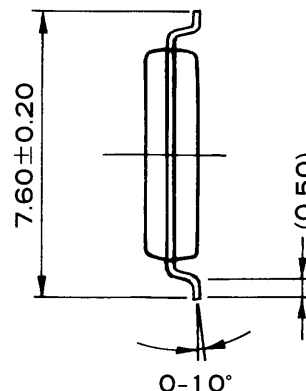
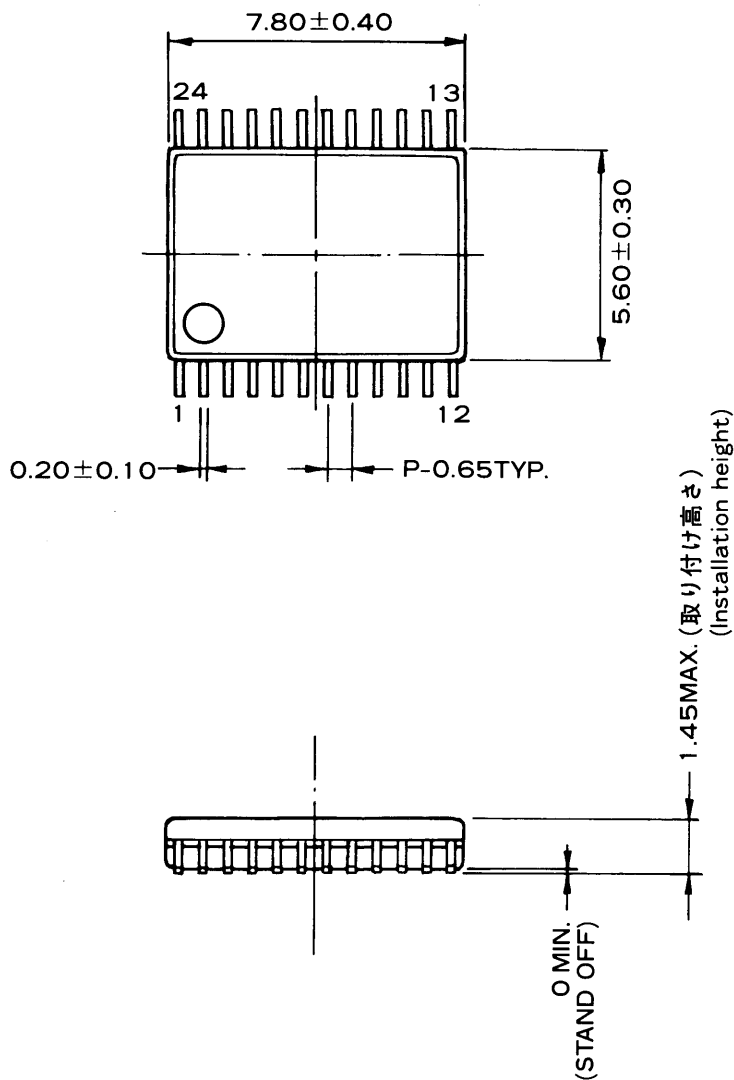


Chart 3. Reset Timing

■ PACKAGE

YAC516-E (24SSOP)



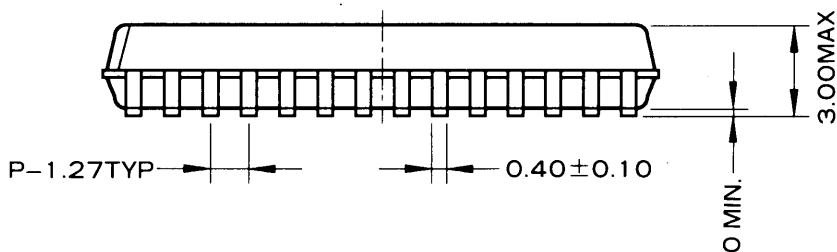
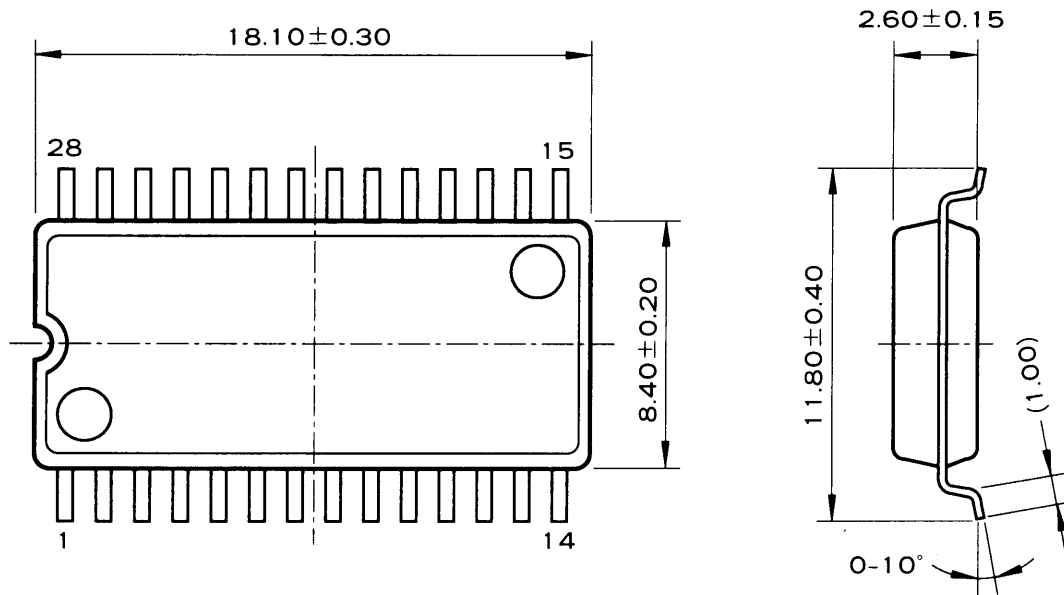
端子厚さ : 0.17±0.05
(LEAD THICKNESS)

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モールド外形寸法はバリを含まない。
単位(UNIT) : mm(millimeters)

The figure in the parenthesis ()
should be used as a reference.
Plastic body dimensions do not
include burr of resin.
UNIT: mm

Note : The LSIs for surface mount need especial consideration on strage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

YAC516-M (28SOP)



端子厚さ : 0.15 ± 0.10
(LEAD THICKNESS)

カッコ内の寸法値は参考値とする。
単位(UNIT) : mm(millimeters)

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UNIT: mm

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