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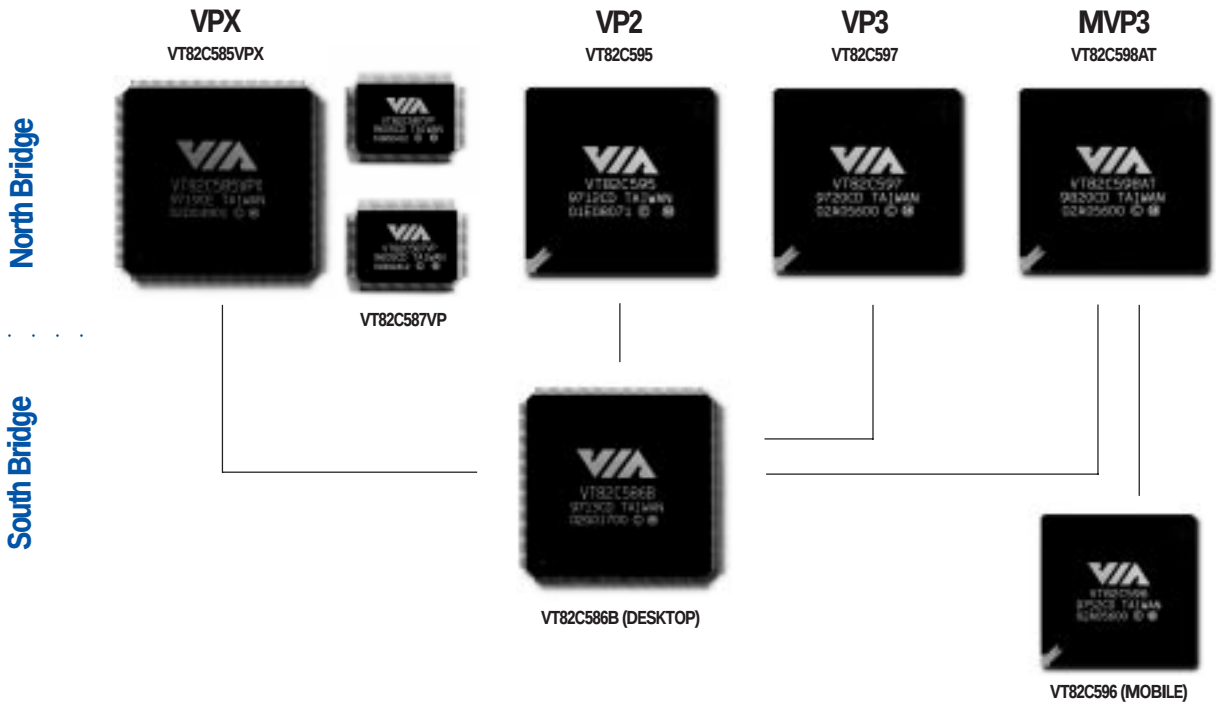
# Introduction

VIA Technologies, Inc., has emerged as a leader in the highly competitive core logic chipset market. Across the board, VIA is pushing the technological edge to offer the highest level of performance, integration, and functionality for the full range of system designs.

**Why run with VIA?**
Top-tier companies choose top-of -the-line products. Keeping with this theme, VIA counts leading system and mainboard OEMs worldwide as key customers. In terms of performance, VIA-based mainboards consistently place among the top finishers in the complete range of performance tests by the editors of the industry's leading IT publications. At the core, VIA's engineering strength is driving the company into a recognized technology leadership role.

**Major changes**
PC architecture is in transition. Changes are in motion, but these changes will take an extended period of time before they are the industry standard. Strongly in place, the current Socket 7 mainboard infrastructure continues with a competitive edge, providing PC buyers a high performance and economical alternative well into the future.

**Roadmap**
While ready for the upcoming era with a proven Slot 1 product, VIA also remains strongly focused on the Socket 7 infrastructure and will continue to deliver a range of leading-edge Socket 7 chipsets.



# Apollo MVP3

## VT82C598AT & VT82C586B DESKTOP

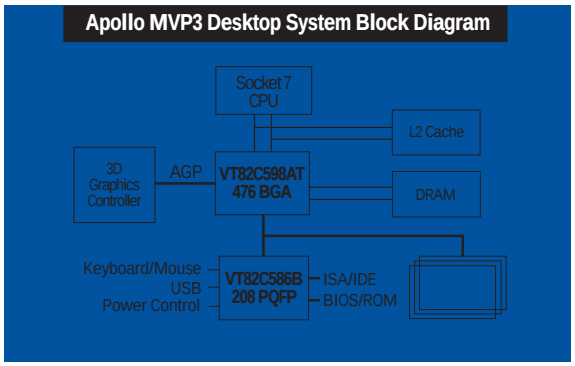
## OVERVIEW

The latest addition to VIA's line of high performance, high integration chipsets is the Apollo MVP3. With support for CPU bus frequencies from 66MHz to 100MHz, Accelerated Graphics Port (AGP), and advanced performance enabling features VIA has once again helped to advance and extend the popular Socket 7 platform.

**100MHz**
The Apollo MVP3 overcomes the limitations of current generation bandwidth-constricted 66MHz PC systems. By connecting the system buses of upcoming 100MHz internal operation CPUs, PC100 SDRAM, and high-speed multimedia technologies like Accelerated Graphics Port (AGP), the Apollo MVP3 delivers performance comparable to current Pentium® II-based systems.

**AGP**
The Apollo MVP3 brings arcade quality graphics to desktop systems with its AGP support. Compliant with 1x and 2x AGP implementations, the chipset is designed to operate the full range of 3D graphics cards from the industry's leading vendors.

**Compatibility**
VIA is working to provide the highest level of technology integration for the Socket 7 mainboard infrastructure. The VIA Apollo MVP3 supports the Intel Pentium® and Pentium® processor with MMX™ technology, Cyrix 6x86™ and 6x86MX™, AMD K6™, and IDT Winchip™ C6™ processors.




**PC98 Compliance**
The VIA Apollo MVP3 for desktops, features the VIA VT82C586B south bridge controller chip. Highly integrated, this chip complies with the Microsoft® PC98 industry standard by supporting ACPI/OnNow and USB(UHCI) technologies.

**Performance**
The Apollo MVP3 takes the Apollo VP3's ground-breaking design and brings it to a new level. Optimized for a new generation of performance, the Apollo MVP3 features support for the new 100MHz CPUs, up to 1GB of high speed DDR SDRAM, SDRAM, EDO, and up to 2MB of L2 cache. The Apollo MVP3 also supports Ultra DMA/33 protocol.

- 66 / 75 / 83 / 100MHz support
- 1GB DRAM Support
- 2MB Cache Support
- AGP
- DDR SDRAM
- PC98
- EC/ECC

# VT82C598AT North Bridge Controller

**AGP / PCI / ISA Mobile and Deep Green PC Ready**
- Supports 3.3V and sub-3.3V interface to CPU
- Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
- PC98 compatible using VIA VT82C586B (208-pin PQFP) south bridge chip with ACPI Power Management for cost-efficient desktop applications
- Modular power management and clock control for mobile system applications
- Combine with VIA VT82C596 (Intel PIIX4 pin compatible 324-pin BGA) "Mobile South" south bridge chip for state-of-the-art mobile applications

**High Integration**
- Single chip implementation for 64-bit Socket 7-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC/CMOS on chip

**High Performance CPU Interface**
- Supports all Socket 7 processors including 64-bit Intel Pentium/Pentium with MMX™, AMD 6K86™(K6™), Cyrix/IBM 6x86™/6x86MX™, and IDT Winchip™ C6™ CPUs
- 66 / 75 / 83 / 100 MHz CPU external bus speed (internal 300MHz and above)
- Built-in deskew DLL (Delay Lock Loop) circuitry for optimal skew control within and between clocking regions
- Cyrix/IBM 6x86 linear burst support
- AMD 6K86 write allocation support
- System management interrupt, memory remap and STPCLK mechanism

**Advanced Cache Controller**
- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support
- Flexible cache size: 0K / 256K / 512K / 1M / 2MB
- 32 byte line size to match the primary cache
- Integrated 8-bit tag comparator
- 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access up to 100 MHz
- Tag timing optimized (less than 4ns setup time) to allow external tag SRAM implementation for most flexible cache organization
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM & PCI bus post write buffers up to 100 MHz
- Supports CPU single read cycle L2 allocation
- System and video BIOS cacheable and write-protect
- Programmable cacheable region

**Full Featured Accelerated Graphics Port (AGP) Controller**
- Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control
- AGP v1.0 compliant
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)

| PCI | AGP | CPU | Mode |
|---|---|---|---|
| 33MHz | 66MHz | 100MHz | 3x synchronous |
| 33MHz | 66MHz | 83MHz | 2.5x pseudo-synchronous |
| 30MHz | 60MHz | 75MHz | 2.5x pseudo-synchronous |
| 33MHz | 66MHz | 66MHz | 2x synchronous |

- Supports 133MHz 2X mode for AD and SBA signalling
- Pipelined split-transaction long-burst transfers up to 533 MB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (128 bytes)
- Sixteen level (quadwords) write data FIFO (64 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
- One level TLB structure
- Sixteen entry fully associative page table
- LRU replacement scheme
- Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

**Concurrent PCI Bus Controller**
- PCI buses are synchronous / pseudo-synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Supports up to five PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- PCI master snoop ahead and snoop filtering
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
- Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
- Delay transaction from PCI master accessing DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

**Advanced High-Performance DRAM Controller**
- DRAM interface synchronous with host CPU (66/75/83/100 MHz) or AGP (66MHz) for most flexible configuration
- Concurrent CPU and AGP access
- FP, EDO, SDRAM, and DDR SDRAM
- Supports JEDEC DDR SDRAM standard (edge DQ for read and central DQ for write)
- Virtual Channel SDRAM support
- Enhanced Synchronous DRAM (ESDRAM) support
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Dynamic Clock Enable (CKE) control for SDRAM power reduction in mobile systems
- Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
- 6 banks up to 1GB DRAMs
- Flexible row and column addresses
- 64-bit data width only
- 3.3V DRAM interface with 5V-tolerant inputs
- Programmable I/O drive capability for MA, command, and MD signals
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU

# VT82C586B PCI to ISA South Bridge Controller

**PC98 Compliant PCI to ISA Bridge**
- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and two function ports
- Integrated master mode enhanced IDE controller with enhanced PCI bus commands and UltraDMA-33 extensions
- PCI-2.1 compliant with delay transaction
- Eight double-word line buffer between PCI and ISA bus
- One level of PCI to ISA post-write buffer
- Supports type F DMA transfers
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Fast reset and Gate A20 operation
- Edge trigger or level sensitive interrupt
- Flash EPROM, 2MB EPROM and combined BIOS support
- Programmable ISA bus clock
- Supports external IOAPIC interface for symmetrical multiprocessor configurations

**Enhanced Master Mode PCI IDE Controller with Extension to UltraDMA-33**
- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Sixteen levels (doublewords) of prefetch and write buffers
- Interlaced commands between two channels
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

**Universal Serial Bus Controller**
- USB v.1.0 and Intel Universal HCI v.1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and two function ports
- Integrated physical layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

**Sophisticated PC98-Compatible Power Management**
- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v.1.0 Compliant (all required features plus extensions for most efficient desktop power management)
- APM v.1.2 Compliant
- Supports soft-off (suspend to disk) and power-on suspend with hardware automatic wake-up
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Dedicated input pin for external modem ring indicator for system wake-up
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Normal, doze, sleep, suspend and conserve modes
- System event monitoring with two event classes
- Five multi-purpose I/O pins plus support for up to 16 general purpose input ports and 16 output ports
- $I^2C$ serial bus support for JEDEC-compatible DIMM identification and on-board-device power control
- Seven external event input ports with programmable SMI condition
- Primary and secondary interrupt differentiation for individual channels
- Clock throttling control
- Multiple internal and external SMI sources for flexible power management models

**Plug and Play Controller**
- PCI interrupts steerable to any interrupt channel
- Three steerable interrupt channels for on-board plug and play devices
- Microsoft Windows 95™ and plug and play BIOS compliant

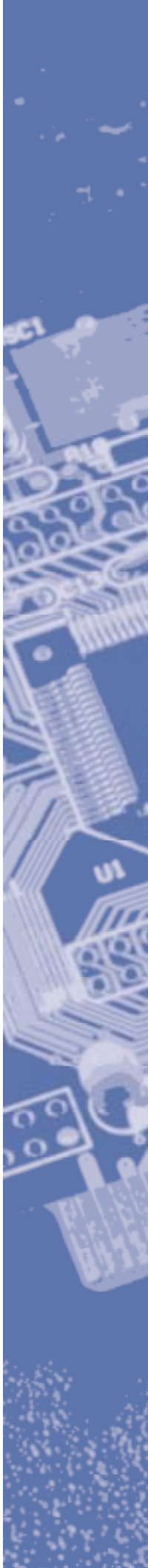
**Pin-compatible upgrade from VT82C586 and VT82C586A for existing designs (VT82C586B)**

**Built-in Nand-tree pin scan test capability (VT82C586B and VT82C598AT)**

**3.3V, 0.5um, high speed / low power CMOS process (VT82C598AT)**

**0.5um mixed voltage, high speed / low power CMOs process (VT82C586B)**

**Single chip 208 pin PQFP (VT82C586B), 476 pin BGA Package (VT82C598AT)**



# Apollo MVP3

## VT82C598AT & VT82C596 MOBILE

## OVERVIEW

VIA's solution to the growing need for desktop performance in notebook computers is the Apollo MVP3, mobile version. With support for CPU bus frequencies from 66MHz to 100MHz, Accelerated Graphics Port (AGP), and advanced performance enabling features VIA has helped to bring the highest possible perfromance to your notebook system.

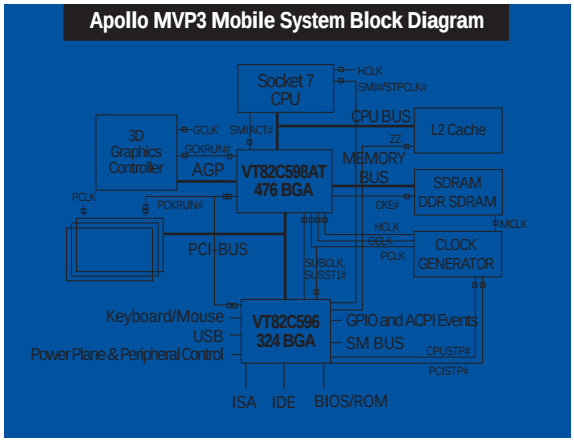
**100MHz**
The Apollo MVP3, mobile version, overcomes the limitations of current generation bandwidth-constricted 66MHz PC systems. By connecting the system buses of upcoming 100MHz internal operation CPUs, PC100 SDRAM, and high-speed multimedia technologies like Accelerated Graphics Port (AGP), the Apollo MVP3, mobile version, delivers increased performance to notebook computers.

**Mobile South Bridge**
Combined with the VT82C596 mobile south bridge controller, the Apollo MVP3, mobile version, provides all the features and support needed for sophisticated notebook implementations.

**AGP**
The Apollo MVP3, mobile version, brings arcade quality graphics to notebook systems with its AGP support. Compliant with 1x and 2x AGP implementations, the chipset is designed to operate the full range of 3D graphics cards from the industry's leading vendors.

**Compatibility**
VIA is working to provide the highest level of technology integration for the Socket 7 mainboard infrastructure. The VIA Apollo MVP3, mobile version, supports the Intel Pentium and Pentium processor with MMX technology, Cyrix 6x86 and 6x86MX, AMD K6, and IDT Winchip C6 processors.

**Apollo MVP3 Mobile System Block Diagram**




**PC98 Compliance**
The VIA Apollo MVP3, mobile version, features the VIA VT82C596 mobile south bridge controller chip. Highly integrated, this chip complies with the Microsoft PC98 industry standard by supporting ACPI/OnNow and USB(UHCI) technologies.

**Performance**
The Apollo MVP3, mobile version, allows for notebook-class power management functionality with ACPI and legacy APM compliance. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-disk) are supported with hardware automatic wake-up. Additional features include event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

- 66 / 75 / 83 / 100MHz support
- Mobile Ready
- Advanced power management
- 1GB DRAM Support
- 2MB Cache Support
- AGP
- DDR SDRAM
- PC98
- EC/ECC

# VT82C598AT North Bridge Controller

**AGP / PCI / ISA Mobile and Deep Green PC Ready**
- Supports 3.3V and sub-3.3V interface to CPU
- Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
- Modular power management and clock control for mobile system applications

**High Integration**
- Single chip implementation for 64-bit Socket 7-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC/CMOS on chip

**High Performance CPU Interface**
- Supports all Socket 7 processors including 64-bit Intel Pentium/Pentium with MMX™, AMD 6K86™(K6™), Cyrix/IBM 6x86™/6x86MX™, and IDT Winchip™ C6™ CPUs
- 66 / 75 / 83 / 100 MHz CPU external bus speed (internal 300MHz and above)
- Built-in deskew DLL (Delay Lock Loop) circuitry for optimal skew control within and between clocking regions
- Cyrix/IBM 6x86 linear burst support
- AMD 6K86 write allocation support
- System management interrupt, memory remap and STPCLK mechanism

**Advanced Cache Controller**
- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support
- Flexible cache size: 0K / 256K / 512K / 1M / 2MB
- 32 byte line size to match the primary cache
- Integrated 8-bit tag comparator
- 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access up to 100 MHz
- Tag timing optimized (less than 4ns setup time) to allow external tag SRAM implementation for most flexible cache organization
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM & PCI bus post write buffers up to 100 MHz
- Supports CPU single read cycle L2 allocation
- System and video BIOS cacheable and write-protect
- Programmable cacheable region

**Full Featured Accelerated Graphics Port (AGP) Controller**
- Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control
- AGP v1.0 compliant
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)

| PCI | AGP | CPU | Mode |
|---|---|---|---|
| 33MHz | 66MHz | 100MHz | 3x synchronous |
| 33MHz | 66MHz | 83MHz | 2.5x pseudo-synchronous |
| 30MHz | 60MHz | 75MHz | 2.5x pseudo-synchronous |
| 33MHz | 66MHz | 66MHz | 2x synchronous |

- Supports 133MHz 2X mode for AD and SBA signalling
- Pipelined split-transaction long-burst transfers up to 533 MB/sec
- Eight level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (128 bytes)
- Sixteen level (quadwords) write data FIFO (64 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
- One level TLB structure
- Sixteen entry fully associative page table
- LRU replacement scheme
- Independent GART lookup control for host / AGP / PCI master accesses
- Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support

**Concurrent PCI Bus Controller**
- PCI buses are synchronous / pseudo-synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Supports up to five PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- PCI master snoop ahead and snoop filtering
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
- Supports L1/L2 write-back merged w/ PCI master post-write to minimize DRAM utilization
- Delay transaction from PCI master accessing DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

**Advanced High-Performance DRAM Controller**
- DRAM interface synchronous with host CPU (66/75/83/100 MHz) or AGP (66MHz) for most flexible configuration
- Concurrent CPU and AGP access
- FP, EDO, SDRAM, and DDR SDRAM
- Supports JEDEC DDR SDRAM standard
- Virtual Channel SDRAM support
- Enhanced Synchronous DRAM (ESDRAM) support
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Dynamic Clock Enable (CKE) control for SDRAM power reduction in mobile systems
- Mixed 1M / 2M / 4M / 8M / 16MxN DRAMs
- 6 banks up to 1GB DRAMs
- Flexible row and column addresses
- 64-bit data width only
- 3.3V DRAM interface with 5V-tolerant inputs
- Programmable I/O drive capability for MA, command, and MD signals
- Optional bank-by-bank ECC or EC for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 8-bank interleave banks are allocated based on LRU
- Seamless DRAM command scheduling for maximum DRAM bus utilization
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Four quadwords of CPU/cache to DRAM read prefetch buffers
- Concurrent DRAM writeback
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 5-2-2-2-2-2-2-2 back-to-back accesses for EDO DRAM
- 6-1-1-1-2-1-1-1 back-to-back accesses for SDRAM
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate and refresh on populated banks only
- CAS before RAS or self refresh

**Mobile System Support**
- Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
- PCI and AGP bus clock run and clock generator control
- VTT suspend power plane preserves memory data (598AT Only)
- Suspend-to-DRAM and Self-Refresh operation mobile features
- Dynamic clock gating for internal functional blocks for normal operation power reduction
- Low-leakage I/O pads

# VT82C596 Mobile PCI to ISA South Bridge Controller

**PC98 Compliant PCI to ISA Bridge**
- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and two function ports
- Integrated UltraDMA-33 master mode EIDE controller with enhanced PCI bus commands
- PCI-2.1 compliant with delay transaction
- Eight double-word line buffer between PCI and ISA bus
- One level of PCI to ISA post-write buffer
- Supports type F DMA transfers
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Sideband signal support for PC/PCI and serial interrupt for docking and non-docking applications
- Fast reset and Gate A20 operation
- Edge trigger or level sensitive interrupt
- Flash EPROM, 2MB EPROM and combined BIOS support
- Supports positive and subtractive decoding
- Supports external APIC interface for symmetrical multiprocessor configurations

**UltraDMA-33 Master Mode PCI EIDE Controller**
- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Thirty-two levels (doublewords) of prefetch and write buffers
- Dual DMA engine for concurrent dual channel operation
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support
- Supports glue-less “Swap-Bay” option with full electrical isolation

**Universal Serial Bus Controller**
- USB v.1.0 and Intel Universal HCI v.1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and two function ports
- Integrated physical layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

**System Management Bus Interface**
- Host interface for processor communications
- Slave interface for external SMBus masters

**Sophisticated PC98-Compatible Mobile Power Management**
- Supports both ACPI and legacy (APM) power management
- ACPI v.1.0 Compliant
- APM v.1.2 Compliant
- CPU clock throttling and clock stop control for complete ACPI C0 to C3 state suppor
- PCI bus clock run and PCI/CPU clock generator stop control
- Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- System event monitoring with two event classes
- Primary and secondary interrupt differentiation for individual channels
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- Up to 22 general pupose input ports and 31 output ports
- Multiple internal and external SMI sources for flexible power management models
- Two programmable chip selects and one microcontroller chip select
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Thermal alarm support
- Cache SRAM power-down control
- Hot docking support
- I/O pad leakage control

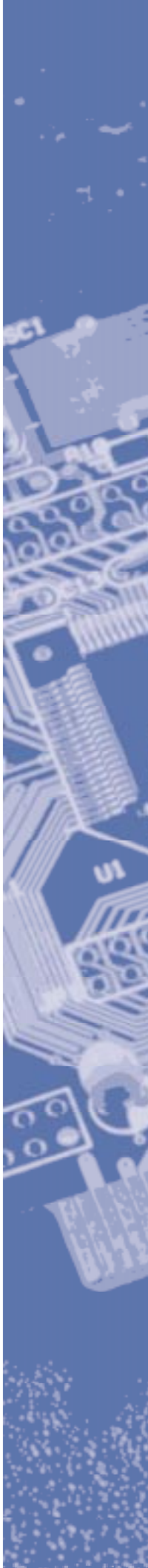
**Plug and Play Controller**
- PCI interrupts steerable to any interrupt channel
- Three steerable interrupt channels for on-board plug and play devices
- Microsoft Windows 95™ and plug and play BIOS compliant

**Built-in NAND-tree pin scan test capability (VT82C596 and VT82C598AT)**

**0.5um, 3.3V, low power CMOS process (VT82C596)**

**3.3V, 0.35um, high speed / low power CMOS process (VT82C598AT)**

**Single chip 324 pin BGA (VT82C596), 476 pin BGA Package (VT82C598AT)**



# Apollo VP3

## VT82C597 & VT82C586B

## OVERVIEW

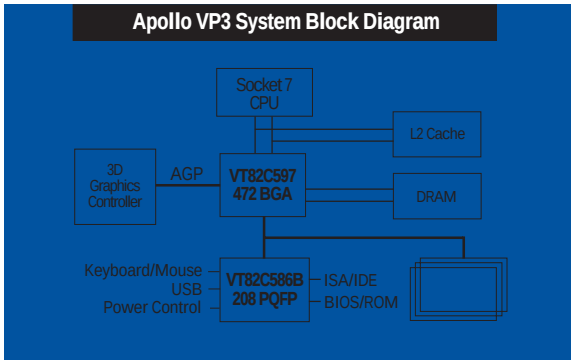
With Accelerated Graphics Port (AGP) technology and advanced performance enabling features, the Apollo VP3 laid the groundwork for the 100MHz MVP3. The Apollo VP3 integrates all the features needed to achieve the highest level of mainstream-priced multimedia-intensive PC computing.

**AGP Ready**
The Apollo VP3 enables arcade quality 3D graphics in mainstream-priced PC systems. Compliant with both 1x and 2x AGP implementations, the chipset is designed to operate the full range of 3D graphic cards from the industry's leading vendors.

**Compatibility**
VIA is working to provide the highest level of technology integration for the Socket 7 mainboard infrastructure. The VIA Apollo VP3 supports Intel Pentium and Pentium processor with MMX technology, Cyrix 6x86 and Cyrix 6x86MX, AMD K5 and K6, and IDT Winchip C6 processors.

**PC97 Compliance**
The VIA Apollo VP3 features the VIA VT82C586B south bridge controller chip. Highly integrated, this chip complies with the Microsoft PC97 industry standard by supporting ACPI/OnNow, Ultra DMA/33 and USB technologies.

**Performance**
The Apollo VP3 builds on the legacy of the VIA Apollo VP2, the tested and proven highest performing Socket 7 chipset. Optimized for a new generation of




performance, the Apollo VP3 features support for up to 1GB of high speed SDRAMs, EDO and FPM DRAM types, and up to 2MB of L2 cache. Increased bandwidth between main memory and the VT82C597 System Controller speeds up system performance and frees up valuable space for CPU transactions.

**Reliability**
To provide the highest level data transfer, the Apollo VP3 incorporates both EC and Error Checking and Correcting (ECC) capabilites.

- AGP
- 2MB cache support
- 1GB DRAM support
- PC 97
- EC/ECC
- All Socket 7 processors
- DDR SDRAM


## VT82C597 North Bridge Controller

**PCI/ISA Green PC Ready**
- Supports separately powered 3.3V (5V tolerant) interfaces to system memory, AGP, and PCI bus
- Supports 3.3V and sub-3.3V interface to CPU

**High Integration**
- Single chip implementation for 64-bit Socket 7-CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- Six TTLs for a complete main board implementation

**Flexible CPU Interface**
- Supports 64-bit Pentium , AMD 5K86™ , AMD 6K86™ , Cyrix 6x86™ and IDT Winchip C6 CPUs
- CPU external bus speed up to 66 MHz (internal 233MHz and above)
- Supports CPU internal write-back cache
- System management interrupt, memory remap and STPCLK mechanism
- Cyrix 6X86 linear burst support
- CPU NA# / Address pipeline capability
- 4 cache lines of CPU/cache-to-DRAM post-write buffers
- 4 quadwords of CPU/cache-to-DRAM read-prefetch buffers

**Advanced Cache Controller**
- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support (with global write enable feature)
- Flexible cache size: 0K/256K/512K/1M/2MB
- 32 byte line size to match the primary cache
- Integrated 10-bit tag comparator
- 3-1-1-1 read/write timing for PBSRAM access at 66 Mhz
- 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access at 66 Mhz
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66Mhz
- Data streaming for simultaneous primary and secondary cache line fill
- System and video BIOS cacheable and write-protect
- Programmable cacheable region and cache timing

**AGP Controller**
- AGP v1.0 compliant
- Supports SideBand Addressing (SBA) mode
- Supports 133MHz 2X mode for AD and SBA signalling
- Eight level read request queue
- Four level post-write request queue
- Thirty-two level (quadwords) read data FIFO
- Sixteen level (quadwords) write data FIFO
- Maximum four outstanding pipeline GNTs for maximum AGP bus utilization
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Supports AGP read snoop host post-write buffer

**GART**
- One level TLB structure
- Sixteen entry fully associative page table
- LRU replacement scheme
- Independent GART lookup control for host/AGP/PCI master accesses

**Intelligent PCI Bus Controller**
- PCI buses are synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Separate data buffers for the two PCI buses
- Write transactions allowed between the two PCI buses
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Allows PCI master access while ISA master/DMA is active
- PCI master snoop ahead and snoop filtering
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Supports single-write-merge and delay-read for better DRAM utilization
- Supports L1/L2 write-back forward to PCI master read to minimize PCI read latency
- Supports L1/L2 write-back merged with PCI master post-write to minimize DRAM utilization
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.1 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

**Advanced High-Performance DRAM Controller**
- 66MHz DRAM interface
- Concurrent CPU and AGP access
- FP, EDO, SDRAM, and DDR SDRAM
- 66MHz DDR (Double Data Rate) supported for DDR SDRAM (supports central-DQ, bidirectional DS, and optional SDR write)
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Mixed 1M/2M/4M/8M/16MxN DRAMs
- 6 banks up to 1GB DRAMs
- Flexible row and column addresses
- 64-bit data width only
- 3.3V DRAM interface with 5V-tolerant inputs
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
- Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Concurrent DRAM writeback
- Speculative DRAM access
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 4-2-2-2 on page, 7-2-2-2 start page and 9-2-2-2 off page timing for EDO DRAMs at 50/60MHz
- 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66MHz
- 6-1-1-1 on page, 8-1-1-1 start page and 10-1-1-1 off page for SDRAMs at 66 MHz
- 5-2-2-2-3-1-2-2 back-to-back access for EDO DRAM at 66 MHz
- 6-1-1-1-3-1-1-1 back-to-back access for SDRAM at 66 MHz
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only

## VT82C586B PCI to ISA South Bridge Controller

**PC97 Compliant PCI to ISA Bridge**
- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and two function ports
- Integrated master mode enhanced IDE controller with enhanced PCI bus commands and UltraDMA-33 extensions
- PCI-2.1 compliant with delay transaction
- Eight double-word line buffer between PCI and ISA bus
- One level of PCI to ISA post-write buffer
- Supports type F DMA transfers
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Fast reset and Gate A20 operation
- Edge trigger or level sensitive interrupt
- Flash EPROM, 2MB EPROM and combined BIOS support
- Programmable ISA bus clock
- Supports external IOAPIC interface for symmetrical multiprocessor configurations

**Enhanced Master Mode PCI IDE Controller with Extension to UltraDMA-33**
- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Sixteen levels (doublewords) of prefetch and write buffers
- Interlaced commands between two channels
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

**Universal Serial Bus Controller**
- USB v.1.0 and Intel Universal HCI v.1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and two function ports
- Integrated physical layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

**Sophisticated PC97-Compatible Power Management**
- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v.1.0 Compliant (all required features plus extensions for most efficient desktop power management)
- APM v.1.2 Compliant
- Supports soft-off (suspend to disk) and power-on suspend with hardware automatic wake-up
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Dedicated input pin for external modem ring indicator for system wake-up
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Normal, doze, sleep, suspend and conserve modes
- System event monitoring with two event classes
- Five multi-purpose I/O pins plus support for up to 16 general purpose input ports and 16 output ports
- $I^2C$ serial bus support for JEDEC-compatible DIMM identification and on-board-device power control
- Seven external event input ports with programmable SMI condition
- Primary and secondary interrupt differentiation for individual channels
- Clock throttling control
- Multiple internal and external SMI sources for flexible power management models

**Plug and Play Controller**
- PCI interrupts steerable to any interrupt channel
- Three steerable interrupt channels for on-board plug and play devices
- Microsoft Windows 95™ and plug and play BIOS compliant

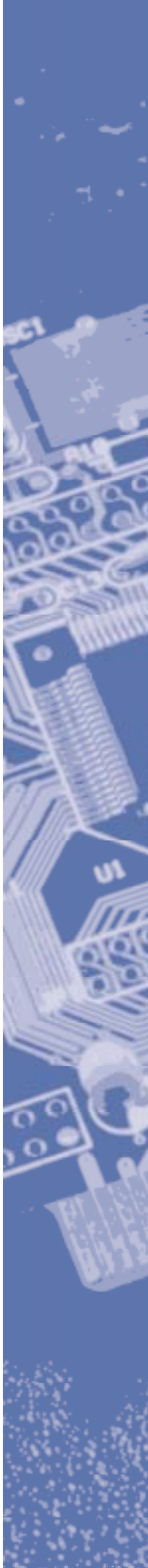
**Pin-compatible upgrade from VT82C586 and VT82C586A for existing designs (VT82C586B)**

**Built-in Nand-tree pin scan test capability (VT82C597 and VT82C586B)**

**3.3V, 0.5um, high speed / low power CMOS process (VT82C597)**

**0.5um mixed voltage, high speed / low power CMOs process (VT82C586B)**

**Single chip 208 pin PQFP (VT82C586B), 472 pin BGA Package (VT82C597)**



# Apollo VP2

## VT82C595 & VT82C586B

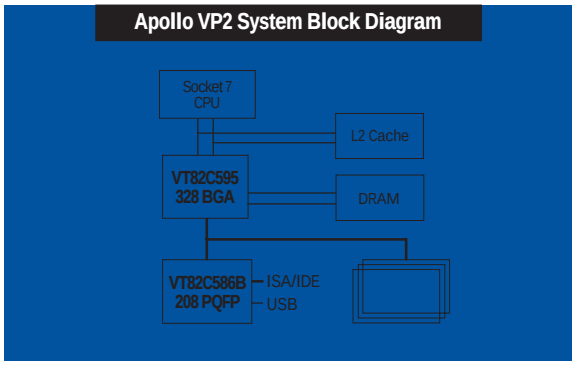
## OVERVIEW

Licensed by AMD and adopted by Compaq for its Deskpro 2000 and 4000 lines, the Apollo VP2 is the cornerstone of VIA's current generation Apollo chipsets. With features that include ECC, PC97-compliance, SDRAM, as well as support for up to 512MB DRAM and 2MB cache, the VP2 is a leading-edge product with the highest levels of integration, performance and compatibility.

**Compatibility**
The Apollo VP2 supports the full range of Socket 7 processors including Intel Pentium and Pentium processor with MMX technology, Cyrix 6x86 and Cyrix 6x86MX, AMD K5 and K6, and IDT Winchip C6. The chipset supports Linear Burst Mode for Cyrix 6x86 and 6x86MX, as well as Write Allocation for the AMD K6 processors.

**PC97 Compliance**
The VIA Apollo VP2 features the VIA VT82C586B south bridge controller chip. Highly integrated, this chip complies with the Microsoft PC97 industry standard by supporting ACPI/OnNow, Ultra DMA/33 and USB technologies.

**Performance**
Key to the Apollo VP2's industry leading performance features is support for up to 2MB L2 cache, SDRAM and UltraDMA/33. In mainboard tests by the




industry's leading Internet and print publications, the Apollo VP2 has consistantly clocked in as the highest performing Socket 7 chipset.

**Reliability**
For server data transfer integrity, the Apollo VP2 incorporates Error Checking and Correcting (ECC).

- ECC
- 2MB cache support
- 512MB DRAM support
- PC97 Compliant
- SDRAM

## VT82C595 North Bridge System Controller

**High Integration**
- Single chip implementation for 64-bit Pentium-CPU, 64-bit system memory, and 32-bit PCI interface
- VT82C590 Apollo VP2 Chipset: VT82C595 system controller and VT82C586B PCI to ISA bridge
- Chipset includes UltraDMA-33 EIDE, USB, and Keyboard / PS2-Mouse Interfaces plus RTC /CMOS on chip
- Six TTLs for a complete main board implementation

**PCI/ISA Green PC Ready**
- Supports 3.3V or 5V interface to CPU, system memory, and / or PCI bus
- Supports CPUs with internal voltages below 3.3V
- PC97 compatible using VT82C586B South Bridge with ACPI Power Management

**Flexible CPU Interface**
- Supports 64-bit Intel Pentium and Pentium with MMX™ , AMD K5™ and AMD-K6™, Cyrix 6x86™ and Cyrix 6x86 MX™, and IDT Winchip C6 CPUs
- CPU external bus speed up to 66 Mhz (internal 200Mhz and above)
- Supports CPU internal write-back cache
- System management interrupt, memory remap and STPCLK mechanism
- Cyrix 6x86 linear burst support
- CPU NA# / Address pipeline capability

**Advanced Cache Controller**
- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support (with global write enable feature)
- Flexible cache size: 0K/256K/512K/1M/2MB
- 32 byte line size to match the primary cache
- Integrated 10-bit tag comparator
- 3-1-1-1 read/write timing for PBSRAM access at 66 Mhz
- 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access at 66Mhz
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66Mhz
- Data streaming for simultaneous primary and secondary cache line fill
- System and video BIOS cacheable and write-protect
- Programmable cacheable region and cache timing

**Fast DRAM Controller**
- Fast Page Mode/EDO/Synchronous-DRAM support in a mixed combination
- Mixed 1M/2M/4M/8M/16MxN DRAMs
- 6 banks up to 512MB DRAMs
- Flexible row and column addresses
- 3.3v and 5v DRAM without external buffers
- Optional bank-by-bank ECC (single-bit error correction and multi-bit error detection) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Concurrent DRAM writeback
- Speculative DRAM access
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 4-2-2-2 on page, 7-2-2-2 start page and 9-2-2-2 off page timing for EDO DRAMs at 50/60 MHz
- 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66MHz
- 6-1-1-1 on page, 8-1-1-1 start page and 10-1-1-1 off page for SDRAMs at 66 MHz
- 5-2-2-2-3-1-2-2 back-to-back access for EDO DRAM at 66 MHz
- 6-1-1-1-3-1-1-1 back-to-back access for SDRAM at 66 MHz
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only

**Intelligent PCI Bus Controller**
- 32 bit 3.3/5v PCI interface
- Synchronous divide-by-two PCI bus interface
- PCI master snoop ahead and snoop filtering
- PCI master peer concurrency
- Synchronous bus to CPU clock with divide-by-two from the CPU clock
- Automatic detection of data streaming burst cycles from CPU to the PCI bus
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Complete steerable PCI interrupts
- Supports L1 write-back forward to PCI master read to minimize PCI read latency
- Supports L1 write-back merged with PCI master post-write to minimize DRAM utilization
- Provides transaction timer to fairly arbitrate between PCI masters
- PCI-2.1 compliant

**Built-in nand-tree pin scan test capability**

**0.6um mixed voltage, high-speed / low power CMOA process**

**328-pin Low-Profile BGA Package**

## VT82C586B PCI to ISA South Bridge Controller

**PC97 Compliant PCI to ISA Bridge**
- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and two function ports
- Integrated master mode enhanced IDE controller with enhanced PCI bus commands and UltraDMA-33 extensions
- PCI-2.1 compliant with delay transaction
- Eight double-word line buffer between PCI and ISA bus
- One level of PCI to ISA post-write buffer
- Supports type F DMA transfers
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Fast reset and Gate A20 operation
- Edge trigger or level sensitive interrupt
- Flash EPROM, 2MB EPROM and combined BIOS support
- Programmable ISA bus clock
- Supports external IOAPIC interface for symmetrical multiprocessor configurations

**Enhanced Master Mode PCI IDE Controller with Extension to UltraDMA-33**
- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Sixteen levels (doublewords) of prefetch and write buffers
- Interlaced commands between two channels
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

**Universal Serial Bus Controller**
- USB v.1.0 and Intel Universal HCI v.1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and two function ports
- Integrated physical layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

**Sophisticated PC97-Compatible Power Management**
- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v.1.0 Compliant (all required features plus extensions for most efficient desktop power management)
- APM v.1.2 Compliant
- Supports soft-off (suspend to disk) and power-on suspend with hardware automatic wake-up
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Dedicated input pin for external modem ring indicator for system wake-up
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Normal, doze, sleep, suspend and conserve modes
- System event monitoring with two event classes
- Five multi-purpose I/O pins plus support for up to 16 general purpose input ports and 16 output ports
- I²C serial bus support for JEDEC-compatible DIMM identification and on-board-device power control
- Seven external event input ports with programmable SMI condition
- Primary and secondary interrupt differentiation for individual channels
- Clock throttling control
- Multiple internal and external SMI sources for flexible power management models

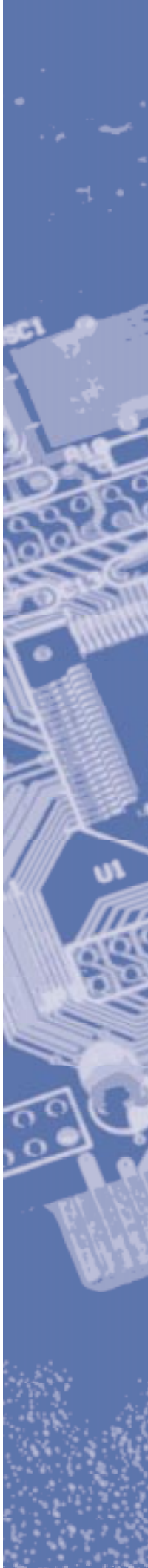
**Plug and Play Controller**
- PCI interrupts steerable to any interrupt channel
- Three steerable interrupt channels for on-board plug and play devices
- Microsoft Windows 95™ and plug and play BIOS compliant

**Pin-compatible upgrade from VT82C586 and VT82C586A for existing designs**

**Built-in Nand-tree pin scan test capability**

**0.5um mixed voltage, high speed and low power CMOS process**

**Single chip 208 pin PQFP**



# Apollo VPX

## VT82C585VPX, VT82C587VP & VT82C586B

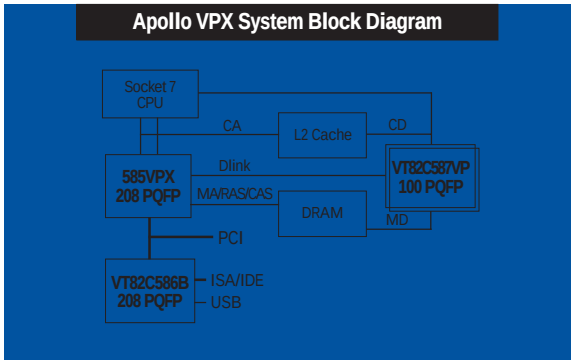
## OVERVIEW

The VIA VT82C580VPX Apollo VPX core logic chipset is a high performance, fully compatible and cost-effective core logic chipset for Socket 7 mainboards. With key features that include an asynchronous 75MHz CPU bus, Microsoft PC98-compliance, and specific performance enhancements, the VIA Apollo VPX is the optimum choice for the full range of system designs.

**Compatibility**
The VIA Apollo VPX provides support for Intel Pentium, and Pentium processor with MMX technology, Cyrix 6x86 and Cyrix 6x86MX, AMD K5 and K6, and IDT Winchip C6 processors. For true implementation of the Cyrix/IBM 6x86 233 processor, the chipset features an asynchronous CPU bus operational at either 66 or 75 MHz speeds. Apollo VPX also supports Linear Burst Mode for the Cyrix 6x86 and Cyrix 6x86MX, as well as Write Allocation for AMD K6 processors.

**PC97 Compliance**
The VIA Apollo VPX features the VIA VT82C586B south bridge controller chip. Highly integrated, this chip complies with the PC97 industry standard by supporting ACPI/OnNow, Ultra DMA/33 and USB technologies.

**Performance**
The Apollo VPX builds on the legacy of its predecessor, the VIA VT82C580VP Apollo VP, widely recognized by leading international IT publications as the highest performing Socket 7 chipset in its class. The VPX supports up to 512MB of SDRAM, EDO, BEDO and FPM DRAM types, and up to 2MB of L2 cache.




**Mainboard Upgradability**
The four-chip Apollo VPX provides mainboard designers a clear upgrade path to high integration. For a considerable cost savings, the chipset is manufactured in proven and economical PQFP packaging.

- 75 MHz asynchronous local bus
- 2MB cache
- 512MB DRAM support
- PC 97
- All Socket 7 processors
- SDRAM

## VT82C585VPX North Bridge System Controller

**Flexible CPU Interface**
- Supports 64-bit Intel Pentium® and Pentium® with MMX™, AMD K5™ and AMD K6™, Cyrix 6x86™ and 6x86 MX™, IDT Winchip C6 CPUs
- CPU external bus speed up to 75 MHz (asynchronous) or 66MHz (synchronous) (internal 200Mhz and above)
- Supports CPU internal write-back cache
- System management interrupt, memory remap and STPCLK mechanism
- Cyrix 6x86 linear burst support
- CPU NA# / Address pipeline capability

**Low Cost**
- PQFP packaging for low-cost implementation of 64-bit Pentium-CPU, 64-bit system memory, and 32-bit PCI
- VT82C580 Apollo VPX Chipset: VT82C585VPX system controller and VT82C587VP Data Buffers
- VT82C586B includes UltraDMA-33 EIDE, USB, and Keyboard / Mouse Interfaces plus RTC / CMOS on chip
- Six TTLs for a complete main board implementation

**Advanced Cache Controller**
- Direct map write back or write through secondary cache
- Pipelined burst synchronous SRAM (PBSRAM) cache support
- Flexible cache size: 0K/256K/512K/1M/2MB
- 32 byte line size to match the primary cache
- Integrated 10-bit tag comparator
- 3-1-1-1 read/write timing for PBSRAM access at 66/75 MHz
- 3-1-1-1-1-1-1-1 back to back read timing for PBSRAM access at 66/75 MHz
- Sustained 3 cycle write access for PBSRAM access or CPU to DRAM and PCI bus post write buffers at 66/75 MHz
- Data streaming for simultaneous primary and secondary cache line fill
- System and video BIOS cacheable and write-protect
- Programmable cacheable region and cache timing

**Fast DRAM Controller**
- Fast Page Mode/EDO/Synchronous-DRAM support in a mixed combination
- Mixed 1M/2M/4M/8M/16MxN DRAMs
- 6 banks up to 512MB DRAMs
- Flexible row and column addresses
- 64-bit or 32-bit data width in arbitrary mixed combination
- 3.3v and 5v DRAM without external buffers
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support (14 MA lines)
- Four cache lines (16 quadwords) of CPU/cache to DRAM write buffers
- Concurrent DRAM writeback
- Speculative DRAM access
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- 4-2-2-2 on page, 7-2-2-2 start page and 9-2-2-2 off page timing for EDO DRAMs at 50 / 60MHz
- 5-2-2-2 on page, 8-2-2-2 start page and 11-2-2-2 off page timing for EDO DRAMs at 66MHz
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- 5-2-2-2-3-1-2-2 back-to-back access for EDO DRAM at 66 MHz
- 6-1-1-1-3-1-1-1 back-to-back access for SDRAM at 66 MHz
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- Programmable refresh rate, CAS-before-RAS refresh and refresh on populated banks only

**Intelligent PCI Bus Controller**
- 32 bit 3.3/5v PCI interface
- Synchronous divide-by-two and asynchronous PCI bus interface
- PCI master snoop ahead and snoop filtering
- PCI master peer concurrency
- Synchronous bus to CPU clock with divide-by-two from the CPU clock
- Automatic detection of data streaming burst cycles from CPU to the PCI bus
- Five levels (double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- Forty-eight levels (double-words) of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Complete steerable PCI interrupts
- Supports L1 write-back forward to PCI master read to minimize PCI read latency
- Supports L1 write-back merged with PCI master post-write to minimize DRAM utilization
- Provides transaction timer to fairly arbitrate between PCI masters
- PCI-2.1 compliant

**Built in Nand-tree pin scan test capability**

**0.5um mixed voltage, high speed / low power CMOS process**

**VT82585VPX: 208-pin PQFP**

**VT82C587VP: 100-pin PQFP**

## VT82C586B PCI to ISA South Bridge Controller

**PC97 Compliant PCI to ISA Bridge**
- Integrated ISA Bus Controller with integrated DMA, timer, and interrupt controller
- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated USB Controller with root hub and two function ports
- Integrated master mode enhanced IDE controller with enhanced PCI bus commands and UltraDMA-33 extensions
- PCI-2.1 compliant with delay transaction
- Eight double-word line buffer between PCI and ISA bus
- One level of PCI to ISA post-write buffer
- Supports type F DMA transfers
- Distributed DMA support for ISA legacy DMA across the PCI bus
- Fast reset and Gate A20 operation
- Edge trigger or level sensitive interrupt
- Flash EPROM, 2MB EPROM and combined BIOS support
- Programmable ISA bus clock
- Supports external IOAPIC interface for symmetrical multiprocessor configurations

**Enhanced Master Mode PCI IDE Controller with Extension to UltraDMA-33**
- Dual channel master mode PCI supporting four Enhanced IDE devices
- Transfer rate up to 33MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface
- Sixteen levels (doublewords) of prefetch and write buffers
- Interlaced commands between two channels
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

**Universal Serial Bus Controller**
- USB v.1.0 and Intel Universal HCI v.1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Root hub and two function ports
- Integrated physical layer transceivers with over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

**Sophisticated PC97-Compatible Power Management**
- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v.1.0 Compliant (all required features plus extensions for most efficient desktop power management)
- APM v.1.2 Compliant
- Supports soft-off (suspend to disk) and power-on suspend with hardware automatic wake-up
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Dedicated input pin for external modem ring indicator for system wake-up
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Normal, doze, sleep, suspend and conserve modes
- System event monitoring with two event classes
- Five multi-purpose I/O pins plus support for up to 16 general purpose input ports and 16 output ports
- $I^2C$ serial bus support for JEDEC-compatible DIMM identification and on-board-device power control
- Seven external event input ports with programmable SMI condition
- Primary and secondary interrupt differentiation for individual channels
- Clock throttling control
- Multiple internal and external SMI sources for flexible power management models

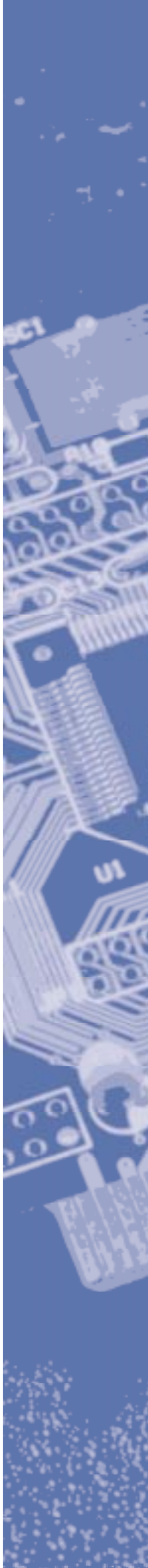
**Plug and Play Controller**
- PCI interrupts steerable to any interrupt channel
- Three steerable interrupt channels for on-board plug and play devices
- Microsoft Windows 95™ and plug and play BIOS compliant

**Pin-compatible upgrade from VT82C586 and VT82C586A for existing designs**

**Built-in Nand-tree pin scan test capability**

**0.5um mixed voltage, high speed / low power CMOS process**

**Single chip 208-pin PQFP**



# Comparison

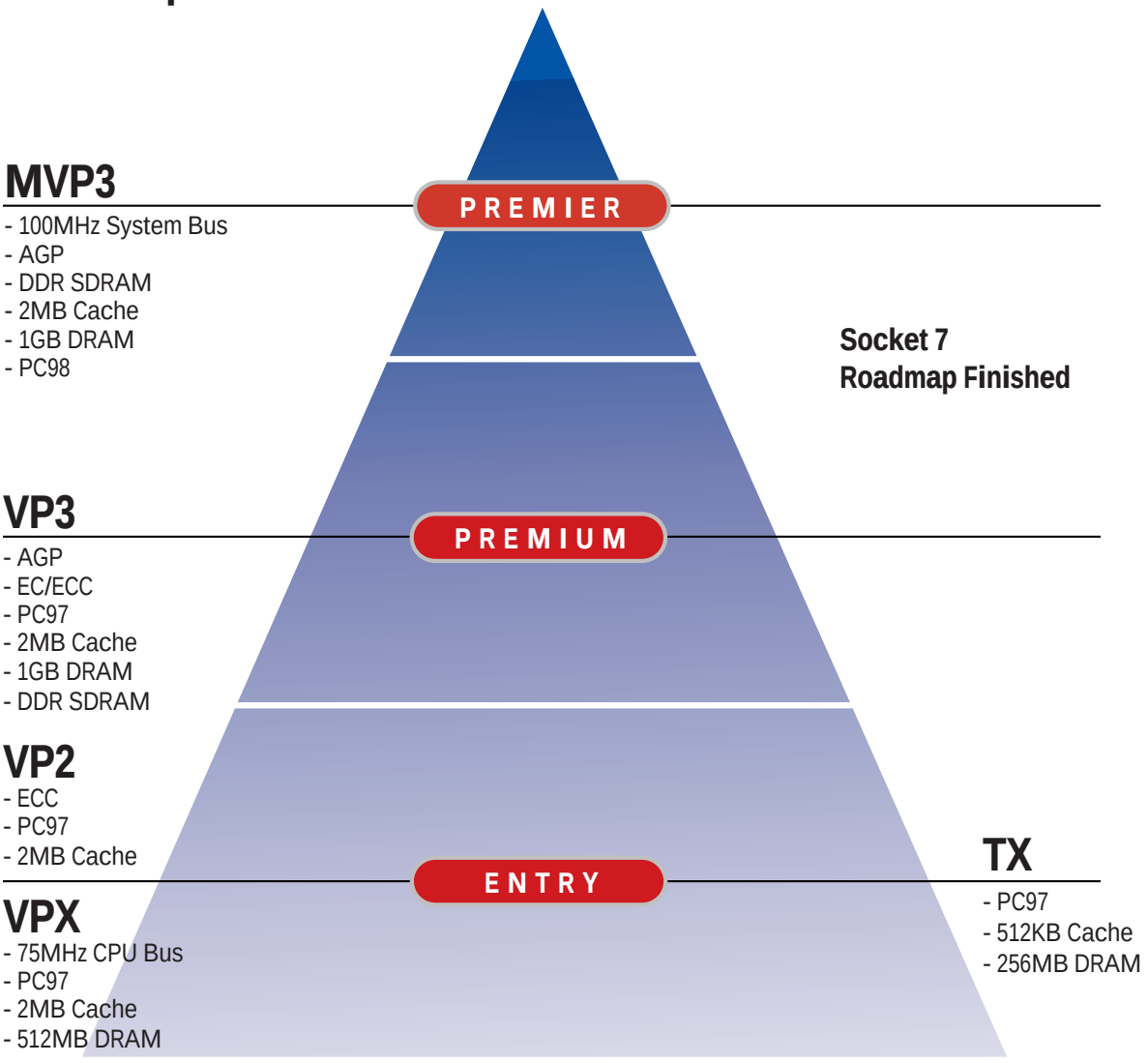
| | Apollo VPX | Apollo VP2 | Apollo VP3 | ApolloMVP3 | Intel 430TX |
|---|---|---|---|---|---|
| **Processor Support** | | | | | |
| Intel P54C | Y | Y | Y | Y | Y |
| Intel P55C | Y | Y | Y | Y | Y |
| Cyrix 6x86 | Y | Y | Y | Y | * |
| Cyrix 6x86MX | Y | Y | Y | Y | * |
| AMD K5 | Y | Y | Y | Y | * |
| AMD K6 | Y | Y | Y | Y | * |
| IDT Winchip C6 | Y | Y | Y | Y | Y |
| **L1 Cache** | | | | | |
| Write Allocate | Y | Y | Y | Y | N |
| Write Support | WB/WT | WB/WT | WB/WT | WB/WT | WB |
| Linear Burst | Y | Y | Y | Y | N |
| **L2 Cache** | | | | | |
| Max. L2 Cache size | 2MB | 2MB | 2MB | 2MB | 512KB |
| Local Bus Speed | 66/75MHz | 66MHz | 66MHz | 66/75/83/100MHz | 66MHz |
| Cache Type | ASYNCH/PB | SYNCH/PB | SYNCH/PB | SYNCH/PB | SYNCH/PB |
| Cachable Area | 512MB | 512MB | 1GB | 1GB | 64MB |
| **DRAM Interface** | | | | | |
| Max. DRAM | 512MB | 512MB | 1GB | 1GB | 256MB |
| PM Burst | 4-2-2-2 | 4-2-2-2 | 4-2-2-2 | 4-2-2-2 | 4-2-2-2 |
| EDO Burst | 5-2-2-2 | 5-2-2-2 | 6-2-2-2 | 4-2-2-2 | 5-2-2-2 |
| SDRAM Burst | 3-1-1-1 | 3-1-1-1 | 3-1-1-1 | 3-1-1-1 | 5-1-1-1 |
| AGP | N | N | Y | Y | N |
| ECC | N | Y | Y | Y | N |
| **Write Buffer** | | | | | |
| CPU to DRAM | 16 QWords | 16 QWords | 32 QWords | 32 QWords | 16 QWords |
| CPU to PCI | 6 DWords | 6 DWords | 6 DWords | 6 DWords | 6 DWords |
| PCI to DRAM | 48 DWords | 48 DWords | 48 DWords | 48 DWords | 18 DWords |
| ACPI Unit | Y | Y | Y | Y | Y |
| **PCI to ISA** | | | | | |
| UltraDMA/33 | Y | Y | Y | Y | Y |
| USB (UHCI) | Y | Y | Y | Y | Y |
| Integrated KBC | Y | Y | Y | Y | N |
| Integrated RTC | Y | Y | Y | Y | Y |
| Chip Count | 4 | 2 | 2 | 2 | 2 |

* Intel PCIsets do not support Cyrix 6x86 and 6x86MX Linear Burst Mode and AMD K5 and K6 Write Allocation and therefore are not optimized to operate with the full range of Socket 7 processors available.

# Positioning

Apollo

Triton




**MVP3**
- 100MHz System Bus
- AGP
- DDR SDRAM
- 2MB Cache
- 1GB DRAM
- PC98

**Socket 7**
**Roadmap Finished**

**VP3**
- AGP
- EC/ECC
- PC97
- 2MB Cache
- 1GB DRAM
- DDR SDRAM

**VP2**
- ECC
- PC97
- 2MB Cache

**VPX**
- 75MHz CPU Bus
- PC97
- 2MB Cache
- 512MB DRAM

**TX**
- PC97
- 512KB Cache
- 256MB DRAM