SIEMENS

AEM, INC.
4001 Shady Oak
Marion, Iowa 52302
Tel: (319) 377-1129
Fax: (319) 377-15

CMOS Color Palette SAB 82C176

Advanced Information

- 50 MHz maximum pixel rate
- 256 colors out of 262144 possible colors
- Monolithic CMOS
- Three 6-bit DACs
- Analog RGB composite blank output to drive directly into doubly terminated 75 Ω cable
- Compatible with RS343A / RS170A video standard
- Pixel address input mask function
- Read back of lookup table and register contents
- 28-pin plastic dual-in-line package, P-DIP-28 (600 mil)
- Single 5V power supply
- Fully pin and function compatible with industry standard color palette for VGA and MCGA systems

The SAB 82C176 is a monolithic CMOS color palette including a color lookup table and a digital to analog converter. The analog outputs are designed to drive an analog 75 Ω doubly terminated input of a RS170A or RS343A standard monitor (37.5 Ω load).

The SAB 82C176 is used in graphics systems working with up to 256 colors, which may independently be taken from a total of 262144 colors.

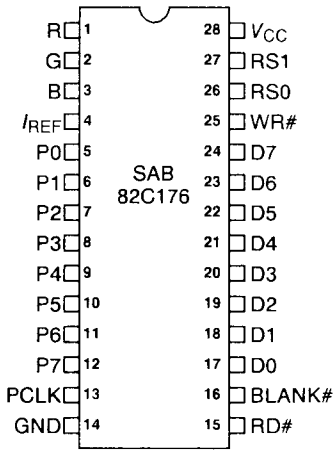
The SAB 82C176 is pin and functional compatible to the industry standard color palette for VGA and MCGA systems.

Ordering Information

Type	Ordering code	Package	Description
SAB 82C176-40-P	Q67120-P308	P-DIP-28	CMOS Color Palette, 40MHz
SAB 82C176-50-P	Q67120-P309	P-DIP-28	CMOS Color Palette, 50MHz

Pin Configuration

P-DIP-28



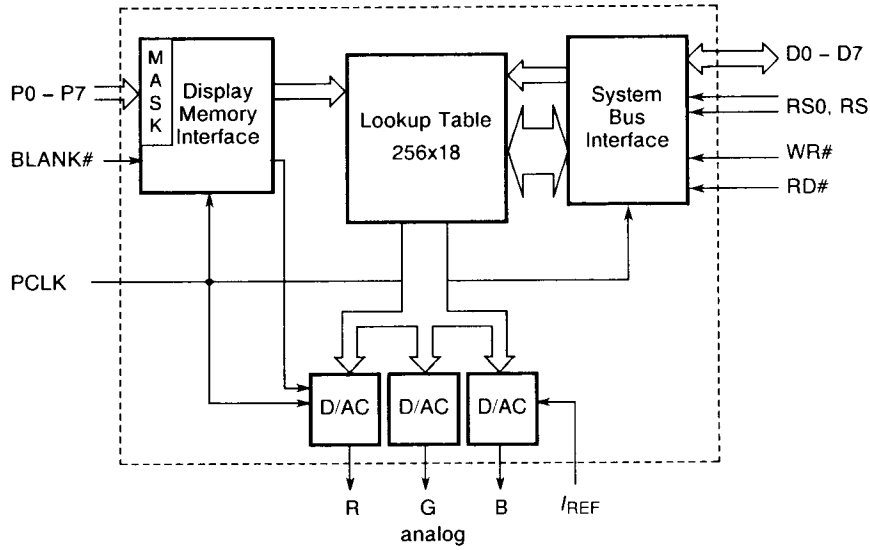
Pin Names

D0 - D7	Data Bus
RD#	Read
WR#	Write
RS0, RS1	Register Select
P0 - P7	Pixel Address
R, G, B	Red, Green, Blue
I_{REF}	Reference Current
BLANK#	Blanking
PCLK	Pixel Clock
V_{CC}	Power Supply (+ 5V)
GND	Ground (0V)

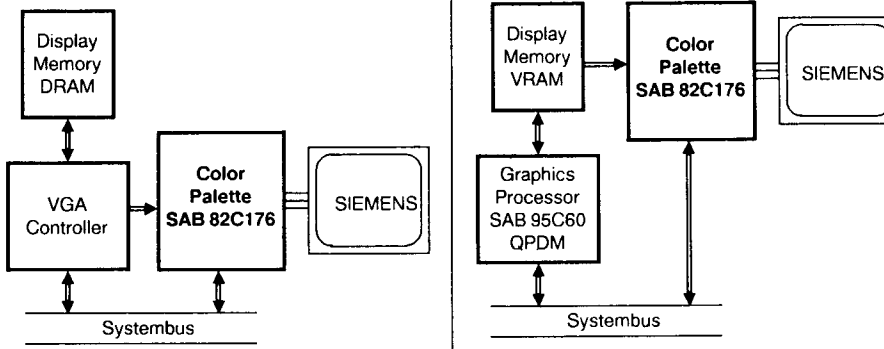
Pin Definitions and Functions

Symbol	Pin	Input (I) Output(O)	Function
PCLK	13	I	**Pixel Clock** provides the video timing control of the SAB 82C176 through the three pipeline stages from pixel address and blank inputs to the three analog outputs.
P0-P7	5-12	I	**Pixel Address** value ANDed with the pixel mask register is used as direct address to the color lookup table (these inputs are sampled with the rising edge of PCLK).
BLANK#	16	I	**BLANK** input (active low) forces the DACs of the SAB 82C176 to the value zero, delayed by 3 clocks according to the pipeline (this input is sampled with the rising edge of PCLK).
R, G, B	1, 2, 3	O	**Red, Green, Blue** Analog outputs of the three 6-bit DACs to drive a doubly terminated 75 Ω input of a RS343A or RS170A standard monitor.
I_{REF}	4	I	**Current Reference** Reference analog input for the DACs reference current, is drawn from V_{CC}.
D0-D7	17-24	I/O	**Databus** (bidirectional) The SAB 82C176 color palette is programmed via this 8-bit data bus.
RS0, RS1	26, 27	I	**Register Select** These pins select the register to be accessed during a system bus read or write cycle.
WR#	25	I	**Write#** A active low value on this pin performs a write access of the register, selected by RS0, RS1.
RD#	15	I	**Read#** A active low value on this pin performs a read access of the register, selected by RS0, RS1.
V_{CC}	28	-	**Power supply** (+ 5V)
GND	14	-	**Ground** (0V)

Block Diagram



Two Typical Applications



Functional Description

General

The SAB 82C176 color palette is a device designed for use as the output stage of raster scan video systems. It contains a high speed lookup table (RAM) of 256 x 18-bit, three 6-bit DACs, a systembus interface and a display memory interface including a pixel word mask.

Typically the color palette is placed between the monitor and the display controller with its display memory.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

Video Path

The video path is the path, where the pixel information is brought through the color palette from the display memory interface via the lookup table to the analog outputs. The video path is designed for a very high throughput.

An 8-bit value, written to the pixel address input of the display memory interface, is used by the palette as a read address for the lookup table.

On the rising edge of pixel clock the pixel address and BLANK inputs are sampled, after three further rising edges of pixel clock the relevant analog outputs appear.

The color palette includes a pixel word mask, which is controlled via the systembus and is used for masking the pixel address inputs of the display memory interface.

Each location of the lookup table, addressed by the pixel address inputs, contains an 18-bit word. Partitioned into three 6-bit words, the 18-bit data coming out of the lookup table is converted by three 6-bit DACs. The resulting three analog signals, red, green and blue, directly drive the R, G, B output for a RS170A / RS343A standard color or monochrome monitor.

The analog outputs of the DACs are designed for driving a doubly terminated 75 Ω cable. Due to this the effective analog output load ($R_{EFFECTIVE}$) is 37.5 Ω. With an I_{REF} of 8.88 mA the DACs are capable of producing an amplitude of 0.7 V for peak white.

The BLANK signal input acts on all three of the analog outputs driving them to 0V when active. An internal delay on the BLANK signal is used to correct the relationship of the BLANK signal and the pipelined pixel stream at the analog outputs.

The corresponding I_{REF} for various peak white voltages and effective output loading combinations may be calculated according to the following expression:

$$I_{REF} = \frac{V_{PEAK\ WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note: For all values of I_{REF} and output loading: $V_{BLACK\ LEVEL} = 0\ V$

Systembus Interface

The system bus interface is used for initialization and controlling the device. It contains an 8-bit bidirectional databus, two register select lines, a read line and a write line.

With the falling edge of the read or write signal the register select input is latched and decoded for selecting a register, with the rising edge data is transferred.

An internal synchronizing circuit enables access the lookup table asynchronous to the video path without any visable shnow effect on the screen.

Register Description

The list below shows the three systembus interface registers of the SAB 82C176 and the four register addresses through which they can be accessed. All registers are able to perform read and write accesses.

RS1	RS0	Register Name
0	0	Pixel address (preparing a color value write access)
1	1	Pixel address (preparing a color value read access)
0	1	Color value
1	0	Pixel mask

Pixel Address Register

There is a single pixel address register within the SAB 82C176. It is used for addressing the lookup table for read and write accesses by the systembus interface.

A write to the pixel address register via register select 00 is preparing a write access to the color-value-register (see"Writing to the lookup table").
A write to the pixel address register via register select 11 is preparing a read access from the color-value register (see"Reading from the lookup table").

The contents of the pixel address register can be read from both, register select 00 and 11.

Color Value Register

This 18-bit wide register is used as a buffer between the systembus and the lookup table. An 18-bit value can be written to or read from this register in three sequential accesses of 6-bit for each color. The sequence is: red-green-blue. The 6-bit value is transferred via the pins D0 - D5 of the systembus interface. Pins D6 and D7 are not used in write operations and are set to logical zero at read cycles.

Pixel Mask Register

The pixel mask register is accessed via the systembus and is independent of the color value and the pixel address register. The pixel address inputs of the video path are bitwise ANDed with the contents of the pixel mask register. In other words the logical value of a pin of the pixel address input is ignored and driven to "0" if the equivalent bit in the mask register is "0".

Writes to the pixel mask register are synchronized internally to the pixel clock. Thus any access to the pixel mask register can be asynchronous to the pixel clock.

The pixel mashing function can be used to create blinking or flashing objects and to ignore unused pixel address inputs.

Accessing the Lookup Table

The color palette SAB 82C176 is designed for fast access to the lookup table via the system bus interface. Therefore it can be set into two different modes: read mode for lookup table read access and write mode for lookup table write access. The modes are set and changed by writing into the pixel address register: for setting read mode the pixel address register is written via register select 11 and for setting write mode the pixel address register is written via register select 00.

Whenever the pixel address register is updated any unfinished color value read or write sequence is aborted and a new one may begin.

Writing to the Lookup Table

To set a new color definition, a value specifying a location in the color lookup table is first written to the pixel address register (register select 00). By this the color palette is set into write mode and automatically performs the following operation:

1. Specifying of an address within the lookup table.
2. Initializing of the color value register.

The values for the red, green and blue intensities are then written sequentially to the color value register (register select 01). After the blue data is written to the color value register the new color definition is transferred to the color lookup table and the pixel address register is automatically incremented pointing to the next location.

Due to this increment mechanism, it is simple to write a set of consecutive locations with new color definitions. First the start address of the set is written to the pixel address register. Then the color values for each location are written sequentially to the color value register.

Reading from the Lookup Table

In order to read a color definition a value specifying the location in the lookup table to be read is written to the pixel address register (register select 11). By this the color palette is set into read mode and automatically performs the following operation:

1. Addressing one 18-bit word of the lookup table.
2. Loading the color value register with the contents of that word.
3. Increment of the address from operation 1.

The red, green and blue intensity values then can be read by a sequence of three reads from the color value register (register select 01). After the blue value has been read, the location in the lookup table, currently specified by the pixel address register, is copied to the color value register and the pixel address register is again incremented automatically.

Thus a set of color definitions in consecutive locations can be read simply by writing the start address of the set to the pixel address register and then sequentially reading the color values for each location in the set.

Due to the increment mechanism, during each read access of the color value register containing the value of location 'n', the pixel address register contains the value 'n + 1'.

Asynchronous Lookup Table Access

The pixel address and color value registers may be accessed totally asynchronous to the high speed timing of the pixel stream being processed by the SAB 82C176. Data transfers between the lookup table and the color value register are internally synchronized to the pixel clock in the period between microprocessor interface accesses. Due to this logic, various minimum periods are specified between systembus interface accesses, to allow for the appropriate transfers to take place.

Reading from the Pixel Address Register

There is no difference from a read from address 1.1 to a read from address 0.0. In both ways the actual contents of the pixel address register are put out to the systembus interface. The contents of the pixel address register are not changed by this operation. But if a value 'n 'was written by register select 11 to the pixel address register, in a following read access the value 'n + 1' is put out, due to the increment.

Absolute Maximum Ratings

Voltage on V_{CC}	7.0 V
Voltage on any other pin	V_{SS} – 1.0 V to V_{CC} + 0.5 V
Temperature under bias	– 45 to 85 °C
Storage temperature (ambient)	– 65 to 150 °C
Power dissipation	1W
Reference current	–15 mA
Analog output current (per output)	45 mA
DC digital output current	25 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{CC}[12)] = 5 V ± 10 %; V_{SS} = 0 V

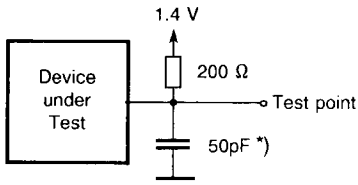
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Average power supply current	I_{CC}	–	160	mA	SAB 82C176-50 1)
Average power supply current	I_{CC}	–	155	mA	SAB 82C176-40 1)
Digital input current (any input)	I_{IN}	–	± 10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
Reference current	I_{REF}	-7.0	–	–10	mA
Off state digital output current	I_{OZ}	–	± 50	µA	–
Input logic "1" voltage	V_{IH}	2.0	–	V_{CC} + 0.5	V
Input logic "0" voltage	V_{IL}	-0.5	–	0.8	V
Output logic "1"	V_{OH}	2.4	–	V	I_{OUT} = – 5 mA
Output logic "0"	V_{OL}	–	0.4	V	I_{OUT} = 5 mA
Voltage at I_{REF} input (pin 4)	V_{REF}	V_{CC} – 3	V_{CC}	V	$V_{SS} \le V_{IN} \le V_{CC}$
Digital input capacitance	C_{IN}	–	7	pF	2)
Digital output capacitance	C_{OUT}	–	7	pF	2) 3)

Notes see page 13.

D/A Converter Characteristics 4) 5)

Parameter	Symbol	Limit values			Unit	Test condition
		min.	typ.	max.		
Resolution		6	–	–	bits	–
Maximum output voltage	V_{OUT} (max)	1.5	–	–	V	$I_{OUT} \leq 10$ mA
Maximum output current	I_{OUT}	21	–	–	mA	$V_{OUT} \leq 1$ V
Full scale error		–	–	±5	%	6)
DAC to DAC correlation		±2	–	–	%	7)
Integral linearity		±0.5	–	–	LSB	8)
Rise time (10% to 90%)		–	–	8	ns	9)
Full scale settling time		–	–	20	ns	SAB 82C176-50, 9) 2) 10)
Full scale settling time		–	–	25	ns	SAB 82C176-40, 9) 2) 10)
Glitch energy		–	120	–	pVsec	9) 2)
Analog Output Capacitance	C_{AOUT}	–	–	10	pF	2) 11)

Test load for digital outputs



*) including scope and jig capacitance

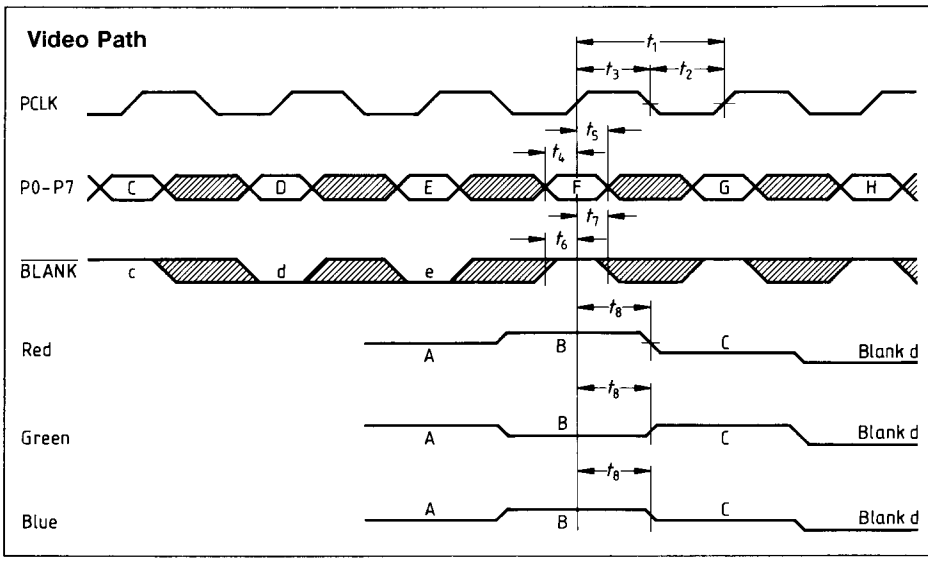
AC Test Conditions

Input pulse levels . . . . . V_{SS} to 3 V
Typical input rise and fall times (10 to 90%) . . . . . 3 ns
Digital input timing reference level . . . . . 1.5 V
Digital output timing reference level . . . . . 0.8 and 2.4 V

Notes see page 13.

AC Characteristics

Parameter	Symbol	Limit values				Unit	Test condition
		SAB 82C176-40		SAB 82C176-50			
		min.	max.	min.	max.		
Video Path							
Video Path PCLK Period	t_1	25	10000	20	10000	ns	
PCLK jitter	Δt_1	–	± 2.5	–	± 2.5	%	
PCLK width low	t_2	9	10000	6	10000	ns	
PCLK width high	t_3	7	10000	6	10000	ns	
Pixel word setup time	t_4	5	–	4	–	ns	13)
Pixel word hold time	t_5	5	–	4	–	ns	13)
BLANK setup time	t_6	5	–	4	–	ns	
BLANK hold time	t_7	5	–	4	–	ns	
PCLK to valid DAC output	t_8	5	30	5	30	ns	14)
Differential output delay between the analog outputs of the same device	Δt_8	–	2	–	2	ns	
PCLK transition time	–	–	50	–	50	ns	



Notes see page 13.

AC Characteristics (cont'd)

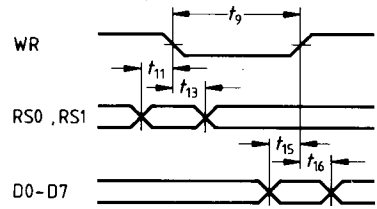
Parameter	Symbol	Limit values				Unit	Test condition
		SAB 82C176-40		SAB 82C176-50			
		min.	max.	min.	max.		
Systembus Interface							
WR# pulse width low	t_9	50	–	50	–	ns	
RD# pulse width low	t_{10}	50	–	50	–	ns	
Register select setup time to WR# low	t_{11}	15	–	10	–	ns	
Register select setup time to RD# low	t_{12}	15	–	10	–	ns	
Register select hold time to WR# low	t_{13}	15	–	10	–	ns	
Register select hold time to RD# low	t_{14}	15	–	10	–	ns	
Write data setup time	t_{15}	15	–	10	–	ns	
Write data hold time	t_{16}	15	–	10	–	ns	
Output turn-on delay	t_{17}	5	–	5	–	ns	
Read enable access time	t_{18}		40		40	ns	
Output hold time	t_{19}	5	–	5	–	ns	
Output turn-off delay	t_{20}		20		20	ns	15)
Successive write interval	t_{21}	$3 \cdot t_1$	–	$3 \cdot t_1$	–	ns	
Write followed by read interval	t_{22}	$3 \cdot t_1$	–	$3 * t_1$	–	ns	16)
Successive read interval	t_{23}	$3 \cdot t_1$	–	$3 \cdot t_1$	–	ns	17)
Read followed by write interval	t_{24}	$3 \cdot t_1$	–	$3 \cdot t_1$	–	ns	18)
Write after color write	t_{25}	$3 \cdot t_1$	–	$3 \cdot t_1$	–	ns	
Read after color write	t_{26}	$3 \cdot t_1$	–	$3 \cdot t_1$	–	ns	
Read after read blue color value	t_{27}	$6 \cdot t_1$	–	$6 \cdot t_1$	–	ns	
Write after read blue color value	t_{28}	$6 \cdot t_1$	–	$6 \cdot t_1$	–	ns	
Read after read-address write	t_{29}	$6 \cdot t_1$	–	$6 \cdot t_1$	–	ns	
Write/Read enable transition time	–	–	50	–	50	ns	

Notes see page 13.

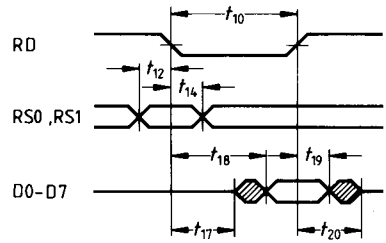
Notes for pages 9), 10), 11 and 12)

1) I_{CC} is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated pixel clock frequency. $I_{OUT} = I_{OUT}$ (max.).
2) This parameter is sampled, not 100% tested.
3) Voltage on READ# pin $\geq V_{IH}$ (min.) to disable D0 – D7).
4) Tested with I_{REF} = – 8.88 mA.
5) To assure the quality of the DACs, the power supply and I_{REF} must be absolutly constant.
6) Full scale error from the value predicted by the design equations.
7) About the mid point of the distribution of the three DACs measured at full scale deflection
8) Linearity measured from the least squares best fit line through the DAC characteristics. Monotonicity guaranteed.
9) Load = 37.5 Ω + 30 pF.
10) From a 2% change in the output voltage until settling to within 2% of the final value.
11) Voltage on BLANK# $\leq V_{IL}$(max) to disable R, G, B output.
12) This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.
13) The pixel address input has to be setup as a valid logic level with the appropriate setup and hold times to each rising edge of the PCLK (this requirement includes the blanking period).
14) A valid analog output is defined as when the changing analog signal is 50% between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions
15) Measured ± 200 mV from steady state output voltage
16) Except after writing to pixel address register with RS = 1,1 (see t_{29})
17) Except after writing blue color value (see t_{27})
18) Except after reading blue color value (see t_{28})

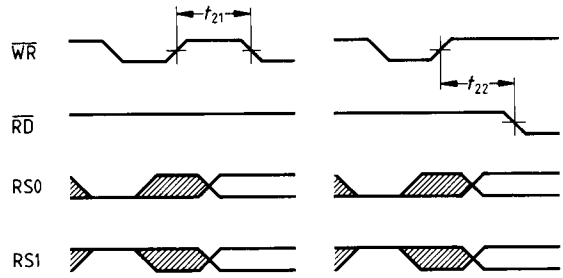
Basic Write Cycle



Basic Read Cycle

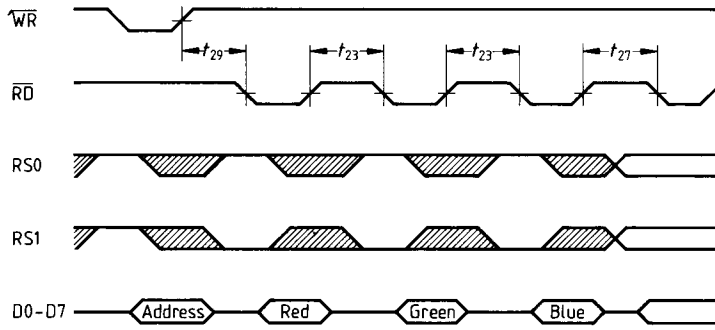


Write to Pixel Mask Register Followed by any Access

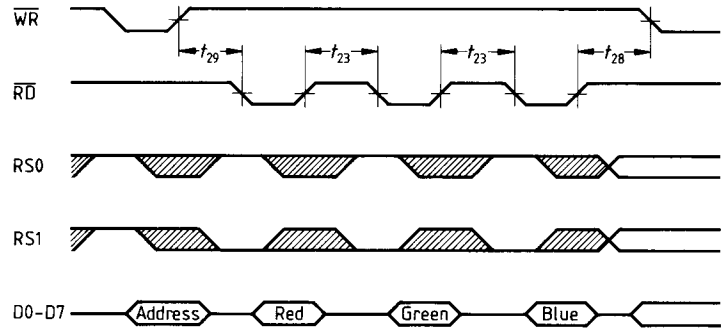


Read from Pixel Mask or Pixel Address Register Followed by any Access

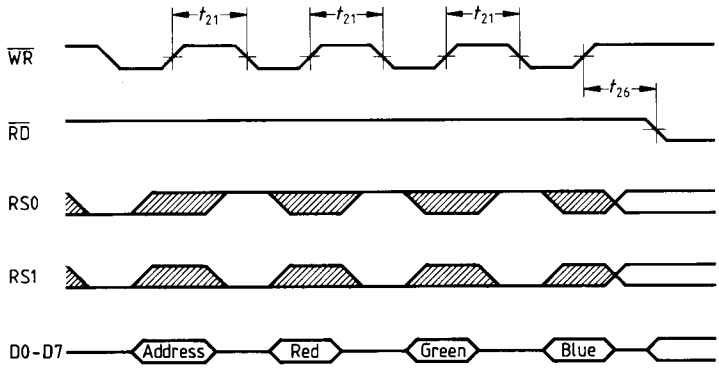
Color Value Read Followed by any Read



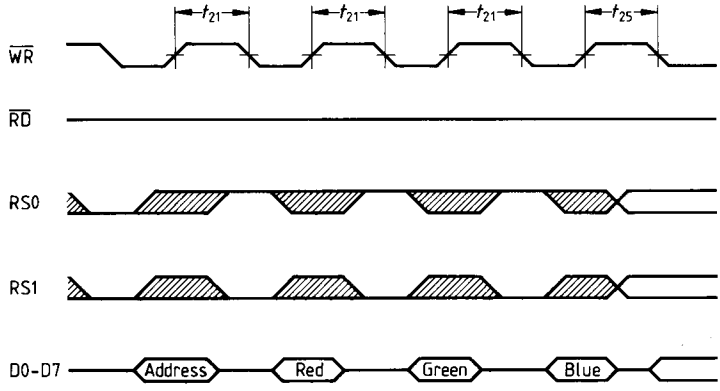
Color Value Read Followed by any Write



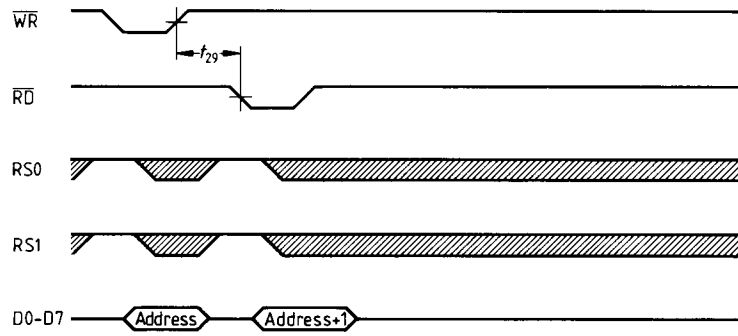
Color Value Write Followed by any Read



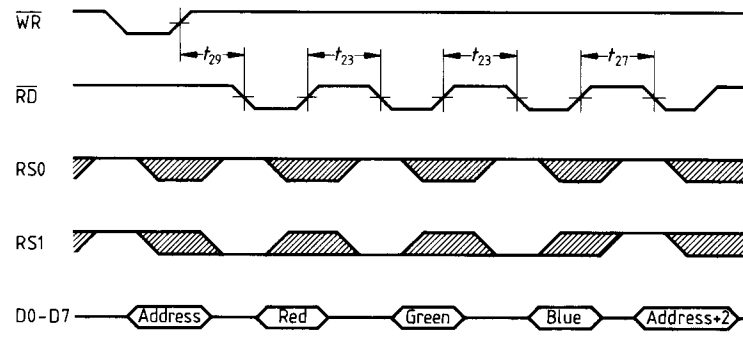
Color Value Write Followed by any Write



Color Value Read Followed by Address Register Read

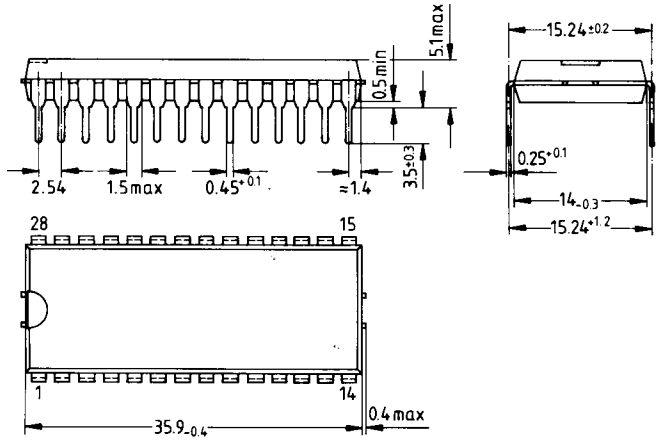


Address Register Write Followed by Address Register Read



Package Outlines

Plastic-Package, P-DIP-28
(dual-in-line-package)
20 B 28 DIN 41870 T10



Dimensions in mm