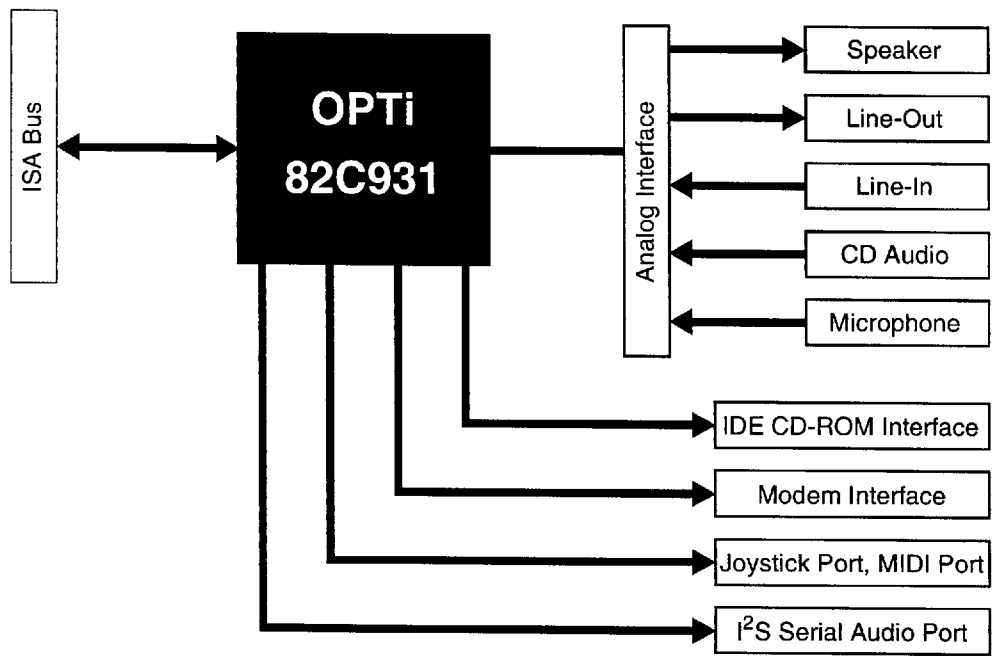
Plug and Play Integrated Audio Controller

1.0 Features

- Integrated sound controller compatible with:
  - Sound Blaster Pro™
  - Ad Lib™
  - Microsoft® Windows™ Sound System™
- Microsoft® PC-97 compliant
- Built-in high-quality 22 voice, 52 operator, OPTiFM™ music synthesizer with enhanced bass
- Built-in 7-channel mixer: five stereo, two mono
- Built-in 16-bit sigma-delta stereo codec
- ISA Plug and Play Specification 1.0a compatible, supports a maximum of six logical devices:
  - Sound Blaster Pro, Windows Sound System, FM synthesis
  - MPU-401 MIDI interface
  - CD-ROM interface
  - Joystick/game port
  - Modem interface
  - 82C931 control
- Supports external serial EEPROM (optional)
- External modem chipset interface
- Full duplex operation: record and playback simultaneously using two 8- or 16-bit DMA channels
- Supports IMA ADPCM, μ-law, A-law decompression
- 8- or 16-bit stereo sound data up to 48KHz stereo
- Supports 16-bit Type F DMA playback, accelerates telephony-audio applications
- Digital joystick interface support, improves responsiveness (Microsoft SideWinder™)
- I^2S serial interface supports Zoom Video Port, wavetable controller and modem chipset
- DirectSound™ interface support
- Power-down modes
- Silence mode to turn-off all audio functions
- Hardware and software volume control via push-button interface
- 100-pin PQFP (Plastic Quad Flat Pack)
- 100-pin TQFP (Thin Quad Flat Pack)

Figure 1-1 System Block Diagram



PAGE(S) INTENTIONALLY BLANK

2.0 Overview

The OPTi 82C931 is a sin le-chip Plu -and-Pla audio s s-tem controller and codec that provides compatibilit with Sound Blaster Pro™, Microsoft Windows Sound S stem™, OPL3, and MPU-401 interfaces. The 82C931 inte rates a 16-bit stereo si ma-delta codec and PC-97 compliant internal resource structure. This provides an effective audio solution for Windows 95 operatin s stems, DirectSound™, and advanced audio applications.

The 82C931 provides front panel push-button volume control, external modem chip interface, serial EEPROM for further customizin , support for 16-bit T pe F DMA pla back and an I^2S serial interface to a Zoom Video Port, wavetable control-ler, or modem chipset.

The 82C931 includes the followin functions: ISA bus inter-face, Sound Blaster Pro-compatible Di ital Audio Processor, MIDI interface, Windows Sound S stem interface, FM s n-thesizer interface, 16-bit codec/mixer, ame port timer, and IDE CD-ROM interface. The device also includes dual DMA channels that support full duplex operation for simultaneous record and pla back, a silence mode, power-down modes, and software pro rammable interrupts. Fi ure 2-1 shows a functional block dia ram of the 82C931. Fi ure 2-2 shows the 82C931 data flow block dia ram.

The 82C931 Inte rated Audio Controller provides all of the functions and interfaces for Sound Blaster Pro-compatible and Microsoft Windows Sound S stem-compatible cards. The 82C931 is intended to provide an inte rated audio solu-tion for business audio, educational/entertainment sound, and multimedia applications.

Figure 2-1 Functional Block Diagram

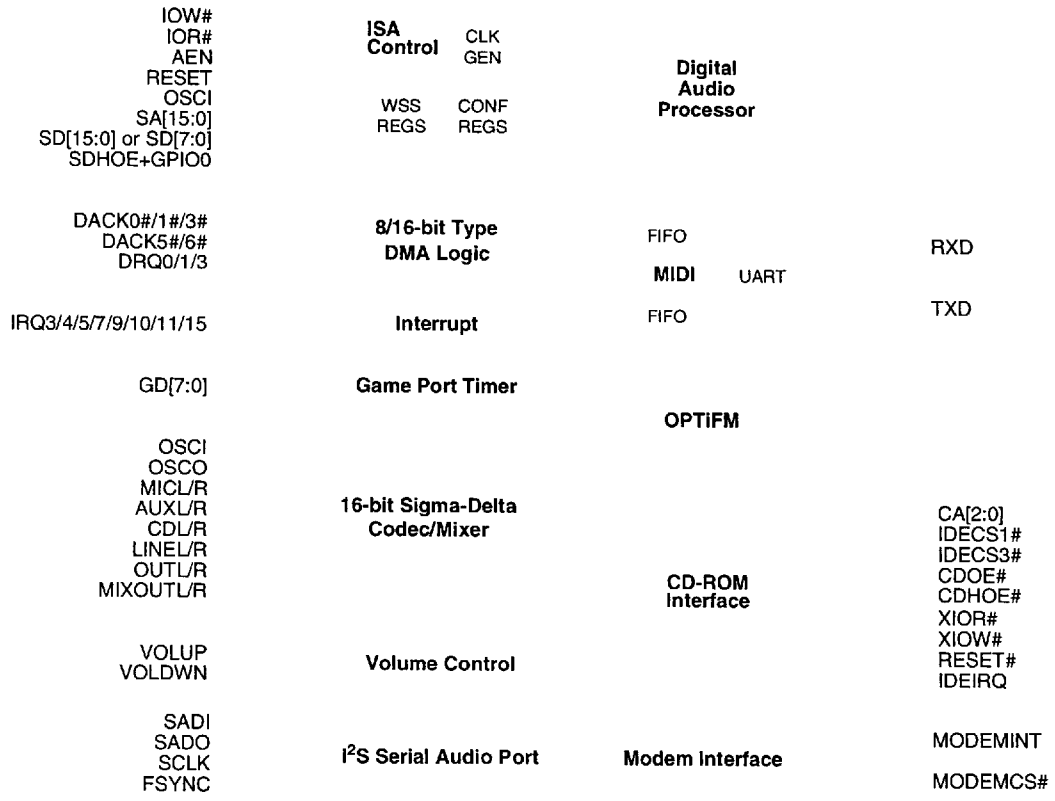
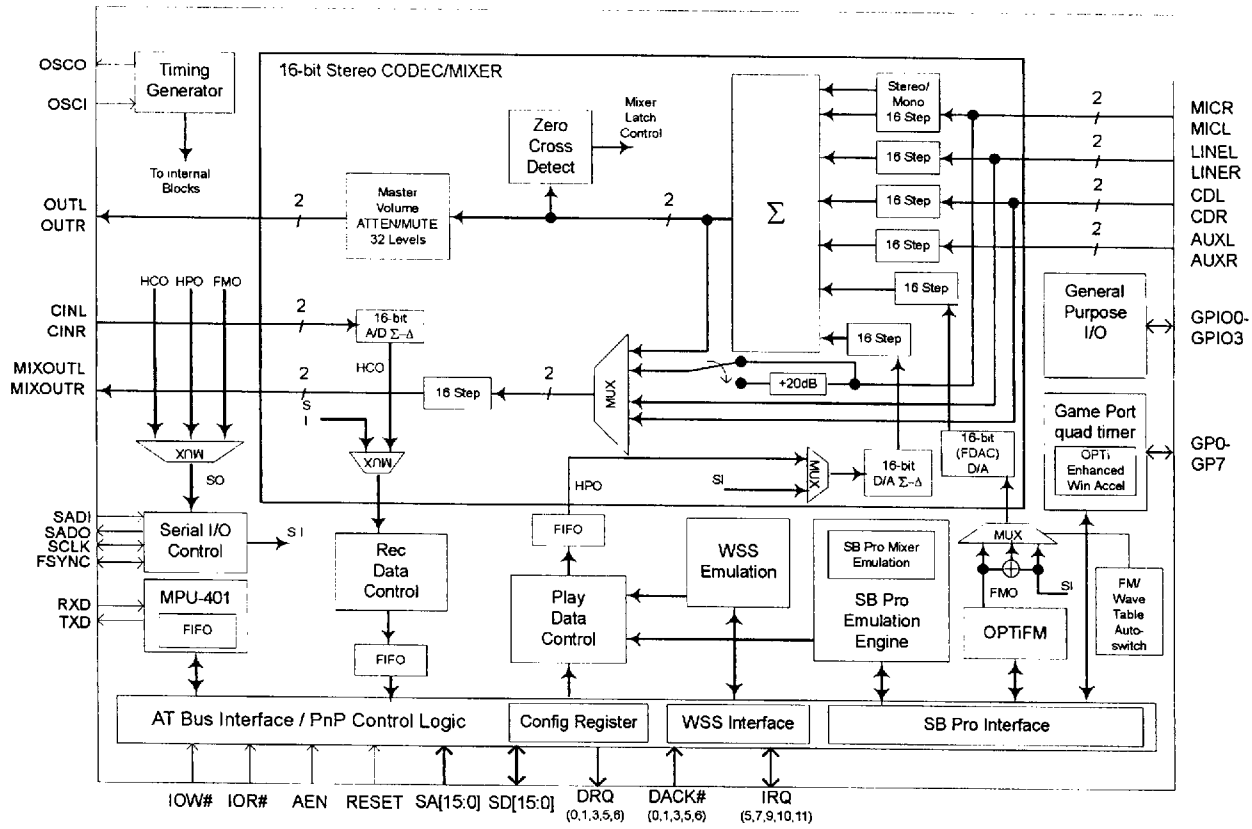


Figure 2-2 Data Flow Block Diagram



Note: There are four signals which are referenced by acronyms to make connections within the block diagram.

HCO = Host Capture Output
HPO = Host Playback Output
FMO = FM Output
SI = Serial In
SO = Serial Out

3.0 Signal Definitions

3.1 Mode Selection

The 82C931 can be configured into two different modes:

- 931-MB Mode
  - Single-chip motherboard application with 16-bit DMA support to enhance telephony-audio application performance.
- 931-AD Mode
  - Single chip adaptor card with support for IDE CD-ROM and modem interfaces.

Pins 11 is used to select the desired mode of the 82C931 (as shown in Table 3-1). Table 3-2 details the features in both of these modes.

Table 3-1 Mode Selection

Pin 11	Mode
1	931-MB
0	931-AD

Table 3-2 Mode Features

Feature	931-MB	931-AD[4]
IDE CD Interface	No	Yes
IDE Interrupt Redirect	No	Yes
Modem Interface	No	Yes[1]
Volume Control	Yes[2]	Yes[2]
Serial Audio Port	Yes[3]	Yes
Internal OPTiFM	Yes	Yes
16-Bit DMA	Yes	No

1. Pins are shared between second Game Port and Modem interface.
2. Volume Control can be used when second Game Port is not used by others.
3. Pins are shared between second Game Port and Serial Audio port.
4. The IDE and modem resources are programmable in 931-AD mode (available in 931 silicon revision 1.1 only).

Some pins of the 82C931 take on different functions depending upon its configured mode. The following subsections give the pin assignment and definitions for both the 931-MB and 931-AD modes, respectively.

In addition to mode defined pins, the 82C931 has multiplexed pins. These pins are denoted with a plus (+) sign between signal names. Their definitions can also be found in the signal description tables.

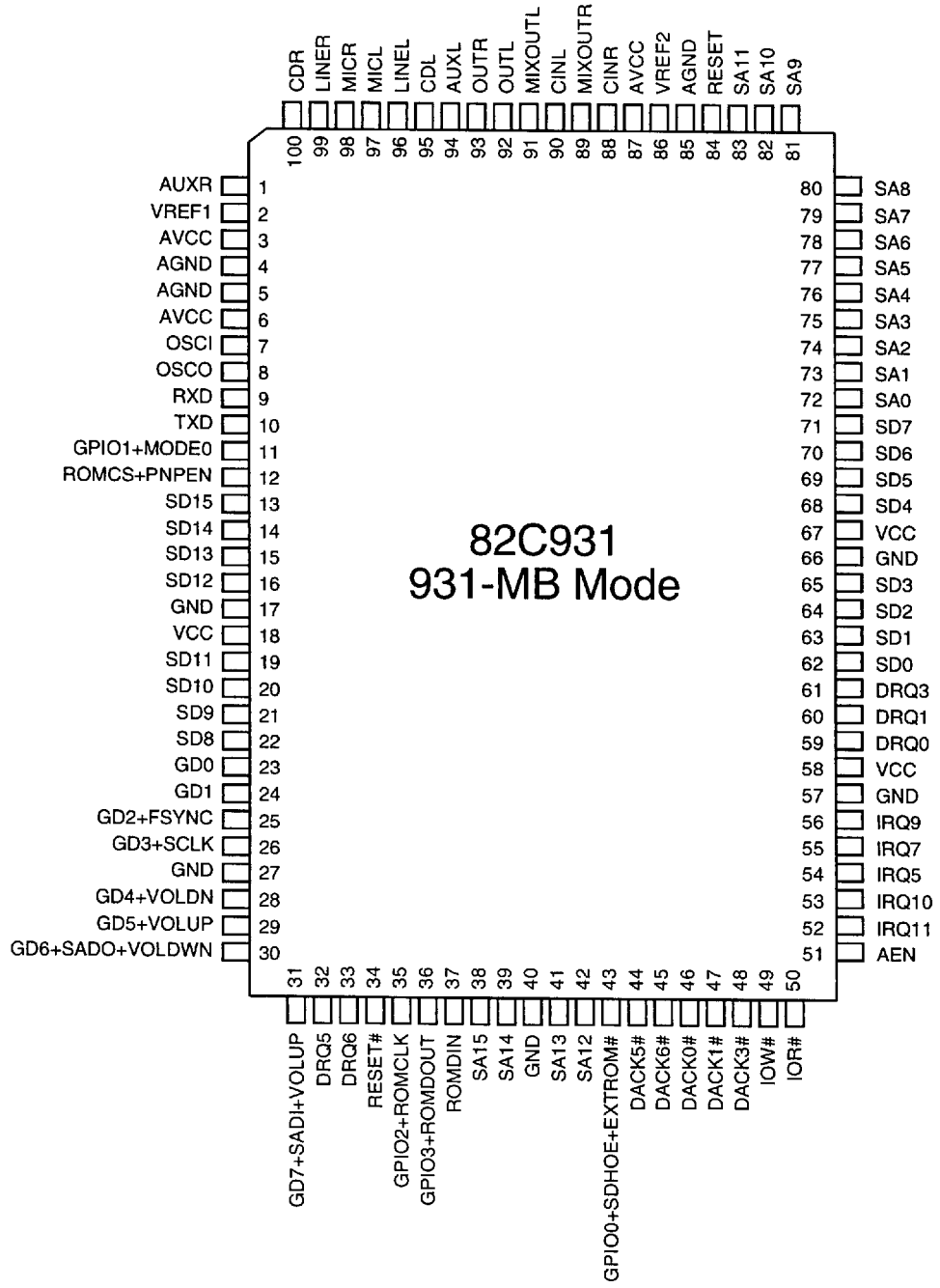
Table 3-3 defines abbreviated terms that are used throughout this section.

Table 3-3 Signal Definitions Legend

Mnemonic	Description
Analog	Analog-level compatible
CMOS	CMOS-level compatible
Ext	External
G	Ground
I	Input
Int	Internal
I/O	Input/Output
Mux	Multiplexer
O	Output
OD	Open drain
P	Power
PD	Pull-down resistor
PU	Pull-up resistor
Smt	Schmitt-trigger
TS	Tristate
TTL	TTL-level compatible

3.2 931-MB Mode

Figure 3-1 931-MB Mode PQFP Pin Diagram*



* Pinout for TQFP Package is identical to pinout for PQFP Package.

Table 3-4 931-MB Mode Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin Type
1	AUXR	I
2	VREF1	O
3	AVCC	P
4	AGND	G
5	AGND	G
6	AVCC	P
7	OSCI	I
8	OSCO	O
9	RXD	I
10	TXD	O
11	GPIO1+MODE0	I/O
12	ROMCS+PNPEN	I/O
13	SD15	I/O
14	SD14	I/O
15	SD13	I/O
16	SD12	I/O
17	GND	G
18	VCC	P
19	SD11	I/O
20	SD10	I/O
21	SD9	I/O
22	SD8	I/O
23	GD0	I/O
24	GD1	I/O
25	GD2+FSYNC	I/O
26	GD3+SCLK	I/O
27	GND	G
28	GD4+VOLDN	I/O
29	GD5+VOLUP	I/O
30	GD6+SADO+VOLDWN	I/O
31	GD7+SADI+VOLUP	I/O
32	DRQ5	O-TS
33	DRQ6	O-TS
34	RESET#	O
35	GPIO2+ROMCLK	I/O
36	GPIO3+ROMDOUT	I/O
37	ROMDIN	I/O
38	SA15	I
39	SA14	I
40	GND	G
41	SA13	I
42	SA12	I
43	GPIO0+SDHOE +EXTROM#	I/O
44	DACK5#	I
45	DACK6#	I
46	DACK0#	I
47	DACK1#	I
48	DACK3#	I
49	IOW#	I
50	IOR#	I
51	AEN	I
52	IRQ11	I/O
53	IRQ10	I/O
54	IRQ5	I/O
55	IRQ7	I/O
56	IRQ9	I/O
57	GND	G
58	VCC	P
59	DRQ0	O-TS
60	DRQ1	O-TS
61	DRQ3	O-TS
62	SD0	I/O
63	SD1	I/O
64	SD2	I/O
65	SD3	I/O
66	GND	G
67	VCC	P
68	SD4	I/O
69	SD5	I/O
70	SD6	I/O
71	SD7	I/O
72	SA0	I
73	SA1	I
74	SA2	I
75	SA3	I
76	SA4	I
77	SA5	I
78	SA6	I
79	SA7	I
80	SA8	I
81	SA9	I
82	SA10	I
83	SA11	I
84	RESET	I
85	AGND	
86	VREF2	O
87	AVCC	
88	CINR	
89	MIXOUTR	O
90	CINL	I
91	MIXOUTL	O
92	OUTL	O
93	OUTR	O
94	AUXL	I
95	CDL	
96	LINEL	I
97	MICL	
98	MICR	
99	LINER	I
100	CDR	

Table 3-5 931-MB Mode Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Type
AEN	51	I
AGND	4	G
AGND	5	G
AGND	85	G
AUXL	94	I
AUXR	1	I
AVCC	3	P
AVCC	6	P
AVCC	87	P
CDL	95	I
CDR	100	I
CINL	90	I
CINR	88	I
DACK0#	46	I
DACK1#	47	I
DACK3#	48	I
DACK5#	44	I
DACK6#	45	I
DRQ0	59	O-TS
DRQ1	60	O-TS
DRQ3	61	O-TS
DRQ5	32	O-TS
DRQ6	33	O-TS
GD0	23	I/O
GD1	24	I/O
GD2+FSYNC	25	I/O
GD3+SCLK	26	I/O
GD4+VOLDN	28	I/O
GD5+VOLUP	29	I/O
GD6+SADO+VOLDWN	30	I/O
GD7+SADI+VOLUP	31	I/O
GND	17	G
GND	27	G
GND	40	G
GND	57	G
GND	66	G
GPIO0+SDHOE +EXTROM#	43	I/O
GPIO1+MODE0	11	I/O
GPIO2+ROMCLK	35	I/O
GPIO3+ROMDOUT	36	I/O
IOW#	49	I
IOR#	50	I
IRQ5	54	I/O
IRQ7	55	I/O
IRQ9	56	I/O
IRQ10	53	I/O
IRQ11	52	I/O
LINEL	96	I
LINER	99	I
MICL	97	I
MICR	98	I
MIXOUTL	91	O
MIXOUTR	89	O
OSCI	7	I
OSCO	8	O
OUTL	92	O
OUTR	93	O
RESET	84	I
RESET#	34	O
ROMCS+PNPEN	12	I/O
ROMDIN	37	I/O
RXD	9	I
SA0	72	I
SA1	73	I
SA2	74	I
SA3	75	I
SA4	76	I
SA5	77	I
SA6	78	I
SA7	79	I
SA8	80	I
SA9	81	I
SA10	82	I
SA11	83	I
SA12	42	I
SA13	41	I
SA14	39	I
SA15	38	I
SD0	62	I/O
SD1	63	I/O
SD2	64	I/O
SD3	65	I/O
SD4	68	I/O
SD5	69	I/O
SD6	70	I/O
SD7	71	I/O
SD8	22	I/O
SD9	21	I/O
SD10	20	I/O
SD11	19	I/O
SD12	16	I/O
SD13	15	I/O
SD14	14	I/O
SD15	13	I/O
TXD	10	O
VCC	18	P
VCC	58	P
VCC	67	P
VREF1	2	O
VREF2	86	O

3.2.1 931-MB Mode Signal Descriptions

3.2.1.1 ISA Bus Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
IOW#	49	I-TTL-Smt, 50KΩ PU	***I/O Write Command***
IOR#	50	I-TTL-Smt, 50KΩ PU	***I/O Read Command***
AEN	51	I-TTL-Smt	***DMA Address Enable***
RESET	84	I-TTL-Smt, 50KΩ PD	***System Reset Input***
SA[15:0]	38, 39, 41, 42, 83:72	I-TTL	***System Address Bus Lines 15 through 0***
SD[15:8]	13:16, 19:22	I/O-TTL (12mA)	***System Data Bus Lines 15 through 8***
SD[7:0]	71:68, 65:62	I/O-TTL (16mA)	***System Data Bus Lines 7 through 0***
DACK0# DACK1# DACK3#	46 47 48	I-TTL, 50KΩ PU	***8-Bit DMA Acknowledge Bits 0, 1, and 3***
DRQ0 DRQ1 DRQ3	59 60 61	O-TS (12mA), 50KΩ PD	***8-Bit DMA Request Bits 0, 1, and 3***
DACK5# DACK6#	44 45	I-TTL	***16-Bit DMA Acknowledge Bits 5 and 6***
DRQ5 DRQ6	32 33	O-TS (12mA)	***16-Bit DMA Request Bits 5 and 6***
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	54 55 56 53 52	OD-I/O-TTL (12mA)	***Interrupt Request Bits 5, 7, and 9 through 11:*** IRQ7 and IRQ9-11 are bidirectional for WSS auto interrupt determination.

3.2.1.2 MIDI Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
RXD	9	I-TTL-Smt	***Receive Data from 32KBaud MIDI UART Port***
TXD	10	O (20mA)	***Transmit Data to 32KBaud MIDI UART Port***

931-MB Mode Signal Descriptions (cont.)

3.2.1.3 Configuration and External PnP EEPROM Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
ROMCS	12	I/O-TTL, PU (8mA)	***External Serial EEPROM Chip Select***
PNPEN			***PNP Mode Enable Jumper Input:*** Jumper setting is latched at reset power-on reset. This pin has an internal pull-up. Jumper pull-up: enable (default), pull-down: disable
GPIO1	11	I/O-TTL, PU (8mA)	***General Purpose Input/Output***
MODE0			***931 Mode Configuration Bit 0:*** This pin is used to configure the 82C931 in either the 931-MB or 931-AD mode (refer to Table 3-1). These settings are latched into the 82C931 at reset.
GPIO2	35	I/O-TTL, PD (12mA)	***General Purpose Input/Output***
ROMCLK			***External Serial EEPROM Clock***
GPIO3	36	I/O-TTL, PU (12mA)	***General Purpose Input/Output***
ROMDOUT			***External Serial EEPROM Data Out***
ROMDIN	37	I/O-TTL, PD (12mA)	***External Serial EEPROM Data In*** EEPROM enable jumper input function is removed
RESET#	34	O (12mA)	***Buffered Reset*** (active low)
GPIO0	43	I/O-TTL, PU (8mA)	***General Purpose I/O Bit 0***
SDHOE			***SD[15:8] Buffer Output Enable:*** Set MCIR19[7] = 1 to enable SDHOE function on this pin.
EXTROM			***External EEPROM enable jumper input:*** jumper setting is latched at power-on reset. This pin has internal pull-up. Jumper pull-up: disable (default), pull-down: enable

3.2.1.4 Game Port and Serial Audio Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
GD7	31	I/O-CMOS-Smt (8mA)	***Game Port 2 Data Line 7***
SADI			***Serial Audio Data Input***
VOLUP			***Volume Up:*** Interface for push-button volume control. Used to increase volume. An external pull-up is required on this pin.
GD6	30	I/O-CMOS-Smt (16mA)	***Game Port 2 Data Line 6***
SADO			***Serial Audio Data Output***
VOLDWN			***Volume Down:*** Interface for push-button volume control. Used to decrease volume. An external pull-up is required on this pin.
GD5	29	I/O-CMOS (8mA)	***Game Port 1 Data Line 5*** An External pull-up is required on this pin.
VOLUP			***Volume Up:*** Interface for push-button volume control. Used to increase volume. VOLUP on pin 29 is only available in rev. 1.1 silicon.

931-MB Mode Signal Descriptions (cont.)

3.2.1.4 Game Port and Serial Audio Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
GD4	28	I/O-CMOS (8mA)	***Game Port 1 Data Line 4*** An External pull-up is required on this pin.
VOLDN			***Volume Down:*** Interface for push-button volume control. Used to decrease volume. VOLDN on pin 28 is only available in rev. 1.1 silicon.
GD3	26	I/O-CMOS (8mA)	***Game Port 2 Data Line 3***
SCLK			***Serial Audio Clock***
GD2	25	I/O-CMOS (8mA)	***Game Port 2 Data Line 2***
FSYNC			***Serial Audio Synchronization***
GD1	24	I/O-CMOS (8mA)	***Game Port 1 Data Line 1***
GD0	23	I/O-CMOS (8mA)	***Game Port 1 Data Line 0***

3.2.1.5 Codec/Mixer Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
MICL	97	I-Analog	***Microphone Input Left***
MICR	98	I-Analog	***Microphone Input Right***
LINEL	96	I-Analog	***Line Input Left***
LINER	99	I-Analog	***Line Input Right***
CDL	95	I-Analog	***CD Input Left***
CDR	100	I-Analog	***CD Input Right***
AUXL	94	I-Analog	***Auxiliary Input Left***
AUXR	1	I-Analog	***Auxiliary Input Right***
OUTL	92	O-Analog	***Output Left***
OUTR	93	O-Analog	***Output Right***
MIXOUTL	91	O-Analog	***Mixer Output Left***
MIXOUTR	89	O-Analog	***Mixer Output Right***
CINL	90	I-Analog	***ADC Filter Pin Left***
CINR	88	I-Analog	***ADC Filter Pin Right***
VREF1	2	O-Analog	***Analog Common:*** Normally connected to AGND with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor.
VREF2	86	O-Analog	***Voltage Reference:*** Nominal 1.85V reference available externally. Not meant for current sourcing or sinking. Normally connected to AGND with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor.

931-MB Mode Signal Descriptions (cont.)

3.2.1.5 Codec/Mixer Interface Signals

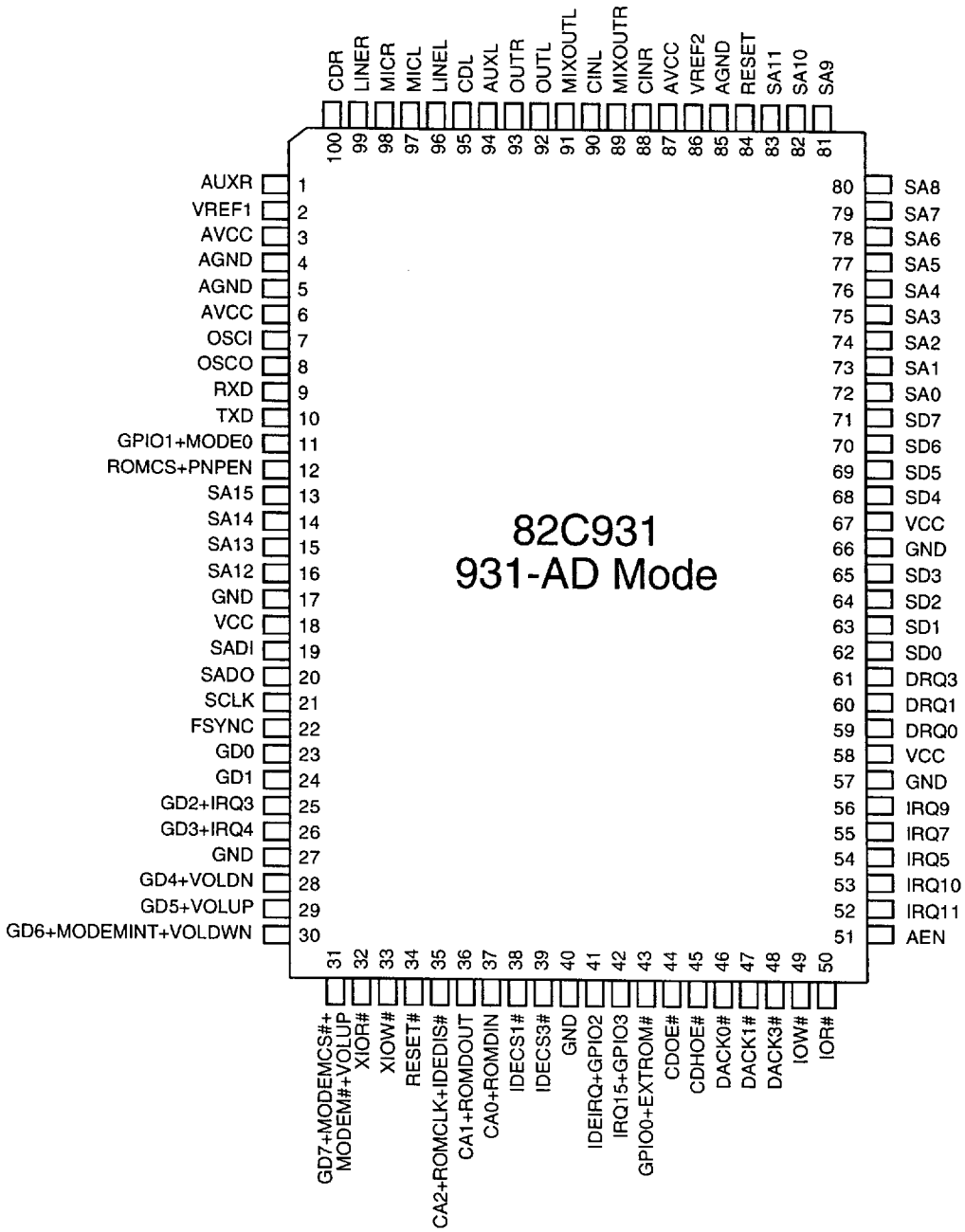
Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
OSCI	7	I-Analog	***Oscillator Input:*** A 14.318MHz crystal oscillator is to be connected across this pin and the OSCO pin.
OSCO	8	O-Analog	***Oscillator Output:*** See OSCI.

3.2.1.6 Power and Ground Pins

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
VCC	18, 58, 67	P	***Power Connection***
GND	17, 27, 40, 57, 66	G	***Ground Connection***
AVCC	3, 6, 87	P	***Analog Power Connection***
AGND	4, 5, 85	G	***Analog Ground Connection***

3.3 931-AD Mode

Figure 3-2 931-AD Mode PQFP Pin Diagram*



* Pinout for TQFP Package is identical to pinout for PQFP Package.

Table 3-6 931-AD Mode Numerical Pin Cross-Reference List

Pin No.	Pin Name	Pin Type
1	AUXR	I
2	VREF1	O
3	AVCC	P
4	AGND	G
5	AGND	G
6	AVCC	P
7	OSCI	I
8	OSCO	O
9	RXD	I
10	TXD	O
11	GPIO1+MODE0	I/O
12	ROMCS+PNPEN	I/O
13	SA15	I/O
14	SA14	I/O
15	SA13	I/O
16	SA12	I/O
17	GND	G
18	VCC	P
19	SADI	I
20	SADO	O
21	SCLK	I/O
22	FSYNC	I/O
23	GD0	I/O
24	GD1	I/O
25	GD2+IRQ3	I/O
26	GD3+IRQ4	I/O
27	GND	G
28	GD4+VOLDN	I/O
29	GD5+VOLUP	I/O
30	GD6+MODEMINT+ VOLDWN	I/O
31	GD7+MODEMCS#+ +MODEM#+VOLUP	I/O
32	XIOR#	O
33	XIOW#	O
34	RESET#	O
35	CA2+ROMCLK+ IDEDIS#	I/O
36	CA1+ROMDOUT	I/O
37	CA0+ROMDIN	I/O
38	IDECS1#	O
39	IDECS3#	O
40	GND	G
41	IDEIRQ+GPIO2	I/O
42	IRQ15+GPIO3	I/O
43	GPIO0+EXTROM#	I/O
44	CDOE#	O
45	CDHOE#	O
46	DACK0#	I
47	DACK1#	I
48	DACK3#	I
49	IOW#	I
50	IOR#	I
51	AEN	I
52	IRQ11	I/O
53	IRQ10	I/O
54	IRQ5	I/O
55	IRQ7	I/O
56	IRQ9	I/O
57	GND	G
58	VCC	P
59	DRQ0	O-TS
60	DRQ1	O-TS
61	DRQ3	O-TS
62	SD0	I/O
63	SD1	I/O
64	SD2	I/O
65	SD3	I/O
66	GND	G
67	VCC	P
68	SD4	I/O
69	SD5	I/O
70	SD6	I/O
71	SD7	I/O
72	SA0	I/O
73	SA1	I/O
74	SA2	I/O
75	SA3	I/O
76	SA4	I/O
77	SA5	I/O
78	SA6	I/O
79	SA7	I/O
80	SA8	I/O
81	SA9	I/O
82	SA10	I/O
83	SA11	I/O
84	RESET	I
85	AGND	
86	VREF2	O
87	AVCC	
88	CINR	
89	MIXOUTR	O
90	CINL	I
91	MIXOUTL	O
92	OUTL	O
93	OUTR	O
94	AUXL	I
95	CDL	
96	LINEL	I
97	MICL	
98	MICR	
99	LINER	I
100	CDR	

Table 3-7 931-AD Mode Alphabetical Pin Cross-Reference List

Pin Name	Pin No.	Pin Type
AEN	51	I
AGND	4	G
AGND	5	G
AGND	85	G
AUXL	94	I
AUXR	1	I
AVCC	3	P
AVCC	6	P
AVCC	87	P
CA0+ROMDIN	37	I/O
CA1+ROMDOUT	36	I/O
CA2+ROMCLK+ IDEDIS#	35	I/O
CDHOE#	45	O
CDL	95	I
CDOE#	44	O
CDR	100	I
CINL	90	I
CINR	88	I
DACK0#	46	I
DACK1#	47	I
DACK3#	48	I
DRQ0	59	O-TS
DRQ1	60	O-TS
DRQ3	61	O-TS
FSYNC	22	I/O
GD0	23	I/O
GD1	24	I/O
GD2+IRQ3	25	I/O
GD3+IRQ4	26	I/O
GD4+VOLDN	28	I/O
GD5+VOLUP	29	I/O
GD6+MODEMINT +VOLDWN	30	I/O
GD7+MODEMCS#+ +MODEM#+VOLUP	31	I/O
GND	17	G
GND	27	G
GND	40	G
GND	57	G
GND	66	G
GPIO0+EXTROM#	43	I/O
GPIO1+MODE0	11	I/O
IDECS1#	38	O
IDECS3#	39	O
IDEIRQ+GPIO2	41	I/O
IRQ5	54	I/O
IRQ7	55	I/O
IRQ9	56	I/O
IRQ10	53	I/O
IRQ11	52	I/O
IRQ15+GPIO3	42	I/O
IOR#	50	I
IOW#	49	I
LINEL	96	I
LINER	99	I
MICL	97	I
MICR	98	I
MIXOUTL	91	O
MIXOUTR	89	O
OSCI	7	I
OSCO	8	O
OUTL	92	O
OUTR	93	O
RESET	84	I
RESET#	34	O
ROMCS+PNPEN	12	I/O
RXD	9	I
SA0	72	I/O
SA1	73	I/O
SA2	74	I/O
SA3	75	I/O
SA4	76	I/O
SA5	77	I/O
SA6	78	I/O
SA7	79	I/O
SA8	80	I/O
SA9	81	I/O
SA10	82	I/O
SA11	83	I/O
SA12	16	I/O
SA13	15	I/O
SA14	14	I/O
SA15	13	I/O
SADI	19	I
SADO	20	O
SCLK	21	I/O
SD0	62	I/O
SD1	63	I/O
SD2	64	I/O
SD3	65	I/O
SD4	68	I/O
SD5	69	I/O
SD6	70	I/O
SD7	71	I/O
TXD	10	O
VCC	58	P
VCC	18	P
VCC	67	P
VREF1	2	O
VREF2	86	O
XIOR#	32	O
XIOW#	33	O

3.3.1 931-AD Mode Signal Descriptions

3.3.1.1 ISA Bus Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
IOW#	49	I-TTL-Smt 50KΩ PU	***I/O Write Command***
IOR#	50	I-TTL-Smt 50KΩ PU	***I/O Read Command***
AEN	51	I-TTL-Smt	***DMA Address Enable***
RESET	84	I-TTL-Smt 50KΩ PD	***System Reset Input***
SA[15:0]	13:16, 83:72	I/O-TTL (12mA)	***System Address Bus Lines 15 through 0***
SD[7:0]	71:68, 65:62	I/O-TTL (16mA)	***System Data Bus Lines 7 through 0***
DACK0# DACK1# DACK3#	46, 47, 48	I-TTL 50KΩ PU	***DMA Acknowledge Bits 0, 1, and 3***
DRQ0 DRQ1 DRQ3	59 60 61	O-TS, 50KΩ PD (12mA)	***DMA Request Bits 0, 1, and 3***
GPIO0	43	I/O-TTL, PU (8mA)	***General Purpose I/O Bit 0***
EXTROM#			***External EEPROM Enable Jumper Input:*** Jumper setting is latched at reset time. (If pin 43 is pulled up, external EEPROM is enabled.)
IRQ5 IRQ7 IRQ9 IRQ10 IRQ11	54 55 56 53 52	OD, I/O-TTL (12mA)	***Interrupt Request Bits 5, 7, and 9 through 11:*** IRQ7 and IRQ[9:11] are bidirectional for WSS auto interrupt determination
IRQ15	42	I/O-TTL (12mA)	***Interrupt Request Bit 15***
GPIO3			***General Purpose I/O Bit 1***

3.3.1.2 MIDI Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
RXD	9	I-TTL-Smt	***Receive Data from 32KBaud MIDI UART Port***
TXD	10	O (20mA)	***Transmit Data to 32KBaud MIDI UART Port***

931-AD Mode Signal Descriptions (cont.)

3.3.1.3 Configuration, External PnP EEPROM, and IDE CD-ROM Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
ROMCS	12	I/O-TTL, PU (8mA)	***External Serial EEPROM Chip Select***
PNPEN			***PNP Mode Enable Jumper Input:*** Jumper setting is latched at power-on reset. This pin has an internal pull-up. Jumper pull-up: enable (default), pull-down: disable.
GPIO1	11	I/O-TTL, PU (8mA)	***General Purpose I/O Bit 1***
MODE0			***931 Mode Configuration Bit 0:*** This pin is used to configure the 82C931 in either the 931-MB or 931-AD mode (refer to Table 3-1). These settings are latched into the 82C931 at reset.
CA2	35	I/O-TTL, PD (12mA)	***IDE CA2:*** Buffered SA2 for CD-ROM
ROMCLK			***External Serial EEPROM Clock***
IDEDIS#			***IDE Disable:*** Jumper selection to disable IDE resource. No connect equals IDE enabled. Pull down equals IDE disabled. (Available in revision 1.1 silicon only.)
CA1	36	I/O-TTL, PD (12mA)	***IDE CA1:*** Buffered SA1 for CD-ROM.
ROMDOUT			***External Serial EEPROM Data Out***
CA0	37	I/O-TTL, PD (12mA)	***IDE CA0:*** Buffered SA0 for CD-ROM.
ROMDIN			***External Serial EEPROM Data In***
IDECS1#	38	O-TTL (12mA)	***IDE CD-ROM Chip Select Bit 1:*** CD-ROM chip select for address decode range 0170h through 0177h.
IDECS3#	39	O-TTL (12mA)	***IDE CD-ROM Chip Select Bit 3:*** CD-ROM chip select for ISA address decode range 0376h through 0377h.
IDEIRQ	41	I/O-TTL (12mA)	***IDE CD-ROM Interrupt:*** Interrupt input from IDE CD-ROM which redirect to IRQ5, 7, 9, 10, 11, 15 according to PNP logic.
GPIO2			***General Purpose I/O Bit 2***
RESET#	34	O (12mA)	***Buffered Reset*** (active low)
CDOE#	44	O-TTL (8mA)	***CD Output Enable:*** Enables low-order [7:0] of the CD data buffer.
CDHOE#	45	O-TTL (8mA)	***CD High Output Enable:*** Enables high-order [15:8] of CD data buffer.
XIOR#	32	O-TTL (12mA)	***IDE Buffered IOR#***
XIOW#	33	O-TTL (12mA)	***IDE Buffered IOW#***

931-AD Mode Signal Descriptions (cont.)

3.3.1.4 Game Port and Modem Interface Signals

Signal Name	Pin No.	Signal Type (Drive)	Signal Description
GD7	31	I/O-CMOS-Smt (8mA)	***Game Port 2 Data Line 7***
MODEMCS#			***Modem Chip Select:*** Output to external modem chip select pin.
MODEM#			***Modem Interface Enable Jumper Input:*** Jumper setting is latched at power-on reset. Jumper pull-up: disable (default), pull-down: enable. An external pull-up is required on this pin.
VOLUP			***Volume Up:*** Interface for push-button volume control. Used to increase volume.
GD6	30	I/O-CMOS-Smt (8mA)	***Game Port 2 Data Line 6***
MODEMINT			***Modem Interrupt:*** Interrupt signal from external modem.
VOLDWN			***Volume Down:*** Interface for push-button volume control. Used to decrease volume. An external pull-up is required on this pin.
GD5	29	I/O-CMOS (8mA)	***Game Port 1 Data Line 5*** An external pull-up is required on this pin.
VOLUP			***Volume Up:*** Interface for push-button volume control. Used to increase volume. VOLUP on pin 29 is only available in rev. 1.1 silicon.
GD4	28	I/O-CMOS (8mA)	***Game Port 1 Data Line 4*** An external pull-up is required on this pin.
VOLDN			***Volume Down:*** Interface for push-button volume control. Used to decrease volume. VOLDN on pin 28 is only available in rev. 1.1 silicon.
GD3	26	I/O-CMOS (8mA)	***Game Port 2 Data Line 3***
IRQ4			***Interrupt Request Bit 4***
GD2	25	I/O-CMOS (8mA)	***Game Port 2 Data Line 2***
IRQ3			***Interrupt Request Bit 3***
GD1	24	I/O-CMOS (8mA)	***Game Port 1 Data Line 1***
GD0	23	I/O-CMOS (8mA)	***Game Port 1 Data Line 0***

3.3.1.5 Codec/Mixer Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
MICL	97	I-Analog	***Microphone Input Left***
MICR	98	I-Analog	***Microphone Input Right***
LINEL	96	I-Analog	***Line Input Left***
LINER	99	I-Analog	***Line Input Right***
CDL	95	I-Analog	***CD Input Left***
CDR	100	I-Analog	***CD Input Right***

931-AD Mode Signal Descriptions (cont.)

3.3.1.5 Codec/Mixer Interface Signals (cont.)

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
AUXL	94	I-Analog	***Auxiliary Input Left***
AUXR	1	I-Analog	***Auxiliary Input Right***
OUTL	92	O-Analog	***Output Left***
OUTR	93	O-Analog	**Output Right**
MIXOUTL	91	O-Analog	***Mixer Output Left***
MIXOUTR	89	O-Analog	***Mixer Output Right***
CINL	90	I-Analog	***ADC Filter Pin Left***
CINR	88	I-Analog	***ADC Filter Pin Right***
VREF1	2	O-Analog	***Analog Common:*** Normally connected to AGND with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor.
VREF2	86	O-Analog	***Voltage Reference:*** Nominal 1.85V reference available externall y. Not meant for current sourcing or sinking. Normally connected to AVS with a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor.
OSCI	7	I-Analog	***Oscillator Input:*** A 14.318MHz crystal oscillator is to be connected across this pin and the OSCO pin.
OSCO	8	O-Analog	***Oscillator Output:*** See OSCI.

3.3.1.6 Serial Audio Interface Signals

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
SADI	19	I-TTL	***Serial Audio Data Input***
SADO	20	O-TTL	***Serial Audio Data Output***
SCLK	21	I/O-TTL	***Serial Audio Clock***
FSYNC	22	I/O-TTL	***Serial Audio Synchronization***

3.3.1.7 Power and Ground Pins

Signal Name	Pin No.	Signal/Pin Type (Drive)	Signal Description
VCC	18, 58, 67	P	***Power Connection***
GND	17, 27, 40, 57, 66	G	***Ground Connection***
AVCC	3, 6, 87	P	***Analog Power Connection***
AGND	4, 5, 85	G	***Analog Ground Connection***

PAGE(S) INTENTIONALLY BLANK

4.0 Functional Description

The 82C931 is an optimized sin le chip solution with built-in Plu -and-Pla functions, built-in FM s nthesizer and 16-bit Si ma-Delta Codec to provide all of the features needed to create the followin sound characteristics and applications:

- 16-bit sound ualit Sound Blaster Pro and Windows Sound S stem compatible card
- 22 voice FM s nthesis
- 16-bit CD- ualit di ital wave audio up to 44.1KHz stereo
- Game port
- MPU-401 MIDI interface
- Wavetable s nthesis up rade

The followin sub-sections will discuss these built-in functions in detail.

4.1 Plug and Play

The OPTi 82C931 supports the ISA Plu and Pla PnP Specification 1.0a. After power-up, the 82C931 is isolated from other PnP cards in the host s stem b the s stem software. With this mechanism, the I/O address, IRQ and DMA usa e of the 82C931 can be confi ured b the s stem accordin to the free resources available. As a result, the chance of ettin a resource conflict is minimized.

The PnP function is disabled b pullin pin 12 PNPEN of the 82C931 low at power-up; otherwise the 82C931 will operate in PnP mode.

A PnP confi uration se uence is carried out b either the s stem BIOS supportin PnP or Confi uration Mana er software of the operatin s stem. It is used to map the various functional blocks lo ical devices within the 82C931 into the host s stem address space as well as to confi ure the DMA and IRQ channels. The confi uration se uence occurs as follows:

1. The 82C931 is isolated from the s stem.
2. A uni ue indentifier handle is pro rammed into the 82C931 and the resource data is read.
3. After the resource re uirement and capabilities are determined, the handle is used to assi n conflict-free resources b pro rammin the appropriate information into the 82C931 confi uration re isters a lo ical device at a time
4. After the confi uration re isters are pro rammed, the 82C931 leaves the confi uration mode and each lo ical device is activated individuall . The bus interface of each lo ical device is then enabled.

The 82C931 supports the followin lo ical devices:

- IDE CD-ROM interface
- Windows Sound S stem
- FM s nthesis
- Sound Blaster Pro
- Game Port
- MPU-401 MIDI interface
- Modem interface
- 82C931 Master Control

4.2 16-Bit Codec/Mixer

4.2.1 Codec

Features of the built-in 16-bit stereo sigma-delta codec include:

- Sigma-delta stereo ADC with 128X over-sampling
- Sigma-delta stereo DAC with 128X over-sampling
- On-chip 8X Interpolation Filter
- On-chip analog post filter
- Single-ended input and output
- Sampling rate of 5KHz to 48KHz

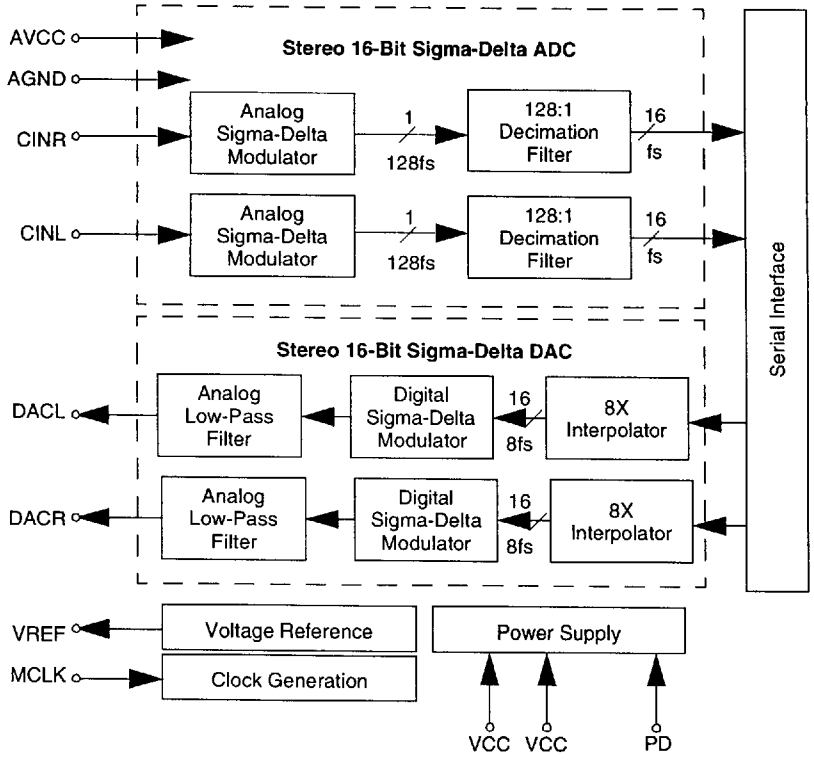
The codec serial interface provides a means to read and write 16-bit stereo data from the ADC or to the DAC respectively. The interface (as shown in Figure 4-1) consists of the following lines:

- DAC[15:0] - to write to the DAC 16-bit input
- ADC[15:0] - to read the ADC 16-bit output
- L/R - to select between the left and right channels for both the ADC and DAC data.
- MCLK - This internal master clock signal is synthesized by the frequency synthesizer from the crystal reference of 14.318MHz. One of 236 frequencies may be selected through the 8-bit FSEL line. MCLK is not active when the frequency synthesizer is powered down. The frequency of MCLK is 256 times the sampling frequency.

The DAC left/right 16-bit input data are multiplexed onto DAC[15:0] and fed into the codec. The L/R signal qualifies the data. The period of L/R is equal to that of the codec sampling frequency. One set of left/right 16-bit input data to the DAC is sent every L/R cycle. When L/R is low, the data on DAC[15:0] is meant for the left channel; when L/R is high, the data is meant for the right channel. This means that the DAC treats data packets L1 and R1 as belonging to the same sampling instance; while L2 and R2 are data for the next sampling instance.

The ADC left/right 16-bit output data are similarly multiplexed onto the ADC[15:0] bus.

Figure 4-1 Functional Block Diagram

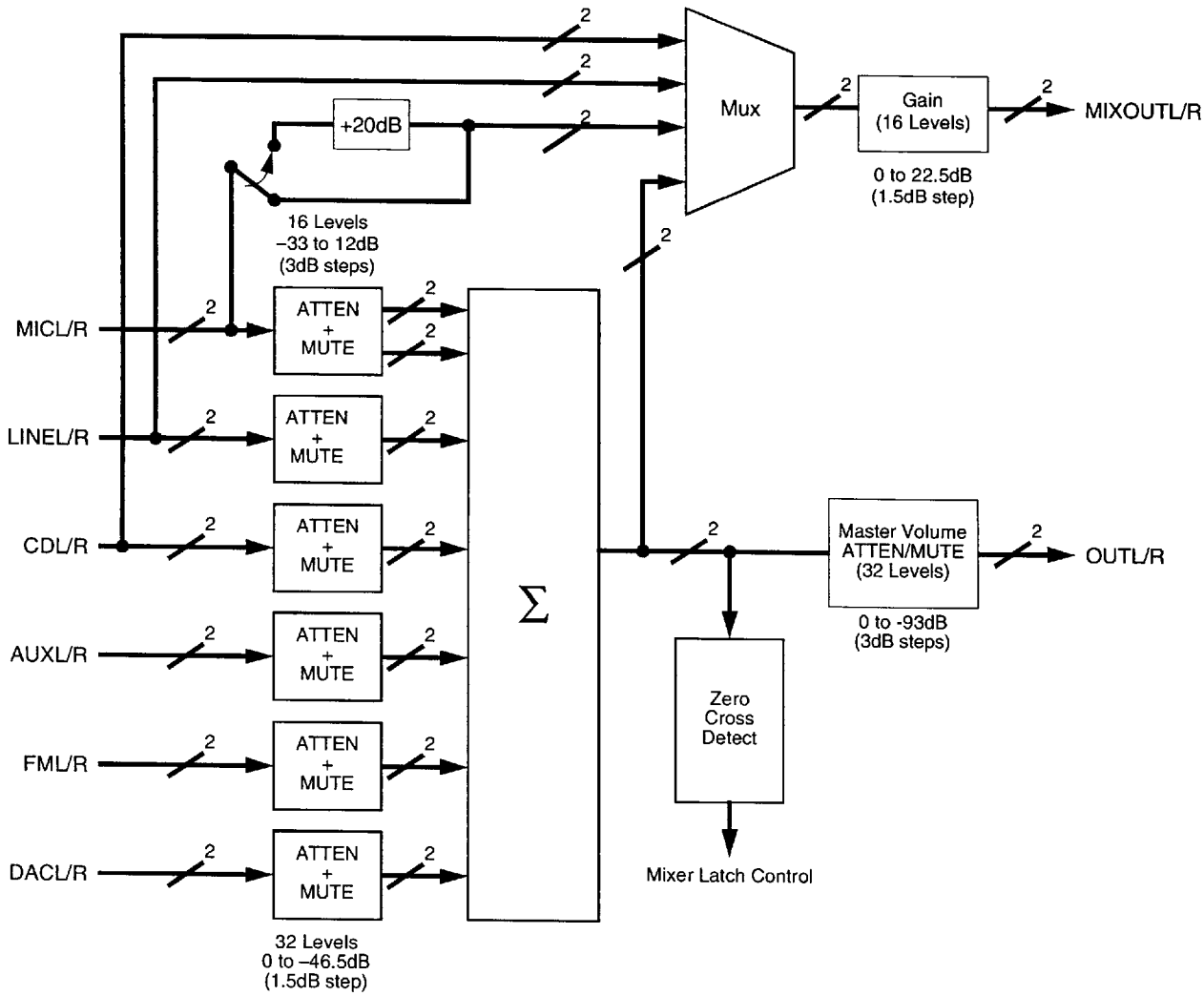


4.2.2 Mixer

The built-in mixer mixes two mono microphone level inputs (MICL/R) and five stereo analog line level input sources (LINEL/R, CDL/R, AUXL/R, FML/R, and DACL/R) with individual mixer programmable gain and mute control. The DACL/R stereo analog inputs are routed to a programmable circuit with 1.5dB steps (total of 32 levels). Internal amplifiers with a programmable 20dB gain block are provided for the MIC input (only). The remaining stereo analog inputs are routed to a programmable gain circuit which can be programmed in 3dB steps (total of 16 levels). Also, internal amplifiers with a programmable 20dB gain block are provided. Level changes only take effect on zero crossings to minimize audible artifacts. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified.

MIXOUTL (mixer record output left) must be connected to CINL (codec analog input left) with a ceramic capacitor. MIXOUTR (mixer record output right) must be connected to CINR (codec analog input right) with a ceramic capacitor. MIXOUT/R are routed via gain control (1.5dB steps: total of 16 levels). Analog output OUTL/R are routed via a master volume control which provides 0db to 94.5db of attenuation, adjustable in 3dB steps. The Codec Indirect Registers used for programming the various functions/gain levels for the mixer. For details regarding these registers, refer to Table 5-10 and Table 5-11 in the Register Section. Figure 4-2 shows a functional block diagram of the mixer.

Figure 4-2 Mixer Block Diagram



4.3 Frequency Synthesizer

The Frequency Synthesizer (FS) block generates the codec sampling clock from a reference crystal oscillator of 14.318MHz. The output frequency of the FA is equal to 256 times fs (where fs = codec sampling frequency).

One of the 236 frequencies may be generated by the FS. The selection of the FS output frequency is done via programming eight register bits in the Digital Audio Processor Write Command/Data (40h/FSEL[7:0]).

Table 4-1 gives the Frequency Selection, where the FSEL[7:0] address is given in decimal equivalent. FOUT-actual is the FS output frequency for a given FSEL code and %error gives the difference between the FOUT-actual and the target FOUT-spec.

Shaded table entries refer to the 14 critical samplin g frequencies. The error for these frequencies fall within ±0.15%.

Table 4-1 FS Output Frequencies

FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)	FSEL	FOUT-actual (Hz)
0	3909.064	43	4713.176	86	5887.335	129	7877.421	172	11910.952	215	24394.863
1	3924.890	44	4716.962	87	5915.640	130	7935.969	173	12046.394	216	24989.860
2	3938.710	45	4739.804	88	5949.967	131	7989.955	174	12189.804	217	25634.440
3	3947.978	46	4759.973	89	5992.466	132	8066.782	175	12356.559	218	26303.566
4	3951.554	47	4783.460	90	6023.197	133	8129.315	176	12494.931	219	27446.976
5	3957.289	48	4806.457	91	6059.049	134	8196.592	177	12663.325	220	27703.490
6	3994.978	49	4833.430	92	6101.420	135	8262.340	178	12817.220	221	28566.238
7	4030.968	50	4847.240	93	6138.624	136	8329.953	179	12983.677	222	29417.563
8	4033.391	51	4877.589	94	6168.715	137	8389.453	180	13159.926	223	30295.247
9	4047.543	52	4906.113	95	6214.410	138	8474.195	181	13332.077	224	31254.825
10	4067.614	53	4934.972	96	6260.786	139	8544.813	182	13511.104	225	32007.953
11	4084.752	54	4955.795	97	6292.090	140	8636.202	183	13697.066	226	33080.364
12	4092.416	55	4971.528	98	6331.663	141	8691.776	184	13866.865	227	34502.080
13	4112.477	56	4993.722	99	6377.947	142	8773.284	185	14099.921	228	35691.971
14	4131.170	57	5019.331	100	6408.610	143	8849.634	186	14286.387	229	37053.418
15	4142.940	58	5049.208	101	6453.425	144	8924.950	187	14487.810	230	38003.505
16	4164.977	59	5084.517	102	6491.839	145	9005.628	188	14703.165	231	40005.262
17	4178.655	60	5115.520	103	6544.963	146	9088.574	189	14914.583	232	41693.039
18	4209.761	61	5126.888	104	6579.963	147	9175.964	190	15147.624	233	44098.407
19	4221.108	62	5151.419	105	6615.339	148	9219.179	191	15380.664	234	45495.044
20	4237.097	63	5178.675	106	6670.513	149	9321.614	192	15627.413	235	48006.315
21	4255.520	64	5202.762	107	6711.562	150	9433.923	193	15871.938		
22	4276.976	65	5243.408	108	6750.135	151	9519.947	194	16018.697		
23	4302.284	66	5268.739	109	6802.259	152	9599.872	195	16379.408		
24	4302.284	67	5290.646	110	6848.533	153	9710.015	196	16665.917		
25	4327.892	68	5326.637	111	6895.441	154	9805.854	197	16948.390		
26	4350.087	69	5346.220	112	6935.281	155	9904.215	198	17244.987		
27	4369.507	70	5377.855	113	6991.211	156	10025.133	199	17537.275		
28	4386.642	71	5412.550	114	7049.961	157	10098.416	200	17839.642		
29	4415.502	72	5437.608	115	7089.679	158	10209.387	201	18177.148		
30	4433.451	73	5456.555	116	7139.960	159	10302.837	202	18511.939		
31	4448.952	74	5493.094	117	7190.960	160	10418.275	203	18905.810		
32	4462.475	75	5514.194	118	7250.145	161	10532.214	204	19225.830		
33	4488.185	76	5519.377	119	7295.177	162	10634.518	205	19617.129		
34	4500.090	77	5523.920	120	7359.169	163	10755.709	206	20034.515		
35	4523.725	78	5592.969	121	7402.459	164	10875.217	207	20418.775		
36	4544.287	79	5668.549	122	7457.292	165	10986.188	208	20836.550		
37	4565.689	80	5680.359	123	7512.943	166	11028.389	209	21286.672		
38	4584.401	81	5720.082	124	7573.812	167	11263.617	210	21750.434		
39	4601.810	82	5746.201	125	7626.775	168	11360.718	211	22049.203		
40	4605.974	83	5785.830	126	7690.332	169	11485.561	212	22721.435		
41	4609.590	84	5804.024	127	7752.630	170	11616.166	213	23238.391		
42	4660.807	85	5843.400	128	7813.706	171	11774.671	214	23821.904		

4.4 16-Bit Type F DMA Playback

The 82C931 supports the Type F DMA playback.

4.5 Modem Interface

The 82C931 includes the modem as a PnP logical device, as well as interface pins to connect to a modem chipset. When PnP is activated (931-AD Mode), the 82C931 provides the resource configuration for the modem chipset, such as the I/O address range and interrupt level.

The modem interface pins include pin 31 (MODEMCS#), pin 30 (MODEMINT), pin 25 (IRQ3), and pin 26 (IRQ4). To use the modem interface, pin 31 (MODEM#) must be pulled low. If a modem is connected with the 82C931, the joystick port will provide support for one joystick only.

4.6 Push Button Volume Control

In silicon revision 1.0, two pins of the joystick interface can be used as volume control push-buttons (pin 30 as volume down, and pin 31 as volume up) so that the speaker volume can be controlled through front panel buttons in desktop or notebook PCs. Appropriate software drivers are needed to enable this feature.

When the volume control feature is enabled, only one joystick will be supported by the joystick port.

In silicon revision 1.1, the volume pins are additionally available in pins 28 and 29, as shown:

pin#31 & 29 Volume up

pin#30 & 28 Volume down

These two pins are active-low, edge-triggering and pulled up internally. When the button is pressed and the corresponding pin is activated, the register bits MCIR16[5:4] are set accordingly. The software drivers poll these two bits periodically. The scheme is as follows:

Buttons	MCIR[5:4] (BUTUP:BUTDN)	Action required for the driver
Press UP button	10	increase the volume by one step
Press Down button	01	decrease the volume by one step
Press both Up & Down button	11	mute

The register bits MCIR[5:4] will be cleared automatically after they are read by the driver.

4.7 External Serial EEPROM

The 82C931 has the resource data and serial identifier required by the PnP specification stored internally. If an OEM customer wants to use a different resource data and serial identifier to customize their application, an external EEPROM can be used. To use an external EEPROM, pin 43 (EXTROM#) must be pulled low. This enables the resource data and serial identifier to be read from the external EEPROM instead of the 82C931's internal storage.

The 82C931 provides a serial EEPROM interface that is compatible with devices from a number of vendors. A 512- byte EEPROM is sufficient for information required by PnP. Pin 35 of the 82C931 provides the data clock for the EEPROM. Pin 36 provides data to the EEPROM, while pin 37 gets input from the EEPROM.

4.8 Serial Audio Interface

When the 82C931 is implemented in MB mode, the SAIO connector is coming from pins 25, 26, 30 and 31.

	931-MB mode (no pull-down at pin#11)	931-AD mode (pull-down at pin#11)
SCLK	pin#26	pin#21
FSYNC (LRCLK)	pin#25	pin#22
SADI	pin#31	pin#19
SADO	pin#30	pin#20

The 82C931's serial audio interface supports the following formats:

- I^2S-justified format (ZV port) and its variations.
- Sony format (short right-justified format, used by OPTi's wavetable chip and the Philips TDA1311AT DAC).
- AT&T PCM codec T7525 compatible16-bit mono format.

Please refer to sections 4.8.6, *ZV-Port I2S*, 4.8.7, *Advanced Precision General Purpose Serial Port*, 4.8.8, *TDA1311 Stereo Continuous Calibration*, for the respective timing diagrams.

4.8.1 I^2S-justified format and its variations

In the I^2S-justified format (ZV-port), LRCLK is low for the left channel, and high for the right channel. The left-channel MSB is left-justified to the high-to-low LRCLK transition with a single SCLK delay. SDATA could be SADI when the 931 is in receive mode, and SADO when the 931 is in transmit mode. The LRCLK period is programmable with a minimum of 32 SCLKs (MC22[4]). The following example assumes LRCLK period is greater than 32 SCLKs. Please note that in ZV port, there is one more signal MCLK defined but this is not needed for the 931.

To program the 931 in the I^2S-justified mode, the MC22 and MC21 registers need to be set. The relevant MC22 and MC21 bit definitions are shown below for reference.

I^2S-justified mode (ZV-port):
MC22[7:0] = "00110001" (31H).
MC21[7:0] = "10000010" (82H).

There are other I^2S variations: left-justified and right-justified.

For the left-justified, LRCLK is high for the left channel, and low for the right channel. The MSB is left-justified to an LRCLK transition, with zero SCLK delay.
MC22[7:0] = "00110100" (34H).
MC21[7:0] = "10000010" (82H).

For the right-justified, LRCLK is high for the left channel, and low for the right channel. The MSB is delayed from an LRCLK transition, the LSB will be right-justified to the next LRCLK transition.
MC22[7:0] = "00010100" (14H).
MC21[7:0] = "10000010" (82H).

4.8.2 Sony format[1]

This data format is essentially the same as the I^2S right-justified format. Normally there are only 32 SCLKs in a LRCLK period. The LRCLK is high for the left channel, and low for the right channel. The MSB comes in first. To set up the 931 in Sony format:
MC22[7:0] = "00000100" (04H).
MC21[7:0] = "10000010" (82H).

4.8.3 AT&T PCM codec T7525 compatible 16-bit mono format

The 931 supports the T7525 receive timing - word format with positive FSYNC. The benefit is that the 931's secondary DAC could be used to save a T7525 as the voice codec in modem/audio combo solution. To program the 931 in T7525 mode:
MC22[7:0] = "00110010" (32H)
MC21[7:0] = "10000010" (82H)

In short summary:

	I^2S-justified	left-justified	right-justified	Sony format	T7525 format
MC22[7:0]	31H*	34H*	14H*	04H*	32H
MC22[7:0]	82H				

* The MC22[4] bit setting may vary, depending on the LRCLK period (32 SCLK or more).

4.8.4 Testing I^2S format (ZV port) with Audio Precision machine

The Audio Precision machine system two 2322 has a serial audio data port that can generate a test tone in the I^2S format with programmable FSYNC, ranging from 24KHz to 48KHz. The 931 was tested with AP machine in various test tones: 256Hz, 1KHz and 3KHz in both sine wave and square wave with FSYNC = 48KHz.

To test out the feature, the AP machine is hooked up with the 931 with appropriate connections (AP's pin#6, 12, 14 are SDATA, SCLK and FSYNC, respectively). The next step is to setup the MC22 to "31H" and MC21 to "82H". Then the test tone could be heard from the speaker connected to the 931. Please note that there might be some noise in the speaker. This is due to unshielded cable used to connect the serial audio interface. Shielding the cable would help improve the audio quality.

4.8.5 Relevant MC register settings

MC22 Serial Audio format control register (R/W)							Default: 00h
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reset ASIO	ASIO test enable	First16-bit	CLK32	SCLK Polarity	FSYNC Polarity	Pulse Mode	I^2S Mode

Bit 5 First16-bit: Specifies where the data is located in the LRCLK period
0: data located at the last 16 bits of the left/right channel in an LRCLK period
1: data located at the first 16 (or 17) bit of the left/right channel in an LRCLK period

Bit 4 CLK32: Specifies the number of SCLKs per LRCLK period, used only in delay-mode or pulse-mode ASIO
0: 32 SCLK per LRCLK period
1: more than 32 SCLK per LRCLK period

1. Short right-justified format, used by OPTi's wavetable chip and the Philips TDA1311AT DAC.

Bit 3 SCLK polarity:
- 0: SDATA and LRCLK change at the rising edge of SCLK
- 1: SDATA and LRCLK change at the falling edge of SCLK

Bit 2 FSYNC (LRCLK) polarity:
- 0: LRCLK is LOW for the left channel, HIGH for the right channel
- 1: LRCLK is HIGH for the left channel, LOW for the right channel

Bit 1 Pulse mode: Used for AT&T T7525 codec or CS8412 DSP data format
- 0: Pulse mode disabled
- 1: Pulse mode enabled, used for AT&T T7525 or CS8412 data format

Bit 0 I^2S mode: MSB delay mode
- 0: Zero SCLK delay from an LRCLK transition to MSB data
- 1: One SCLK delay from an LRCLK transition to MSB data

MC21 Serial Audio selection control register (R/W)							**Default: 00h**
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
CTL_SEL[1:0]		P2S_SEL[1:0]		SPCDSEL	ADCSEL	**FDACSEL**	DACSEL

bit [7:6] CTL_SEL[1:0]: ASIO shift clock selection
- 00/11: Use the shift clock from internal FS
- 01: Use FM timing
- 10: Use external SCLK

bit 1 FDACSEL: selects the data source to the FDAC
- 0: FDAC takes FM data
- 1: FDAC takes SADI (if SPCDSEL=0) or second DMA playback data (if SPCDSEL=1)

4.8.6 ZV-Port I^2S

4.8.6.1 LRCLK

This signal determines which audio channel (left/right) is currently being input on the audio Serial Data input line. LRCLK is low to indicate the left channel and high to indicate the right channel. Typical frequency values for this signal are 48KHz, 44.1KHz, 32KHz, and 22KHz.

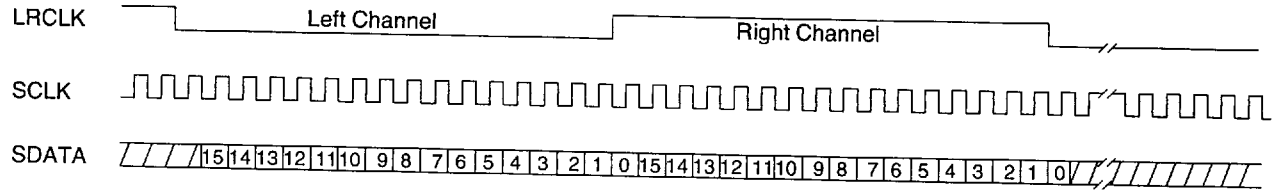
4.8.6.2 SDATA

This signal is the digital PCM signal that carries the audio information. Digital audio data is transferred using the I^2S format.

I^2S Format

The I^2S format is shown below. The digital audio data is left channel-MSB justified to the high-to-low going edge of the LRCLK plus one SCLK delay.

Figure 4-3 I^2S Format



4.8.6.3 SCLK

This signal is the serial digital audio PCM clock.

4.8.6.4 MCLK

This signal is the Master clock for the digital audio. MCLK is asynchronous to LRCLK, SDATA and SCLK.

The MCLK must be either 256x or 384x the desired Input Word Rate (IWR). IWR is the frequency at which words for each channel are input to the DAC and is equal to the LRCLK frequency. The following table illustrates several standard audio word rates and the required MCLK and LRCLK frequencies. Typically, most devices operate with 384fx master clock.

The ZV Port audio DAC should support an MCLK frequency of 384fs. This results in the frequencies shown below.

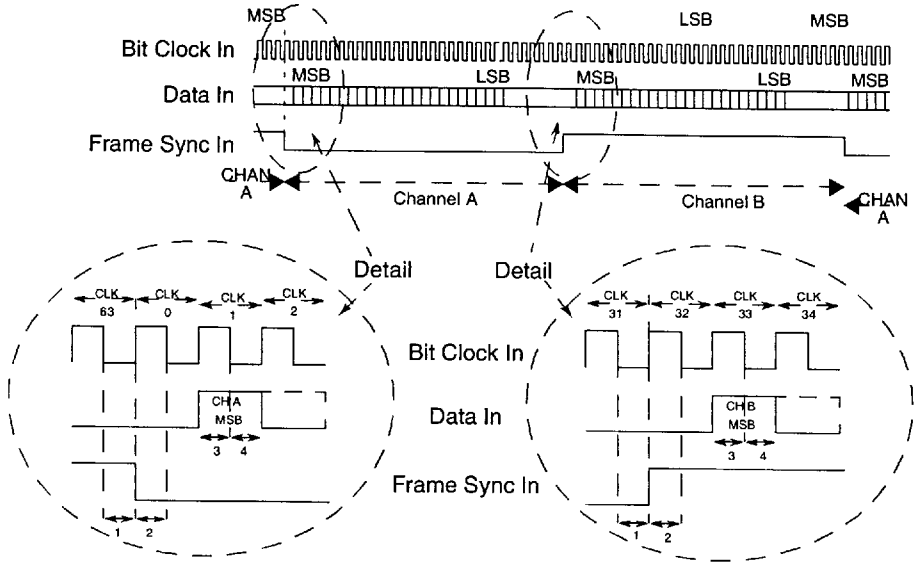
LRCLK (KHz) Sample Frequency	SCLK (MHz) 32xfs	MCLK (MHz) 384x
22	0.704	8.448
32	1.0240	12.2880
44.1	1.4112	16.9344
48	1.5360	18.4320

4.8.7 Advanced Precision General Purpose Serial Port

The 15-pin "D-sub" connector on the rear panel provides all input and output signals for a general purpose serial input.output port, plus DSP-program specific input and output pins which may be used in certain DSP (.AZ2) programs. The pinout of the connector is detailed below. All inputs are TTL level compatible CMOS. All outputs are CMOS isolated by 50Ω series resistors and rise time limiting networks.

Pin	Function	Pin	Function
1	Ground	9	Serial Input Master Clock (input)
2	+5V (tied to unused inputs high)	10	Serial Input Bit Clock (input)
3	Auxiliary Input (DSP program specific)	11	Auxiliary Output (DSP program specific)
4	Ground	12	Serial Output Bit Clock (output)
5	Ground	13	Serial Input Data (input)
6	Serial Output Data (output)	14	Serial Output Frame Sync (output)
7	Ground	15	Serial Input Frame Sync (input)
8	Ground		

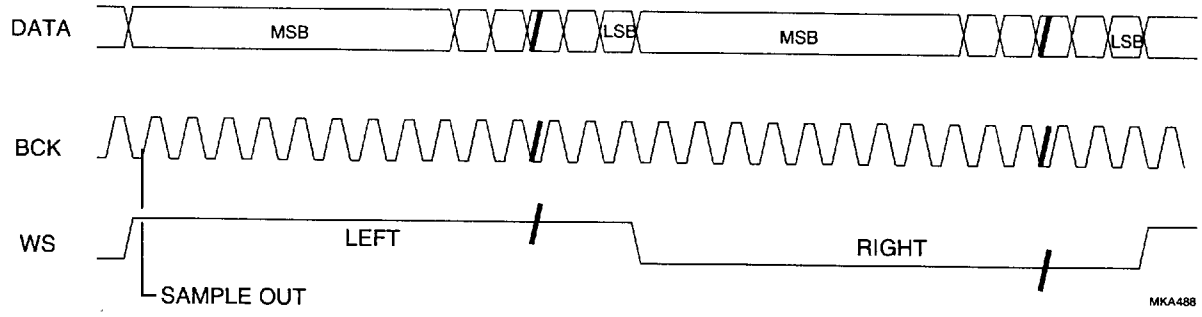
Figure 4-4 General Purpose Serial Port, Timing Relationships



1. FRAME SYNC INPUT SETUP TIME (from falling edge, las bit clock previous subframe) 30nS minimum
2. FRAME SYNC INPUT SETUP TIME (to falling edge, first bit clock of present subframe) 30nS minimum
3. DATA INPUT SETUP TIME (to bit clock falling edge) 30nS minimum
4. DATA INPUT HOLD TIME (from bit clock falling edge) 45nS minimum

4.8.8 TDA1311 Stereo Continuous Calibration

Figure 4-5 Format of Input Signals



PAGE(S) INTENTIONALLY BLANK

5.0 Register Descriptions

5.1 I/O Base Addresses

Table 5-1 lists the I/O base address re isters of the 82C931. These base addresses are pro rammable, which assists in avoidin possible I/O port conflicts amon different devices.

The confi uration re isters, called MC Indirect Re isters, located via MCBase control most functions of the 82C931. An indirect addressin scheme is used to access the MC Indirect Re isters.

The MC address 0E0Eh-0EFEh and data 0E0Fh-0FFFh I/O port addresses are full pro rammable. The onl fixed I/O port used b the 82C931 is at 0F8Dh.

The remainin I/O base address re isters are accessed b the same t pe of indexin scheme as MCBase CPU Direct I/O R/W .

Table 5-2 ives the re ister map of the 82C931.

5.2 MCBase Register

MCBase is the Direct MC base address re ister which controls access to the MC Indirect Re isters MCIR1-23 . MCIR1-23 control most of the basic functions of the 82C931 i.e., CD-ROM select, base decode address select, etc. .

To avoid possible conflict of I/O ports with different devices, the 82C931 uses a uni ue indirect addressin scheme with the base addresses bein pro rammable. Under this desi n scheme, the onl fixed I/O port used b 82C931 is at 0F8Dh. The MC address and data I/O port addresses are full pro- rammable, from 0E0Eh-0EFEh address port and 0E0Fh-0FFFh data port . To access the MC re isters:

1 All MC re isters in 82C931 are password protected. To read or write into the MC re isters, the password E4h must be written into I/O Port 0F8Dh before accessin the address or data port.

2 The address and data access port address can be full pro rammable b writin the desired base address selection into I/O port 0F8Dh bit 4 to bit 0, [b4..b0]. The port address can be read as '111b4, b3..b0, 1110' for the address port and '111b4, b3..b0, 1111' for the data port. Therefore, the possible address and data access ports can be an one from 0E0Eh-0FFEh address port and 0E0Fh-0FFFh data port .

Table 5-1 82C931 I/O Base Addresses

Base Register	Function	Address Selections
MCBase	Confi uration	0F8D; 0E0[E..F] to 0FF[E..F]
SBBase	Di ital Audio Processor	220/240
WSBase	Windows Sound S stem	530/640/E80/F40
IDEBase	IDE CD ROM	170/370
ALBase	AdLib	388
OPL4Base	OPL4	380
MIDIBase	MPU-401	300/310/320/330

Table 5-2 82C931 Register Map

I/O Address	Register Name (Type)
SBBase+00h (or ALBase+00h)	Left FM Status Port (RO)
SBBase+00h (or ALBase+00h)	Left FM Re ister Address Port (WO)
SBBase+01h (or ALBase+01h)	Left FM Data Port (WO)
SBBase+02h (or ALBase+02h)	Ri ht FM Re ister Address Port (WO)
SBBase+03h (or ALBase+03h)	Ri ht FM Data Port (WO)
SBBase+04h	Mixer Address Port (WO)
SBBase+05h	Mixer Data Port (R/W)
SBBase+06h	DAP Reset (WO)
SBBase+08h	FM Status Port (RO)
SBBase+08h	FM Re ister Address Port (WO)
SBBase+09h	FM Data Port (WO)
SBBase+0Ah	DAP Read Data (RO)
SBBase+0Ch	DAP Write Data/Cmd (WO)
SBBase+0Ch	DAP Write Buffer Status (RO)
SBBase+0Eh	DAP Output Buffer Status (RO)
WSBase+00h-03h	Confi uration (WO)
WSBase+00h-03h	Version (RO)
WSBase+04h	Codec Index Re (R/W, exists in Codec and shadowed in 82C931)
WSBase+05h	Codec Indexed Data Re (R/W, exists in Codec onl)
WSBase+06h	Codec Status Re (R/W, exists in Codec onl)
WSBase+07h	Codec Direct Data (R/W, exists in Codec onl)
200h-201h	Game Port (R/W)
0F8Dh	MCBase/Password Re ister - Specifies: MC Index Port Address (R/W) MC Data Port Address (R/W)
380-383/388-38B	OPL4 (R/W)
388-38F	OPL5 (R/W)

(3) To access MCIR1-23, write the corresponding register index into the address access port and read (or write) the data from (or to) the data access port. This read or write is only possible if the correct password (E4h) has been written into Port 0F8Dh, or is disabled (0F8Dh[7] = 1).

Tables 5-3 through 5-5 illustrate the necessary steps to access MCIR1-23. Table 5-6 gives the bit formats for the MCIR1-23.

Table 5-3 MCBase, Direct MC Register

7	6	5	4	3	2	1	0
Port 0F8Dh			**MCBase Register (WO)**				
Pass word protection for access to address or data port: 0 = Enable 1 = Disable	Reserved		These bits specify the address for MCIdx[8:4] and MCData[8:4]: (Refer to Table 5-4.) Address range = 00000 through 11111				

Table 5-4 McBase, Index (MCIndx) and Data (MCData) Ports Address Range

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Index Port Address [15:0]															
0	0	0	0	1	1	1	Specified by MCBase[4:0] (Refer to Table 5-3)					1	1	1	0
Data Port Address [15:0]															
0	0	0	0	1	1	1	Specified by MCBase[4:0] (Refer to Table 5-3)					1	1	1	1

Table 5-5 MCIdx and MCData Registers

7	6	5	4	3	2	1	0
MCIdx							
0	0	0	Specifies which MCIR register is to be accessed. 00000 = Disable 00001 = MCIR1:Base/Type Configuration 00010 = MCIR2: Reserved 00011 = MCIR3: SB/WSS Configuration 00100 = MCIR4: User Programmable GP 00101 = MCIR5: Option 00110 = MCIR6: MIDI Interface 00111 = MCIR7: Semaphore Software 01000 = MCIR8: Reserved 01001 = MCIR9: Test Control 01010 = MCIR10: Test Control 01011 = MCIR11: Status 01100 = MCIR12: Test 01101 = MCIR13: PNP Status 01110 = MCIR14: PNP CSN 01111 = MCIR15: PNP READ_DATA 10000 = MCIR16: Volume Control 10001 = MCIR17: Serial EEPROM 10010 = MCIR18: CONFIG Status 10011 = MCIR19: FM Control 10100 = MCIR20: GPIO Control 10101 = MCIR21: Serial Audio Control 10110 = MCIR22: Serial Audio Control 10111 = MCIR23: Reserved Remaining combinations = Reserved					
MCData (refer to Table 5-6)							

Table 5-6 MC Indirect Registers

7	6	5	4	3	2	1	0
MCIR1			**Base/Type Configuration Register**				**Default = 06h**
Sound Blaster I/O base address (SBBase): 0 = 220 1 = 240	Reserved	Windows Sound System I/O base address (WSBase): 00 = 530 10 = F40 01 = E80 11 = 640		CD-ROM interface: The sense of these bits is reversed during writes. To disable CD, write b'011'. 000 = Disabled 100 = Secondary IDE All others = Reserved			Game port: 0 = Disable 1 = Enable
MCIR2			**BAUD 96 register**				**Default = 00h**
Reserved Set to 0.				BAUD96: This bit could be used by PDA devices to communicate with other devices 0 = Disabled, normal MIDI UART in RXD pin. 1 = Enabled, 9600 baud rate UART in RXD pin	Reserved Set to 0.		
MCIR3			**Sound Blaster/Windows Sound System Configuration Register**				**Default = 00h**
Reserved: Must be set to 0.	Reserved: Must be set to 0 for normal operation in WSS.	DAP IRQ select: 000 = Disable 100 = IRQ11 001 = IRQ7 101 = IRQ5 010 = IRQ9 110 = Reserved 011 = IRQ10 111 = Reserved		DAP DMA select: 000 = Disabled 100 = Disable DRQ1(1) 001 = DRQ0 101 = DRQ0 DRQ1(1) 010 = DRQ1 110 = DRQ1 DRQ0(1) 011 = DRQ3 111 = DRQ3 DRQ0(1)			
(1) If CIR9[2] = 0 (Codec Indirect Register 9, bit 2), then DAP DMA[4:7] can be selected							
MCIR4			**User Programmable General Purpose Register**				**Default = 10h**
Playback FIFO flow control: 00 = Empty 10 = Full-4 01 = Full-2 11 = Not full		OPL select: 00 = OPL2 10 = OPL4 01 = OPL3 11 = OPL5		Digital-Analog controller zero: 0 = Hold 1 = Clear	Audio:(1) 0 = Disable 1 = Enable	Sound Blaster version: 00 = 2.1 10 = 3.2 01 = 1.5 11 = 4.4	
(1) Bit 2 can also accessed through the MC register or through PNP logic.							
MCIR5			**Option Register**				**Default = 00h**
Reserved		Codec Expanded Mode:(1) 0 = Disable 1 = Enable	Sound Blaster ADPCM: 0 = Disable 1 = Enable	Command FIFO in Sound Blaster mode: 0 = Disable 1 = Enable	Volume effect for Sound Blaster Pro mixer voice volume emulation: 0 = Disable 1 = Enable	DMA watch dog timer: 0 = Disable 1 = Enable When enabled, the 82C931 will generate internal DACK after the DRQ pending time-up.	Reserved
(1) Bit 5 must be set in order to access the CIR16-31, the Expanded Mode of the Codec Indirect Registers. Refer to Table 5-9 an d Table 5-11.							

Table 5-6 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR6			**MIDI Interface Register (WO)**				**Default = 00h**
MPU-401: 0 = Disable 1 = Enable	MPU-401 base address select: 00 = 330 10 = 310 01 = 320 11 = 300		MPU-401 interrupt select: 00 = IRQ9 10 = IRQ5 01 = IRQ10 11 = IRQ7		Reserved	Windows sound system mode: 0 = Disable 1 = Enable	Sound Blaster mode: 0 = Disable 1 = Enable
MCIR7			**Semaphore Software Register (Software use only)**				**Default = 00h**
D7	D6	D5	D4	D3	D2	D1	D0
MCIR8			**Reserved Register**				**Default = 00h**
MCIR9			**Test Control Register**				**Default = 00h**
Digital power-down: 0 = Normal 1 = Power-down	Analog power-down: 0 = Normal 1 = Power-down	Reserved				Software reset: 0 = Disable 1 = Enable	
MCIR10			**Test Control Register**				**Default = 00h**
Playback reset: 0 = Normal 1 = Reset (playback data path clear, active high)	Capture reset: 0 = Normal 1 = Reset (capture data path clear, active high)	PNP test mode: 0 = Normal 1 = Test (PNP logic is set to Sleep mode)	Reserved				
MCIR11			**Status Register (RO)**				**Default = 00h**
Playback DMA pending? 0 = No 1 = Yes	Capture DMA pending? 0 = No 1 = Yes	MPU interrupt pending? 0 = No 1 = Yes	CD interrupt pending? 0 = No 1 = Yes	Capture interrupt pending? 0 = No 1 = Yes	Playback interrupt pending? 0 = No 1 = Yes	Playback FIFO empty? 0 = No 1 = Yes	Capture FIFO empty? 0 = No 1 = Yes
MCIR12			**Test Register**				**Default = 00h**
Reserved			Digital test mode output high/low byte select (WO)	Digital test mode output select (WO)			
MCIR13			**PNP Status Register (RO)**				**Default = 01h**
CSN not zero - active high: 1 = PNP configuration manager assigned a CSN to 82C931.(1)	Modem interface logical device: 0 = Disable 1 = Enable	IDE logic device: 0 = Disable 1 = Enable	MC logical device: 0 = Disable 1 = Enable	CONFIG mode: 1 = 82C931's PNP logic is in the CONFIG mode	ISOLATE mode: 1 = 82C931's PNP logic is in the ISOLATE mode	SLEEP mode: 1 = 82C931's PNP logic is in the SLEEP mode	WAIT4KEY mode: 1 = 82C931's PNP logic is in the WAIT4KEY mode

(1) When a CSN is assigned to the 82C931, it switches to the PNP mode and the resource configuration is controlled through the PNP registers.

Table 5-6 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR14			**PNP CSN Register (RO)**				**Default = 00h**
PNP card select number: This registers shows the CSN assigned to the 82C931 by the PNP configuration manager.							
MCIR15			**PNP Read Port Address Register (RO)**				**Default = 00h**
PNP READ_DATA port: This registers shows the READ_DATA port assigned by the PNP configuration manager.							
MCIR16			**Volume Control Register**				**Default = 00h**
Reserved	Push-bottom volume control interrupt enable	UP bottom is pushed? 0 = No 1 = Yes This bit is cleared after a read.	DOWN bottom is pushed? 0 = No 1 = Yes This bit is cleared after a read.	Master volume mute control (active high)	Push-bottom volume control interrupt status (RO) This bit is cleared after a read.	Volume control interrupt select: 00 = Disable 01 = IRQ5 10 = IRQ10 11 = IRQ11	
MCIR17			**Serial EEPROM Control Register**				**Default = 00h**
Write to external serial EEPROM: 0 = Disable 1 = Enable	External serial EEPROM chip select: 0 = Disable 1 = Enable	External serial EEPROM clock: 0 = Disable 1 = Enable	External serial EEPROM data out: 0 = Disable 1 = Enable Connected to DIN of external EEPROM	External serial EEPROM data out: 0 = Disable 1 = Enable Connected to DIN of external EEPROM	External serial EEPROM capability (R/W) When read for status: 0 = Disable 1 = Enable When write to change: 0 = Enable 1 = Disable Note: read polarity is the opposite of write's.	PNP setting (R/W): **Read:** 0 = enabled 1 = disabled **Write:** 0 = disabled 1 = enabled Note:the polarity of the read is the opposite of the write.	Reserved
MCIR18			**CONFIG Status Register**				**Default = xxh**
Modem interface capability (R/W): When read for status: 0 = Disable 1 = Enable When write to change: 0 = Enable 1 = Disable Note: read polarity is the opposite of write's	ASIO function: 0 = Disable 1 = Enable	Reserved 0 = Default	Mode 0 status (RO): reflects 931 pin#11 setting. 0 = 931-AD for adapter 1 = 931-MD for motherboard	Chip Revision ID (RO) Silicon rev. 0.1 = 0x8 Silicon rev. 1.1 = 0x9			

Table 5-6 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR19			**FM Control Register**				**Default = xxh**
IDE IRQ input routed to IRQ output: 0 = Disable 1 = Enable	SDHOE function on pin 43 when configured for MB Mode: 0 = Disable 1 = Enable	IRQ3, IRQ4: 0 = Disable 1 = Enable	Reserved		MEGA bass: 0 = Disable 1 = Enable	OPTi mode for enhanced FM features: 0 = Disable 1 = Enable	External FM select: 0 = Disable 1 = Enable
MCIR20			**GPIO Control Register 0**				**Default = 00h**
GPIO3 mapping: 0 = Pin 42 931-AD 1 = Pin 36 931-MB	GPIO3 pin type: 0 = Input 1 = Output	GPIO2 mapping: 0 = Pin 41 931-AD 1 = Pin 35 931-MB	GPIO2 pin type: 0 = Input 1 = Output	GPIO1 mapping: Pin 11 for 931-AD and 931-MB	GPIO1 pin type: 0 = Input 1 = Output	GPIO0 mapping: Pin 43 for 931-AD and 931-MB	GPIO0 pin type: 0 = Input 1 = Output
Note: GPIO function is available only when the specified pin is not being used for another function.							
MCIR21			**Serial Audio Control Register 0**				**Default = 00h**
CTL_SEL[1:0] ASIO shift clock selection 00/11 = Use the shift clock from internal FS 01 = Use FM timing 10 = Use external SCLK		P2S_SEL[1:0] SAO data source selection 00/11 = From DMA Playback 01 = From FM 10 = From ADC, captured from analog section		SPCDSEL Enables dual playback 0 = 2nd DMA channel is used for DMA capture 1 = 2nd DMA is used with 1st DMA channel for DMA playback	ADCSEL Selects DMA data capture source 0 = ADC data (from analog section) 1 = SAI data	FDACSEL Selects FDAC data source 0 = FDAC takes FM data 1 = FDAC takes SADI (if SPCDSEL=0), 2nd DMA playback data (if SPCDSEL=1)	DACSEL Selects DAC data souce 0 = DMA playback 1 = SAI
MCIR22			**Serial Audio Control Register 1**				**Default = 00h**
Reset ASIO: 0 = Normal 1 = Reset	ASIO test mode: 0 = Normal 1 = Test	F16 Specify ASIO sample period data location: 0 = Last 16 bits of the L/R half sample period 1 = First 16/17 bits of L/R half sample period	CLK32 Number of SLCKs in a sample period (delay-mode or pulse-mode ASIO only) 0 = 32 1 = >32	SCLK polarity: 0 = Reverse 1 = No changed	FSYNC polarity: 0 = Reverse 1 = No changed	PULSE Pulse mode type of serial data (AT&T7525 comp or CS8412 DSP) 0 = Not activated 1 = Activated	

Table 5-6 MC Indirect Registers (cont.)

7	6	5	4	3	2	1	0
MCIR23			**Serial Audio Clock/Output Control Register**				**Default = 00h**
ASDOOE ADO direction control 0 = Input 1 = Output	SCLKOE SCLK direction control 0 = Input 1 = Output	FSYNCOE FSYNC direction control 0 = Input 1 = Output	MCLKEN External MCLK enable (fed through ASDO) 0 = Disabled 1 = Enabled	MCLKSEL[1:0] Master clock divider selection 00 = asdo_clk/8 01 = asdo_clk/4 10 = asdo_clk/2 11 = asdo_clk/1		CLKSEL[1:0] Selects shift clock for serial audio data output (sclk_out) 00 = mclk/8 01 = mclk/4 10 = mclk/2 11 = mclk/1	
MCIR24			**Game Port Counter Setup and Status Register**				**Default = 00h**
JRDY/Game Port IRQ Readback of '1' indicates the game port counters are stopped and the interrups is generated. The IRQ is cleared by writing a '1' to this location.	SOUNDIRQ Shows the status of the audio IRQ, a '1' indicates there is a soundIRQ	GPIRQEN IRQ generation when the game port counter is finish counting 0 = Disabled 1 = Enabled	GPWPEN Auto game port trigger (20x write) 0 = Disabled 1 = Enabled	ACTBY By axis counter enable 0 = Disabled 1 = Enabled	ACTBX Bx axis counter enable 0 = Disabled 1 = Enabled	ACTAY Ay axis counter enable 0 = Disabled 1 = Enabled	ACTAX Ax axis counter enable 0 = Disabled 1 = Enabled
MCIR25			**Game Port Counter Values Register**				**Default = xxh**
GPCOUNT[7:0] Hardware counter values in H-byte L-byte fashion (16-bit). The sequence will be: Joystick A-X axis Joystick A-Y axis Joystick B-X axis Joystick B-Y axix The count value will be changed automatically upon each read of this register. If that particular joystick axis is maksed (disa bled), the count will skip accordingly.							
MCIR26			**FDAC Data Control Register**				**Default = 00h**
JPTSTEN Game port counter test mode, counter toggled by 14.318MHz (default=1MHz) 0 = Disabled 1 = Enabled	Reserved	VCPIN Special volume control pins move the pins to up/down=GD5/4 (normal: up/down = GD7/6 0 = Disabled 1 = Enabled	ASWTST FDAC data auto-switching timer test mode, TxD timer toggled by 14.318MHz (default = 31KHz) 0 = Disabled 1 = Enabled	FDACMUL Multiply FDAC data by 2 0 = Disabled 1 = Enabled	FMMUL Multiply FM data by 2 0 = Disabled 1 = Enabled	FMDIV Divide FM data by 2 0 = Disabled 1 = Enabled	AUTOSW Auto-detect of TxD activity to switch the FDAC data between FM and serial audio (which comes from TxD 0 = Disabled 1 = Enabled

5.3 SBBase Register

SBBase is mainly used to access the Digital Audio Processor (DAP) registers, however, as shown in Table 5-7 other types of registers are also accessible through SBBase. The indexing scheme is the same as when accessing MCBase registers (CPU Direct I/O R/W). Note that in Table 5-7, which gives the SBBase register bit formats, some registers may also be accessed through ALBase. However, use only one Base register for accessing.

Table 5-7 SBBase Registers for FM and DAP Applications

7	6	5	4	3	2	1	0
SBBase+00h (or ALBase+00h)			**Left FM Status Register (RO)**				
SBBase+00h (or ALBase+00h)			**Left FM Address Port Register (WO)**				
SBBase+01h (or ALBase+01h)			**Left FM Data Port Register (WO)**				
SBBase+02h (or ALBase+02h)			**Right FM Address Port Register (WO)**				
SBBase+03h (or ALBase+03h)			**Right FM Data Port Register (WO)**				
SBBase+04h			**Mixer Address Port Register (WO)**				
SBBase+05h			**Mixer Data Port Register (WO)**				
SBBase+06h			**DAP Reset Register**				
			Don't care				DAP software reset at end of the I/O write command: 0 = Disable 1 = Enable(1)
(1) When bit 0 is enabled, it sets a software reset flag. This software reset is terminated by performing another write at this location with bit 0 = 0. A system reset will reset the software reset flag, thus terminating the software reset							
SBBase+08h			**FM Status Port Register (RO)**				
SBBase+08h			**FM Address Port Register (WO)**				
SBBase+09h			**FM Data Port Register (WO)**				
SBBase+0Ah			**DAP Read Data Register (RO)**				
SBBase+0Ch			**DAP Data/Command Register (WO)**				
SBBase+0Ch			**DAP Write Buffer Status Register (RO)**				
DAP Input buffer full:(1) 0 = Empty 1 = Full	SBBase+A[6:0]						
(1) This flag is set when the host CPU writes data in the input data bus buffer and cleared when the data is read by the internal DAP.							

Table 5-7 SBBase Registers for FM and DAP Applications (cont.)

7	6	5	4	3	2	1	0
SBBase+0Eh			**DAP Output Buffer Status Register (RO**				
DAP output buffer is full:(1) 0 = Empty 1 = Full	Output Buffer						

(1) This flag is set in the DAP when data is written in the output data bus buffer and cleared when the host CPU or the DMA controller reads the data in the output data bus buffer.

Note: Reading this register will also clear the Digital Audio Processor interrupt request.

5.4 WSBase Register

Two types of registers can be accessed through WSBase:

- Windows Sound System (WSS) and Codec registers

These registers are accessed through the WSBase register and use the same type of indexing scheme as MCBase (CPU Direct I/O R/W). The bit formats for WSS-related registers are given in Table 5-8 and Table 5-9 shows the Codec-related registers.

Table 5-8 WSBase Registers for Windows Sound System Applications

7	6	5	4	3	2	1	0
WSBase+00h-03h			**WSS Configuration Register (W0)**				**Default = 00h**
Reserved	IRQ sense source: 0 = Normal 1 = auto-interrupt selection	WSS IRQ select: 000 = Disable 001 = IRQ7 010 = IRQ9 011 = IRQ10 100 = IRQ11 101 = IRQ5 110 = Reserved 111 = Reserved			WSS DRQ select: **Playback** / **Capture** 000 = Disable / Disable 001 = DRQ0 / Disable 010 = DRQ1 / Disable 011 = DRQ3 / Disable 100 = Disabled / DRQ1 101 = DRQ0 / DRQ1 110 = DRQ1 / DRQ0 111 = DRQ3 / DRQ0		
WSBase+00h-03h			**WSS Version Register (R0)**				**Default = 00h**
Channel available: 0 = DRQ0/1/3 and IRQ7/9/10/11 available 1 = DRQ1/3 and IRQ7/9 available	IRQ sense: 0 = No interrupt 1 = WSS interrupt active	Version: 04h					

Note that at the Codec Index Address Register (WSBase+04h), bits 4 through 0 are used as the index address for accessing the Codec Indirect Registers (CIR). A write to or a read from the Codec Indexed Data Register (WSBase+05h) will access the Indirect Register which is indexed by the value most recently written to the Codec Index Address Register.

There are 31 Codec Indirect Registers, CIR0-CIR15 are accessed normally. To access CIR16 through CIR31, Expanded Mode registers, MCIR12[5] = 1 (MCBase Indirect Register, bit 5). Table 5-10 gives the bit formats for CIR0-CIR15 and Table 5-11 shows CIR16-CIR31.

Table 5-9 WSBase Register for Codec/Mixer Applications

7	6	5	4	3	2	1	0
WSBase+04h	**Codec Index Address Register (R/W, exists in Codec and shadowed in 82C931)**						**Default = 00h**
Initialization: This bit is set when the codec is in a state which cannot respond to parallel bus cycles.(1)	Mode change: 0 = Disable 1 = Enable	Transfer request:(2) 0 = Transfers enabled during interrupt 1 = Transfers disabled by interrupt	Index address: These bits specify which Codec Indirect Register (CIR) is to be accessed. Note CIR16 through CIR31 are Expanded Modes and require that MCIR12[5] = 1. (Refer to Table 5-10 and Table 5-11 for these registers bit formats.)				
			00000 = CIR0: MIXOUTL Output Cntrl				**Expanded Mode Registers** 10000 = CIR16: AUXL Input Cntrl
			00001 = CIR1: MIXOUTR Output Cntrl				10001 = CIR17: AUXR Input Cntrl
			00010 = CIR2: CDL Input Cntrl				10010 = CIR18: LINEL Input Cntrl
			00011 = CIR3: CDR Input Cntrl				10011 = CIR19: LINER Input Cntrl
			00100 = CIR4: FML Input Cntrl				10100 = CIR20: MICL Input Cntrl
			00101 = CIR5: FMR Input Cntrl				10101 = CIR21: MICR Input Cntrl
			00110 = CIR6: DACL Input Cntrl				10110 = CIR22: OUTL Gain Cntrl
			00111 = CIR7: DACR Input Cntrl				10111 = CIR23: OUTR Gain Cntrl
			01000 = CIR8: Fs & Playback Data Format				11000 = CIR24: Reserved
			01001 = CIR9: Interface Configuration				11001 = CIR25: Reserved
			01010 = CIR10: Pin Cntrl				11010 = CIR26: Reserved
			01011 = CIR11: Error Status & Initialization				11011 = CIR27: Reserved
			01100 = CIR12: Mode and ID (Mode 2 Bit)				11100 = CIR28: Capture Data Format
			01101 = CIR13: Reserved				11101 = CIR29: Reserved
			01110 = CIR14: Playback Upper Base				11110 = CIR30: Capture Upper Base
			01111 = CIR15: Playback Lower Base				11111 = CIR31: Capture Lower Base
(1) Immediately after reset and once the codec has left the initialization state, the initial value of this register will be "0100 0000" (40h). During codec initialization, the Codec Index Register cannot be written and is always read 1000 0000 (80h).							
(2) When bit 5 is set, DMA transfers cease when bit 0 of the Codec Status Register (WSBase+06h) = 1.							
WSBase+05h	**Codec Indexed Data Register (R/W, exists in Codec only)**						**Default = 00h**
Contains the contents of the Codec register referenced by the Index Data Register. During codec initialization, this register cannot be written and is always read as "1000 0000" (80h).							

Table 5-9 WSBase Register for Codec/Mixer Applications (cont.)

7	6	5	4	3	2	1	0
WSBase+06h			**Codec Status Register (R/W, exists in Codec only)**				**Default = 44h**
PIO capture data is ready for upper or lower byte (RO): 0 = Lower 1 = Upper (or any 8-bit mode)	PIO capture data is waiting for right or left channel ADC (RO): 0 = Right 1 = Left (or mono)	PIO Capture Data Register contains data ready for reading by host (RO):(1) 0 = Stale ADC data (do not re-read) 1 = Fresh ADC data (ready for next host data read)	Sample over/underrun (RO): Indicates that the most recent sample was not serviced in time; therefore either an overrun for ADC capture or underrun for DAC playback has occurred.(2)	PIO playback data is needed for upper or lower byte (RO): 0 = Lower 1 = Upper (or any 8-bit mode)	PIO playback data is needed for right or left channel DAC (RO): 0 = Right 1 = Left (or mono)	PIO Playback Data Register ready for more data (RO):(1) 0 = Valid DAC data (do not overwrite) 1 = Stale DAC data (ready for next host data write value)	Interrupt: 0 = Disable 1 = Enable

(1) These bits (5 and 1) should only be programmed when direct programmed I/O data transfers are desired.

(2) If both capture and playback are enabled, the source which set bit 4 ca be determined by reading COR and PUR. Bit 4 changes on a sample-by-sample basis.

Note: Bits 5, 1, and 0 can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value just as these bits are changing (e.g., a value of 1 would not be read until the next host access). This register's initial state after reset is "1100 1100".

WSBase+07h **Codec Direct Data Register - Capture Mode (RO, exists in Codec only)** **Default = 00h**

The Codec Direct Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000" (80h).

PIO Capture Data Register:

This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

WSBase+07h **Codec Direct Data Register - Playback Mode (WO, exists in Codec only)** **Default = 00h**

The Codec Direct Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000" (80h).

PIO Playback Data Register:

This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Table 5-10 Codec Indirect Registers

D7	D6	D5	D4	D3	D2	D1	D0
CIR0			**MIXOUTL Output Control Register**				**Default = 00h**
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTL (dB): 0000 = 0 0110 = +9.0 1011 = +16.5 0001 = +1.5 0111 = +10.5 1100 = +18.0 0010 = +3.0 1000 = +12.0 1101 = +19.5 0011 = +4.5 1001 = +13.5 1110 = +21.0 0100 = +6.0 1010 = +15.0 1111 = +22.5 0101 = +7.5			
CIR1			**MIXOUTR Output Control Register**				**Default = 00h**
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTR (dB): Refer to CIR0[3:0] for decode.			
CIR2			**CDL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for CDL (dB): 0000 = +12 0110 = –6 1011 = –21 0001 = +9 0111 = –9 1100 = –24 0010 = +6 1000 = –12 1101 = –27 0011 = +3 1001 = –15 1110 = –30 0100 = 0 1010 = –18 1111 = –33 0101 = –3 Note: This decode is also applicable for the MIC, LINE, AUX, and FM inputs.				Reserved
CIR3			**CDR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select CDR (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR4			**FML Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FML (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR5			**FMR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FMR (dB): Refer to CIR2[4:1] for decode.				Reserved

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR6			**DACL Input Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): *00000 = 0 00001 = –1.5 00010 = –3.0 00011 = –4.5 00100 = –6.0 00101 = –7.5 00110 = –9.0 00111 = –10.5	 01000 = –12.0 01001 = –13.5 01010 = –15.0 01011 = –16.5 01100 = –18.0 01101 = –19.5 01110 = –21.0 01111 = –22.5	 10000 = –24.0 10001 = –25.5 10010 = –27.0 10011 = –28.5 10100 = –30.0 10101 = –31.5 10110 = –33.0 10111 = –34.5	 11000 = –36.0 11001 = –37.5 11010 = –39.0 11011 = –40.5 11100 = –42.0 11101 = –43.5 11110 = –45.0 11111 = –46.5	
CIR7			**DACR Input Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): Refer to CIR6[4:0] for decode.				
CIR8			**Fs and Playback Data Format Register**				**Default = 00h**
Audio data format - linear PCM or companded for all input and output data (used in conjunction with bit 5):(1) 000 = Linear, 8-bit unsigned 001 = μ-law, 8-bit companded 010 = Linear, 16-bit two's complement, Little Endian 011 = A-Law, 8-bit companded 100 = Reserved 101 = ADPCM, 4-bit, IMA compatible 110 = Linear, 16-bit two's complement, Big Endian 111 = Reserved **Note:** Bit 7 is not available in Mode 1 (forced to 0).			Stereo/mono:(2) 0 = Mono 1 = Stereo	Clock frequency divide / audio sample rate frequency: 0000 = 8.0kHz 0010 = 16.0kHz 0100 = 27.42857kHz 0110 = 32.0kHz 1000 = Reserved 1010 = Reserved 1100 = 48.0kHz 1110 = 9.6kHz		 0001 = 5.5125kHz 0011 = 11.025kHz 0101 = 18.9kHz 0111 = 22.05kHz 1001 = 37.8kHz 1011 = 44.1kHz 1101 = 33.075kHz 1111 = 6.615kHz	

(1) SB/WSS mode switch: In Sound Blaster mode, the software driver should set CDF to 8 bit PCM mode (R8: FM1,FM-,C_L).

(2) Selecting stereo results with alternating samples representing left and right audio channels. Mono playback plays the same a udio sample on both channels. Mono capture only captures data from the left audio channel.

Note: The contents of this register can only be changed if the mode change bit (WSBase+04h[6]) is enabled (set to 1). Writes to this register without the mode change bit enabled will have no affect.

CIR9			**Interface Configuration Register**			**Default = 00h**
Transfer capture data via DMA or PIO: 0 = DMA 1 = PIO	Transfer playback data via DMA or PIO: 0 = DMA 1 = PIO	Reserved	Autocalibrate: 0 = Disable 1 = Enable (autocalibration after power down/reset or mode change	DMA channel mode:(1) 0 = Dual 1 = Single	Capture data in format selected:(2) 0 = Disable 1 = Enable	Playback data in format selected:(3) 0 = Disable 1 = Enable

(1) In Sound Blaster mode, bit 2 is set when playback or capture DMA starts and is reset when DMA ends.

(2) The codec generates CDRQ and responds to CDAK# when bit 1 = 1 and bit 7 = 0. If bit 7 = 1, bit 1 enables PIO capture mode.

(3) The codec generates PDRQ and repents to PDAK# when bit 0 = 1 and bit 6 = 0. If bit 6 = 1, bit 1 enables PIO playback mode

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR10			**Pin Control Register**				**Default = 00h**
Reserved						Interrupt pin:(1) 0 = Disable 1 = Enable (Interrupt pin goes active high when the number of samples programmed in the Base Count Register is reached.)	Reserved
2. In Sound Blaster mode, the software driver should set bit 1 = 1.							
CIR11			**Error Status and Initialization Register (RO)**				**Default = 00h**
Capture overrun:(1) This bit is set when capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample is ignored.	Playback underrun:(1) This bit is set when playback data has not arrived from the host in time to be played. This results in a midscale value sent to the DACs.	Autocalibration state: 0 = In progress 1 = Not in progress	Current status of PDRQ and CDRQ: 0 = Inactive (low) 1 = Active (high)	Indicates under/over range on right input channel:(1) 0 = Less than –1dB under range 1 = Between –1dB and 0dB under range 2 = Between 0dB and +1dB over range 3 = Greater than +1dB over range		Indicates under/over range on left input channel:(1) 0 = Less than –1dB under range 1 = Between –1dB and 0dB under range 2 = Between 0dB and +1dB over range 3 = Greater than +1dB over range	
(1) Bit changes on a sample-by-sample basis. (2) The occurrence of a capture overrun and/or playback underrun is designated in the Status Register's sample overrun/underrun bit (WSBase+06h[4]). The sample overrun/underrun bit is the logical OR of bits 7 and 6. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.							
CIR12			**ID Register**				**Default = 0Ah**
Reserved						Revision ID (RO): These bits define the revision level of the codec.	
CIR13			**Reserved**				**Default = 00h**
CIR14			**Playback Upper Base Count Register**				**Default = 00h**
Upper Base Count: This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written The current count contained in the counters can not be read. When enabled for SB Mode, this register is used for both the Playback and Capture Base Registers.							

Table 5-10 Codec Indirect Registers (cont.)

D7	D6	D5	D4	D3	D2	D1	D0
CIR15			**Playback Lower Base Count Register**				**Default = 00h**
Lower Base Count: This byte is the lower byte of the base count register containing the eight least significant bits of the 16-bit base register. Reads from this register return the same value which was written The current count contained in the counters can not be read. When enabled for SD Mode, this register is used for both the Playback and Capture Base Registers.							

Table 5-11 Expanded Mode CIR

7	6	5	4	3	2	1	0
CIR16			**AUXL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR17			**AUXR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXR (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR18			**LINEL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINEL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR19			**LINER Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINER inputs (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR20			**MICL Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	MICR mixed into OUTL: 0 = Disable 1 = Enable	Reserved	Gain select for MICL (dB): Refer to CIR2[4:1] for decode.				Reserved
CIR21			**MICR Input Control Register**				**Default = 88h**
Mute: 0 = Disable 1 = Enable	MICL mixed into OUTR: 0 = Disable 1 = Enable	Reserved	Gain select for MICR (dB): Refer to CIR2[4:1] for decode.				Reserved

Table 5-11 Expanded Mode CIR (cont.)

7	6	5	4	3	2	1	0
CIR22			**OUTL Output Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTL (dB): 00000 = 0 00001 = –3 00010 = –6 00011 = –9 00100 = –12 00101 = –15 00110 = –18 00111 = –21		01000 = –24 01001 = –27 01010 = –30 01011 = –33 01100 = –36 01101 = –39 01110 = –42 01111 = –45	10000 = –48 10001 = –51 10010 = –54 10011 = –57 10100 = –60 10101 = –63 10110 = –66 10111 = –69	11000 = –72 11001 = –75 11010 = –78 11011 = –81 11100 = –84 11101 = –87 11110 = –90 11111 = –93	Reserved
CIR23			**OUTR Output Control Register**				**Default = 80h**
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTR (dB): Refer to CIR22[5:1] for decode.					Reserved
CIR24-CIR27			**Reserved**				**Default = 00h**
CIR28			**Capture Data Format**				**Default = 00h**
Audio data format - linear PCM or companded for all input and output data (used in conjunction with bit 5):(1) 000 = Linear, 8-bit unsigned 001 = µ-law, 8-bit companded 010 = Linear, 16-bit two's complement, Little Endian 011 = A-Law, 8-bit companded 100 = Reserved 101 = ADPCM, 4-bit, IMA compatible 110 = Linear, 16-bit two's complement, Big Endian 111 = Reserved **Note:** Bit 7 is not available in Mode 1 (forced to 0).		Stereo/mono:(2) 0 = Mono 1 = Stereo		Reserved			
(1) SB/WSS mode switch: In Sound Blaster mode, the software driver should set CDF to 8 bit PCM mode (R8: FM1,FM-,C_L). (2) Selecting stereo results with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel. **Note:** The contents of this register can only be changed if the mode change bit (WSBase+04h[6]) is enabled (set to 1). Writes to this register without the mode change bit enabled will have no affect.							
CIR29			**Reserved**				**Default = 00h**
CIR30			**Capture Upper Base Count**				**Default = 00h**
Upper Base Count: This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written.							
CIR31			**Capture Lower Base Count**				**Default = 00h**
Upper Base Count: This byte is the lower byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written.							

6.0 Electrical Specifications

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	4.5	5.5	V
AVCC	Analog Supply Voltage	4.75	5.25	V
VIN	Input Voltage	–0.5	VCC + 0.5	
VOUT	Output Voltage	–0.5	VCC + 0.5	V
TOP	Operating Temperature	0	70	°C
TSTG	Storage Temperature	–40	125	°C
ESD*	ESD Tolerance (Human Body Model MIL883C, 3015.7, Notice 8)		1000	V

* ESD senstive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the 82C931 features ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Low Level Input Voltage	–0.3	0.8	V	VCC = 5.5V
VIH	High Level Input Voltage	2.4	VCC + 0.3	V	VCC = 4.5V
VIHa	High Level Input Voltage for RESET	3.5	VCC + 0.3	V	VCC = 4.5V
VOL	Low Level Output Voltage		0.2	V	IOL = 4mA, VCC = 4.5
VOH	High Level Output Voltage	VCC – 0.5	5.5	V	IOH = –4mA VCC = 5.5V
IIL	Input Leakage Current		10	µA	VCC = 5.5V
IILa	Input Leakage Current with 5K ohm Pull-up Resistor	–100	–500	µA	VIN = 0V
IILb	Input Leakage Current with 50K ohm Pull-up Resistor	–10	–50	µA	VIN = 0V
IOL	Output Leakage Current		10	µA	VCC = 5.5V
IPD	Static or Power-down Mode Current		300	µA	VCC = 5.5V

6.3 General Specifications: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
IIL	Low Level Input Current	–10		10	µA	VIN = GND
IIH	High Level Input Current	–10		10	µA	VIN = VCC
IOZ	Tristate Output Leakage Current	–10		10	µA	VOUT = 0/VCC
V-	Schmitt Negative Threshold	0.8 1.5		1.3 2.5	V	TTL-STATIC CMOS-STATIC
V+	Schmitt Positive Threshold	1.4 2.5		2.1 3.5	V	TTL-STATIC CMOS-STATIC
VH	Schmitt Hysteresis		0.6 1.0		V	TTL-STATIC CMOS-STATIC
VIL	low Level Input Voltage			0.8	V	TTL-STATIC
VIH	High Level Input Voltage	2.0			V	TTL-STATIC
VOL	Low Level Output Voltage			0.4	V	TTL-STATIC
VOH	High Level Output Voltage	2.4			V	TTL-STATIC
RPD	Pull-down Resistance	50		200	KΩ	VIN = VCC
RPU	Pull-up Resistance	50		200	KΩ	VIN = VCC
CIN	Input Capacitance			5	pF	Frequency = 1MHz @ 0V
COUT	Output Capacitance			5	pF	Frequency = 1MHz @ 0V
CIO	Bidirectional Capacitance			5	pF	Frequency = 1MHz @ 0V
IOS	Short Circuit Output Current		2	25	mA	VOUT = 0V
IKLU	I/O Latch-Up Current	100			mA	V < GND, V > VCC
VESD	Electrostatic Protection	2000			V	C = 100pF, R = 1.5KΩ

6.4 Pin Specifications - Analog (VCC = 5.0V, 25°C)

Pin Name	Parameter	Min	Typ	Max	Unit	Condition
Inputs						
MICR, MICL, LINER, LINEL, CDR, CDL, AUXR, AUXL, CINR, CINL	Signal Bandwidth Input Range	10 0.5		20K 3.0	Hz V	Sine Wave
Outputs						
OUTR, OUTL	Signal Bandwidth Output Range	10 0.5		20K 3.0	Hz V	Sine Wave Load = 10KΩ, 25pF
MIXOUTR, MIXOUTL	Signal Bandwidth Output Range	10		20K	Hz	Sine Wave
VREF1 VREF2			1.75 1.85		V	DC DC

6.5 Volume Setting

Parameter	Min	Typ	Max	Unit	Test Conditions
Input Gain/Atten. Range: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 –33 0 –93 –46.5		 12 22.5 0 0	dB	Input @ 1Hz, 2.5Vpp wrt ACOM
Step Size: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 2.6 1.3 2.6 2.0 1.3	 3.0 1.5 3.0 3.0 1.5	 3.4 1.7 3.4 4.0 1.7	dB	 90 to -81dB) (-84 to -93dB)
Mute Level		–80		dB	
Signal to Noise Ratio		–80		dB	
Total Harmonic Distortion		0.04		%	
Total Dynamic Range		80		dB	
Interchannel Isolation		60		dB	
Interchannel Gain Mismatch	–0.5		0.5	dB	
Gain Drift		100		ppm/°C	

6.6 Analog Characteristics

Test conditions
Temp=25 °C, VDD, VCC=+5v, Input signal= 1kHz sine wave, Analog output passband: 20 Hz to 20kHz, Sample freq = 44.1 kHz

DAC test conditions
16-bit linear mode, Full Scale input, 10 kΩ output load, measured at Line Out.

ADC test conditions
16-bit linear mode, 0 dB Gain, Line Input.

6.6.1 Analog Inputs

Parameters	Min	Typ	Max	Units
Input voltage LINE/CD/AUX/CIN	2.6	2.8	3.1	Vp-p
MIC with 0dB gain	2.6	2.8	3.1	Vp-p
MIC with 20dB gain	0.26	0.28	0.31	Vp-p
Input impedance	10	20		kΩ
Input capacitance			15	pF

6.6.2 Analog Outputs (10kΩ, 25pF)

Parameters	Min	Typ	Max	Units
Full-scale output voltage (OUTR & OUTL)	2.5	2.8	3.1	Vp-p
Vref		1.85		Volts
Output impedance			600	W
External load impedance	10			kΩ

6.6.3 Volume Settings

Parameter	Min	Typ	Max	Units
Master volume step size	1.3	1.5	1.7	dB
Master volume output atten range		46.5		dB
Mute level		80		dB

6.6.4 Analog-to-Digital Converters

Parameters	Min	Typ	Max	Units
Resolution		16		bits
Total dynamic range	75	85		dB
THD			.025	
Interchannel isolation: Line to Line/CD/Aux/Mic		80		dB
Interchannel gain mismatch	-0.5		+0.5	dB
Gain drift		100		ppm/°C

6.6.5 Digital-to-Analog Converters

Parameters	Min	Typ	Max	Units
Resolution		16		bits
Total dynamic range	78	95		dB
THD			.022	
Interchannel isolation:		80		dB
Interchannel gain mismatch	-0.5		+0.5	dB
Gain drift		100		ppm/°C

6.7 AC Timings

Symbol	Parameter	Min	Max	Unit	Condition
ISA Bus					
tOSCP	OSC (14.318MHz) Frequency	14.0	14.5	MHz	
tOSCH	OSC High Width	32	40	ns	
tOSCL	OSC Low Width	32	40	ns	
tSCKP	SYSCLK Frequency	8	9	MHz	
tSCKH	SYSCLK High Width	50	70	ns	
tSCKL	SYSCLK Low Width	55	70	ns	
tRST	RESET to RESET#	40	80	ns	
tCMDW	IOR#/IOW# Command Width	120		ns	
tWDSU	Write Data Setup to IOW# Rising	30		ns	
tWDHD	Write Data Hold from IOW# Rising	15		ns	
tRAC	Read Access Time	20	50	ns	

Symbol	Parameter	Min	Max	Unit	Condition
tASU	Address Setup to IOR#/IOW# Falling	50		ns	
tAHD	Address Hold from IOR#/IOW# Rising	30		ns	
tDKSU	DACK# Setup to IOR#/IOW# Falling	40		ns	
tDKHD	DACK# Hold from IOR#/IOW# Rising	160		ns	
tDHR	SD Hold from IOR# Rising	0	20	ns	
tDRHD	DRQ Hold from IOR#/IOW# Falling	0	25	ns	
CD-ROM					
tCA	SA to CA Delay	3	20	ns	
tXCS	SA to IDECS1#/3#	5	20	ns	
tCMDD	IOR#/IOW# to XIOR#/XIOW# Delay	3	20	ns	

Figure 6-1 RESET and CLK Timing Waveform

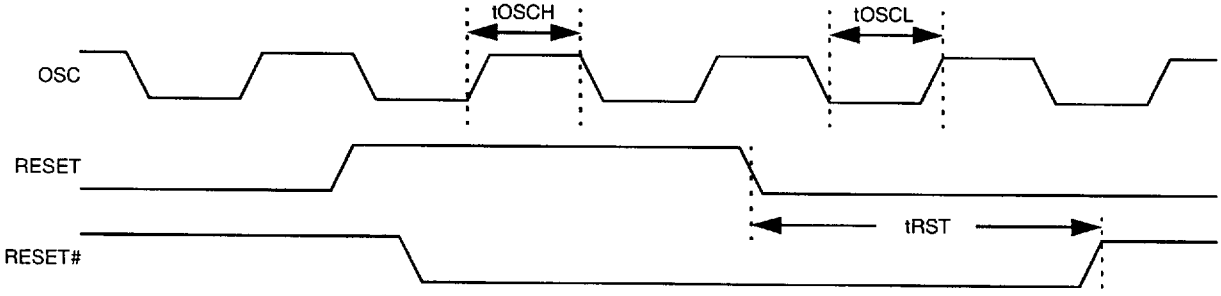
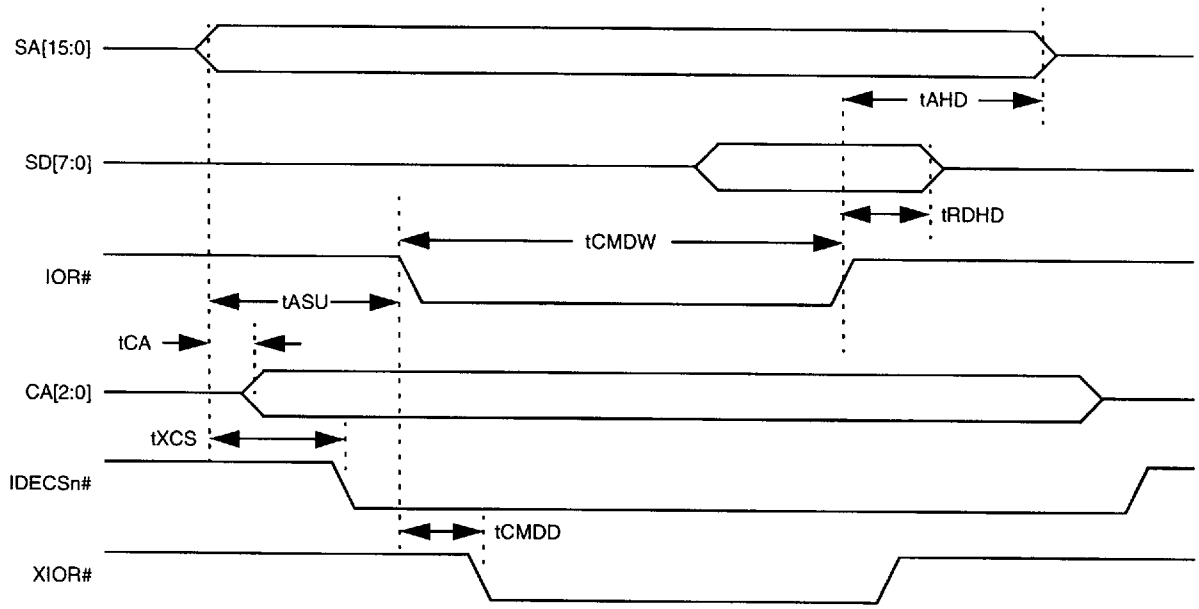
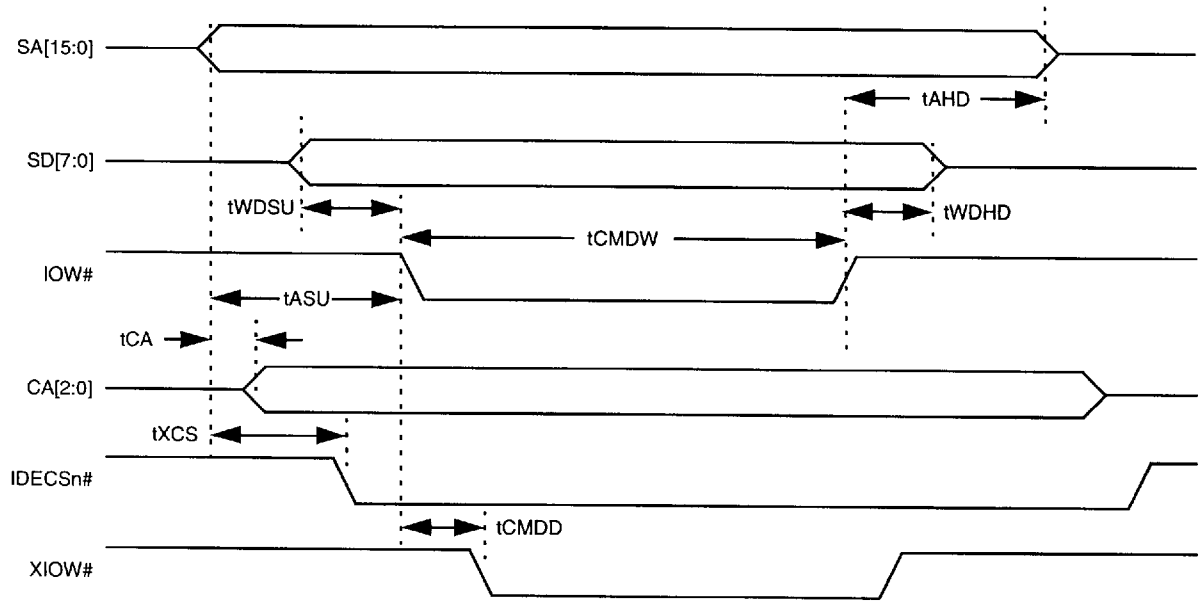


Figure 6-2 CD-ROM I/O Read Cycle



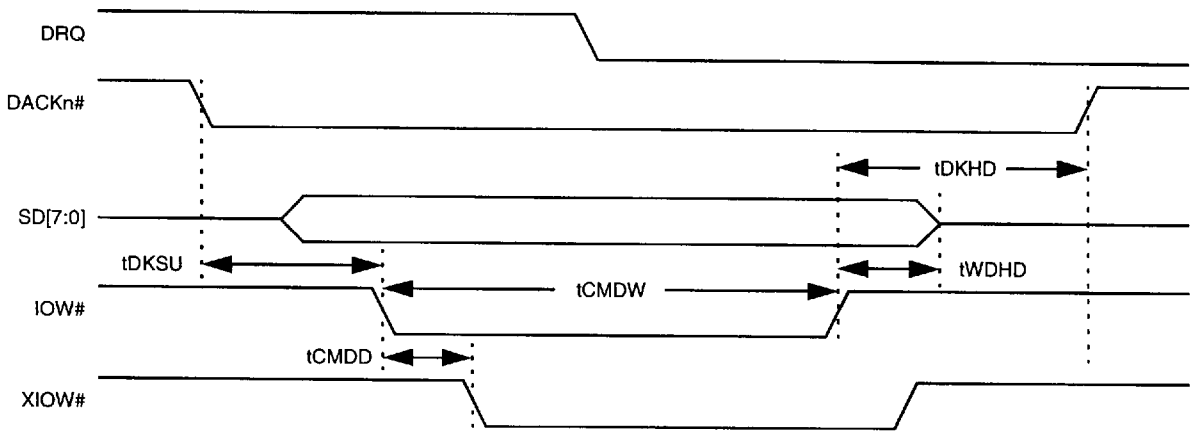
Note: For the above timing, AEN = 0, DRQ = 0, and DACKn# = 1.

Figure 6-3 CD-ROM I/O Write Cycle



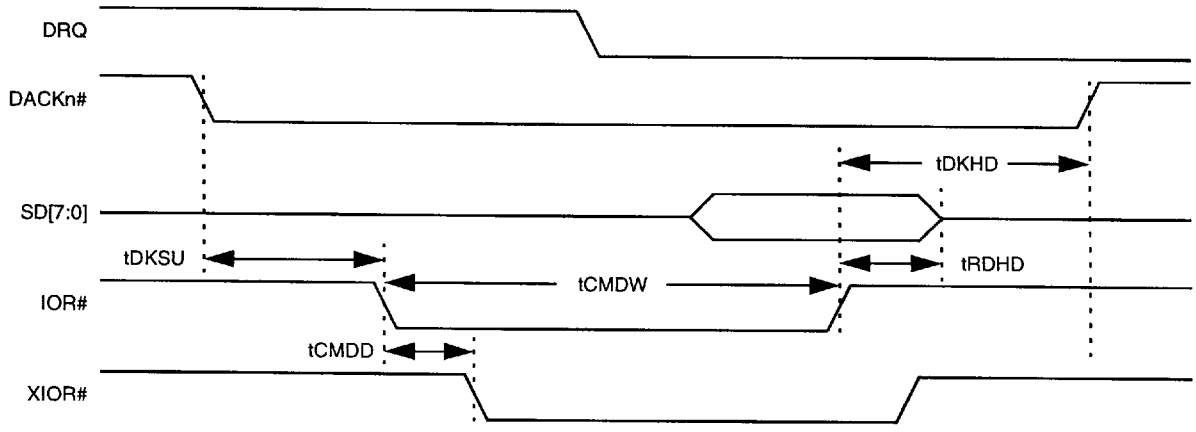
Note: For the above timing, AEN = 0, DRQ = 0, and DACKn# = 1.

Figure 6-4 DMA Write/Playback Cycle



Note: For the above timing, AEN = 1.

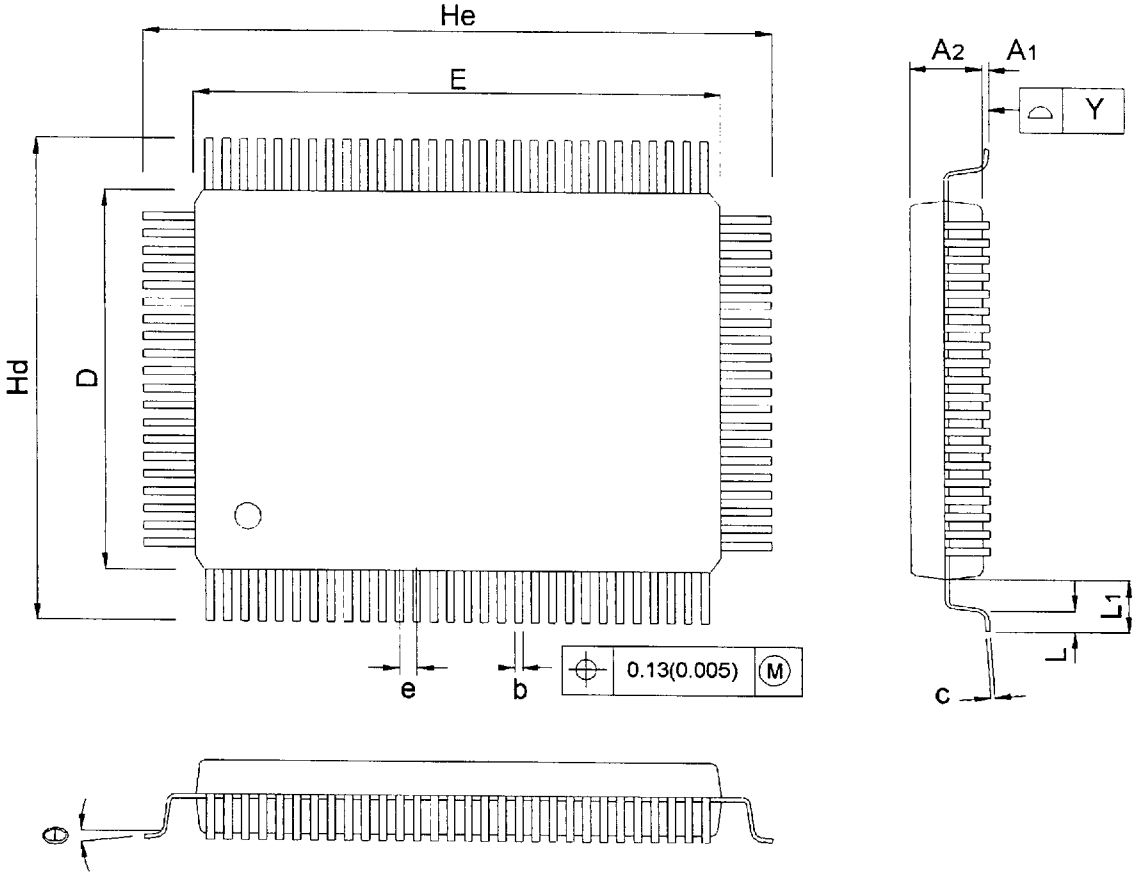
Figure 6-5 DMA Read/Capture Cycle



Note: For the above timing, AEN = 1.

7.0 Mechanical Packages

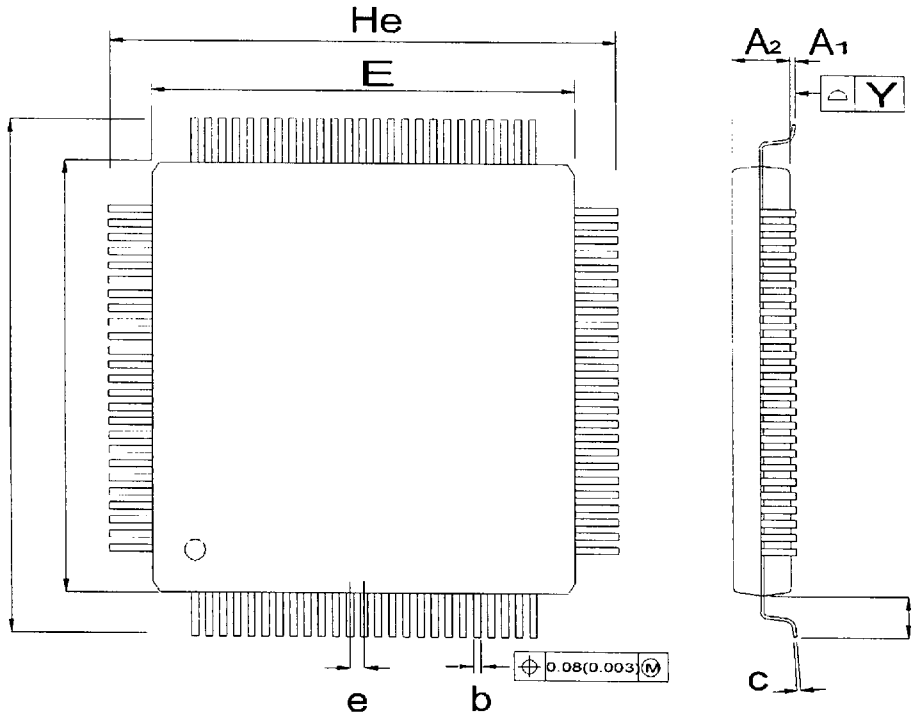
Figure 7-1 100-pin PQFP, Plastic Quad Flat Pack

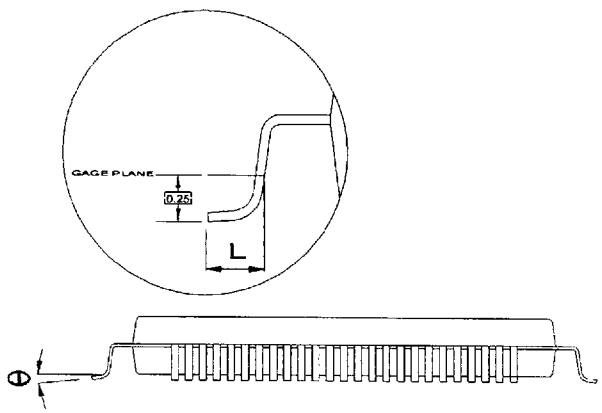


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.25	0.35	0.45	0.010	0.014	0.018
A2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e		0.65			0.026	
Hd	17.00	17.20	17.40	0.669	0.677	0.685
He	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.60			0.063	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.: AS100PQFP-001
Dwg. Rev.: A0 Unit: MM / INCH

Figure 7-2 100-pin TQFP, Thin Quad Flat Package





SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
e		0.50			0.020	
Hd	15.90	16.00	16.10	0.626	0.630	0.634
He	15.90	16.00	16.10	0.626	0.630	0.634
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.:	AS100TQFP-001	
Dwg. Rev.:	A0	Unit: MM / INCH

Note: Pinout for TQFP package is identical to pinout of PQFP package.