Headland
Technology

HTK320
386DX Chip Set

IT-49-17-15

Features

- 2-chip 80386DX PC/AT compatible solution
- Supports CPU speeds of up to 40MHz
- 3167 Weitek and 80387 co-processor supported
- Peripherals supported on local CPU bus
- Port 92 functions
- Posted backplane memory cycles

Cache

- Direct mapped or 2-way set associative cache sizes of 32K, 64K and 128K
- Internal tag RAMs
- Zero wait-state write hits
- Line burst capability from DRAM to cache

Write Buffer

- 4 deep, 32-bit wide write buffers
- Byte gathering
- Full or partial write buffer hit support
- Out of order operation

Memory

- 4-bank DRAM support
- 256K, 1M, 4M, 16M support (up to 256Mb)
- Mix and match memory types
- 2/4-way or disabled interleaving and fast paging
- CAS before RAS, or RAS only Refresh
- EMS 4.0 support
- Single BIOS ROM support
- System and Video BIOS in single ROM

Description

The HTK320 chip set is a 2-chip, high-performance, cost-effective solution for the 80386DX microprocessor. In its minimum configuration, this highly integrated chip set requires only four external TTL devices to implement a fully compatible IBM PC/AT system at speeds up to 40 MHz.

The HTK320 is based on Headland's Bus Architecture and consists of the HT321--ISA Controller and the HT322--Memory Control Unit (MCU) packaged in two 184-pin plastic quad flat packs. Among its features are an on-chip cache controller and internal tag RAM.

Unlike other 3rd generation chip sets that have integral Cache Controllers, the HTK320 integrates the high-speed tag RAM into the chip set to enhance performance and significantly reduce component count and manufacturing cost. The direct mapped or 2-way set associative cache design supports external cache sizes of 32K, 64K, and 128K.

The HTK320 can support Peripheral Devices such as VGA or SCSI controllers on the local processor bus, or any 3rd party device that is designed to work within the '386DX Bus Protocol and Timing. By eliminating the ISA backplane bottleneck, system designers can greatly improve the performance of functions such as graphics generation and disk access.

The HTK320 incorporates a 4-level deep Write Buffer and performs byte gathering into 32 bit accesses to the DRAM. This facilitates real zero wait state writes and, when coupled with the 2-way set associative cache, provides enhanced memory performance.

The HTK320 supports up to 4 banks of DRAM, configurable as 1-4 Banks. This flexible memory architecture allows for any memory type, from 256Kb to 16Mb devices, in any bank. Maximum system performance is achieved from the DRAM banks through various means, including interleave of Memory Bank and/or Page, and CAS before RAS refresh. The memory may also be tuned to its maximum potential through the use of extensive DRAM timing Control Registers, controls include, Precharge time, Access time on Reads, Active time on Writes, as well as CAS and RAS delays. In addition, further system performance is gained by separate timing parameters on the read and write cycles which allow system designers to take maximum advantage of the pipelined structure of the chip set.

The HTK320 also supports extensive mapping registers, which allow system designers to take maximum advantage of system memory. The chip set supports EMS LIM 4.0, allows for mixed Shadow/Remap in 16K blocks between the 640K and 1M boundaries, and eliminates the requirement for external decoding logic by support of 27 Programmable Non-cache regions. With the extensive HTK320 mapping capability, it is feasible to seamlessly place 3rd party devices on the local bus without the need for external TTL support. The HTK320 Mapping structure provides for a single 8-bit EPROM to be used for both the System and Video BIOS, further reducing the system chip count and cost.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT321 Functional Description

This section provides the functional description of the HT321 within the HTK320 Chip Set environment. The main duty of the HT321 is to interface the 8-MHz ISA backplane with the high speed Local Bus. The HT321 provides all the functional blocks necessary for AT Compatible backplane timing, Address/Data Buffering and Latching, as well as circuit equivalents of two Intel 8237's in cascade mode, two 8259's in cascade mode, and an 8254. The HT321 is designed for '386-DX systems that operate between 25 and 40MHz.

In the chip set architecture, the HT321 is the default device for CPU generated cycles, meaning that if no other LOCAL BUS device responds to the current cycle, then the HT321 will be selected to respond and terminate the cycle. The HLOCAL* input provides the information necessary for the HT321 to determine whether or not to respond to the current cycle. Alternatively, if a Local Device cannot support the "HLOCAL*" feature, the HT321 can be programmed for a "decode hole" within its I/O and/or MEMORY map so that when any address matches the Programmed Hole, the HT321 will ignore the cycle allowing another device to respond. Up to two I/O and/or MEMORY holes may be programmed within the HT321 at any given time.

The HT321 becomes the Master Device in the System during DMA cycles, whereby the HT321 will generate all the address and control information necessary for the local bus, just as the CPU does for regular cycles. During DMA cycles,as Master the HT321 provides cycle information to both the LOCAL BUS and the Backplane. If a Local Bus Device does not respond to this cycle then the HT321 will assume the DMA cycle is for a backplane device and adjust accordingly.

Outlined below are the major features of the HT321:

184 PQFP package.

Up to 40 MHz operation.

Fully AT-compatible 8 MHz ISA bus interface.

Posted backplane memory writes.
Interfaces to 8 or 16-bit ROM's.

Ability to map video BIOS into same physical device as system BIOS.

Internal DMA Page Registers and Extended DMA Page Registers.

Port_92 functionality.

Uses 1 micron technology.

Local bus architecture compatible.

Performs all ISA bus address and data buffering.

Built-in Intel equivalents for:
- **i) 8237 DMA controllers.**
- **ii) 8259 PIC's (interrupt controllers).**
- **iii) 8254 PIT (timer).**

Chip-select outputs for Real Time Clock and Keyboard interfacing.

Within the HT321 there are seven (7) major functional blocks (see Figure 2.2). These blocks include:

1. RESETS & CLOCK_GEN
2. LOCAL_BUS INTERFACE
3. ADDRESS BUFFERS & LATCHES
4. DATA BUFFERS & LATCHES
5. ISA BACKPLANE CONTROLLER
6. I/O DECODE & CONFIGURATION MODULE
7. MEGAFUNCTIONS

Powered by ICminer.com Electronic-Library Service CopyRight 2003

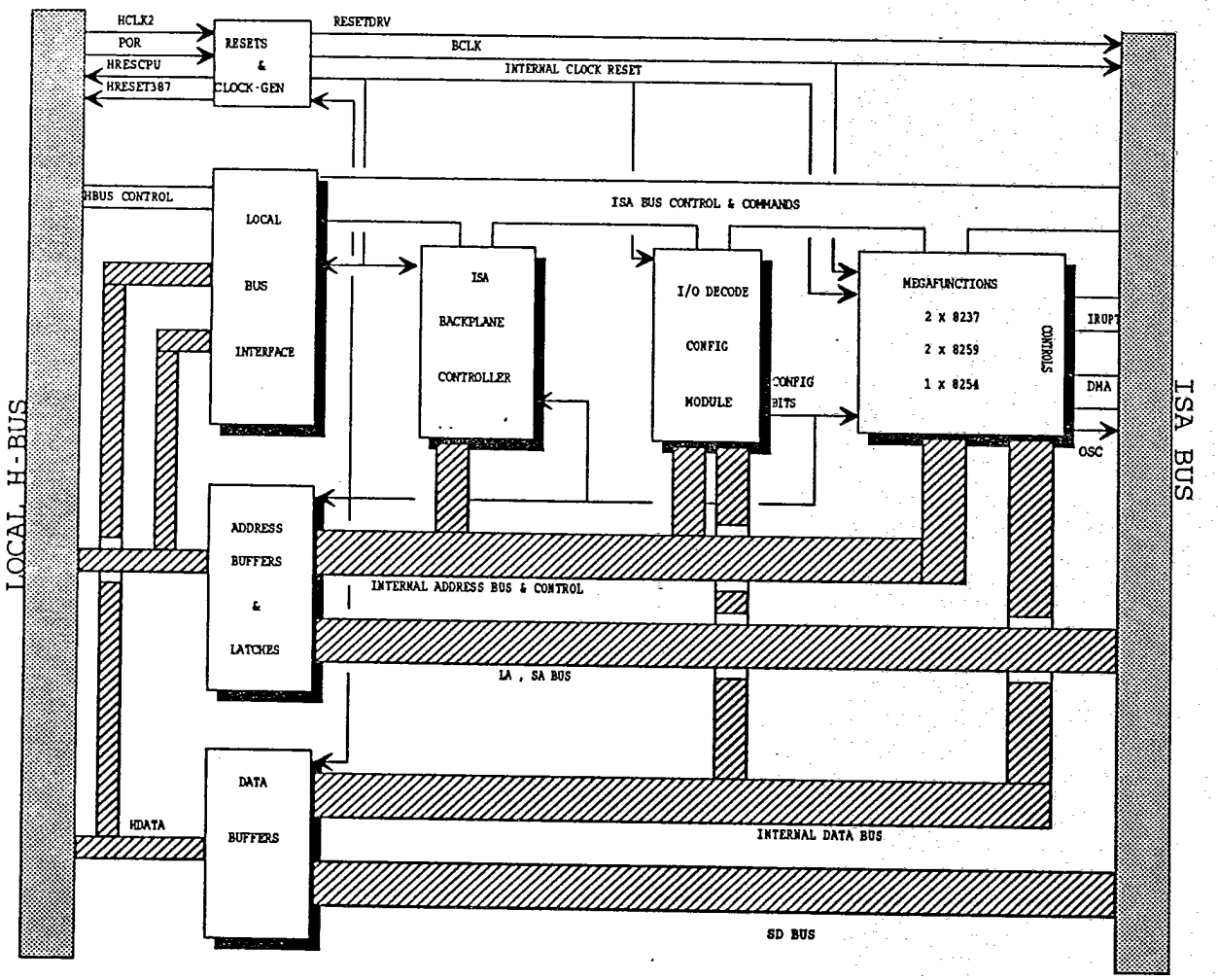


Figure 2.2 - ISA Controller Internal Block Diagram

Powered by ICminer.com Electronic-Library Service CopyRight 2003

The following is a Functional Description for each of these blocks.

1. RESETS & CLOCK_GEN

This module is responsible for generating all the Internal or External Resets and Backplane Clocks required by the HT321. The output signal pins directly affected by this module include BCLK (P68), HRESCPU (P170), RESET387 (P51) and RESET-DRV (P76).

CLOCK_GEN:

The main incoming reference clock signal is HCLK2 which is used to derive BCLK and INTERNAL_CLK. INTERNAL_CLK is just a buffered version of the HCLK2 signal and is used to clock all the internal state machines of the HT321, whereas BCLK is produced by division of the HCLK2 signal by Programmable Ratios of 6, 8, 10, or 12. This Divide Ratio is selected via INDEX 01 of the HT321 where the system bus speed can be programmed to produce a 50% duty cycle 8.0 - 8.33 MHz BCLK signal which is then available to the ISA Backplane. Figure 2.3 shows the timing relationships between HCLK2 and BCLK for different settings of INDEX 01. The BCLK signal is further made available to clock the internal cascaded Intel 8237 DMA Controller equivalents. The user has the choice of supplying the internal 8237's with the 8 MHz BCLK signal directly or dividing this BCLK signal in half to supply the AT standard 4MHz clock to the 8237 DMA functions: Frequency selection for the 8237 clock is programmed via INDEX 06 of the HT321.

The AT Backplane signal, OSC, which is a 14.318 MHz Color Burst Frequency is used within this module to produce the Internal Clock of the Intel equivalent 8254 Timer function. This clock is simply the OSC input divided by 12 to produce the required 1.19MHz clock signal.

RESETS:

POR is the main reset signal input. It indicates either a POWER-ON or HARD RESET situation. Once this signal goes active (high), all internal circuits are reset to their initial default state and the HRESCPU, RESET387 and RESETDRV signals are asserted to Initialize all external system devices.

HRESCPU is the reset required by the 386-DX processor (CLREXPTION) to reset to its initial state. This signal is produced Synchronously using HCLK2 input and Sets the Phasing Information for the entire system by synchronizing the HRESCPU falling edge with the proper edge of the HCLK2 signal. Figure 2.4 shows the basic timing relationship between HCLK2 and HRESCPU. See the AC Timing Specifications Section for detailed timing of this signal. HRESCPU will also be generated for a keyboard initiated reset sequence via the RC(P77) input or the PORT_92 FAST_RC programmable function.

RESET387 is the signal required to initialize the optional system Co-processor. The timing of this signal is identical to the HRESCPU and is only generated as a result of POR or by an I/O write cycle to 0F1H. An I/O write to 0F1H,which produces a RESET387 pulse,defaults to Enabled at Power-on . However, it can be blocked by programming INDEX 04 of the HT321.

RESETDRV is the ISA Backplane reset signal. This Reset signal is Synchronized to the BCLK clock and is produced only during POR.

Figures 2.4, 2.5, 2.6, 2.7, and 2.8 show the timing relationships between HCLK2 and the Reset signals described.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

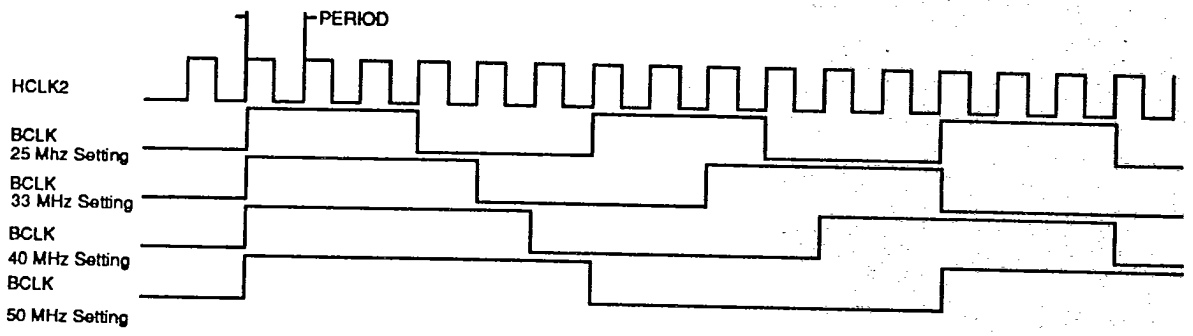


Figure 2.3 - Backplane Clocking (BCLK)

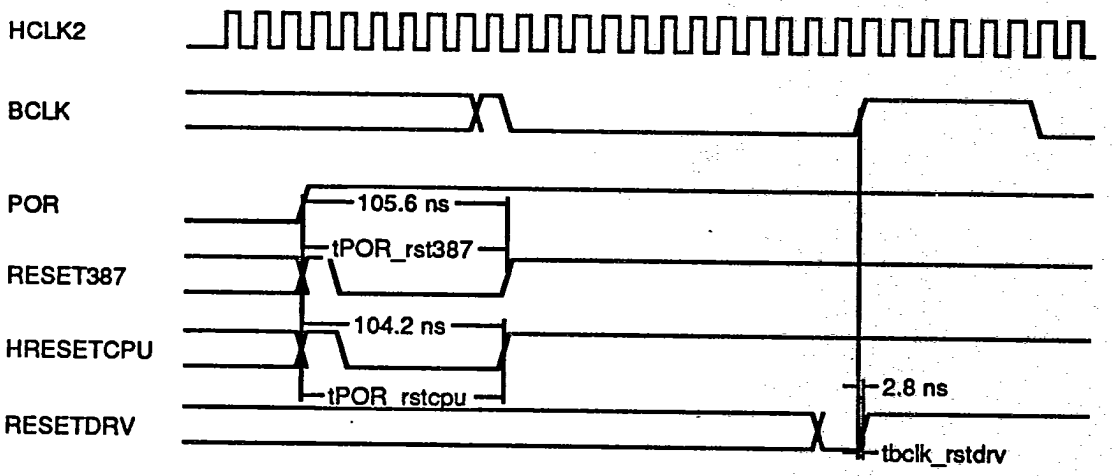


Figure 2.4 - Resets from Initial Power-On

Powered by ICminer.com Electronic-Library Service CopyRight 2003

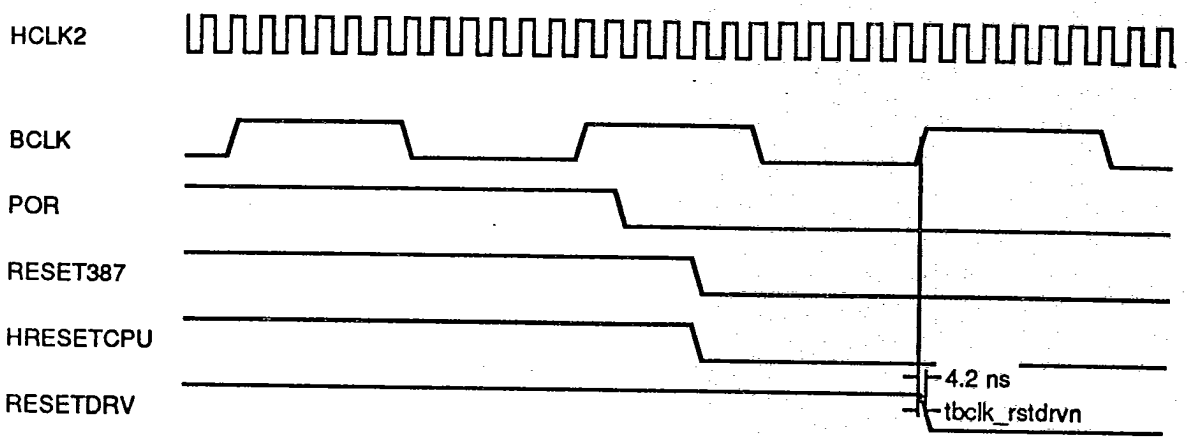


Figure 2.5 - Resets by CLKS at Power Off

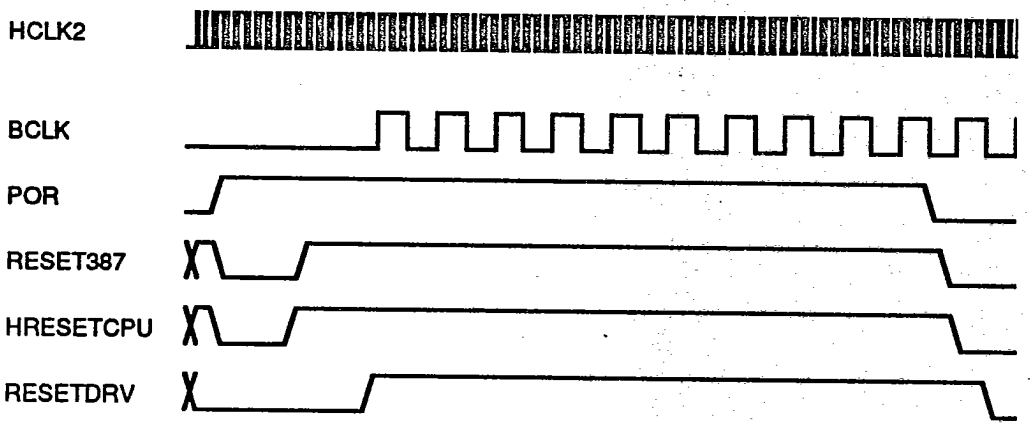


Figure 2.6 - Power On to Off

Powered by ICminer.com Electronic-Library Service CopyRight 2003

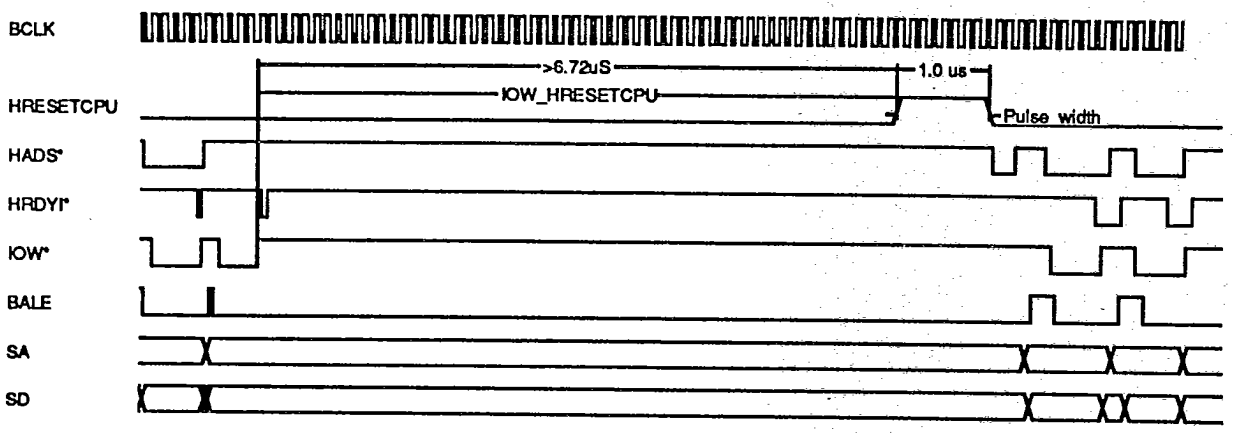


Figure 2.7 - Port 92 Reset Sequence

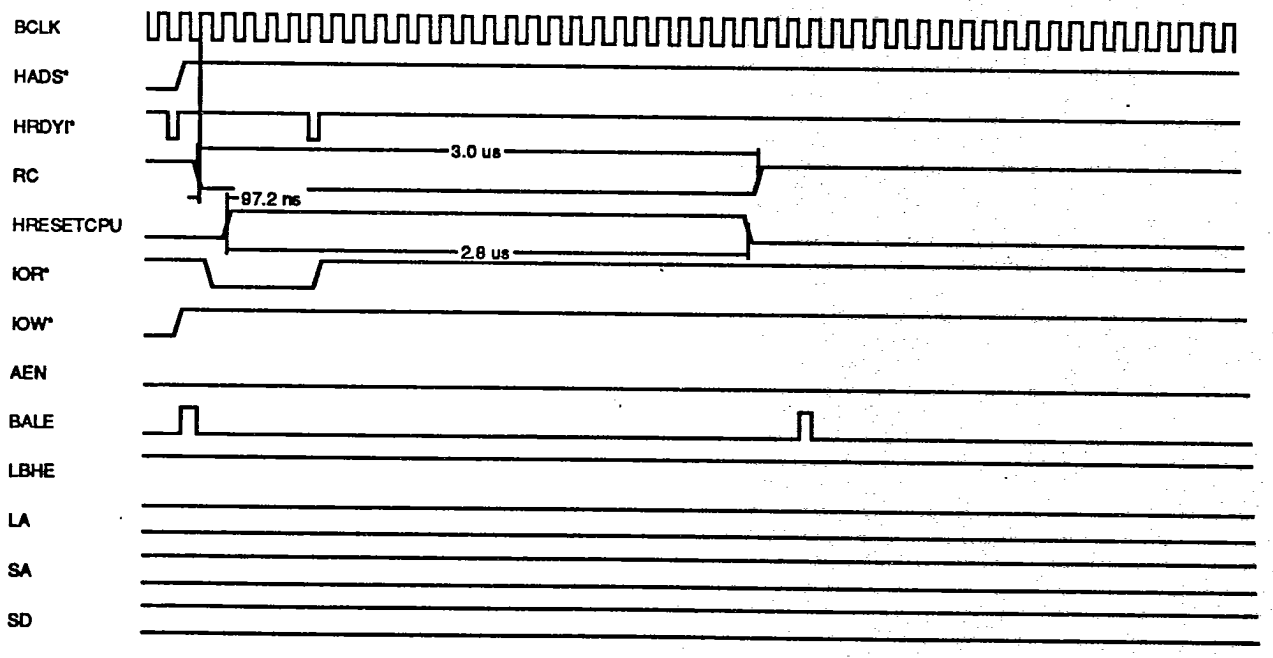


Figure 2.8 - Keyboard Reset Cycle

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2. LOCAL_BUS_INTERFACE

The LOCAL_BUS_INTERFACE module interfaces the HT321 with the Local Bus Control Signals. These signals include HA(P38-25,22-10), HBEN(P40-43), HHLDA(P168), HADSN(P44), HRDYN(P39), HRDYIN(P165), HM_IO(P175), HD_C(P174), HW_R(P173) and HLOCAL*(P167). For CPU initiated transfers, this module must synchronize HTK320 cycles with the ISA Backplane cycles, during DMA transfers this module is responsible for generating all the Bus Control Signals.

The LOCAL_BUS_INT module must monitor the Bus to determine when a HT321 cycle is required. HADS* is the Control Signal in '386-DX system which indicates Start-of-Cycle to all Local Bus devices. Two HCLK2's after HADSN initiates Start-of-Cycle, the HLOCAL* signal is sampled to determine if another Local Device has responded to the cycle. If at this time the HLOCAL* signal is true (low), the HT321 performs no action for the cycle. However, if the HLOCAL* is false (high), the HT321 must respond to the cycle, and the LOCAL_BUS_INTERFACE module will pass the request on to the ISA BACKPLANE CONTROLLER section of the chip. Signals including HA[31, 27:2], HBEN[3:0], HM_IO, HD_C and HW_R are sampled and gated to the rest of the ISA chip. At the conclusion of the ISA cycle, the ISA BACKPLANE CONTROLLER section indicates completion by issuing a READY pulse to the LOCAL_BUS_INTERFACE module. This READY appears on the Local Bus as HRDY* from the HT321. When HRDYI* is returned to the HT321 chip, the real end-of-cycle occurs and the HT321 returns to monitoring the Local Bus for further ISA cycles . Figure 5.4 shows the fundamental timing relationships between HCLK2 and Local Bus signals attached to the HT321. This diagram specifically shows timing for CPU initiated cycles.

For DMA initiated cycles, the '386-DX CPU enters a Hold State in response to the HOLDREQ Signal of the HT321. When the CPU has completed its current tasks and can relinquish the bus, it will assert the HHLDA signal, this is gated to the Cycle Arbiter of the LOCAL_BUS_INTERFACE module. Only when activity is determined complete on the Bus and ISA Backplane Bus is the HHLDA signal gated to the rest of the ISA Chip. For regular DMA cycles, the internal DMA Controller of the ISA Chip will assert the ISA Backplane Command combinations (IOR*/MEMW*, MEMR*/IOW*) which are detected by the LOCAL_BUS_INTERFACE. DMA to/from Local Memory is the only non-MASTER Mode activity supported by the architecture; when a MEMR* or MEMW* Command is detected, the LOCAL_BUS_INTERFACE module asserts an HADS* pulse on the bus, the cycle status information (HM_IO, HD_C, HW_R) is decoded and asserted on the Bus at this time, where it remains valid until the Backplane Commands are de-asserted. HLOCAL* is sampled two HCLK2's after HADS* to determine if the cycle initiated is for a Local Bus device. In this manner, all cycles on the Local Bus look identical, whether they are initiated by DMA or '386-DX CPU. Figure 2.9 shows the timing of HT321 initiated cycles during DMA transfers.

For DMA MASTER mode cycles, events follow the sequence described above, but Backplane MASTER mode devices may have access to I/O as well as Memory locations on the Local Bus. Therefore, during MASTER mode Cycles, when any Backplane command is detected by the LOCAL_BUS_INTERFACE module, an HADS* pulse will be generated for the Bus(Reference HT321 Index 06H). Figure 2.11 shows a MASTER Mode Memory Write Cycle to local memory, whereas Figure 2.10 shows the timing relationships for a MASTER Mode Read Cycle from local memory.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

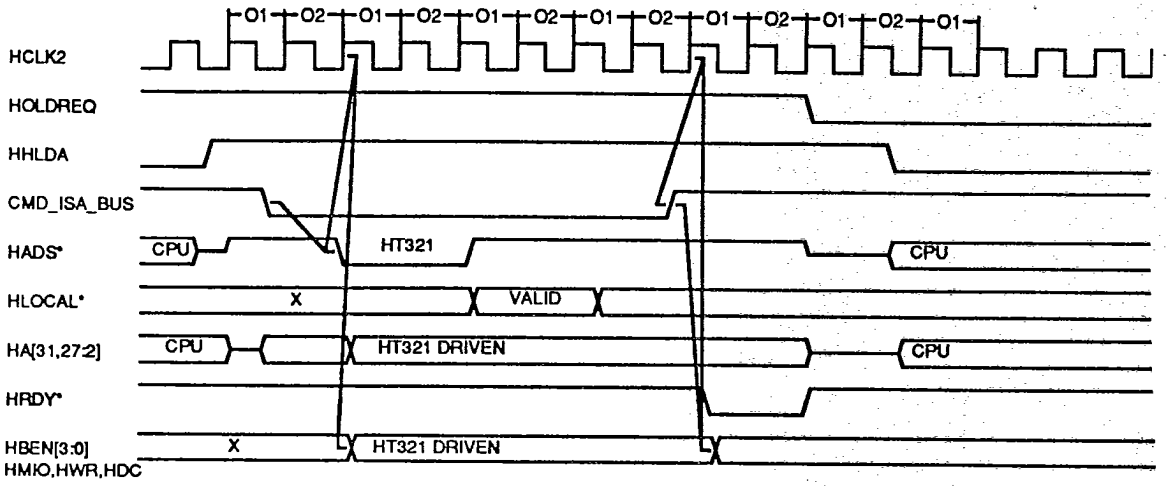


Figure 2.9 - DMA Cycle on the Local Bus

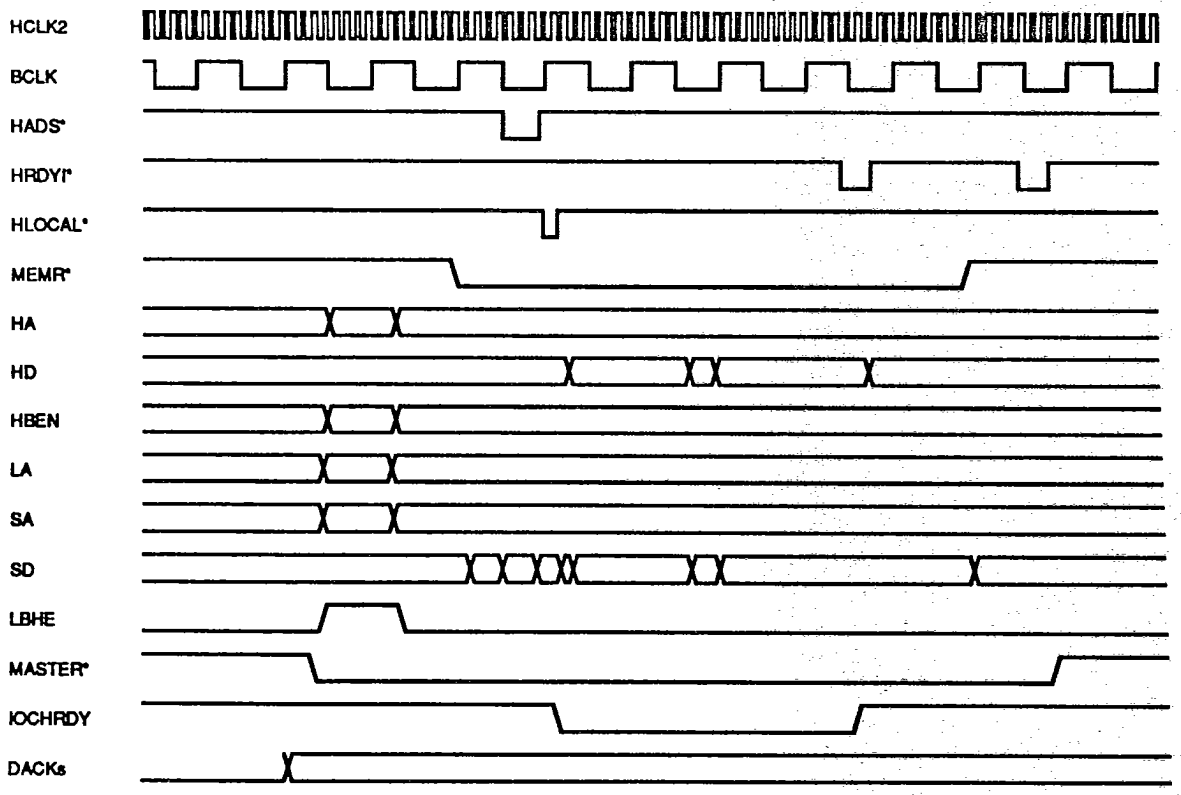


Figure 2.10 - Master Mode Memory Read Cycle to a Local Device

Powered by ICminer.com Electronic-Library Service CopyRight 2003

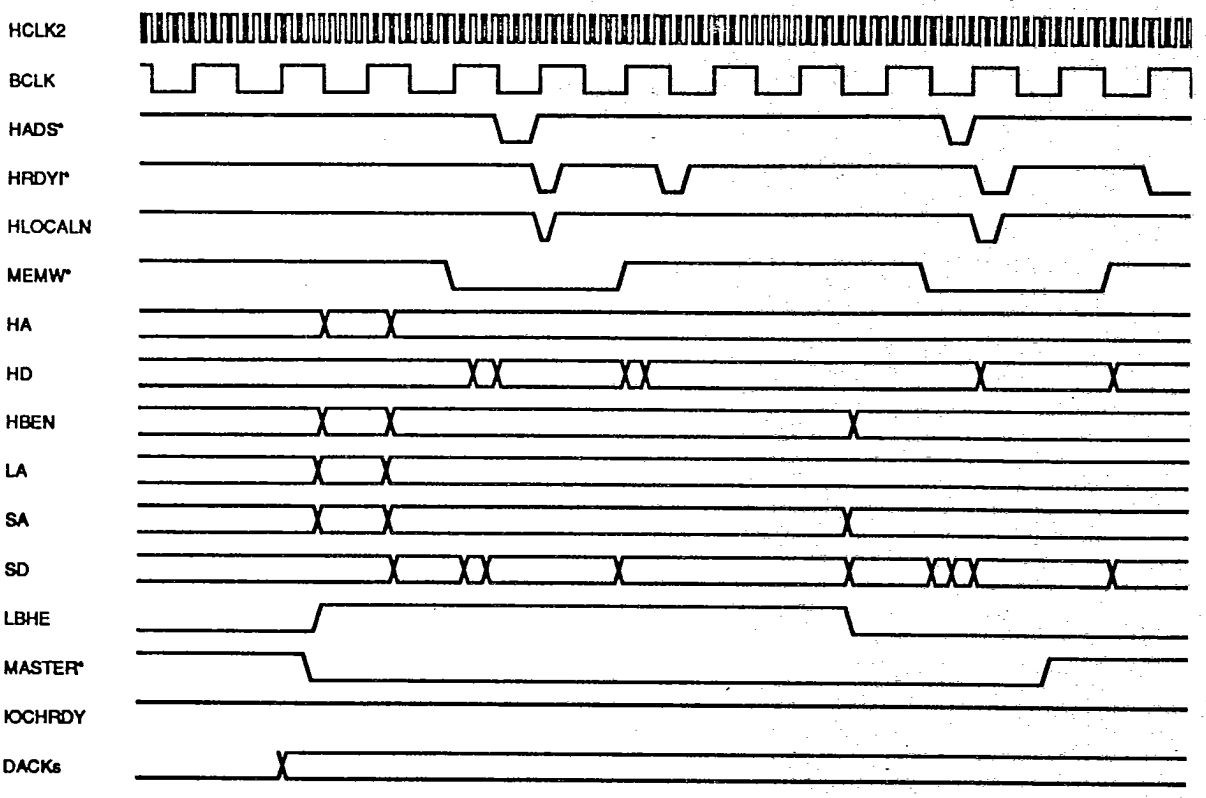


Figure 2.11 - Master Mode Memory Write Cycle to a Local Device

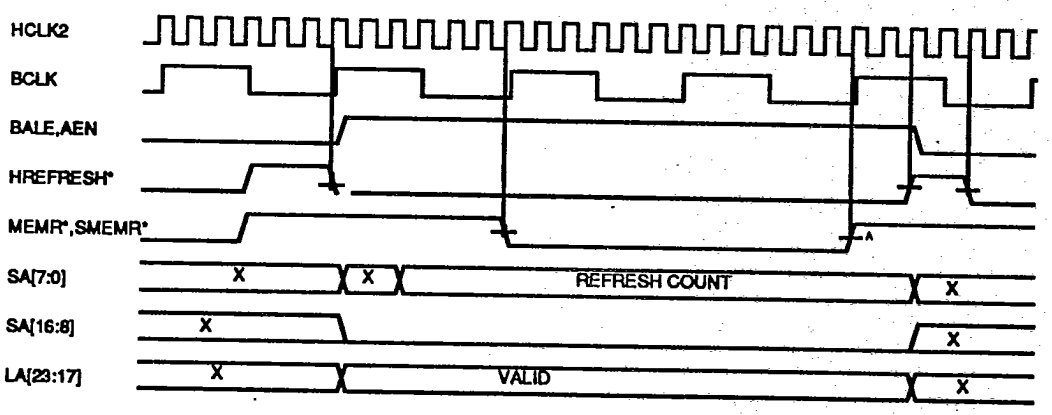


Figure 2.12 - HREFRESH* Timing

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

3. ADDRESS BUFFERS & LATCHES

This module is responsible for providing the necessary ISA Backplane SA[19:0](P136-129,126-117,114-113), LBHEN(P137) and LA[23:17](P112-106) Address Signals during ISA Cycles initiated by the CPU. During DMA cycles, this module will provide the HA [31, 27:2] and HBEN [3:0] Local Bus signals.

For CPU initiated cycles, the SA[19:2] lines are produced from the incoming HA[19:2] signals and gated to the ISA backplane when BALE is true(high). On the falling edge of BALE, ISA Compatible Backplane devices may latch the SA address signals since they are then stable and will remain stable for the entire cycle or until another BALE is generated. Local bus signals HBEN[3:0] generate SA1, SA0 and LBHEN. The significance of these SA address lines depends on the number of bytes requested by the system and whether the target data is located at an odd address. The ISA Backplane LA[23:17] address lines are asserted 2 HCLK2's after HADS* is sampled true, or, during a pipelined cycle, when HADS* and HRDYI* are sampled true by the HT321. These Signals are equivalent to the HA[23:17] input address signals. These LA address lines remain valid until HRDYI* is returned to the HT321 signifying the end of the current cycle.

During REFRESH* cycles, SA[7:0] are driven by the internal refresh counter of the HT321 and contain the Refresh Address. SA[15:8] are asserted to logic 0. SA[19:16] and LA[23:17] significance are controlled by the current programmed value of the Internal DMA PAGE Register at location 8FH. Typically, this register is set to 00 in an AT system. HA address lines are not driven by the HT321 during REFRESH* cycles. The Backplane signal BALE is true(high) for the duration of the cycle. The sequence of a REFRESH* cycle is shown in Figure 2.12.

During DMA cycles, SA[15:0] and LBHEN signals are generated by the Internal Intel 8237 equivalent that has control for the cycle. The significance of SA[19:16] and LA[23:17] signals is controlled by the DMA PAGE register (I/O location 80-8FH) of the acknowledged DMA channel. The value is programmed by application software or BIOS. BALE is always true(high) for the duration of a DMA cycle. A typical DMA transfer cycle, as seen on the ISA Backplane, is shown in Figure 2.28. In this diagram, the DMA clock is set to BCLK/2 (INDEX 06H). A MASTER mode transfer cycle from an ISA Backplane memory device is shown in Figure 2.27. In this case the HLOCALN was not generated by any Local device. Therefore, the whole transfer takes place on the ISA Backplane.

HA[23:2] and HBEN[3:0] lines are asserted by the HT321 during DMA cycles and are the equivalent of the Backplane SA and LA signals. To provide DMA access to the full Local Memory range of a System, Extended DMA PAGE REGISTERS located at I/O address 480-48FH are implemented in the HT321. Use of these registers is controlled via INDEX 06 of the HT321 Registers. When enabled they contain the HA[31:24] Address values required for the Extended DMA transfer. The Extended DMA Page Registers provide for DMA access to/from any location within the system local memory map. The timing of the HA and HBEN signals produced during DMA cycles is equivalent to '386-DX processor timing; that is the addresses are valid when HADSN is generated by the HT321 and remain valid until HRDYIN is returned by the System to terminate the cycle in progress.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

4. DATA BUFFERS & LATCHES

This module is responsible for routing Data to and from the ISA Backplane SD[15:0] and the Local Data Bus HD[15:0]. If Data Bridging is required during the current cycle, this module will provide it. For ISA Backplane requests which require more than one cycle to access the data required by the CPU, temporary storage exists within this module to hold the gathered data until all the data is processed.

The HT321 is limited to a 16 bit transfer of data for any given cycle. To signal this fact to the CPU, BS16* is generated by the HT321 for any CPU cycle requesting data transfer on the upper half of the CPU data bus HD[31:16]. When the BS16* signal is asserted, the '386-DX CPU will automatically adjust and ensure that the data is presented or acquired on the HD[15:0] lines only for the current cycle. Figure 2.14 shows the timing for the generation of the BS16* signal by the HT321 chip. The HT321 has the ability to request pipeline operation from the '386-DX CPU via the HNA* signal. HNA*, however, cannot be asserted for cycles that require BS16*. In this respect, these two signals are mutually exclusive. For any HT321 cycle that BS16* is not required, HNA* will be asserted. Figure 2.15 shows the HNA* timing relationships for cycles when the HT321 asserts the HNA*. During all other conditions the HNA* signal output is left in Tri-state by the HT321.

For CPU initiated WRITE cycles to the ISA Backplane, data is placed on the HD[15:0] inputs of the HT321 and then routed through the chip to the SD[15:0] of the Backplane Bus. For 16-bit devices on the backplane, no Data bridging is required in the HT321 Chip. For 8-Bit ISA Compatible devices, the incoming data is routed automatically to the lower half of the SD bus (SD[7:0]). MEMCS16* and IOCS16* are the backplane signals monitored by the HT321 to determine whether the ISA Backplane device responding is 16- or 8-Bit. For CPU WRITES of 16-bits of data to an 8-Bit Backplane device, the incoming HD[15:0] bus is latched at the start of the first WRITE cycle. A second WRITE cycle is generated by the HT321 to transfer the next 8-bits of data to the Backplane device.

For CPU initiated READ cycles from the ISA Backplane, data is applied to the SD[15:0] Backplane Bus by the responding device and routed through the ISA chip to the HD[15:0] bus so that the '386-DX CPU can acquire the data. The HBEN[1:0] Local Bus signals, generated by the CPU in this case, are used to determine which way to route the backplane data through the HT321. Again, MEMCS16* and IOCS16* are monitored to see what data size will be transferred by the Backplane device. For CPU requests of 16-bits of data from an 8-bit Backplane device, the incoming SD[7:0] bus is latched at the end of the first cycle, and then another cycle is generated by the HT321 to acquire the next 8-bits of data from the Backplane device. During the second cycle of this transfer, both sets of 8-bit data are applied to the HD[15:0] pins to complete the request.

For DMA WRITE and Backplane MASTER mode READ Transfers to/from the Local Bus, the HT321 uses the SA0, SA1 and LBHEN signals to determine the HBEN[3:0] lines. These signals now indicate to the Local Memory device where to expect Valid Data on the HD[15:0] bus. When DMA transfers of data to the upper half of the data bus (HD[31:16]) occur, the HT321 will issue HBEN[3:2] correctly, Local Memory Devices must accept this data on HD[15:0] and bridge the Data to the correct location.

For DMA READ and Backplane MASTER mode WRITE Transfer cycles to/from the Local Bus, the HT321 again asserts the HBEN[3:0] signals but requires a responding Local Memory Device to provide Valid Data only to the HD[15:0] lines.The Memory Device must bridge the data on the HD[15:0] bus as required. No more than two bytes of data will be transferred by the HT321 during a DMA cycle.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

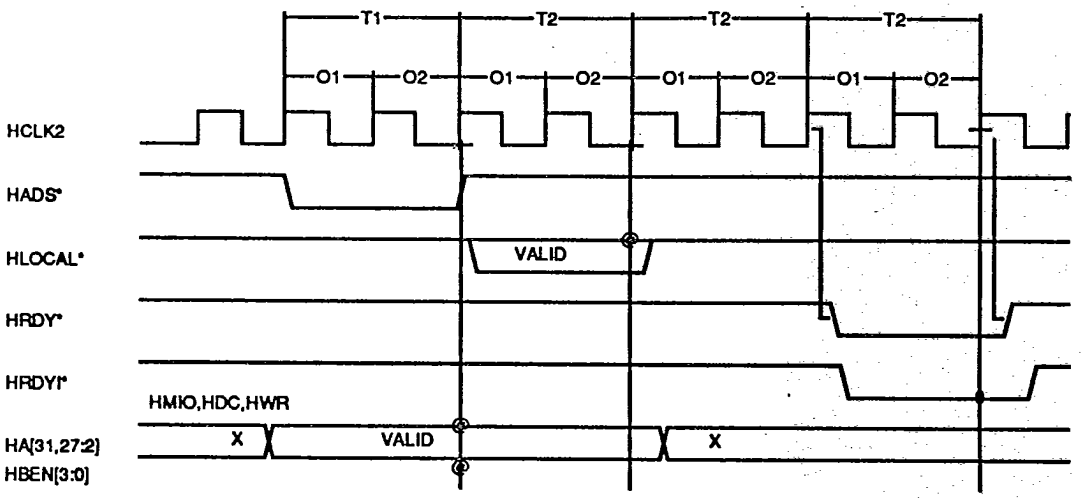


Figure 2.13 - HT321 Local Bus Signal Interface

Powered by ICminer.com Electronic-Library Service CopyRight 2003

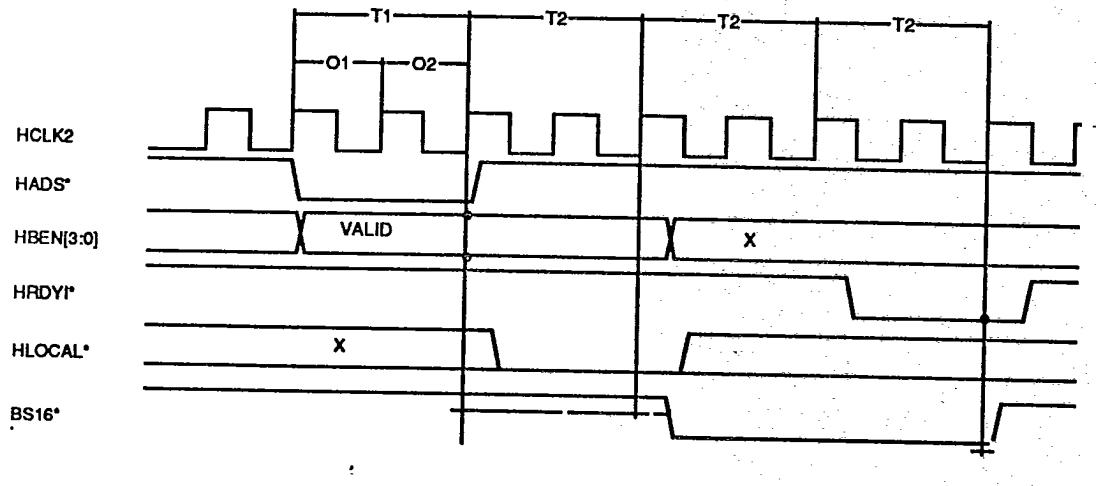


Figure 2.14 - BS16* Assertion

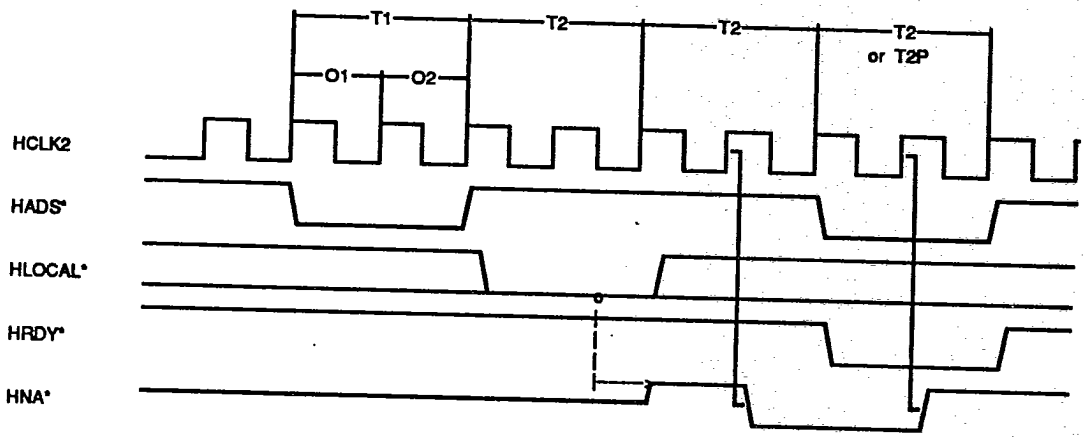


Figure 2.15 - HNA* Assertion

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

5. ISA BACKPLANE CONTROLLER

This module is responsible for producing ISA Compatible timing for the Backplane control signals. These signals include IOW*, IOR*, (S)MEMW*, (S)MEMR*, BALE which are synchronized to BCLK edges. In order to accomplish this, the ISA BACKPLANE CONTROLLER module monitors backplane signals MEMCS16*, IOCS16*, IOCHRDY, and 0WS* to determine the timing required by the current cycle. INDEX 02H may be programmed to set the Default Timing of any backplane access. The AT Compatible setting is of 6 BCLK cycle duration. The options exist to set default as low as 3 BCLK cycles duration for a Backplane cycle. The duration of a Backplane cycle is measured from 1/2 BCLK before the assertion of BALE to the end of the Command asserted for the cycle.

Backplane cycles begin within the HT321 once it is determined that the current Local Bus cycle is for the ISA Controller. This happens two HCLK2's after HADS* is sampled, indicating the start of cycle. At this point the ISA BACKPLANE CONTROLLER module will synchronize to the BCLK signal and begin the sequence by asserting a BALE pulse at the correct phase of BCLK. Dependant on the type of cycle requested and the state of the incoming backplane cycle Moderator Signals, the proper Command(s) will be determined. At the completion of the Command, HRDY* will be issued by the HT321 to the Local Bus indicating the cycle is complete. When HRDYI* is returned to the HT321 the cycle actually completes. For more detail see Figure 5.11, 5.12 of the AC Timing Section of this Data Sheet. A number of typical ISA Backplane cycles are shown in the following figures, 2.16, 2.17, 2.18, 2.19, 2.20, 2.21, 2.22, 2.23, 2.24, 2.25.

For DMA/MASTER MODE operation the BACKPLANE CONTROLLER section of the ISA Chip is disabled,since the Commands will be asserted by the MASTER device. BALE is normally set true(high) for the duration of a DMA cycle, allowing address flow-through to/from the backplane.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

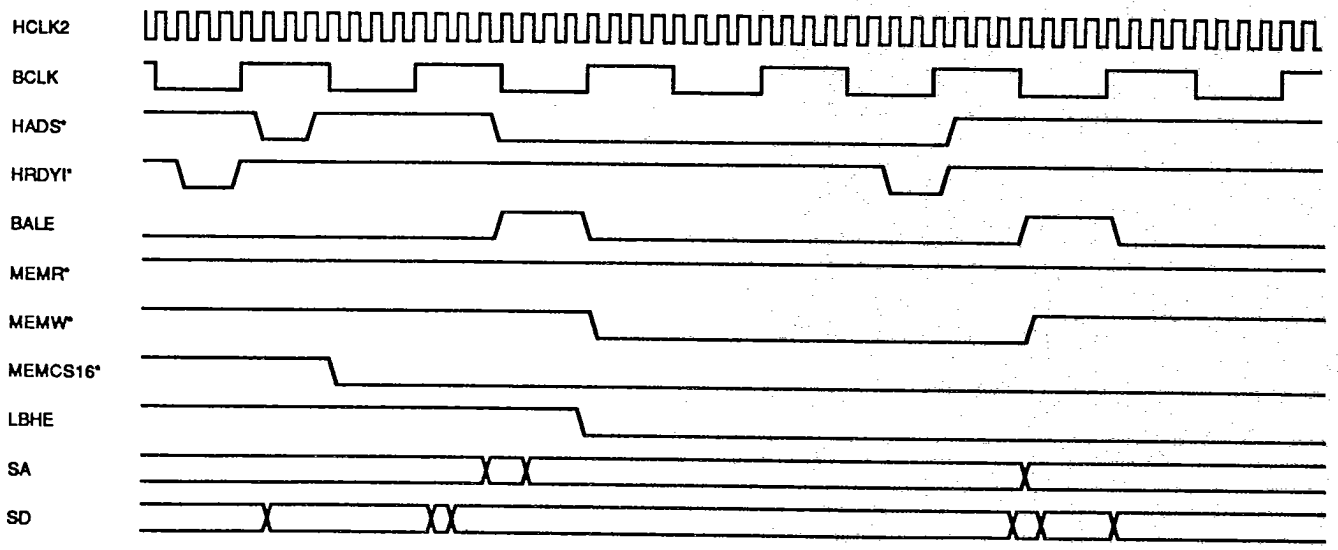


Figure 2.16 - 16-Bit MEMW* Cycle

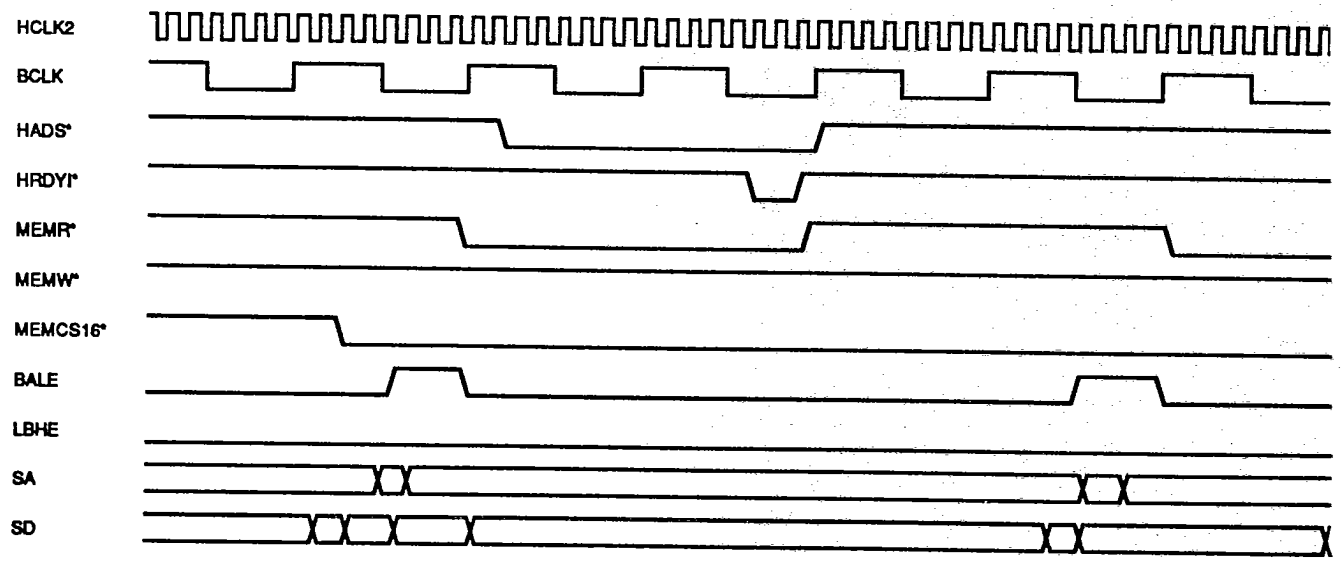


Figure 2.17 - 16-Bit MEMR* Cycle

Powered by ICminer.com Electronic-Library Service CopyRight 2003

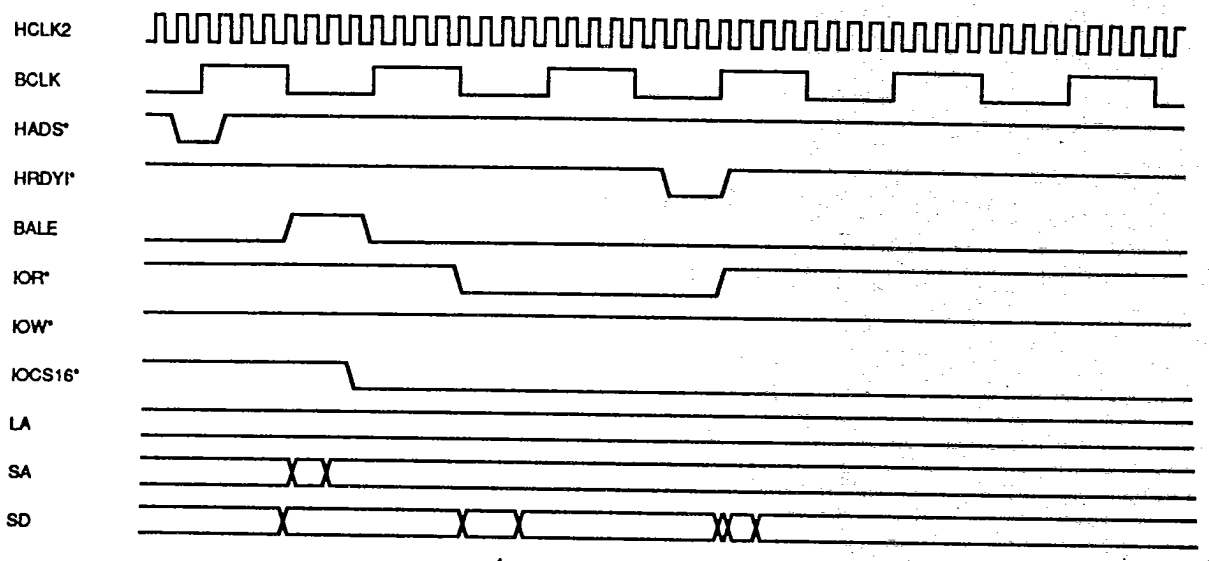


Figure 2.18 - 16-Bit I/O Read Cycle

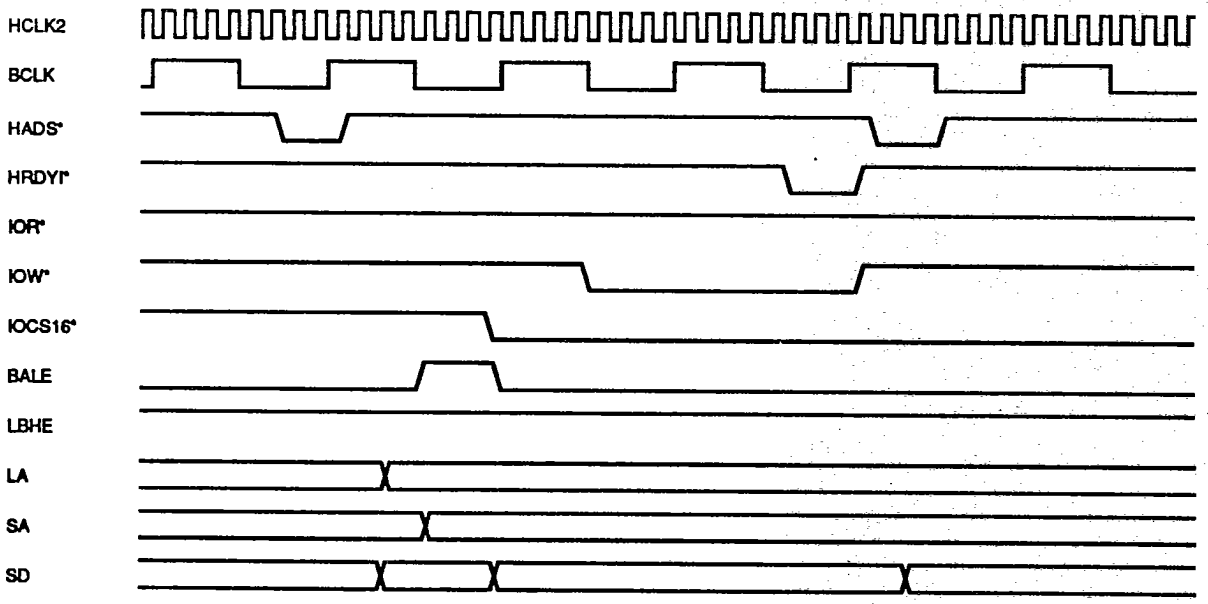


Figure 2.19 - 16-Bit I/O Write Cycle

Powered by ICminer.com Electronic-Library Service CopyRight 2003

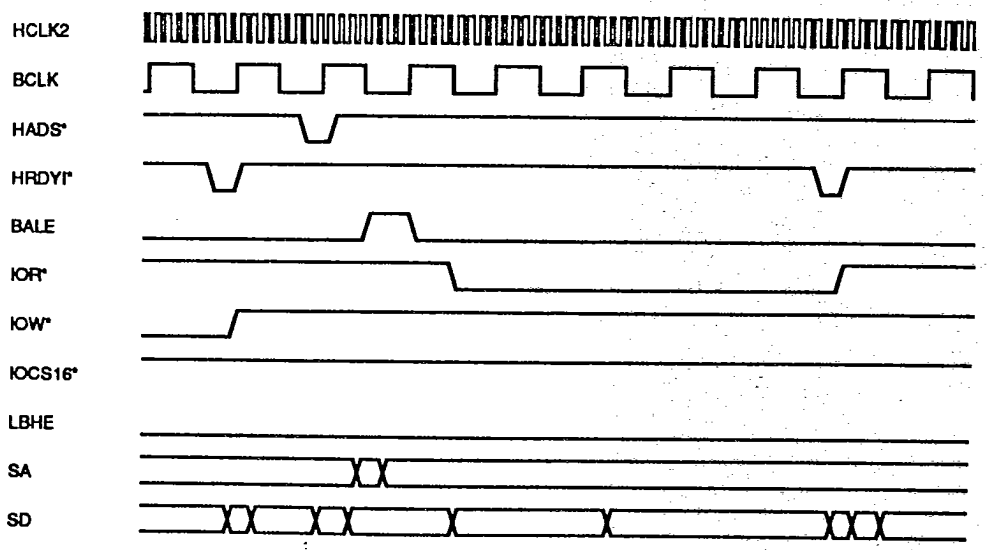


Figure 2.20 8-Bit I/O Read Cycle

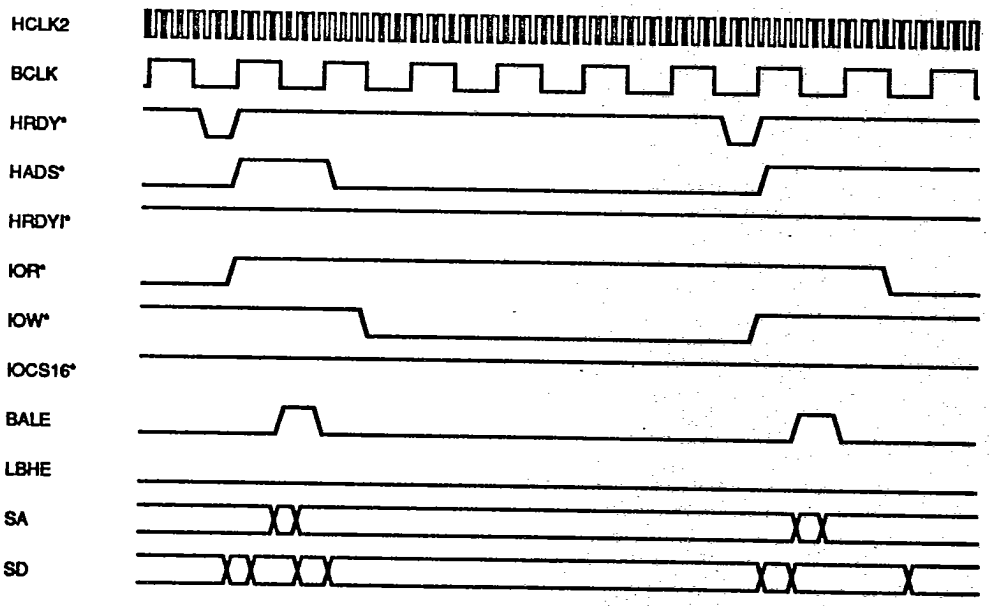


Figure 2.21 8-Bit I/O Write Cycle

Powered by ICminer.com Electronic-Library Service CopyRight 2003

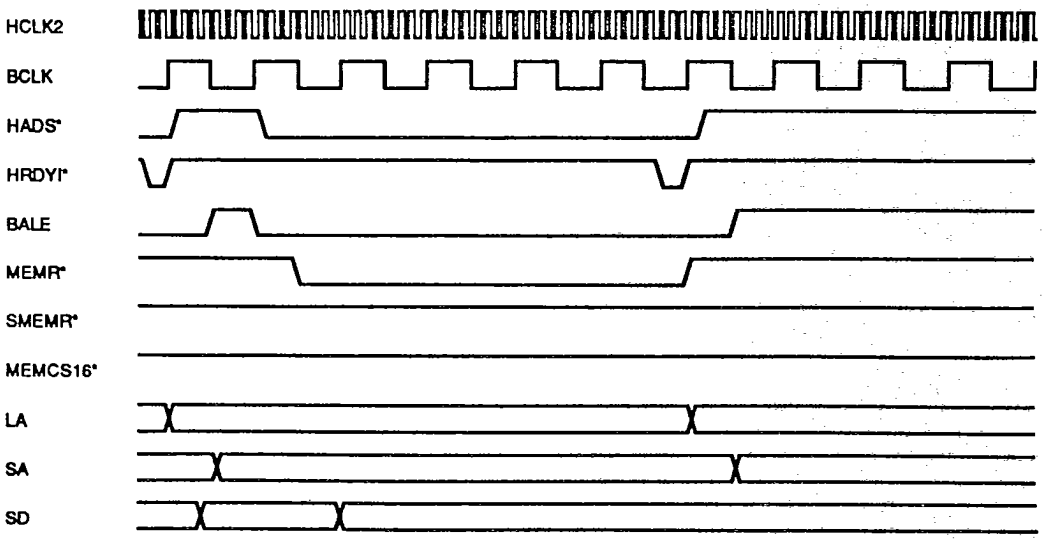


Figure 2.22 - 8-Bit MEMR* Cycle

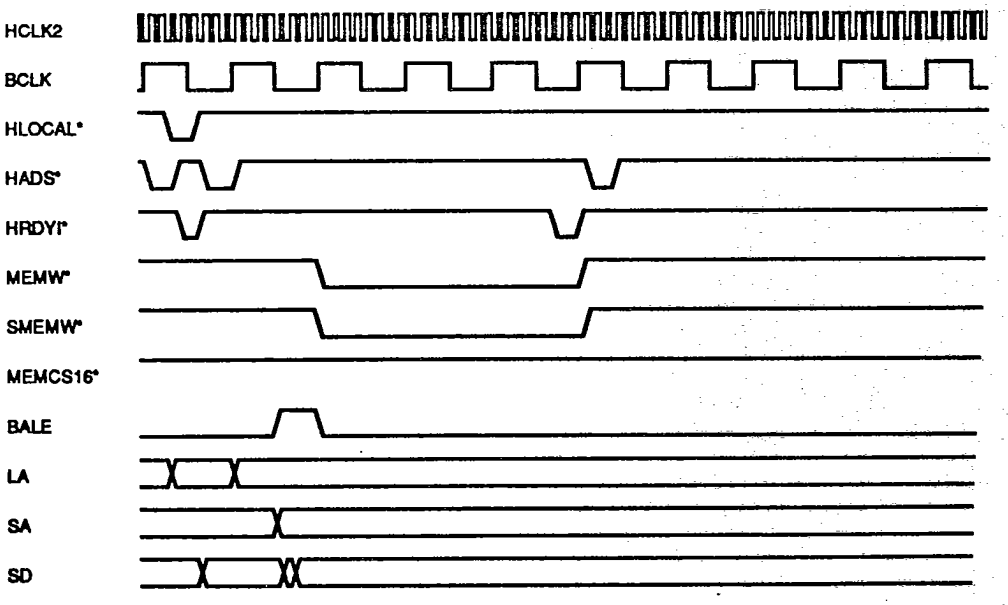


Figure 2.23 - 8-Bit MEMW* Cycle

Powered by ICminer.com Electronic-Library Service CopyRight 2003

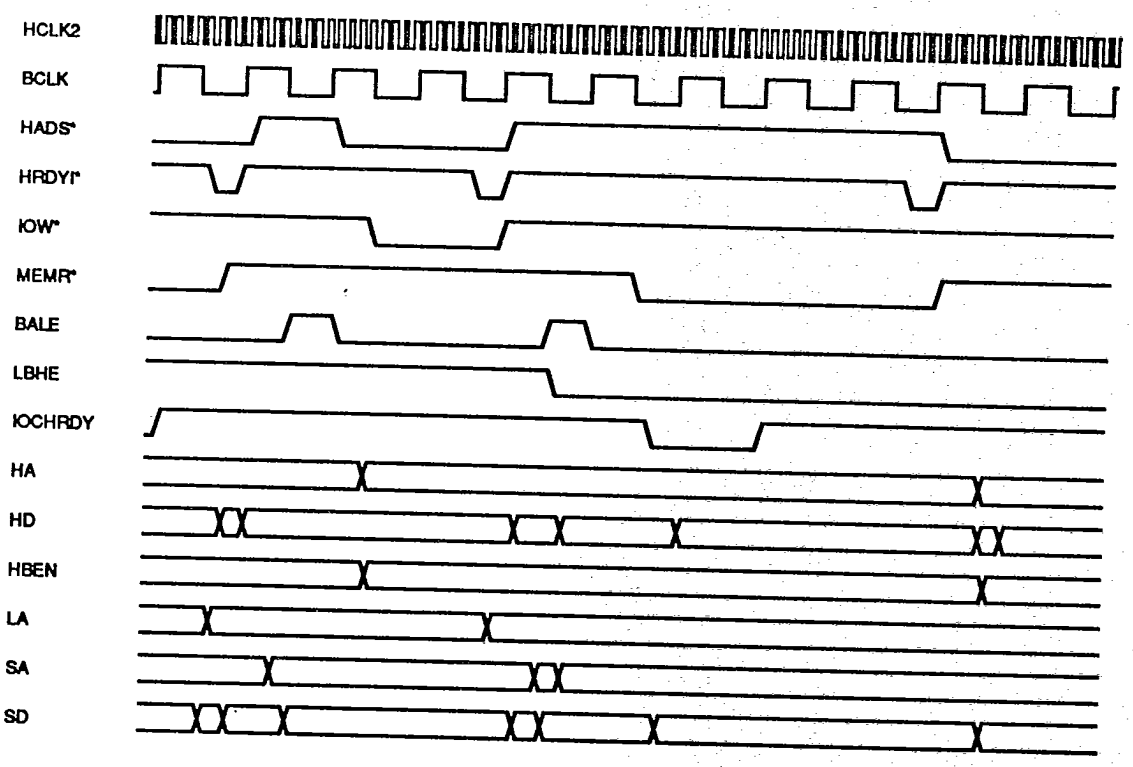


Figure 2.24 - IOCHRDY Wait States

Powered by ICminer.com Electronic-Library Service CopyRight 2003

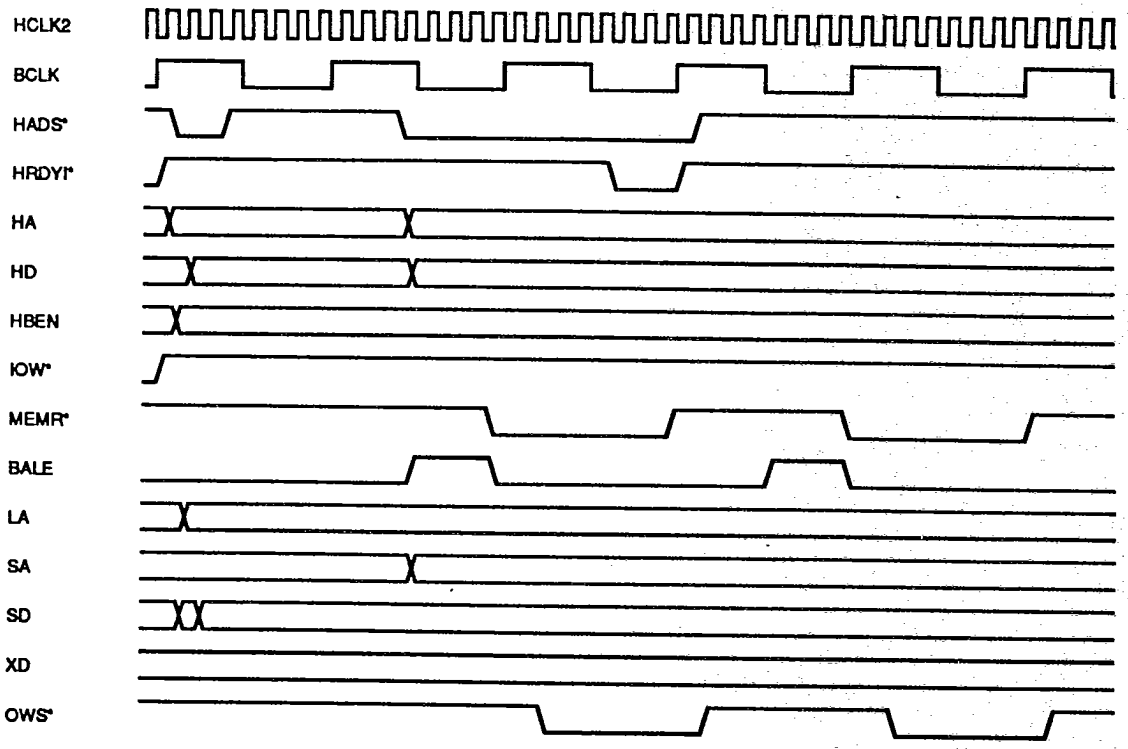


Figure 2.25 - 0WS Cycles

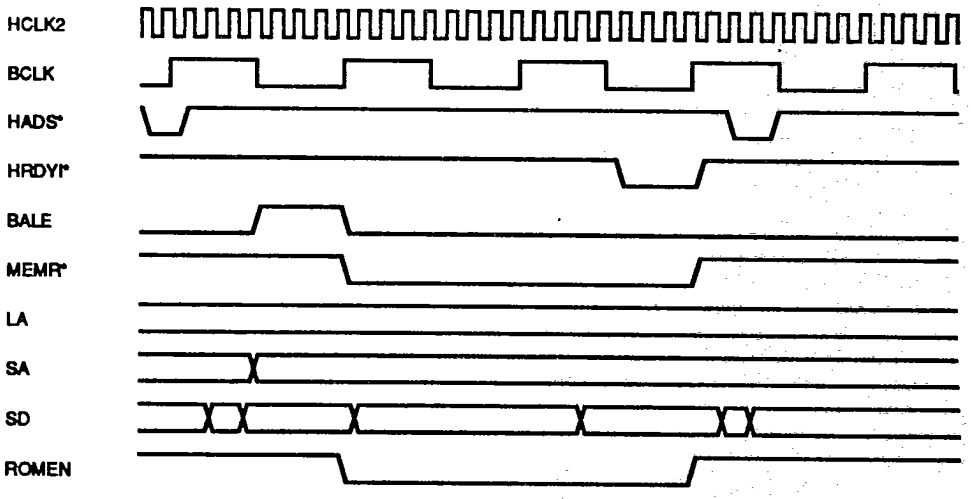


Figure 2.26 - PROM Read Cycles

Powered by ICminer.com Electronic-Library Service CopyRight 2003

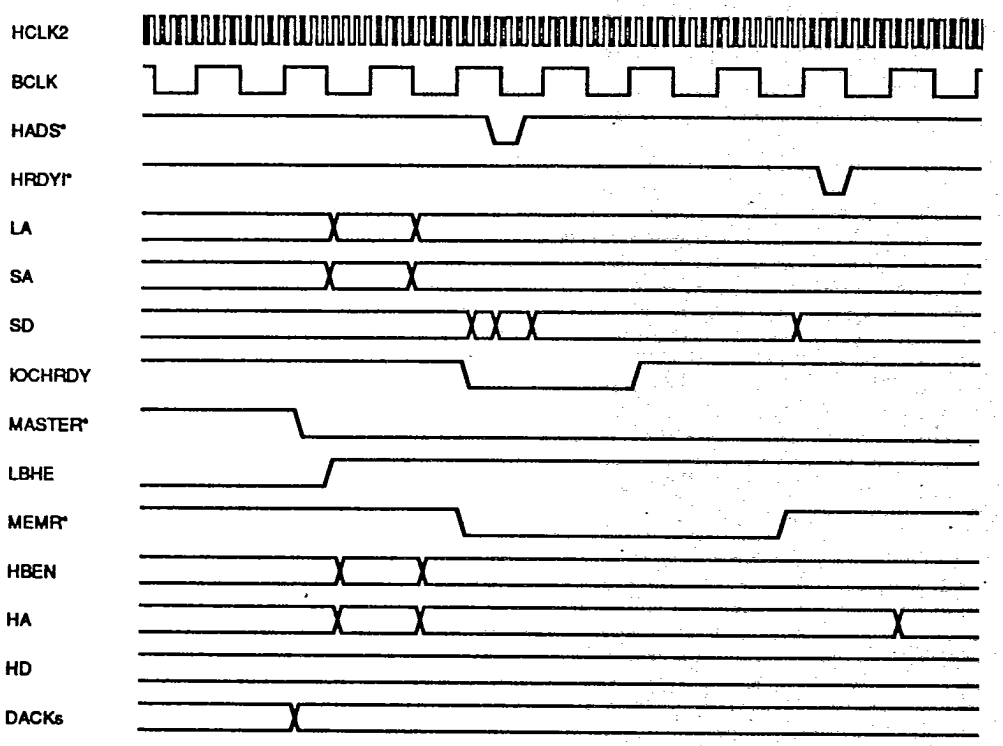


Figure 2.27 - MASTER Mode Backplane Read Cycle

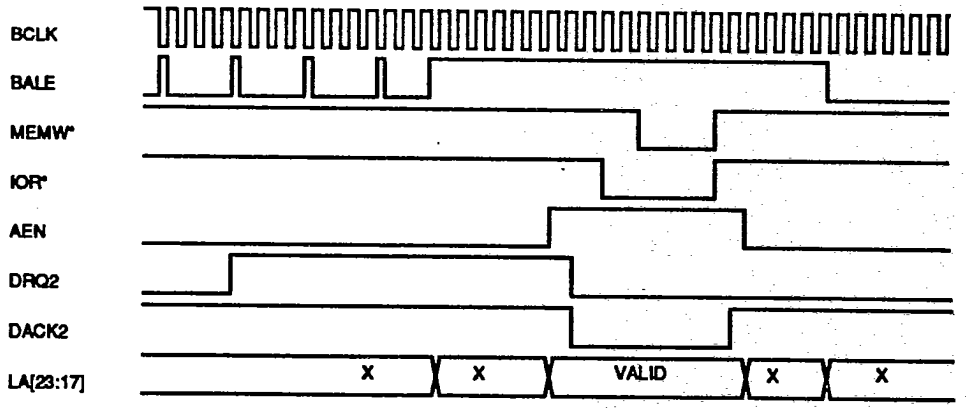


Figure 2.28 - DMA Cycle on the ISA Bus DRQ2/DACK
DMACLK = 4MHz DMA Wait State = 1 (AT Standard)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

6. I/O DECODE & CONFIGURATION

This module contains all the Internal Registers of the HT321 as well as Decodes for Internal and some External Devices. The HT321 provides "Chip Select" signals for two External Devices commonly used in AT Compatible Motherboard systems, they are, Real Time Clock Chip Select (RTCCS* P81) and Keyboard Chip Select (KBCS* P80). The tables below chart the internal I/O decode information of the HT321.

The Configuration Module contains all the INDEX Registers which provide the HT321 Programmable Configuration Controls. The HT321 has a total of 32 mapped Index locations but only those containing programmable bits are implemented and accessible. These ISA Configuration Registers are mapped into INDEX 00 - 1Fh. Most of these registers are Read/Write, but only the bits indicated should be altered. All Unused or Reserved Registers and Bits must be left at Default or Masked off during Configuration to maintain future compatibility.

The ISA Chip is also responsible for maintaining the current Configuration INDEX Pointer Value. Access to I/O location 028H will therefore, be terminated by the HT321. Data Read from I/O location 028H is made available to the CPU via HD[15:0].

The Configuration INDEX Register Bits of the HT321 are described in detail in the Register Description Section of this Data Sheet. Please refer to this section for detail of the Registers, Control Functions and program access to the Registers.

I/O Decode

The following table shows the I/O Decode range for Internal Ports of the HT321.

A15-A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Range(Hex)	Selected Device
0	0	0	0	0	0	0	0	X	X	X	X	X	000 -	DMA1
0													01F	PIC1
0	0	0	0	0	0	0	1	0	0	0	0	X	020 - 021	Config Data
0	0	0	0	0	0	0	1	0	0	1	0	0	024	Port
0	0	0	0	0	0	0	1	0	1	0	0	0	028	Config Address
0	0	0	0	0	0	1	0	X	X	X	X	X	040 - 05F	Port
0	0	0	0	0	0	1	1	0	X	X	X	0	060 - 064	PTC
0	0	0	0	0	0	1	1	1	X	X	X	X	070 - 071	KBC, Port B
0	0	0	0	0	1	0	0	X	X	X	X	X	080 - 08F	RTC, NMI
0	0	0	0	0	1	0	0	1	0	0	1	0	092	DMA Page
0	0	0	0	0	1	0	1	X	X	X	X	X	0A0	Sys Ctrl Port
0	0	0	0	0	1	1	0	X	X	X	X	X	0BF	PIC2
0	0	0	0	0	1	1	1	X	X	X	X	1	0C0	DMA2
	0	1	0	0	1	0	0	0	X	X	X	X	0DF	Reset NPU 287
													0F1	Extended
													480 - 48F	DMA Page

60-64 is KBC if A0=0, and Port B if A0=1, 070-071 is RTC if A0=1 and RTC and NMI if A0=0

All other address ranges are available to devices on the ISA bus.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

I/O Address Map

The following table describes the I/O ports supported by the HT321. The table is numerically ordered by HEX Address from zero.

I/0 TYPE

Addr Port	Read/ Write	Description
DMA Controller #1		
0000H	R/W	Channel 0 current address
0001H	R/W	Channel 0 current word count
0002H	R/W	Channel 1 current address
0003H	R/W	Channel 1 current word count
0004H	R/W	Channel 2 current address
0005H	R/W	Channel 2 current word count
0006H	R/W	Channel 3 current address
0007H	R/W	Channel 3 current word count
0008H	R/W	Command/Status Register
0009H	R/W	Request Register
000AH	R/W	Single Bit Mask Register
000BH	R/W	Mode Register
000CH	R/W	Clear Byte Pointer
000DH	R/W	Master Clear
000EH	R/W	Clear Mask Register
000FH	R/W	Write All Mask Register Bit
Programmable Interrupt Controller #1		
0020H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
0021H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
0023H		Reserved
0024H	R/W	Configuration Data Port
0028H	R/W	Configuration Address Port
0029H - 003FH		Reserved

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Addr Port	Read/ Write	Description
Timer/Counter		
0040H	R/W	Timer 0 Count Load/Read
0041H	R/W	Timer 1 Count Load/Read
0042H	R/W	Timer 2 Count Load/Read
0043H	W	Timer Control Word
0044H - 005FH		Reserved
Write Keyboard Controller		
0060H	R/W	Keyboard Data
0062H - 0063H		Reserved
0064H	R/W	Keyboard Control/Status
Port B		
0061H	R/W	Port B Status Port
Real Time Clock		
0070H	W	Real-Time Clock Index and NMI Mask
0071H	R/W	Real-Time Clock Data Port
DMA Page Registers		
0080H	R/W	Not Used
0081H	R/W	Channel 2 Page Register
0082H	R/W	Channel 3 Page Register
0083H	R/W	Channel 1 Page Register
0087H	R/W	Channel 0 Page Register
0089H	R/W	Channel 6 Page Register
008AH	R/W	Channel 7 Page Register
008BH	R/W	Channel 5 Page Register
System Control Port		
0090H - 0091H		Reserved
0092H	R/W	System Control Port
0093H - 009FH		Reserved

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Programmable Interrupt Controller #2		
00A0H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
00A1H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
DMA Controller #2		
00C0H	R/W	Channel 0 current address
00C4H	R/W	Channel 0 current word count
00C6H	R/W	Channel 1 current address
00C8H	R/W	Channel 1 current word count
00CAH	R/W	Channel 2 current address
00CCH	R/W	Channel 2 current word count
00CEH	R/W	Channel 3 current address
00CFH	R/W	Channel 3 current word count
00D0H	R/W	Command/Status
00D2H	R/W	Request Register
00D4H	R/W	Single Bit Mask Register
00D6H	R/W	Mode Register
00D8H	R/W	Clear Byte Pointer
00DAH	R/W	Master Clear
00DCH	R/W	Clear Mask Register
00DEH	R/W	Write All Mask Register Bit
00DFH - 00EFH		Reserved
Extended DMA Page Registers		
0480H	R/W	Not Used
0481H	R/W	Channel 2 Extended Page Register
0482H	R/W	Channel 3 Extended Page Register
0483H	R/W	Channel 1 Extended Page Register
0487H	R/W	Channel 0 Extended Page Register
0489H	R/W	Channel 6 Extended Page Register
048AH	R/W	Channel 7 Extended Page Register
048BH	R/W	Channel 5 Extended Page Register

Powered by ICminer.com Electronic-Library Service CopyRight 2003

7. MEGAFUNCTIONS

This block of the HT321 contains the Intel Compatible Megafunctions necessary for the implementation of an AT-Compatible system. Within this module there are the equivalents of two Intel 8237 DMA Controllers, two 8259 Intel Interrupt Controllers and one Intel 8254 Programmable Interval Timer. All the support logic necessary to implement and clock these devices is also included. Below is a brief description of each of the Megafunctions in this block. This information, together with the detailed Register Description for these devices located in the REGISTER DESCRIPTION section of this data sheet should provide the user with enough information to properly program and use these devices. If further information is required, please examine the IBM AT Technical Reference manual or the Intel Data Sheet for the particular device in question.

DMA Controller

The HT321 contains two DMA controllers which are compatible to an Intel 8237. Each controller is a four-channel DMA device that can generate the Control Signals and Memory Addresses necessary to transfer information between a Peripheral Device and Memory. The DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection for the two DMA devices.

This arrangement is used to maintain IBM PC AT bus compatibility as documented by the IEEE P996 specification. The DMA functions are arbitrated by internal logic and will gain control of the Local Bus as an Temporary Bus master. To facilitate this operation, the HT321 utilizes the HOLD/HLDA protocol of the microprocessor.

The DMA Controller is clocked via one of two sources:

i) for AT-Compatibility, the DMA Controllers can be clocked with BCLK/2 (4 MHz), or

ii) for systems requiring greater DMA performance, the DMA Controller can be clocked by BCLK (8 MHz).

The clock for the DMA Controllers is selected via INDEX 06 of the HT321. INDEX 06 also controls the DMA Wait States. The option ranges from 0 to 3 additional Wait States inserted into any DMA cycle generated. For AT-Compatibility, the setting should be at 1 Wait State.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Interrupt Controller

The HT321 incorporates two programmable Interrupt Controllers that are functionally compatible to an Intel 8259A. The controllers accept Interrupt Requests from Peripherals, resolve Priority between pending interrupts and interrupts in service, issue an interrupt request to the CPU and supply a vector which is used as an index by the CPU to select the service routine to execute.

A variety of Priority Assignment Modes are provided, which may be changed at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the Operating System requirements. The controllers are cascaded in a fashion compatible with the IBM PC AT and to be compatible with IEEE AT Bus P996 Specification .

The table below shows typical interrupt levels assigned for an AT-compatible I/O bus.

The two devices are coupled in chain fashion by connecting interrupt output of Programmable Interrupt Controller 2 (PIC2) to the interrupt request input 2 of PIC1. To ensure that all 16 interrupt channels operate correctly in arrangement, all channels must be programmed to operate in Cascade Mode. PIC1 is located at addresses 020H - 021H and is configured for Master operation in Cascade Mode. PIC2 is a Slave device and is located at addresses 0A0H - 0A1H(see definitions below). The address location and Cascade interconnection provides compatibility with IEEE AT Bus P996 Specification.

Two additional connections are made to the interrupt request inputs of PICs 1 and 2. The output of Timer 0 in the Counter/Timer Megafunction is connected directly to the input of Channel 0 (IRO) of PIC1 and does not have an external connection. In a standard AT system implementation, IRQ1 is reserved exclusively for the Keyboard Output Buffer Full Flag. Therefore, the input pin for this interrupt has been named OPTBUFUL or Output Buffer Full and should only be used as an input from a Keyboard Controller. IRQ8 differs from the other IRQ's, it has an invertor between the input pin and PIC2. For correct notation it should therefore have a "negated signal symbol" * as an input.

Interrupt	System Functions	I/O Bus
NMI	Parity Check	IOCHCK
IRQ0	Timer	Not Available
IRQ1	Keyboard	Not Available
IRQ3	Serial Port 2	Available
IRQ4	Serial Port 1	Available
IRQ5	Parallel Port 2	Available
IRQ6	Floppy Disk	Available
IRQ7	Parallel Port 1	Available
IRQ8	Real-Time Clock	Not Available
IRQ9	Not Used	Available
IRQ10	Not Used	Available
IRQ11	Not Used	Available

Typical System Interrupts and AT-compatible I/O Channel

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Programmable Interval Timer

The HT321 integrates a Programmable Interval Timer (PIT), which is functionally equivalent to an Intel 8254 Programmable Interval Timer/Counter. The PIT is programmable through internal I/O ports located at 0040H through 0043H.

The Clock inputs of the three channels are driven by a 1.19 MHz clock which is internally generated by dividing the oscillator input (OSC P160 14.31818 MHz) by 12. The outputs of the three channels are as follows:

- Channel 0 is a general purpose and software interrupt timer. The output of this channel is connected directly to the IRQ0 pin of the integral Programmable Interrupt Controller (PIC1). (see the Interrupt Controller Functional Description)
- The output of Channel 1 is used internally by the HT321 to generate refresh requests.
- The output of Channel 2 provides for tone generation for a speaker.The HT321 presents this signal as SPeaKeR (SPKR P78).

Programmable Timer Control

The Programmable Interval Timer (PIT) in the HT321 is general purpose and can be used to generate accurate time delays under software control. The PIT contains three 16-bit counters (Counter[0:2]) which may be programmed as Binary or Binary Coded Decimal (BCD) counters. Each counter operates independently of the other two and each can operate as a Timer or Counter.

The counters have common control logic which decodes control information written to the PIT and has the necessary controls to load, read, configure and direct each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

Mode 0 - Interrupt on terminal count

Mode 1 - Hardware re-triggerable one-shot

Mode 2 - Rate generator

Mode 3 - Square wave generator

Mode 4 - Software triggered strobe

Mode 5 - Hardware re-triggerable strobe

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Functional Description

Introduction

The main purpose of the HT322 Memory Control Unit (MCU) is to provide the interface to DRAM and Cache Memory of the system. Due to pin constraints in the chipset, another, non-memory related function has been assigned to the chip, i.e. numerical co-processor interface and AT-compatible numerical error reporting.

The HT322 is a high performance, pipelined DRAM controller with integral Cache Controller including tag RAMs and Write Buffer. The cache operation is defined as Write-through. The Controller interfaces to '386DX Systems with minimum support logic. The Controller conforms to the Local Bus Specification.

If Valid Data is present in the Cache, a cycle is terminated at the Local Bus at a 0 wait state rate. 4-level Write Buffering is provided, such that if not all write buffers are full, any Write Cycle is terminated at 0 wait state rate. A superior set of DRAM control algorithms has been defined. Utilizing pipelined techniques, a 0 wait state rate has been achieved during Write Cycles on a Page Hit even at high operating frequencies. This, combined with Write Buffering, effectively make Write Cycles 0 Wait States.

Outlined below are the major features of the controller:

One 184 PQFP pin package

Uses 1 micron HCMOS Technology

Fully static operation : 0-40 MHz CPU speeds

Local bus architecture compatible

LIM EMS 4.0 support

Separate Data Bus for DRAMs and Local Bus

Parity generation, detection and reporting.

Built-in Cache Controller with integral tag RAM supporting 2-way set associative 32KB, 64KB and 128KB write-through Data Cache - up to 4 banks of Memory, any number of banks configurable (1, 2, 3 or 4), any mixed memory configuration.

256K, 1Mb, 4Mb, 16Mb DRAM type support.

Up to 256 MB total addressability (4 banks of 16Mb DRAMs).

Shadowing in 16KB increments between 640KB and 1MB.

Up to 384KB of memory, from 640KB to 1MB, may be remapped above the main memory limit. Remapping coexists with Shadowing, meaning any remaining un-shadowed DRAM may be remapped above the main memory limits.

1, 2, 4-way CAS interleave with fast paging .

Middle BIOS Support enable/disable.

Programmable 26 non-cacheable regions.

Refresh hidden from the system.

CAS before RAS or RAS only Refresh.

RAS staggering during Refresh.

Programmable Timing Parameters for DRAM access.

Programmability for Read and Write Cycle Timing separate.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

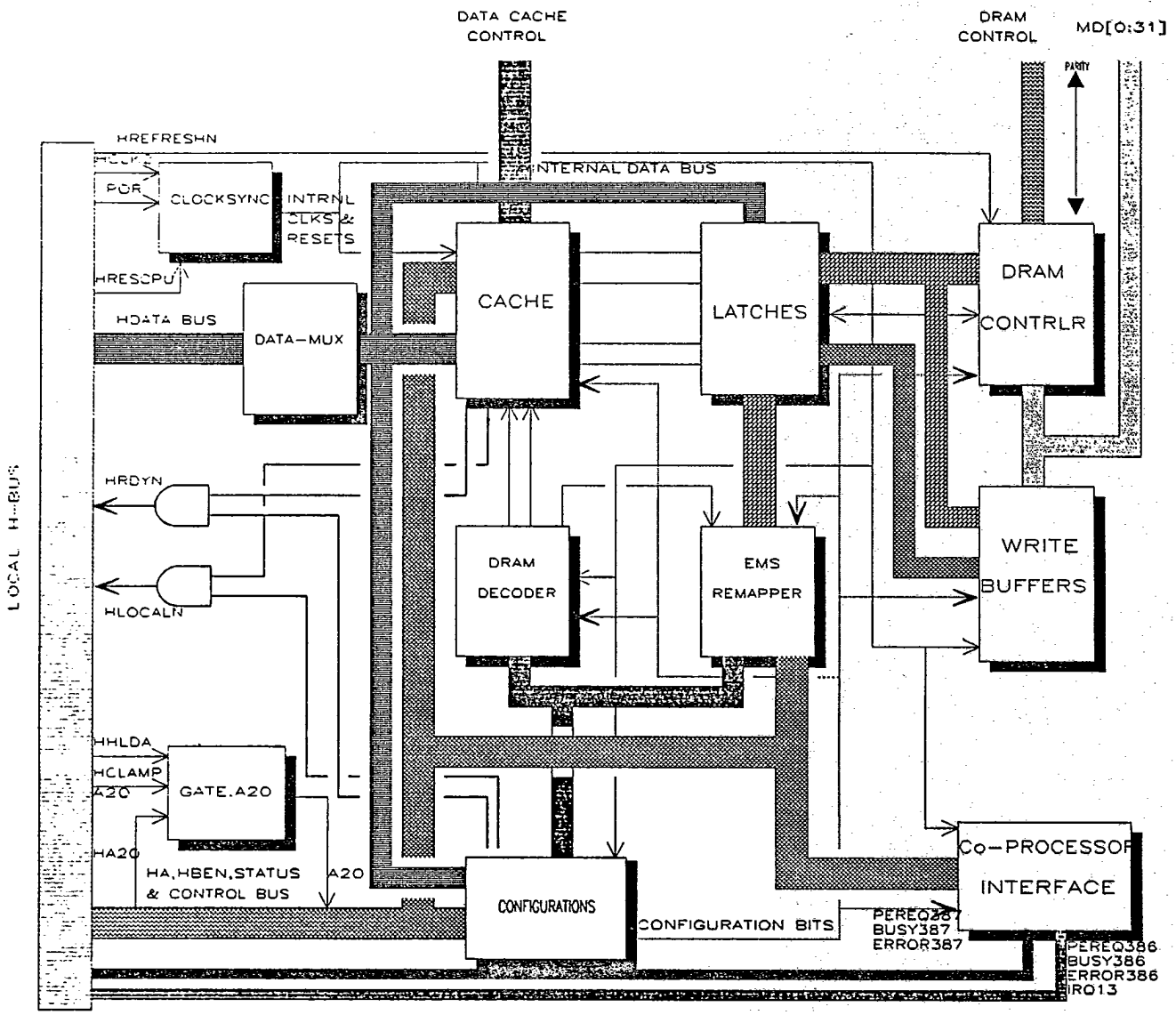


Figure 2.29 - HT322 MCU Internal Block Diagram

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Traditional Cache Update on Read Misses and Write Hits.

4 double-word line size.

A separate address tag for 4/8/16 Lines (dependant on the cache size).

A separate valid tag bit for each line.

4 double-word deep Write Buffering.

Byte gathering support.

Out of order operation (reads propagate ahead of writes if there is no hit in the write buffers).

Ability to respond from within the Write Buffer for a Write Buffer Read Hit.

Fully AT-compatible '387 co-processor interface with error reporting.

Architecture

The HT322, as a functional device, provides three major operational sections: Cache Controller, Write Buffers and a DRAM Controller implementing complete DRAM Control functions. These three major modules, shown in the Block Diagram on Page 37, are called CACHE, WRITE_BUFFERS and DRAM_CONTROLLER respectively. They are organized in a pipelined fashion. The CACHE module generates all cycles for the WRITE_BUFFERS, thus implementing a classical memory cache interface. The WRITE_BUFFERS module generates cycles for the DRAM_CONTROLLER module as a second stage of the pipeline. These three megamodules are distinct and independent entities.Their major functions are described below.

CACHE

The Cache Controller supports 3 configurations of data cache size : 32KB, 64KB and 128KB. The main organizational mode of the cache is 2-way set associative. This means that the 32/64/128 KB RAM space is split into two even 16/32/64 KB blocks of memory, called "ways". Each of these ways is further divided into 1024/2048/4096 units, called "lines". A line is the smallest transfer unit between the CACHE module and the WRITE_BUFFERS module when a data cache memory update occurs. A line is four dwords long(32 Bytes). During a Read Miss cycle, when the data cache RAM is updated (provided the memory region is defined as cacheable), a line of data will be read from the DRAM memory (using the WRITE_BUFFERS local protocol), it can be stored into one of two line locations in one of the ways. The decision, which way to store the data, depends on whether the ways contain any previous valid data (the next free way will be used). If both contain some valid data, the LRU(Least Recently Used) algorithm is used to resolve the replacement question. For write-through operation, data is always passed to the DRAMs from the actual write cycle.

A cache directory integral to the Cache Controller RAM Memory (called TAG RAM) contains necessary information about the data currently resident in the Cache. This TAG RAM is organized as 2 banks — a bank for each way of data cache RAM.

A Valid bit for each of the lines, indicates integrity of current stored data.

An Address tag is associated with each group of 4/8/16 lines within a way. This tag stores upper A[27:14]/A[27:15]/A[27:16] (for 32/64/128 KB Cache Size respectively) addresses associated with the lines within the group. In order to determine if the current cycle is a Cache Hit (meaning valid data is in the cache RAM) a comparison of the CPU upper address and the prestored tag address bits must result in a match, the valid bit must also be set. The lower CPU Address Bits are used to address both banks of TAG RAM. A tag match and a true valid bit set produces the hit within one of the ways. A hit may occur in only one of the ways any violation of this specification can be produced only by a system malfunction.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

An LRU RAM is associated with both ways. This RAM stores LRU bits showing which way was least recently accessed. When both ways of a particular address contain valid data one must be replaced.

The following Cycles are possible for the Cache Controller:

Read hit

If cacheable, the cycle is always terminated at a 0 wait state rate - none of the tags are changed, nor is a cycle on the WRITE_BUFFERS internal local bus generated. LRU RAM is always updated.

Figure 2.30 illustrates a Cacheable Read Hit Cycle. HRDY* terminates the cycle at 0 wait state, OEA* (or OEB*) is generated at the same Clock edge as HRDY*, all CHIPSEL*[3:0] are activated, CA1 and CA0 are set accordingly and CALE is active throughout the whole cycle.

If the cycle is non-cacheable, the tag entry for the cycle is invalidated and the data access passed to the DRAM Memory.

Read miss

A cycle fetching the entire line is generated on the WRITE_BUFFERS internal local bus unless the cycle is identified as non-cacheable (flagged by a configuration setup or early assertion of NON_CACHE* signal - early means at the clock edge when HADS* from the CPU is sampled asserted). In the case of invalidation by NON-CACHE* the cycle is limited to one d-word fetch (the one requested by the CPU). During a line fetch the Data Cache RAMs are updated and the tags are also updated with the new information.

Figure 2.32 illustrates a Cacheable Read Miss Cycle. HRDY* terminates the cycle only after all four dwords of the line have been fetched and written to the data cache RAM. WEA* (or WEB*) writes consecutive dwords to the RAM. CA1 and CA0 address the RAM in a way that the last dword fetched is the one requested by the CPU. The '486 CPU burst addressing sequence is used. CALE is active throughout the cycle.

Write Hit

The data cache is updated immediately unless the target address is defined as non-cacheable. The tag entry for the Address is Invalidated if the address is non-cacheable. A write cycle is started on the WRITE_BUFFERS internal local bus immediately if/when the status of the bus is IDLE or about to become IDLE. At the same time, the data and address are latched, and the cycle on the Local Bus is terminated. For IDLE and about to be IDLE status of the WRITE_BUFFERS local bus the cycles are terminated at a 0 wait state rate thanks to the single write buffering in the LATCHES module (see block diagram). Further buffering of write cycles performed at the WRITE_BUFFERS level will be discussed later.

Figure 2.33 illustrates a 1 wait state Cacheable Write Hit Cycle. HRDY* terminates the cycle, WEA* (or WEB*) write bytes specified by the CPU to the RAM. CHIPSEL*[3:0] select the bytes. CALE is active throughout the cycle.

Figure 2.31 illustrates a 0 wait state Cacheable Write Hit Cycle. HRDY* terminates the cycle at 0 wait state rate. CALE is deactivated at the end of the cycle.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

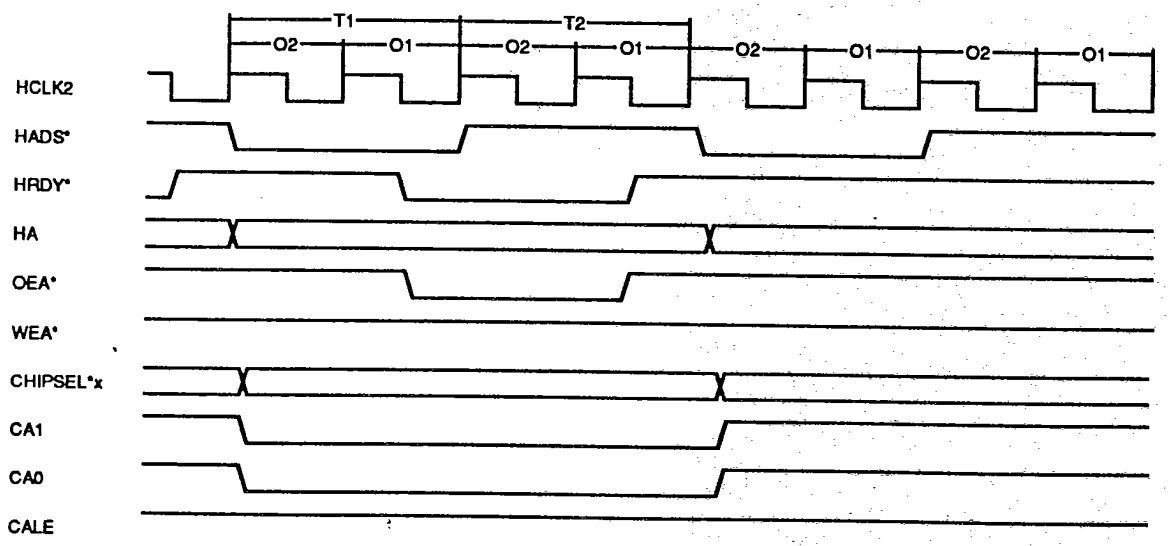


Figure 2.30 - CACHE Read Hit

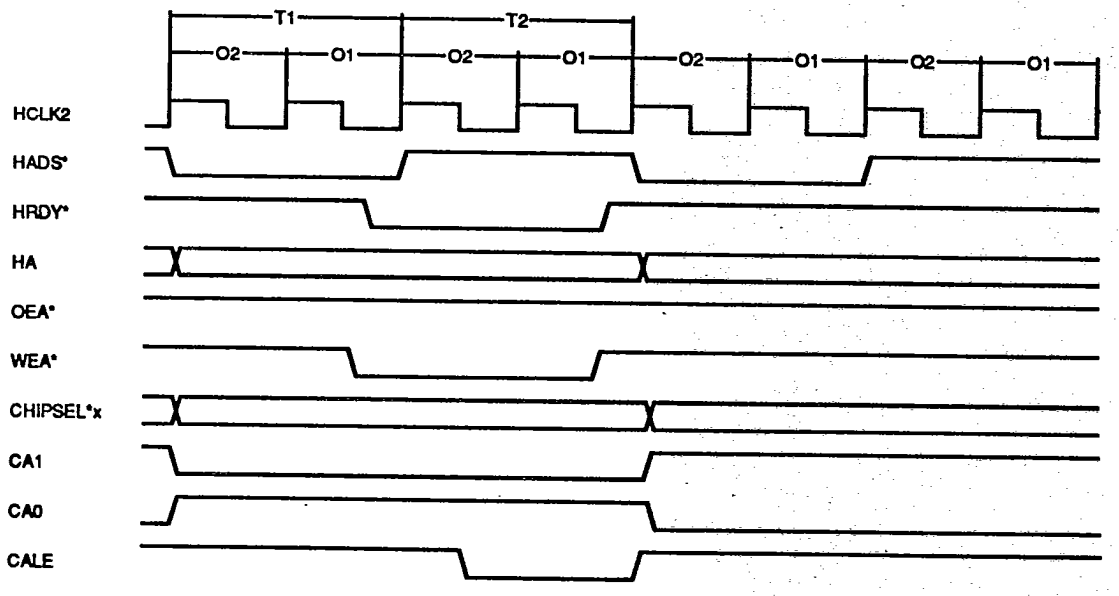


Figure 2.31 - CACHE Write Hit 0 Wait State

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

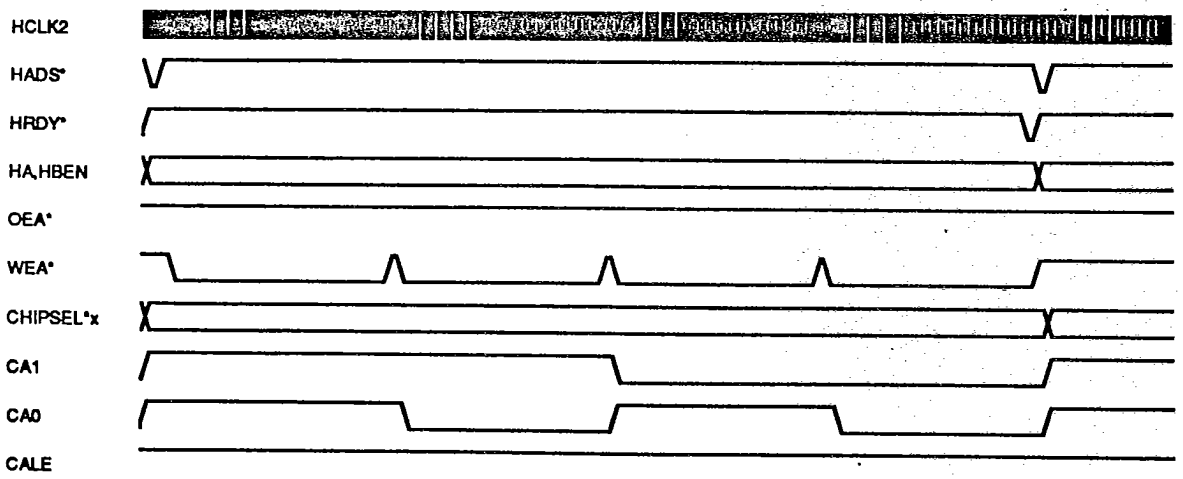


Figure 2.32 - CACHE Read Miss

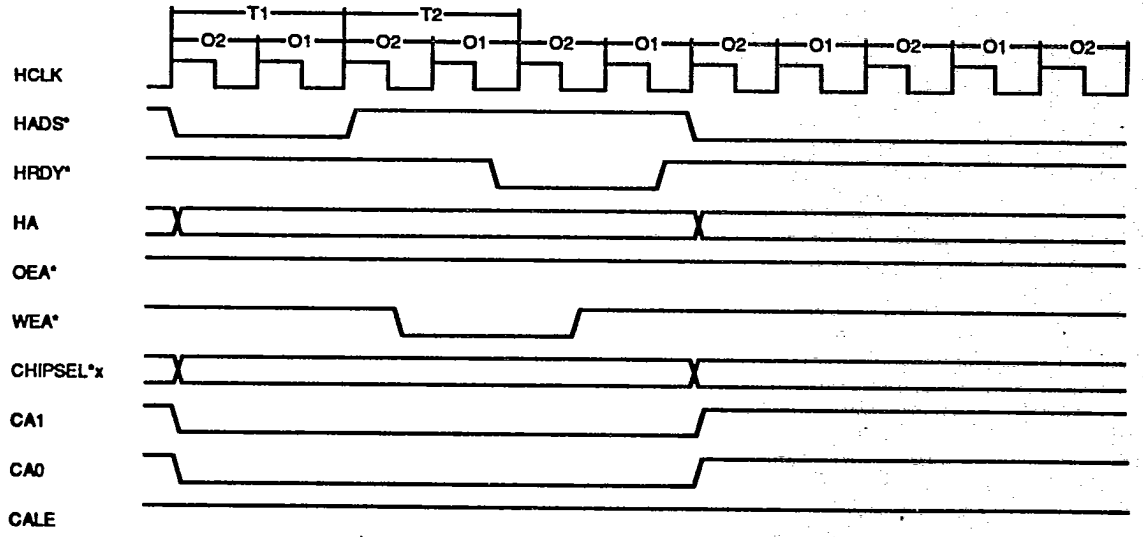


Figure 2.33 - CACHE Write Hit 1 Wait State

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Write Miss

This cycle never updates the cache. The Data is latched in the LATCHES module as soon as the WRITE_BUFFERS bus state is IDLE or about to be IDLE. At this moment the cycle is terminated on the local bus.

WRITE_BUFFERS

The second major function of the HT322; is buffering of write data. The module WRITE_BUFFERS, controls cycles on the DRAM_CONTROLLER local bus.

Write buffering is a common feature in older CPU caches with write-through algorithms, as well as newer RISC Architectures. It provides buffering of write cycles. The performance improvement is significant mostly because, in cache systems, after the CPU code is fetched and resides in the cache, most of the cycles outside of the cache are write cycles. In non-cached systems write cycles occupy 20% of a system's bus bandwidth. This means if one write occurs every 4 reads and all reads are cached, a 3/4 wait state buffered write cycle (buffered and terminated at 0 wait state rate) might not slow down the CPU at all. Since 1 write per 5 access cycles is a statistical rate, having more than a single write buffer is important for all those situations "at an edge of the statistical curve" when writes occur back to back.

Whenever one of the write buffers fills, the WRITE_BUFFERS module starts its unload sequence by generating cycles on the DRAM_CONTROLLER local bus. Write cycles from the module are always FIFO.

An important feature of the WRITE_BUFFERS module is byte gathering.

If data being written by the CACHE to the WRITE_BUFFERS happens to be a 'Write Buffer Write Hit'(an address match for the data of the cycle occurs for data already in the WRITE_BUFFERS , queued for unload) then the data will be directed to the write buffer where the match occured. Multiple hits are impossible. This aligns with the 16-bit nature of currrent software written for '286 machines to be run on '386 DX Systems.

Another feature of the WRITE_BUFFERS module is out of order operation. Any read cycle will be processed before any write unload cycle, eliminating slow down by the collision of cache read miss cycles with latency of the write buffer unloads. This feature is tightly coupled with another feature of the WRITE_BUFFERS, which is an ability to respond from its buffers to a Write Buffer Read Hit. Typically what happens is that for Write Buffer Read Hits only a part of the data requested is present in the write buffer, the remainder is fetched from the DRAM.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

DRAM_CONTROLLER

The third major unit of the HT322 is the DRAM_CONTROLLER. This unit provides all DRAM control algorithms.

The DRAM_CONTROLLER supports up to 4 banks of DRAM memory of 256Kb, 1Mb, 4Mb and 16Mb types. Any combination of these types of DRAM memory may be used, meaning it is possible to install any type of DRAM in any bank. From one to four banks may be used. This provides for unlimited flexibility of system upgrade. The DRAM_CONTROLLER supports programmable 2-way or 4-way CAS interleave. It is possible to select 2-way interleaving between two lower banks, and between two upper banks or between lower and upper banks. For 4-way interleave all 4 banks have to be installed. The interleaved banks must be populated by the same type of DRAMs. HA2 address line determines 2-way CAS interleave. HA2 and HA3 are used for 4-way interleave.

Fast paging is also supported by the DRAM_CONTROLLER. Internal Pipelined Local Buses between the CACHE and WRITE_BUFFERS and the WRITE_BUFFERS and DRAM_CONTROLLER have 'bursting capability'.This technique along with the CAS interleaved scheme of DRAM control makes for faster Cacheable Read Miss Cycles.

The tables below describe mapping of the HA to MA lines :

A. No Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA2	HA3	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13
RAS Address	X	Y	Z	HA14	HA15	HA16	HA17	HA18	HA19	HA20	HA21	HA22

where:	X	Y	Z	
	HA11	HA12	HA13	for 256K DRAMs
	HA12	HA13	HA21	for 1M DRAMs
	HA13	HA22	HA23	for 4M DRAMs
	HA23	HA24	HA25	for 16M DRAMs

Powered by ICminer.com Electronic-Library Service CopyRight 2003

B. 2-way Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA3	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13	HA14
RAS Address	X	Y	Z	HA15	HA16	HA17	HA18	HA19	HA20	HA21	HA22	HA23

where:	X	Y	Z	
	HA12	HA13	HA14	for 256K DRAMs
	HA13	HA14	HA22	for 1M DRAMs
	HA14	HA23	HA24	for 4M DRAMs
	HA24	HA25	HA26	for 16M DRAMs

C. 4-way Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13	HA14	HA15
RAS Address	X	Y	Z	HA16	HA17	HA18	HA19	HA20	HA21	HA22	HA23	HA24

where:	X	Y	Z	
	HA13	HA14	HA15	for 256K DRAMs
	HA14	HA15	HA23	for 1M DRAMs
	HA15	HA24	HA25	for 4M DRAMs
	HA25	HA26	HA27	for 16M DRAMs

RAS only or CAS before RAS Refresh methods are supported. Internal refresh counters generate refresh address during RAS only refresh. The RAS signals during refresh can be staggered.

A powerful set of Timing Options have been implemented, allowing the user to adjust timing to suit specific system and DRAM speeds:

a) RAS delay - 0 or 2 HCLK2

Selects MA setup time on RAS. For zero RAS delay setup time becomes 2xHCLK2 +/-system and internal delays. For two HCLK2 RAS delay the setup time is 2 HCLK2 longer.

b) CAS delay - 2 or 4 HCLK2

This parameter defines RAS to CAS delay. Switching MA lines from RAS to CAS Address always occurs in the middle of the delay. This parameter controls MA setup time to CAS, and MA hold time for RAS.

Separate CAS delay for read and write may be defined. This is possible because while paging write cycles are pipelined, the setup time for MA to CAS during a page hit is improved significantly compared to read cycles.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

c) RAS Active time on Reads - 4 to 16 HCLK2.

This parameter is determined by DRAM Specification of Read access time from RAS.

d) RAS Active time for Writes - 4 to 10 HCLK2.

This parameter is determined by DRAM minimum RAS width specification.

e) RAS precharge time - 2 to 8 HCLK2

f) CAS active time on reads - 2 to 8 HCLK2

Determined by DRAM specification of read access time from CAS.

g) CAS active time on writes - 2 to 4 HCLK2

Determined by DRAM specification of minimum CAS width and CAS data hold time on CAS.

h) CAS precharge - 1 or 2 HCLK2

i) Bus Recovery time - 0 , 1 or 2 HCLK2

This parameter affects to back to back CAS signals to alternate banks when interleaving is enabled. If there is no Recovery time specified the CAS signals will happen back to back while bursting. Specifying a Recovery time creates the inactive delay required for all CAS signals between consecutive dword fetches.

j) First burst read delay - 0 or 2 HCLK2

One more wait state will be inserted during the first cycle of a burst during a page hit on a read miss cycle. This parameter is determined by the DRAM Specification of address access time during a page hit.

k) CAS Hold on RAS - 2 or 4 HCLK2

Applies to CAS before RAS Refresh timing. Sets the delay between RAS being activated and CAS deactivated during the cycle.

Figure 2.37 and 2.38 illustrate basic RAS/CAS Read and Write Cycles with paging disabled. The differences are: WEN is not activated during a Read Cycle and the timing control parameters are from separate configuration registers. TRAR/TRAW parameters refer to RAS active time on Reads/ Writes (respectively), TCDR/TCDW to CAS delay on Reads/Writes, TCAR/TCAW to CAS active time on Reads/Writes, and TRP to RAS precharge.

Figure 2.34 illustrates the basic RAS/CAS Cycle with paging and no interleave. The TCP parameter refers to CAS precharge. BANKSELEV* (BANKSELODD) signals are stable throughout the cycle.

Figure 2.35 illustrates the basic RAS/CAS Cycle with Paging and 2-way Interleave. BANKSELEV* and BANKSELODD are stable throughout the cycle. The figure shows consecutive dwords accessed in an interleaved fashion with the HA2 Address line as the Interleave control. TBR refers to the Bus Recovery parameter described above.

Figure 2.36 illustrates the basic CAS/RAS cycle with Paging and 4-way Interleave. BANKSELEV* and BANKSELODD are controlling CAS activation. There is always at least one HCLK2 Setup and Hold time provided when switching CASEVN* and CASODD* between banks. The figure shows consecutive dwords accessed in an interleaved fashion with HA2/HA3 as the interleave controls.

Figure 2.39 illustrates the CAS before RAS Refresh Cycle. TCHR refers to minimum timing parameter of CAS Hold on RAS described above.

Figure 2.40 illustrates the RAS-only Refresh Cycle.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Co-Processor Interface

This module is independent of the rest of the HT322 Modules. It monitors three Numerical Co-processor Signals : PEREQ,BUSY,ERROR-387 and presents AT-compatible Numerical Co-processor Error Reporting. Three signals,PEREQ,BUSY,ERROR-386 are presented to the '386DX CPU. The IRQ13 line is activated to provide Error Status.

CLOCKSYNC.

This module generates internal clocks and resets for the HT322. It samples HRESCPU input in order to determine the phase of the HCLK2 to the '386 and sets the HT322 phase accordingly.

DRAM_DECODER.

The main purpose of this module is to generate an internal signal called DRAM_SPACE. This signal determines whether a cycle is targeted at the DRAM subsystem controlled by the HT322. It is exclusively resolved when HADS* is sampled as asserted. Two further internal signals generated by the module are CACHEABLE and EMS. These signals determine whether a cycle is to be cached and whether an EMS translation is required.

DATA_MUX.

This module provides multiplexing of the output data. The multiplexing occurs between data being read from configuration registers and data from the DRAM memory. The module also bridges data bytes during DMA cycles as required. (This occurs because the HT321 is a 16-bit device and it is the only source of DMA cycles). The bridging occurs between lower (HD0-15) and upper (HD16-31) data bits.

EMS_REMAPPER.

EMS_REMAPPER is an address translator which changes the current host's local bus addresses (HA lines) into physical DRAM subsystem addresses. These addresses reflect the remapping and EMS support schemes. Essentially, the DRAM subsystem is viewed as a contiguous memory. During remapping (if Remap function is enabled) the EMS_REMAPPER changes the host request at some high address above DRAM space to one of the EMS pages (16K memory chunks between 640KB and 1MB address space). For EMS support, an EMS page address is changed to a high memory (but existing in the DRAM subsystem) address according to an offset loaded by the user in the configuration registers.

LATCHES.

LATCHES is a set of data registers and address (HA and HBEN lines) latches for data written into the DRAM subsystem, and data latches for the data coming from the DRAM subsystem during read cycles. LATCHES implement the first stage of write buffering.

CONFIGURATIONS.

This module combines all configuration registers which provide the programmability of the chip set.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

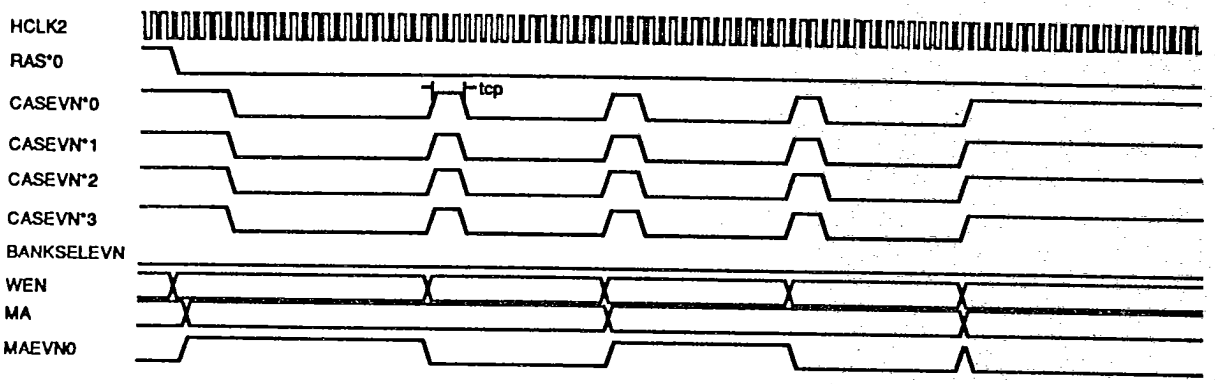


Figure 2.34 - RAS/CAS Cycle Page Mode On; No Interleave

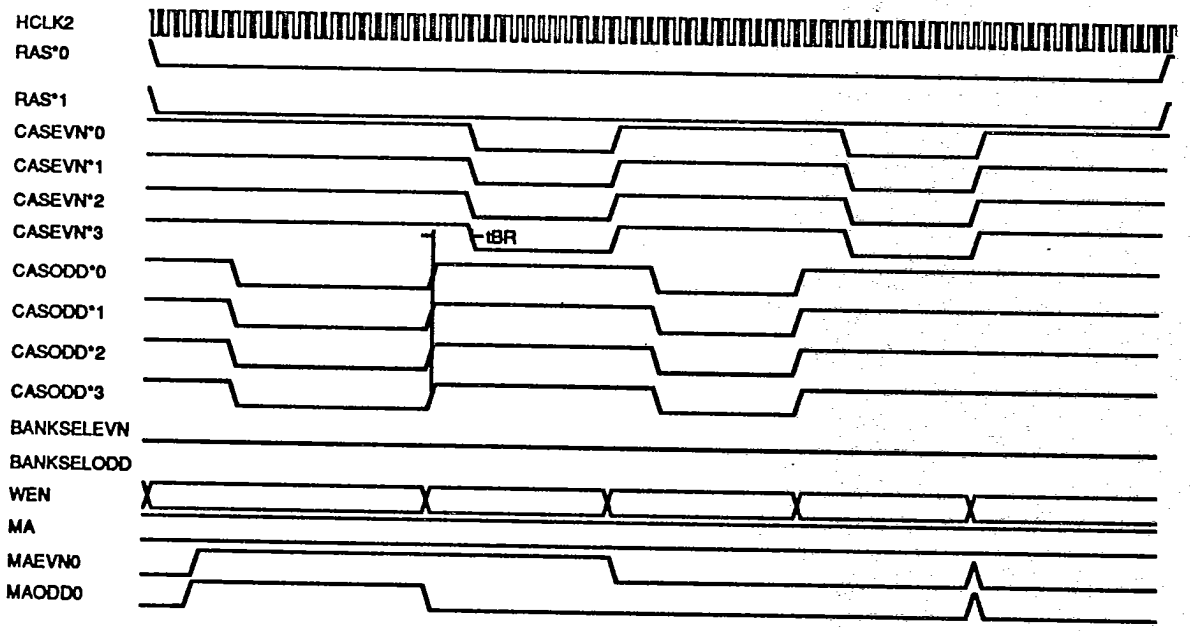


Figure 2.35 - RAS/CAS Cycle Page Mode On; Two-Way Interleave

Powered by ICminer.com Electronic-Library Service CopyRight 2003

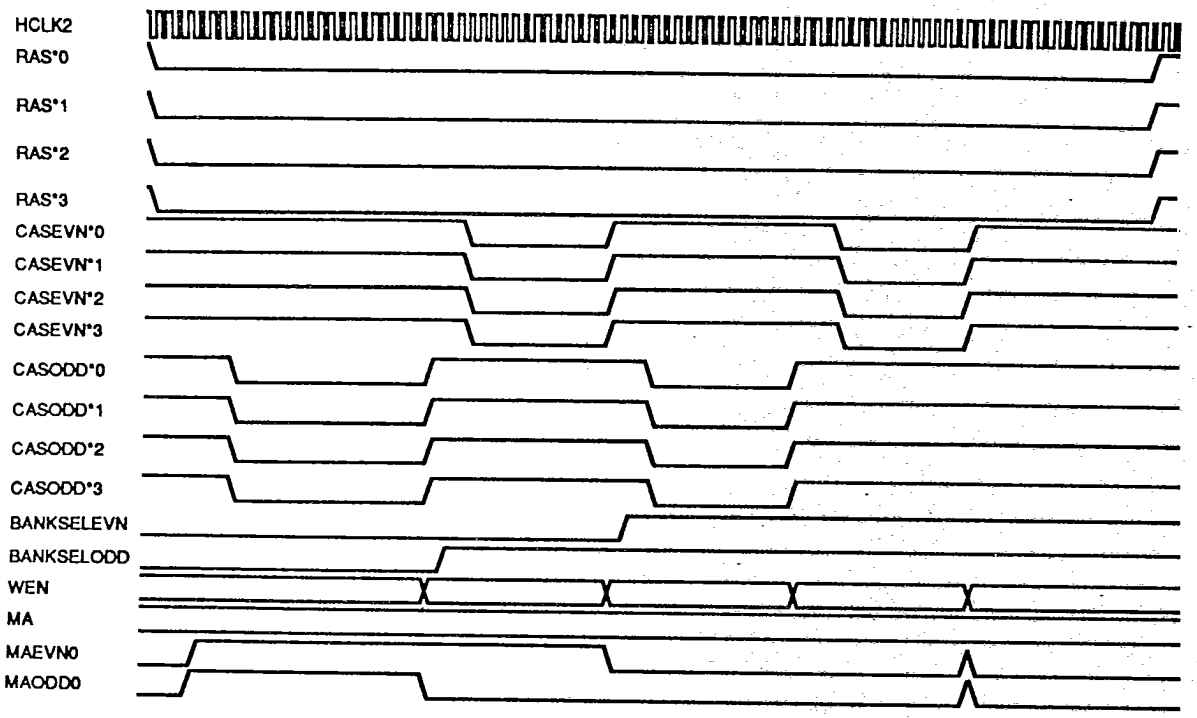


Figure 2.36 - RAS/CAS Cycle Page Mode On; 4-Way Interleave

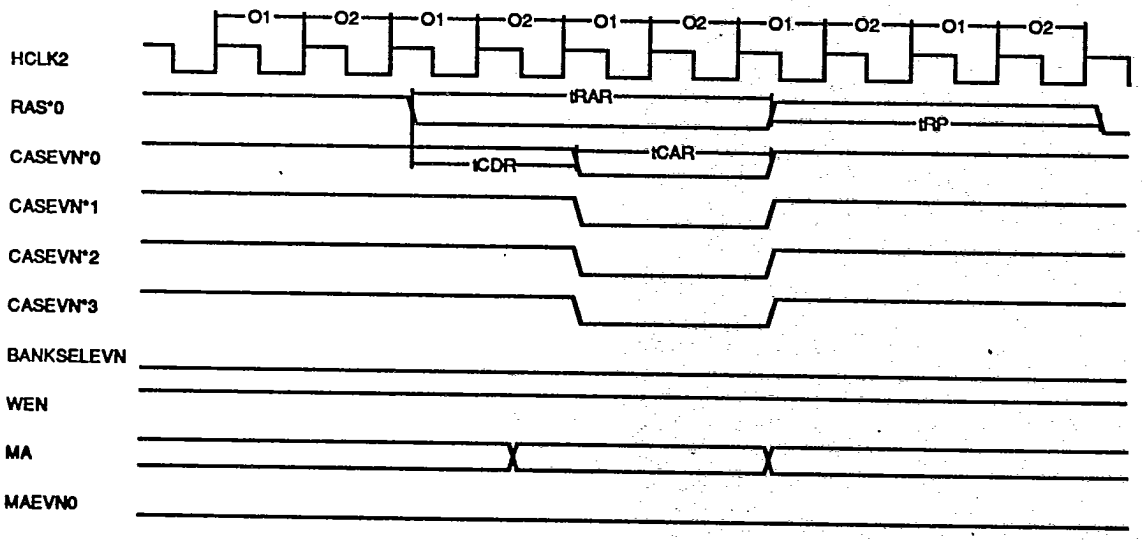


Figure 2.37 - RAS/CAS Read Cycle Page Mode Off

Powered by ICminer.com Electronic-Library Service CopyRight 2003

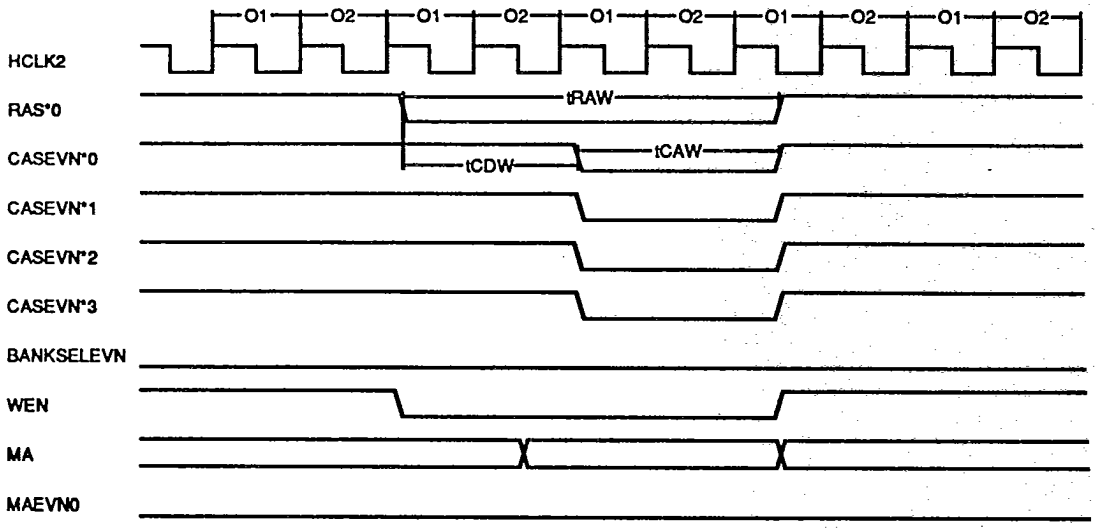


Figure 2.38 - RAS/CAS Write Cycle Page Mode Off

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT321 Register Descriptions

The HT321 chip has a total of 32 INDEX locations mapped into INDEX 00 - 1FH. Each of the Registers is Read/Write, but only the bits mentioned in this text should be programmed. All unused register bits should be left at default to maintain future compatibility.

The HT321 chip is also responsible for holding the current INDEX Pointer Value even when the Target Value is external to the HT321.Any access to I/O location 28H (CNFGASLO) are therefore terminated by the HT321. The data read at this location is made available to the CPU.

To program the INDEX registers, one must execute the following procedure:

i) Write I/O Location 28H with Value = INDEX (00 - 1FH for HT321 chip)

ii) Write to I/O Location 24H with Control Value for the selected INDEX

To Read INDEX registers, execute the following procedure:

i) I/O Write Location 28H with Value = INDEX (00 - 1FH for HT321 chip)

ii) I/O READ Location 24H - Control Value of selected INDEX is presented

To read the INDEX pointer value , one must execute the following procedure:

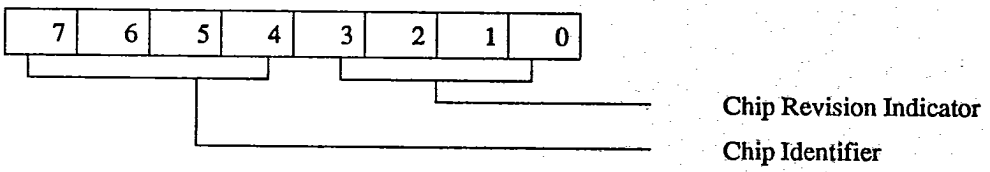
i) I/O READ Location 28H - INDEX ADDRESS (lower byte) presented

When an INDEX pointer is written to I/O location 28H, the pointer remains till another I/O write to 28H. This allows multiple DATA accesses at the INDEXed register .

At POR the INDEX pointer will default to INDEX 00H.

The remaining Indices are organized in the following fashion:

INDEX 00H: Chip/Revision Identifier, Read Only

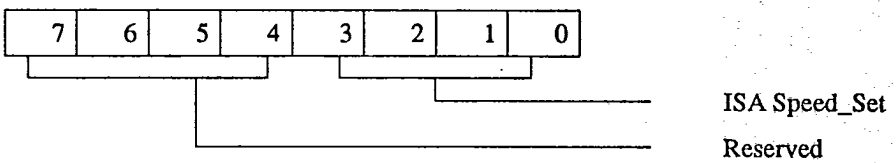


Bit(s)	Value	Meaning
3:0	0 - F	Chip Revision Indicator - (1 = Rev. 1)
7:4	0	Chip Identifier - (0 = HT321)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT321 Register Descriptions

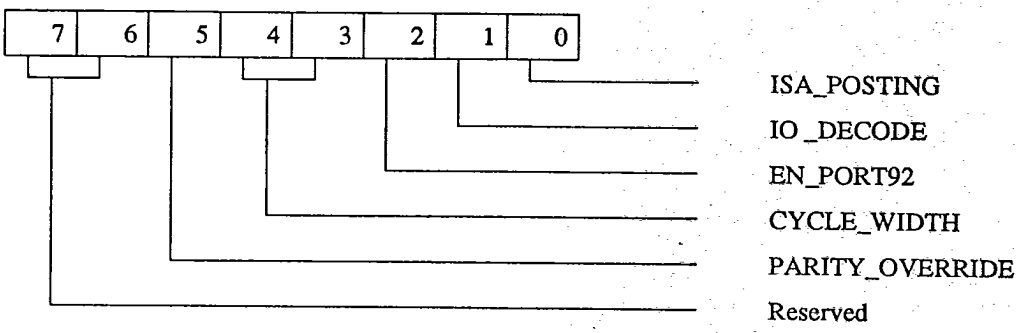
INDEX 01H: System Clocking (Reset State = 00H), R/W



Bit(s)	Value	Meaning
3:0	0000	
	0001	SYSTEM CLK frequency = 66MHz
	0010	
	0011	
	0100	SYSTEM CLK frequency = 50MHz
	0101	SYSTEM CLK frequency = 40MHz
	0110	SYSTEM CLK frequency = 33MHz
	0111	SYSTEM CLK frequency = 25MHz
	1000	SYSTEM CLK frequency = 20MHz
	1001	
	1010	
	1011	
	1100	Reserved, Do not Program
	1101	
	1110	
	1111	
7:4	0	Reserved, always program to 0

Powered by ICminer.com Electronic-Library Service CopyRight 2003

INDEX 02H: System Parameters (Reset State = 00H), R/W



Bit(s)	Value	Meaning
0	0	POSTED Backplane MEMW* cycles disabled
	1	POSTED Backplane MEMW* cycles enabled
1	0	10-Bit I/O decoding enabled
	1	16-Bit I/O decoding enabled
2	0	PORT 92 Functionality disabled
	1	PORT 92 Functionality enabled
4:3	0 0	Backplane Cycle Time = 6 BCLK's
	0 1	Backplane Cycle Time = 5 BCLK's
	1 0	Backplane Cycle Time = 4 BCLK's
	1 1	Backplane Cycle Time = 3 BCLK's
5	0	Parity Error Override OFF
	1	Parity Error Override ON
7:6	0 0	Reserved. Always program to 0

Posted Backplane Memory Writes:

The HT321 is capable of posting Memory Writes to the Backplane. The Feature is enabled by a configuration bit called ISA_POSTING (active high). When Enabled, any memory write access to the backplane will be terminated using the HRDY* signal as early as possible. At this point the CPU may continue while the Backplane Memory Write Cycle is executed by the HT321. Any number of non-ISA cycles can be performed while the backplane sequencer completes the Posted Cycle.

IO_DECODE:

The HT321 by default,decodes Address [9:0] for internal I/O regions. The user has the option of enabling 16-bits of I/O decode, meaning that the HT321 will use Address [15:0] to decode internal I/O regions.

PORT_92:

PORT_92 functions of the HT321 may be used by enabling this feature by setting bit 2 of this register.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

CYCLE_TIME:

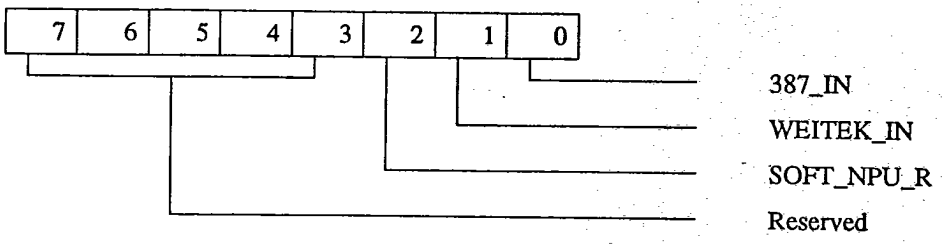
The AT standard time for ISA Backplane Cycles is 6 BCLK's duration. The user has the option of changing this default setting via this register. For non-standard applications, ISA Backplane Cycle Times can be reduced to a minimum of 3 BCLK's duration. For all of these settings, IOCHRDY, 0WS*, MEMCS16* and IOCS16* operate normally.

PARITY_OVERRIDE:

This bit provides a method of shutting off the Parity Detection Circuit of the HT321. With this bit set, Parity Errors flagged by the PARITY* signal asserted low are not passed to the NMI circuitry.(See I/O PORT B Function Bit 2)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

INDEX 04H: Co-Processor (Reset State = 00H), R/W



Bit(s)	Value	Meaning
0	0	80387 Co-Processor not installed
	1	80387 Co-Processor installed
1	0	Weitek Co-Processor not installed
	1	Weitek Co-Processor installed
2	0	Software Co-Processor RESET not blocked(1)
	1	Software Co-Processor RESET blocked(1)
7:3	0	Reserved. Always program to 0

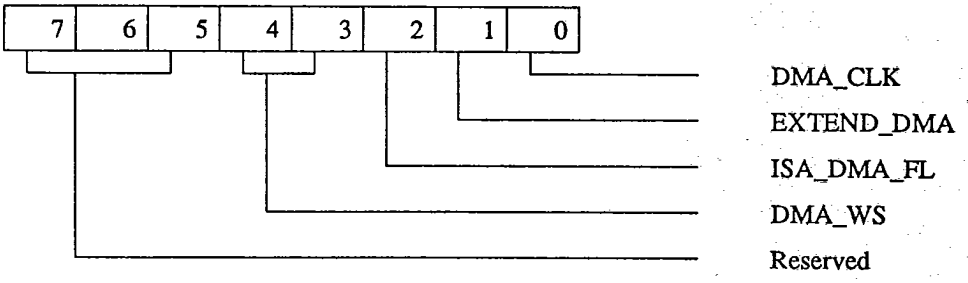
(1)**Software Co-Processor RESET is defined as:**

IOW* Command to I/O location 0F1H, DATA = xx(No Valid Data)
- if blocked, this Command will not result in a RESET387 from the HT321
- if **not** blocked, this command will produce a pulse of the RESET387(P51).

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

INDEX 06H: DMA (Reset State = 00H), R/W



Bit(s)	Value	Meaning
0	0	DMA Clock = BCLK divided by 2
	1	DMA Clock = BCLK inverted
1	0	Extended DMA Page Registers Disabled
	1	Extended DMA Page Registers Enabled
2	0	DMA FLOW_THRU Mode Disabled
	1	DMA FLOW_THRU Mode Enabled ****
4:3	0 0	DMA Wait states = 3
	0 1	DMA Wait states = 2
	1 0	DMA Wait states = 1
	1 1	DMA Wait states = 0
7:5	0	Reserved. Always program to 0

****** NOTE: You must also program the HT322 INDEX 2BH for this Option before use.**

DMA_CLK:

This bit selects the clock frequency presented to the internal 8237 equivalents. The selection is either BCLK inverted or BCLK divided by two.

EXTEND_DMA:

For systems requiring use of the extended DMA page registers (I/O 480 - 48FH), this bit is used to enable use of these registers.

ISA_DMA_FLOW_THRU:

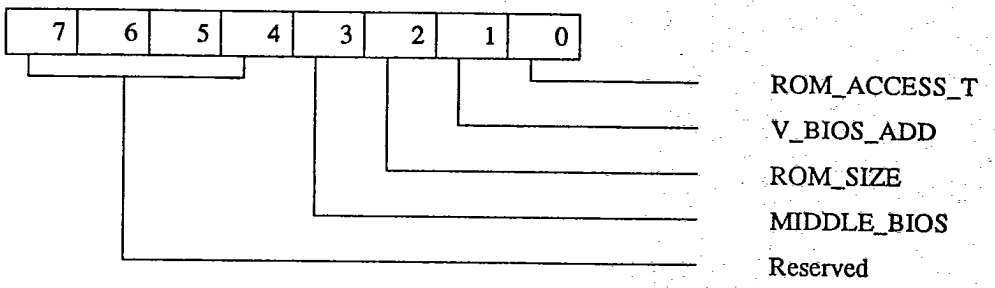
This feature should be enabled for systems that have a "WRITE BUFFER" as part of their memory controller circuitry. The HT322 is one such device. Essentially, with this bit enabled, a handshake mechanism is used to determine when the WRITE BUFFER is empty and DMA cycles can proceed. Once HLDA is issued by the CPU, the HT321 will hold off issuing HLDA to its internal circuits until HRDY* is sampled true. This HRDY* is a signal from the Local Bus (HT322) that indicates the WRITE BUFFER is empty and its presence in the system pipeline has been by-passed.

DMA_WS:

This bit controls the number of DMA_CLK's inserted into the standard DMA cycle controlled by the integral DMA Controller of the HT321 .

Powered by ICminer.com Electronic-Library Service CopyRight 2003

INDEX 07H: EPROM (Reset State = 00H) R/W



Bit(s)	Value	Meaning
0	0	250 nSec ROM Output Enable pulse duration
	1	125 nSec ROM Output Enable pulse duration
1	0	Video BIOS separate from System BIOS
	1	Video BIOS together with System BIOS in same physical device
2	0	ROM size = 64K
	1	ROM size = 128K
3	0	Middle BIOS region of 64K space (below 16 Mb) Disabled
	1	Middle BIOS region of 64K space (below 16 Mb) Enabled
7:4	0	Reserved. Always program to 0

Note:
The data width of the ROM is selected externally via the CLAMPA20* pin. During POR, this pin is read by the HT321. To configure the system for an 8-bit wide BIOS ROM, this pin should be pulled high via an external resistor. To configure the system for a 16-bit wide BIOS ROM, the CLAMPA20* pin should be pulled low via an external resistor.

"HOLES" in HT321 Map

In the HTK320 architecture, the HT321 is usually the default device. There may be some local devices, however, that do not conform to the HLOCAL* type of handshaking mechanism but still can operate on the local bus. For these devices, the HT321 must not start or terminate a cycle or else contention is sure to occur. For these devices, the HT321 has pre-programmed I/O and MEMORY "regions" for which the HT321 will not respond to the cycle. There are two I/O and three MEMORY regions available.

The I/O regions are a minimum of 16 bytes in size and also must be a multiple of 16-bytes. To program the I/O "holes", first set the range of addresses to be exempted via the "I/O HOLE-A(B) LOW ADDRESS" and "I/O HOLE-A(B) HIGH ADDRESS" registers. The "LOW ADDRESS" will contain the starting address of the I/O hole, whereas the "HIGH ADDRESS" should be programmed to the top of hole desired +1. For example, to set an I/O hole between location 320H - 32FH, program the "LOW ADDRESS" register with "32H" and the "HIGH ADDRESS" register with "33H". To enable this newly programmed hole, set the corresponding bit in INDEX 08 of the HT321 configuration register.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT321 Register Descriptions

The MEMORY hole regions are decoded somewhat differently. Firstly, these regions are multiples of 16K chunks, with 16K being the smallest chunk available. MEM_HOLE_A is a fixed-size hole equal to 16K in size. It can be positioned anywhere in the SUMMIT-DX memory space. Simply program the address via the

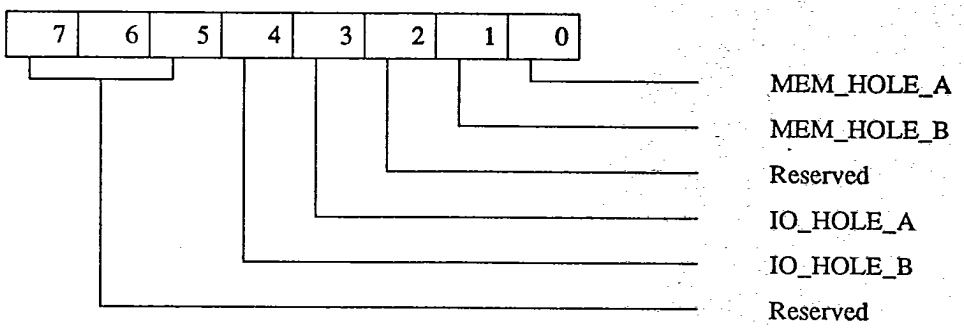
MEM_HOLE_A ADDRESS, LOWER (Address 21:14)

MEM_HOLE_A ADDRESS, UPPER (Address 27:22) registers.

MEM_HOLE_B has no size restriction and is programmed similar to the I/O hole programming described earlier. Again, the "END ADDRESS" should be top of desired hole range +1.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

INDEX 08h: I/O and MEMORY MAP HOLES (Reset State = 00H), R/W



Bit(s)	Value	Meaning
0	0	Memory Map Hole-A Disabled
	1	Memory Map Hole-A Enabled
1	0	Memory Map Hole-B Disabled
	1	Memory Map Hole-B Enabled
2	0	Reserved. Always program to 0
3	0	I/O Map Hole-A Disabled
	1	I/O Map Hole-A Enabled
4	0	I/O Map Hole-B Disabled
	1	I/O Map Hole-B Enabled
7:5	0	Reserved. Always program to 0

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

INDEX 10H: I/O HOLE-A LOW ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Start Address of I/O HOLE-A (Address 11 DOWN to 4)

INDEX 11H: I/O HOLE-A HIGH ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	End Address of I/O HOLE-A (Address 11 DOWN to 4)

INDEX 12H: I/O HOLE-B LOW ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Start Address of I/O HOLE-B (Address 11 DOWN to 4)

INDEX 13H: I/O HOLE-B HIGH ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	End Address of I/O HOLE-B (Address 11 DOWN to 4)

INDEX 16H: MEM HOLE-A ADDRESS, LOWER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Address of MEM HOLE-A (Address 21 DOWN to 14)

INDEX 17H: MEM HOLE-A ADDRESS, UPPER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
5:0	00-3F	Address of MEM HOLE-A (Address 27 DOWN TO 22)
7:6	0	Reserved. Always program to 0

Powered by ICminer.com Electronic-Library Service CopyRight 2003

INDEX 19H: MEM HOLE-B START ADDRESS, LOWER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Address of MEM HOLE-B Start (Address 21 DOWN to 14)

INDEX 1AH: MEM HOLE-B START ADDRESS, UPPER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
5:0	00-3F	Address of MEM HOLE-B Start (Address 27 DOWN to 22)
7:6	0	Reserved. Always program to 0

INDEX 1CH: MEM HOLE-B END ADDRESS, LOWER (Reset State = 00h), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Address of MEM HOLE-B End (Address 21 DOWN to 14)

INDEX 1DH: MEM HOLE-B END ADDRESS, UPPER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
5:0	00-3F	Address of MEM HOLE-B End (Address 27 DOWN to 22)
7:6	0	Reserved. Always program to 0

Powered by ICminer.com Electronic-Library Service CopyRight 2003

PC AT-Compatible Registers

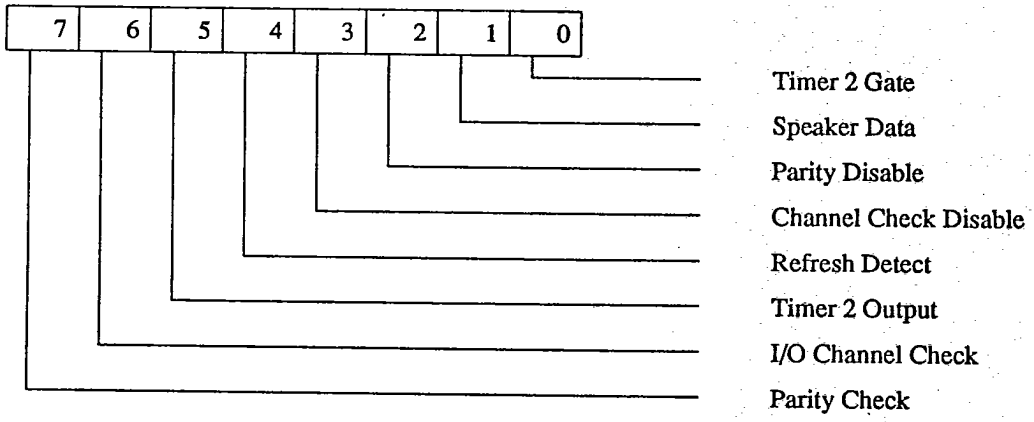
The HT321 has a number of AT-compatible internal registers in order to minimize external circuitry. These include PORT_B, NMI Mask Register, PORT_92 and all the internal Megafunction registers within the 8237's, 8259's and 8254 functions. These registers and their bit definitions are shown below.

Keyboard Controller Interface 0060H, 0062H, 0064H R/W

The HT321 requires an external 8042 equivalent to process keyboard operations. The clock for the 8042 may be derived from BCLK or separate OSC circuit and should have a frequency that is between 6 MHz and 10 MHz when used with standard keyboard controllers.

The 8042 interfaces with the HT321 through OPTBUFUL (IRQ1) and a chip select line KBCS*. The 8042 also provides two output signals: KB_CLAMPA20*(P166) and RC(P77 Reset CPU). These signals are brought into the HT321 and combined internally with Alternate Port 92 FAST GATEA20 and FAST CPU RESET (FAST_RC) functions respectively.

I/0 Port 61H Port B 0061H R/W



This port controls several system level functions.

Bit(s)	Value	Meaning
0		Timer 2 Gate (read/write). This bit controls operation of timer channel 2. 0 = channel 2 timer operation is disabled (default). 1 = channel 2 timer operation is enabled.
1		Speaker Data (read/write). This bit gates the output of channel 2 of the timer/counter. 0 = output is disabled (default). 1 = output is enabled.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

2 Parity Disable (read/write). This bit is used to disable parity error initiation of NMI. This bit is logically ORed with Parity OVERRIDE Option bit 5 of INDEX 02. By this method, System Parity Detect is disabled if this bit (PARITY OVERRIDE) Bit 5 of INDEX 02 is set to a logical 1.

0 = PARITY* sampling is enabled (default).
1 = PARITY* sampling is disabled.

3 Channel Check Disable (read/write). This bit disables NMI generation for Channel Check Errors.

0 = enables IOCHK* sampling (default).
1 = disables IOCHK* sampling.

4 Refresh Detect (read only). This bit toggles for each refresh cycle.

5 Timer 2 Out (read only). This bit returns the state of the Timer 2 output.

6 IOPCHK I/O Channel Check (read only). This bit indicates an I/O Channel Check has occurred (usually a parity error) on the System I/O Channel.

0 = no error occurred.
1 = an error occurred.

7 PCHK Parity Check (read only). This bit indicates a Parity Error has occurred on the local memory.

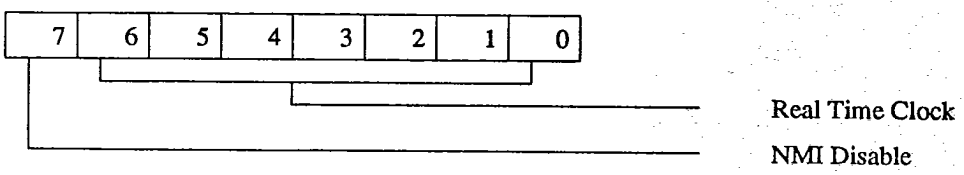
0 = no error occurred.
1 = an error occurred.

IOPCHK and PCHK are derived in the following manner. If IOCHK* is active (low) and IOCHK* sampling is enabled (PORT_B, bit 3 = 0), then IOPCHK is driven high and remains there until IOCHK* sampling is disabled (PORT_B, bit 3 =1) or RESET occurs. The PCHK signal (active high) is used to indicate that a DRAM parity error has occurred on the motherboard. The PARITY* signal, from another device (normally HT322) on the local bus, is sampled on every clock edge. If detected low on a rising HCLK2 edge and if RAM parity checking is enabled (PORT_B, bit 2 = 0), then PCHK is driven high. PCHK remains high until the RAM parity checking bit is disabled (PORT_B, bit 2 = 1) or RESET occurs.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

I/O Port **70H** **RTC Index and NMI Mask** **0070H** **W**



RTC/CMOS Index and NMI mask - This register is used to access the RTC and its CMOS RAM.

Bit 7 is an NMI Mask bit used to mask NMIs from accessing the CPU. Bits[6:0] would be used by external RTC chip. The NMI output is active high and must be enabled before it can become active. NMI defaults on power-up to disabled. Once enabled, NMI equals the OR of the PCHK and IOPCHK signals.

Bit(s)	Value	Meaning
6:0		RTC Index[6:0]. These bits are used as index pointers for external real-time clock.
7		NMI Disable (write only). This bit controls the generation of NMIs. 0 = enables generation of NMIs (default). 1 = disables the generation of NMIs.

PORT_92:

Access to PORT_92 is only enabled when the EN_P92 bit (INDEX 02H, bit 2) is set.

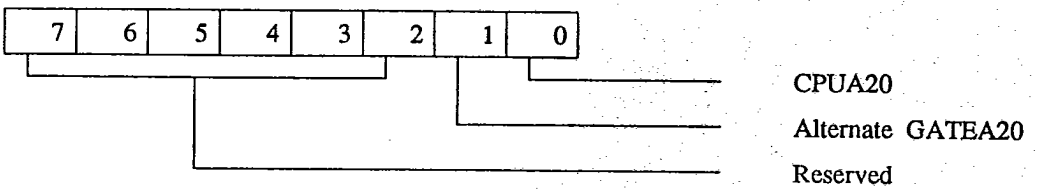
This PORT is located at I/O location 92H in the system address map and defaults on power-up to 00h. Two features of the PORT_92 functionality are implemented in the HT321. These are FAST_RC and Alternate GATEA20*. Bit 0 of this register enables the FAST_RC circuitry , whereas Bit 1 of this register holds the value of Alternate GATEA20*.

The Alternate GATEA20* output is directly connected to Bit 1# of the PORT_92 register. If a "1" is written to Bit 1 of PORT_92, then the CLAMPA20* output will go low. It will remain low until Bit 1 is changed by an IOW* to PORT_92 again.

FAST_RC provides a faster RESET of the CPU compared to the RC signal from the Keyboard Controller. To activate this Reset pulse, a one should be written into Bit 0 of PORT_92. When this is done, a pulse of 125 - 150 ns duration will be generated 6.72 uS after the trailing edge of the IOW* Command that programmed Bit 0 of this port. Only one pulse will be generated. To generate another FAST_RC pulse, Bit 0 of PORT_92 must first be reset to 0, then programmed to 1 again.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

I/O Port 92H System Control Port 0092H R/W Reset State = 00H



This register is used as a fast alternate to Gate A20 and/or Reset the CPU rather than using the 8042 Keyboard Controller. This register is compatible with IBM PS/2 architecture.

Bit(s)	Value	Meaning
0		Alternate CPU RESET (FAST_RC). 0 to 1 transition = a reset pulse is provided on the RESETCPU pin to reset the CPU 6.72 usec later. After activation of a CPU reset, the status is maintained so the BIOS may determine that the reset was caused by a programmed CPU RESET condition.
1		Alternate GATEA20. 1 = CLAMPA20* is forced low (real mode). 0 = Address bit HA20 (on the local bus) should be treated as normal.
7:2		Reserved.

Internal DMA Controller Registers

This section describes the registers used during DMA functions.

Current Address Register 0000, 02, 04, 06 00C0, C6, CA, 00CEH R/W

Each DMA channel has a 16-bit current address register that holds the address used during transfers. Each Channel can be programmed to increment or decrement this register for each transfer completed. This register can be read or written by the CPU as consecutive 8-bit bytes. If Auto-Initialization is selected, this register is reloaded from the Base Address Register upon reaching Terminal Count in the Current Word Count Register. Channel 0 increment or decrement may be disabled by setting the Address Hold Bit in the Command Register.

Current Word Count Register 0001,03,05,07,00C4,C8,CC,CE,00CFH R/W

Each channel has a Current Word Count Register the Value of which determines the number of transfers to execute. The actual number of transfers performed is one greater than the value programmed into the register. A register is decremented after each transfer until it transitions from 0000H to FFFFh. When this roll-over occurs, the HT321 generates T/C(P85), suspends operation for that Channel, sets the appropriate Request Mask Bit or re-loads because of Auto-Initialize and continues.

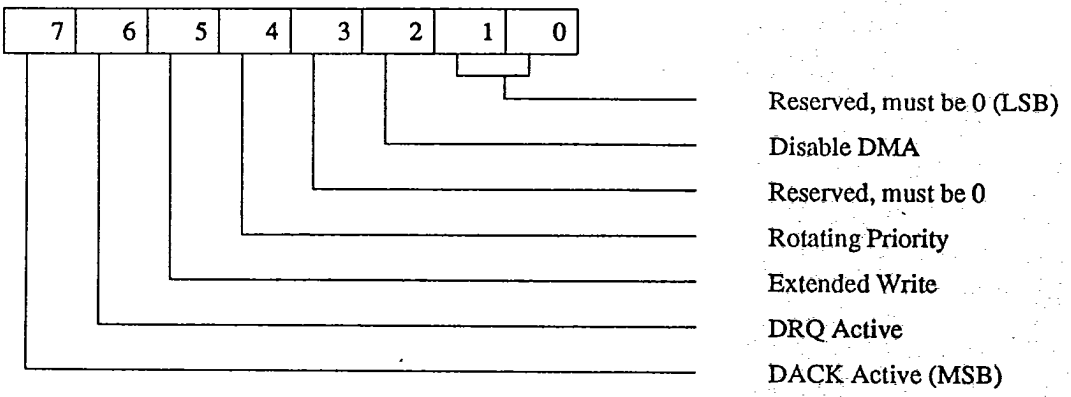
Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. This register's Value is loaded into the Current Word Count Register during Auto-Initialization.

Command Status Register 0008, 00D0H R/W



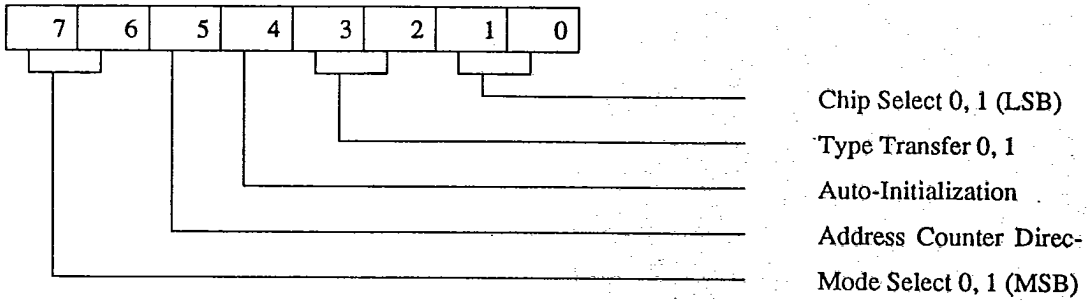
This register controls the overall operation of a DMA subsystem. The register can be Read or Written by the CPU and is cleared by either a POR or a Master Clear command.

Bit(s)	Meaning
1:0	Reserved, must be 0.
2	Disable DMA: Bit 2 is the master disable of the DMA controller. Writing a "1" to this location disables the DMA subsystem (DMA1 or DMA2). This is normally used to prevent DMA cycles from occurring when the CPU needs to reprogram one of the Channels.
3	Reserved, must be 0.
4	Rotating Priority: Writing a "1" to bit 4 causes the HT321 to utilize a Rotating Priority scheme for honoring DMA requests. The default mode is Fixed Priority.
5	Extended Write is enabled by writing a one to bit 5, causing the write commands to be asserted one DMA Clock early during a transfer. The Read and Write commands both begin in state S2 when enabled.
6	DRQ active level is determined by bit 6. Writing a one in this bit position causes DRQ to become active low.Default is active high.
7	DACK active level is determined by bit 7. Programming a one in this bit position makes DACK an active high signal.Default is active low.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Mode Register **000BH, 00D6H** **R/W**



Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of a Write Command to the Mode Register determine which Channel's Mode Register is accessed. The remaining six bits control the Mode of the Selected Channel. Each Channel Mode Register may be read by a sequential Reads to the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point.

During mode read operation, bits 0 and 1 are one.

Bit(s) Value Meaning

1:0 Channel Select 1, 0: Bits 1 and 0 determine which channel's Mode Register is written to. Read back of a mode register results in bits 1 and 0 both being ones.

CS1	CS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

3:2 Transfer Type 1, 0: Bits 3 and 2 control the type of transfer that is to be performed.

T1	T0	
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Don't use

4 Auto-Initialization function is enabled by writing a "1" in bit 4 of the Mode Register.

5 Address Counter Direction: Determines progression of Address count. A "1" in bit 5 decrements the address after each transfer.

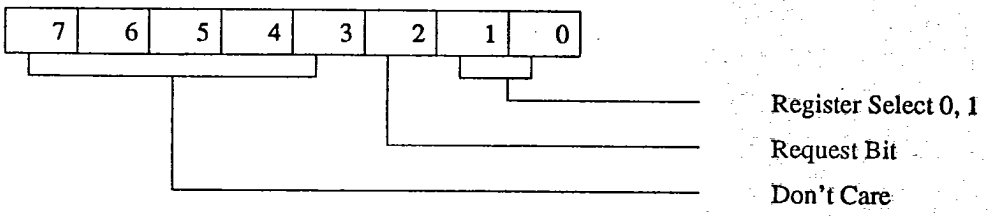
7:6 Mode Select 1, 0 for each channel is accomplished by bits 7 and 6.

M1	M0	
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Request Register **0009H, 00D2H** **W**



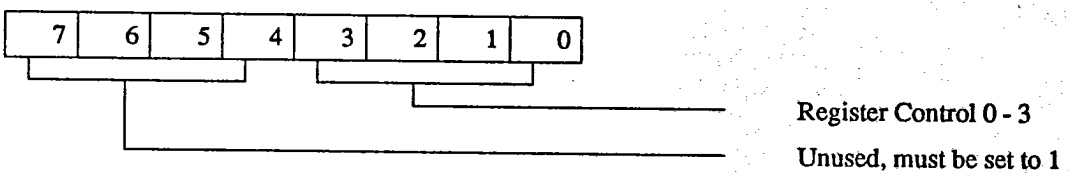
This is a 4-bit Read,3-bit Write Register used to initiate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Request Mask has no effect on software generated requests. All request bits are cleared to zero by a RESET.

Bit(s)	Value	Meaning
1:0		Register Select 0, 1: Bits 1 and 0 determine which channel's Request Register is written to.

RS1	RS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

2		A Channel's Request Bit is set by writing a "1" to bit 2.

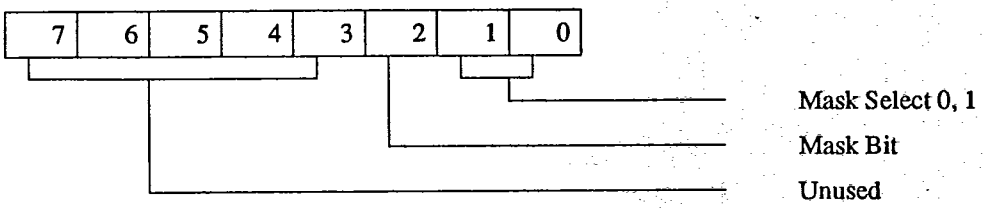
Request Register **0009H, 0002H** **R**



Bit(s)	Value	Meaning
3:0		During a Request Register Read, the state of the request bit associated with each Channel is returned in bits 3 through 0 of the byte. The bit position corresponds to the Channel Number.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Single Bit Mask Register **000AH, 00D4H**



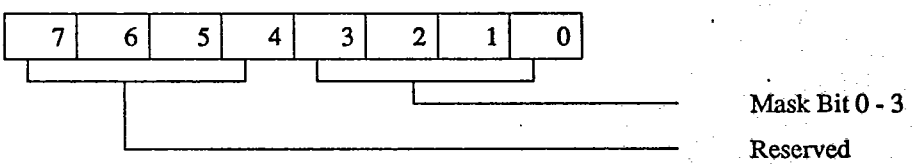
Each channel may be independently masked by Writing to the Single Mask Bit location. The operation of this register is explained below.

Bit(s)	Value	Meaning
1:0		Mask Select 1, 0 - These two bits select the specific Channel Mask Bit to be set or reset.

MS1	MS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

2 Mask Bit sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a "1" to this bit position sets the mask, inhibiting external requests.

Write All Mask Register Bit **000FH, 00DEH** **R/W**



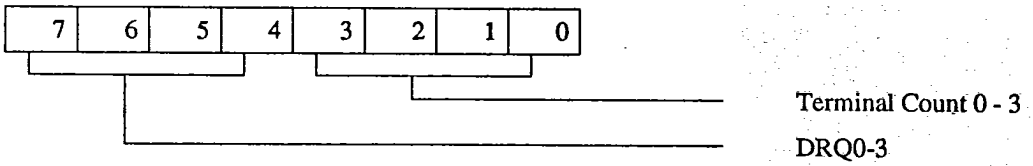
The Write All Mask Register has four active bits that are used to inhibit transfer cycles occurring from external DMA requests. All four mask bits may be programmed in one operation by Writing to the Write All Mask Bit I/O Address. The data format for this function is shown below.

Mask Bits 3 - 0: Each bit position in the field represents the mask bit of the Corresponding Channel. All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits are set , if Auto-Initialize is disabled,when Terminal Count is reached. The entire register can be cleared, enabling all four channels, by executing a Clear Mask Register Operation.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Status Register 0008H, 00D0H R



The status of all four channels can be determined by Reading the Status Register. Information available indicates if a Channel has reached Terminal Count and whether an external service request is pending(DRQ). Bits 3 - 0 of this Register are cleared by a POR Reset, a Master Clear, or each time a Status Read takes place. Bits 7 - 4 are cleared by a POR Reset, a Master Clear, or the removal of the request pending. Bits 7 - 4 are not affected by the state of the Mask Register Bits. The Channel Number correlates to the bit position (Bit7:4=C3:C0 and Bit3:0=C3:C0).

Special Commands

Five Special Commands are provided to make programming the device easier. These commands are activated by access to a Specific I/O Address by assertion of either an IOR* or IOW*. Information on the data lines is ignored by the HT321 whenever an IOW* activated Special Command is issued. Data returned by IOR* activated Special Command is invalid. Descriptions of the five Special Commands follow:

Clear Byte Pointer Flip-Flop - This Command is normally executed prior to reading or writing of the Address or Word Count Register. It initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

Set Byte Pointer Flip-Flop - Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an Address or Word Count Register.

Master Clear - This Command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flops are cleared and the Request Mask Register is Set. Immediately following Master Clear or RESET, the DMA Controller is in the Idle Mode.

Clear Request Mask Register - This command enables all four DMA Channels to accept Requests(DRQx's) by clearing the Mask bits in the Register.

Clear Mode Register Counter - In order to allow access to four Mode Registers using one I/O Address, an additional counter is used. After clearing the counter, all four Mode Registers may be read (Channel 0 first and Channel 3 last)by executing successive Reads at the Read Mode Register Address.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

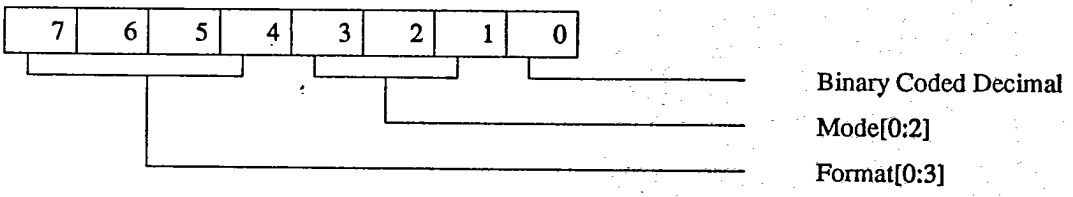
Programmable Interval Timer Registers

After power-up, the condition of PIT Control Registers, counter registers, CE and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written to by writing to the Control Word address (see the following table). The Control Word is a write-only location.

I/O ADDR	Function
040H	Counter 0 (Read/Write)
041H	Counter 1 (Read/Write)
042H	Counter 2 (Read/Write)
043H	Counter Control (Write)

Counter Control Register **(043H Write Only)**



Format[3:0] Bits[7:4] determine the command to be performed as shown in the PIT Command Table.

Mode[2:0] Bits[3:1] determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command Table) or select the counter during a Read-Back Command (see ReadBack Command). Bits[3:1] become "don't care" during Latch Counter Commands.

Binary Coded Decimal - Bit 0 selects Count Format during Read/Write Counter Commands. Where bit 0 is set to zero, the count is binary, when bit 0 is set to "1", the count is Binary Coded Decimal. Note that during Read-Back Command this bit must be zero.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Read/Write Counter Command

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (Counter Latch Command)
1	0	0	1	Read/Write Counter 2 LSB Only

Command Table

When writing to a counter, two conventions must be observed:

Each counter's Control Word must be written before the initial count is written.

Writing the initial count must follow the format specified in the Control Word (Least Significant Byte only Most Significant Byte only, or Least Significant Byte, then Most Significant Byte).

MSB = Most Significant Byte
LSB = Least Significant Byte

A new initial count can be Written to a Counter any time after programming without rewriting the Control Word, as long as the Programmed Format is observed.

During Read/Write Counter Commands M[2:0] are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
x	1	0	Select Mode 2
x	1	1	Select Mode 3
1	1	0	Select Mode 4

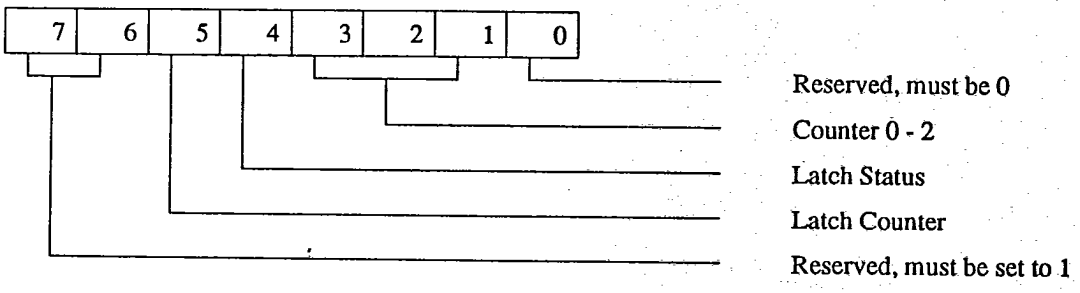
Powered by ICminer.com Electronic-Library Service CopyRight 2003

Latch Counter Command

When a Latch Counter Command is issued, the counter's output latches (COL and COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first Counter to which the Command was issued. Also, multiple Latch Counter Commands issued to the same counter are ignored. The Count Read will be the Count at the time the first Latch Counter Command was issued.

Read-Back Command



The Read-Back Command allows the user to check the Count Value, Mode and State of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

Latch Counter[LC] - Writing a zero in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

Latch Status[LS] - Writing a zero in bit 4 causes the selected counter(s) to latch the current condition of its Control Register, Null Count and Output into the Status Register. The next read of the Counter results in the contents of the Status Register being read (see Status Byte read).

Counter[2:0] - Writing a one in bit 3 causes Counter 2 to latch one or both of the registers specified by Latch Counter and Latch Status. The same is true for bits 2 and 1, except that they latch Counters 1 and 0 respectively.

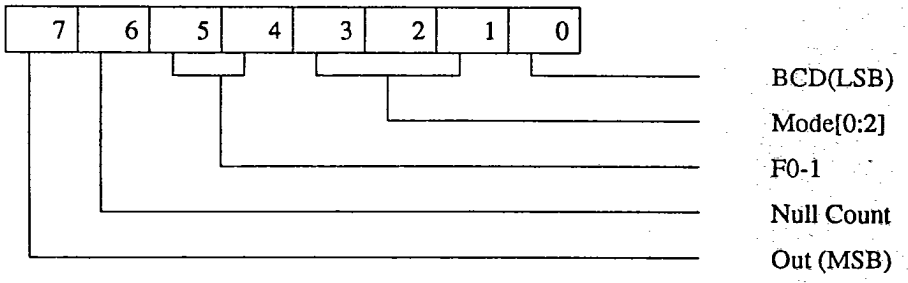
Each counter's latches remain latched until either the latch is Read or the Counter is reprogrammed.

If LS = LC = 0, Status is returned on the next Read from the Counter. The next one or two Reads (depending on whether the Counter is programmed to transfer one or two bytes) from the Counter result in the Count being returned.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Status Byte



OUT - Bit 7 contains the State of the OUT signal of the Counter.

Null Count - Bit 6 contains the Null Count Flag. This Flag is used to indicate that the contents of the CE are valid. Null Count is set to a "1" during a Write to the Control Register or the Counter. It is cleared to a zero whenever the Counter is loaded from the counter input registers.

F[1:0] Bits[5:4] contain the F1 and F0 Command bits, which were written to the Command Register of the counter during initialization. This information is useful when determining whether the high byte, the low byte, or both must be transferred during counter read/write operations.

Mode[2:0] - These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD - Bit 0=1 Indicates the CE is operating in BCD format.

Interrupt Controller Registers

Initialization Command Words

The initialization process consists of writing a sequence of four bytes to each Interrupt Controller(PIC1, PIC2). The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H/0A0H with a "1" in bit 4 of the Data Byte. The Interrupt Controller interprets this as the start of the initialization sequence and does the following:

1 The Initialization Command Word Counter is reset to zero.
2 ICW1 is latched into the device.
3 Fixed Priority Mode is selected.
4 IR7 is assigned the highest priority.
5 The Interrupt Mask Register is cleared.
6 The Slave Mode Address is set to seven.
7 Special Mask Mode is disabled.
8 The IRR is selected for Status Read operations.

The next three I/O Writes to address 021H/0A1H will load ICW2-ICW4. See table below for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all four bytes must be written for the controller to be properly initialized) by writing to address 020H/0A0H with a zero in data bit 4. Note, this causes OCW2 or OCW3 to be written dependant upon how many Writes have occurred.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Initialization Sequence

START

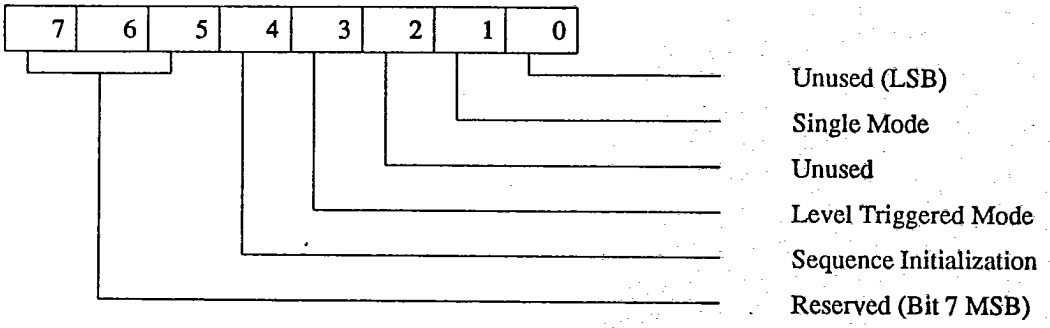
Write ICW1 A0 = 0 D4 = 1
Write ICW2 A0 = 1

Check CASCADE Mode?

YES - Write ICW3 A0 = 1
NO - Optionally Write ICW4

END OF INITIALIZATION Controller Ready

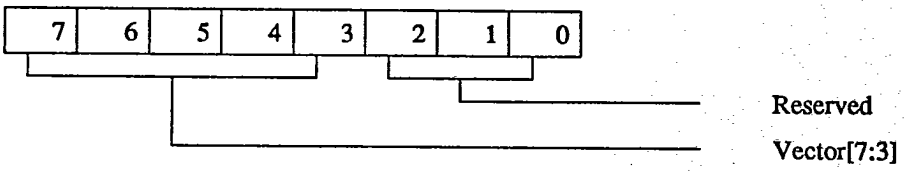
ICW1 **(Address 020h / 0A0h)** **Write Only**



Sequence Initialization - Bit 4 indicates to the Interrupt Controller that an Initialization Sequence is starting and must be a "1" to Write ICW1.

Level Triggered Mode[LTM] - Bit 3 selects level or edge triggered inputs to the IRR. If a "1" is Written to LTM, a high level on the IRR input generates an interrupt request. The IRQ must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector is generated if the IRR input is de-asserted too early), and the IRQ must be removed prior to EOI to prevent a second interrupt from occurring.

ICW2 **(Address 021H / 0A1H Write Only)**

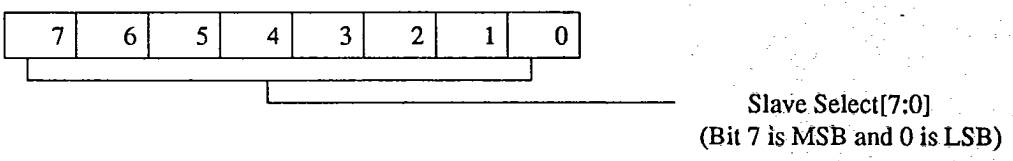


Vector[7:3]: These bits are the upper five bits of the Interrupt Vector and are programmable by the CPU. The lower three bits of the Vector are generated by the Priority Resolver during INTA. PIC1 and PIC2 need not be programmed with the same value of ICW2.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

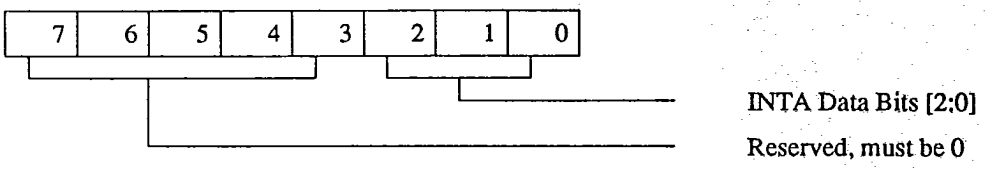
T-49-17-15

ICW3 Format for PIC1 **(Address 021H Write Only)**



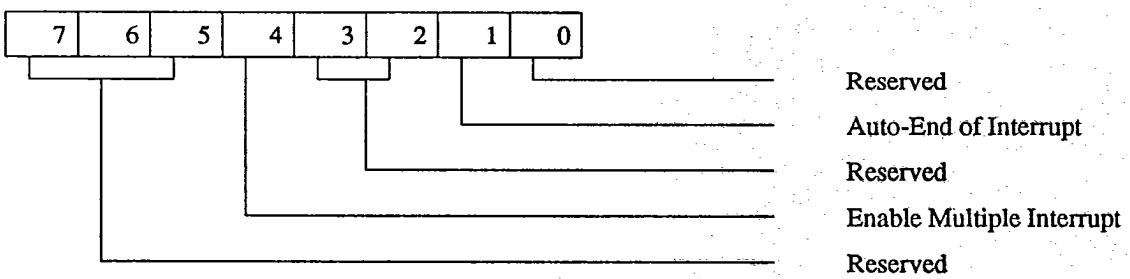
Slave Select[7:0]: Select which IR inputs have Slave Mode controllers connected. ICW3 in PIC1 must be written with 04H for PIC2 to function.

ICW3 Format for PIC2 **(Address 0A1H Write Only)**



INTA Data[2:0]: Determine the Slave Mode address the controllers will respond to during the cascaded INTA sequence. ICW3 in PIC2 should be written with 02H for Cascade Mode operation. Note that bit [7:3] must be zero.

ICW4 **(Address 021H / 0A1H Write Only)**



Enable Multiple Interrupts - Bit 4 enables Multiple Interrupts from the same channel in Fixed Priority Mode. This allows PIC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by PIC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to PIC2 and to check its In Service Register for zero when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to PIC1. If non-zero, no command is issued.

AEOI - Auto End-of-Interrupt - Bit 1 is enabled when ICW4[4:1] is written with a zero in both. The interrupt controller performs a non-specific EOI on the trailing edge of the second INTA cycle. Note that this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

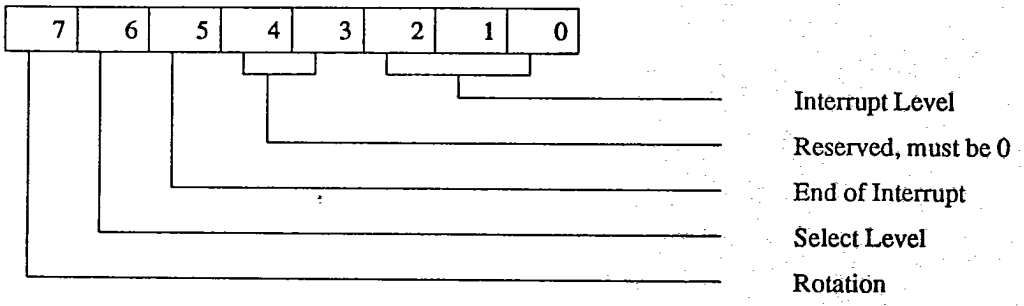
Operational Command Words

Operational Command Word One (OCW1) is located at address 021H/0A1H and may be Written any time the Controller is in Initialization Mode. Operational Command Words Two and Three (OCW2 and OCW3) are located at address 020H/0A0H. Writing to address 020H/0A0H with a zero in bit 4 places the Controller in Operational Mode and loads OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 **(Address 021H / 0A1H Read/Write Register)**

Mask Bits[7:0]: These bits control the state of the interrupt Mask Register. Each interrupt request can be masked by writing a one in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no effect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2 **(Address 020H / 0A0H Write Only)**



Bit(s)	Value	Meaning
2:0		L2, L1, L0 - These bits determine the interrupt level acted upon when the SL bit is active.
4:3	0 0	Reserved, must be 0.
7:5		EOI, SL, R - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is shown below.

	IR Level to be acted upon							
	0	1	2	3	4	5	6	7
L	0	1	0	1	0	1	0	1
L	0	0	1	1	0	0	1	1
L	0	0	0	0	1	1	1	1

Powered by ICminer.com Electronic-Library Service CopyRight 2003

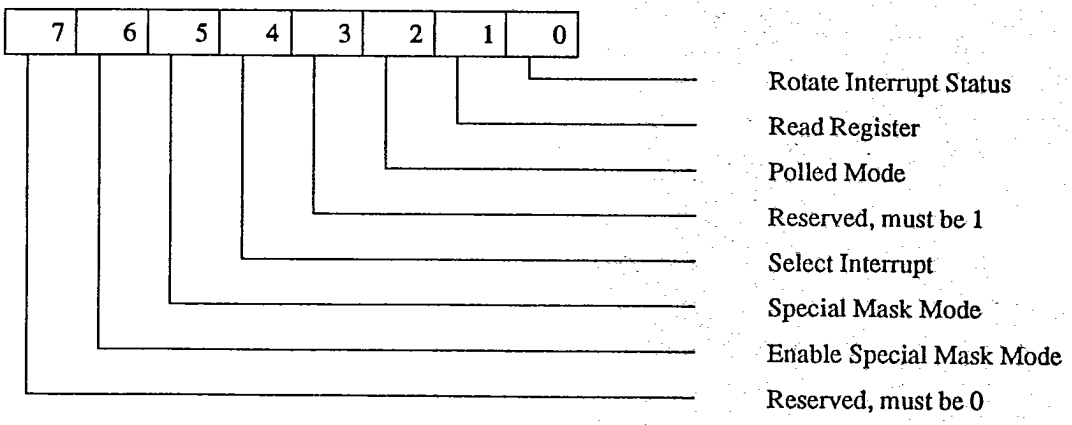
HT321 Register Descriptions

T-49-17-15

R	S	E		
0	0	1	Non-specific EOI Command	End of Interrupt
0	1	1	Specific EOI Command	
0	1	1	Rotate on Non-specific EOI Command	Automatic Rotation
1	0	0	Rotate in Automatic EOI Mode (Set)	
0	0	0	Rotate in Automatic EOI Mode (Clear)	
1	1	1	*Rotate on Specific EOI Command	Specific Rotation
1	1	0	*Set Priority Command	
0	1	0	No Operation	
			*L0-L2 are used	

Powered by ICminer.com Electronic-Library Service CopyRight 2003

OCW3 (Address 020H / 0A0H Write Only)



Bit

0 Rotate Interrupt Status - This bit selects between the IRR and the ISR during Status Read operations if Read Register = 1 is selected. ISR is selected if this bit is set to zero.

1 Read Register - When the bit is a "1", reading the Status Port at address 020H/0A0H causes the contents of IRR or ISR (determined by Rotate Interrupt Status Bit) to be placed on D[7:0]. Asserting Polled Mode forces Read Register reset.

2 Polled Mode is enabled by writing a "1" to bit 2 of OCW3, causing the HT321 to perform the equivalent of an INTA cycle during the next I/O Read Operation to the Controller. The byte read during this cycle sets bit 7 if an Interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request is encoded in bits[2:0]. The IRR remains frozen until the read cycle is completed, at which time the Polled Mode bit is reset.

4 Select Interrupt - Writing a zero in this bit position takes the Interrupt Controller out of initialize mode and writes OCW2 or OCW3.

5 Special Mask Mode - If Enable Special Mask Mode and Special Mask Mode are written with a "1", the Special Mask Mode is enabled. Writing a "1" to Enable Special Mask Mode and a zero to Special Mask Mode disables Special Mask Mode. During Special Mask Mode, Writing a "1" to a Bit position inhibits interrupts and Writing a zero enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition for the ISR.

6 Enable Special Mask Mode - Writing a "1" in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5. Enable Special Mask Mode allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Register Descriptions

T-49-17-15

Identifier Port

INDEX 0020H

Read

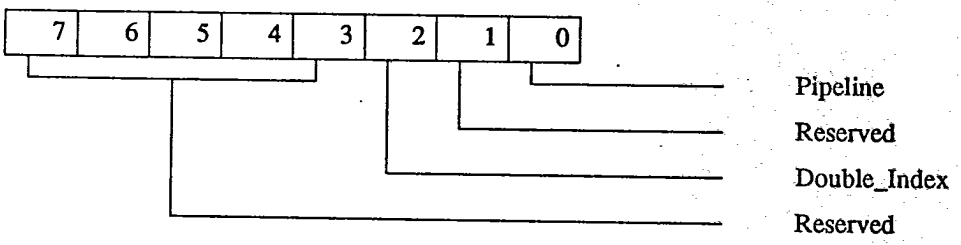
Bit(s)	Value	Meaning
3:0	0 0 0 1	Revision number (1 = Rev. 1)
7:4	0 0 1 0	DRAM controller identifier.

Write

Ignored.

Feature Port

INDEX 0021H : (Reset State = 01H)



Read

Bit(s)	Value	Meaning
0	1	Pipeline supported
	0	Pipeline not supported
1		Reserved
2	1	Second level indexing supported
	0	Second level indexing not supported
7:3		Reserved

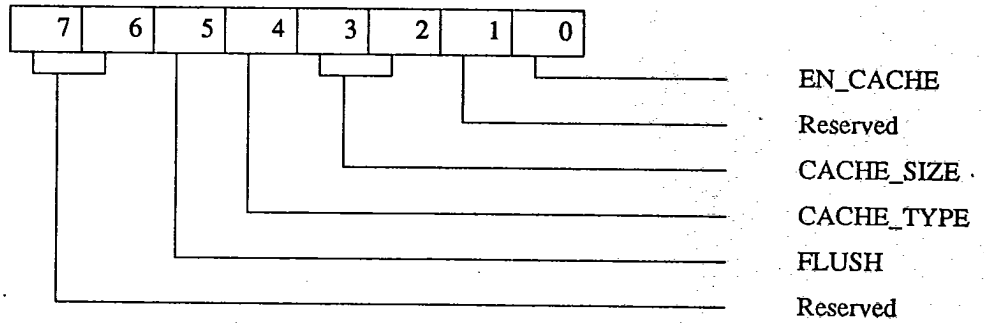
Write

Ignored

Powered by ICminer.com Electronic-Library Service CopyRight 2003

CACHE Options Port # 1

INDEX 0022H: (Reset State = 00H) R/W



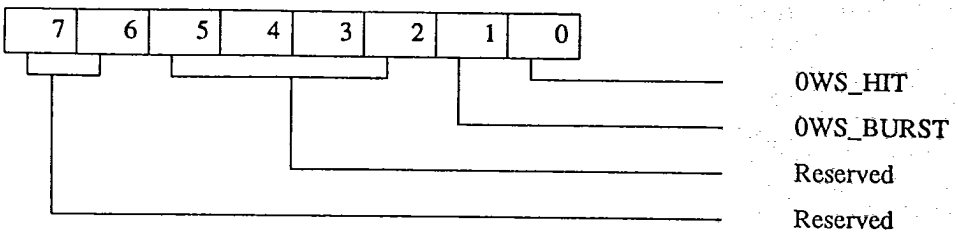
Bit(s)	Value	Meaning
0	1	Cache enabled
	0	Cache disabled
1		Reserved. Do not change contents.
3:2		Cache size:
	0 0	32K
	0 1	64K
	1 0	128K
	1 1	Reserved. Do not USE.
4	0	2-WAY Set Associative Cache
	1	Direct Mapped Cache
5	0	Cache FLUSH Disabled
	1	Cache FLUSH Enabled
7:6		Reserved. Do not change contents.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

CACHE Options Port # 2

INDEX 0023H: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
0	0	0-Wait State Cache Write Hit Disabled
	1	0-Wait State Cache Write Hit Enabled
1	0	0-Wait State Internal Burst Disabled
	1	0-Wait State Internal Burst Enabled
7:6		Reserved. Do not change contents.

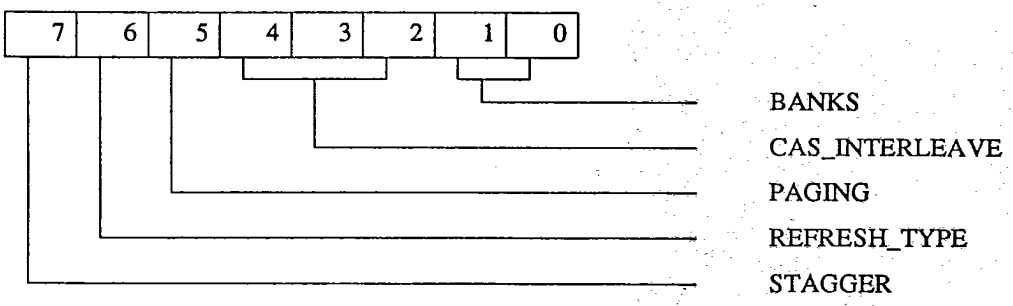
Zero-Wait State Internal Burst.

The 0-wait state internal burst option is an internal timing option which changes the internal burst timing affecting any cache read miss cycle. When disabled, a wait state is added to any burst cycle during a cache line fill. If latching data RAMs are used and the CALE signal is controlling the latching function, the 0-wait state option can be enabled. Otherwise it should be disabled.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DRAM Options Port #1

INDEX 0024H: (Reset State= 00H) R/W



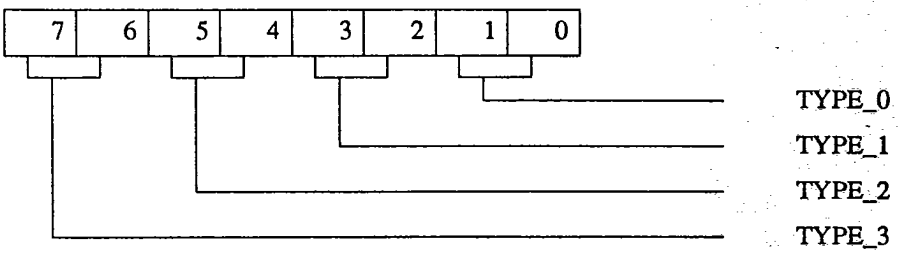
Bit(s)	Value	Meaning
1:0		Number of banks installed:
	0 0	1 bank
	0 1	2 banks
	1 0	3 banks
	1 1	4 banks
4:2		CAS interleave type:
	0 0 0	No interleave
	0 0 1	2-way interleave on LOW Banks
	0 1 0	2-way interleave on HIGH Banks
	0 1 1	2-way interleave on Both LOW and HIGH Banks
	1 0 0	4-way interleave
	1 0 1	Reserved. Do not program.
	1 1 0	Reserved. Do not program.
	1 1 1	Reserved. Do not program.
5	0	DRAM Paging Disabled
	1	DRAM Paging Enabled
6	0	RAS Only Refresh
	1	CAS Before RAS Refresh
7	0	Staggered Refresh Disabled
	1	Staggered Refresh Enabled

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

DRAM Options Port #2

INDEX 0025H: (Reset State = 00H)

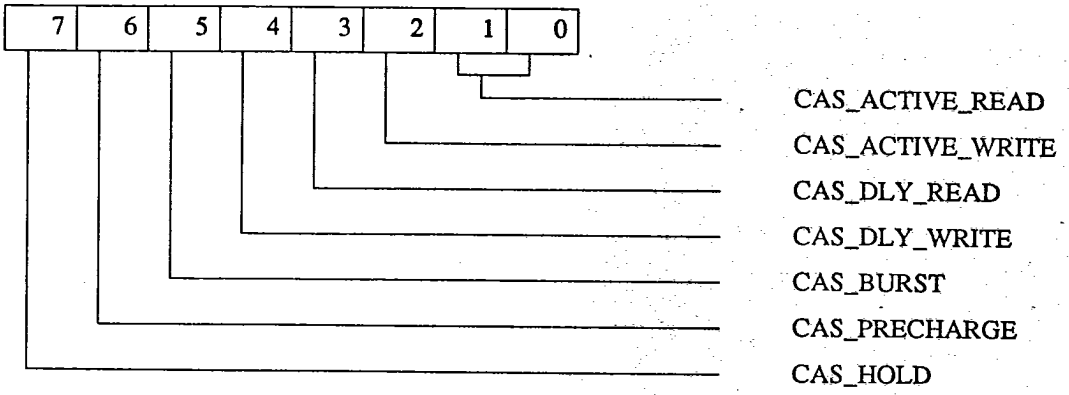


Bit(s)	Value	Meaning
1:0		Type of DRAMs in bank 0
3:2		Type of DRAMs in bank 1
5:4		Type of DRAMs in bank 2
7:6		Type of DRAMs in bank 3
	0 0	256K DRAM type
	0 1	1Mb DRAM type
	1 0	4Mb DRAM type
	1 1	16Mb DRAM type

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DRAM Options Port # 3

INDEX 0026H: (Reset State= FFH) R/W



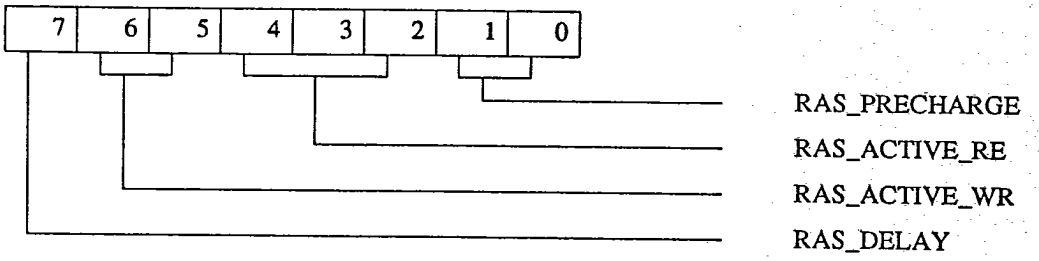
Bit(s)	Value	Meaning
1:0		CAS ACTIVE TIME (READS)
	0 0	2 HCLK2
	0 1	4 HCLK2's
	1 0	6 HCLK2's
	1 1	8 HCLK2's
2		CAS ACTIVE TIME (WRITES)
	0	2 HCLK2
	1	4 HCLK2's
3		CAS DELAY (READS)
	0	2 HCLK2
	1	4 HCLK2's
4		CAS DELAY (WRITES)
	0	2 HCLK2
	1	4 HCLK2's
5		CAS BURST DELAY
	0	NONE
	1	2 HCLK2's
6		CAS PRECHARGE
	0	1 HCLK2
	1	2 HCLK2's
7		CAS HOLD on RAS (CAS before RAS REFRESH)
	0	2 HCLK2's
	1	4 HCLK2's

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

DRAM Options Port # 4

INDEX 0027H: (Reset State = FFH) R/W

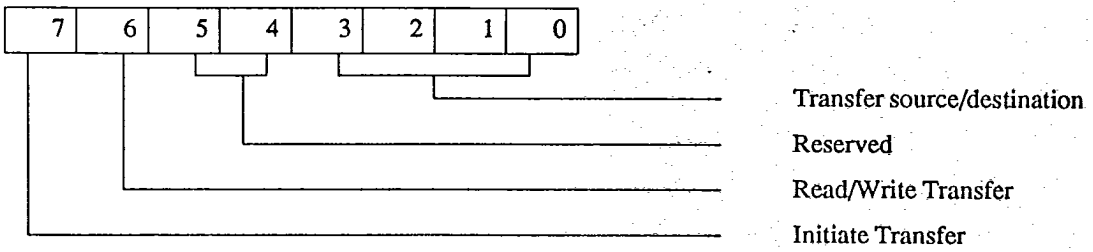


Bit(s)	Value	Meaning
1:0		RAS PRECHARGE
	0 0	2 HCLK2 clocks
	0 1	4 HCLK2clocks
	1 0	6 HCLK2 clocks
	1 1	8 HCLK2 clocks
4:2		RAS ACTIVE (READS)
	0 0 0	4 HCLK2's
	0 0 1	6 HCLK2's
	0 1 0	8 HCLK2's
	0 1 1	10 HCLK2's
	1 0 0	12 HCLK2's
	1 0 1	14 HCLK2's
	1 1 0	16 HCLK2's
	1 1 1	18 HCLK2's
6:5		RAS ACTIVE (WRITES)
	0 0	4 HCLK2's
	0 1	6 HCLK2's
	1 0	8 HCLK2's
	1 1	10 HCLK2's
7		RAS Delay
	0	No RAS Delay
	1	2 HCLK2's

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Data Transfer Control Port

INDEX 28H: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
3:0		Transfer source/destination
	0 0 0 0	EMS translation RAM location (MSB)
	0 0 0 1	EMS translation RAM location (LSB)
	0 0 1 0	REMAP RAM translation location
	0 0 1 1	EMS Page Descriptor RAM location
	0 1 0 0	Reserved. Do not program.
	0 1 0 1	Reserved. Do not program.
	0 1 1 0	Reserved. Do not program.
	0 1 1 1	Reserved. Do not program.
	1 0 0 0	NON_CACHEHIMEM register (MSB)
	1 0 0 1	NON_CACHEHIMEM register (LSB)
	1 0 1 0	NON_CACHE1MLO register
	1 0 1 1	NON_CACHE1MHI register
	1 1 0 0	TOP_OF_REMAP_MEMORY register (MSB)
	1 1 0 1	TOP_OF_REMAP_MEMORY register (LSB)
	1 1 1 0	TOP_OF_MEMORY register (MSB)
	1 1 1 1	TOP_OF_MEMORY register (LSB)
4:5		Reserved. Do not change contents.
6	0	Read transfer.
	1	Write transfer.
7	0	No action.
	1	Initiate transfer.

Writing to this port can initiate a transfer of data to/from the Data Transfer Register. The source/destination of the transfer is specified by the data value written to the port. The direction of the transfer is specified by bit 6. If bit 6 is reset, the transfer will be (if initiated) a read transfer (from a RAM location/register to the Data Transfer Register); otherwise it will be a write transfer (from the Data Transfer Register to a RAM location/register). Setting bit 7 while writing to the port initiates the transfer.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

The source/destination of the transfer specified by bits 3:0 could be :
- one of the RAMs (the location address is specified by the RAM Address Register), or
- one of the Cacheability Registers, or
- one of the Memory Boundary Registers.

Reading from this port brings back the source/destination value on bits 3:0 and the direction of the transfer on bit 6. Bit 7 is not readable since it only controls the transfer operation.

Before initiating a write transfer, data has to be written to the Data Transfer Register. If the write transfer is intended for a RAM location, the RAM Address Register should also be set properly prior to the transfer.

Before initiating a read transfer from a RAM location, the RAM Address Register should be set properly with the address of the RAM location.

After completing the read transfer, data can be read from the Data Transfer Register.

RAM Address Register

INDEX 29H: (Reset State = 00H) R/W

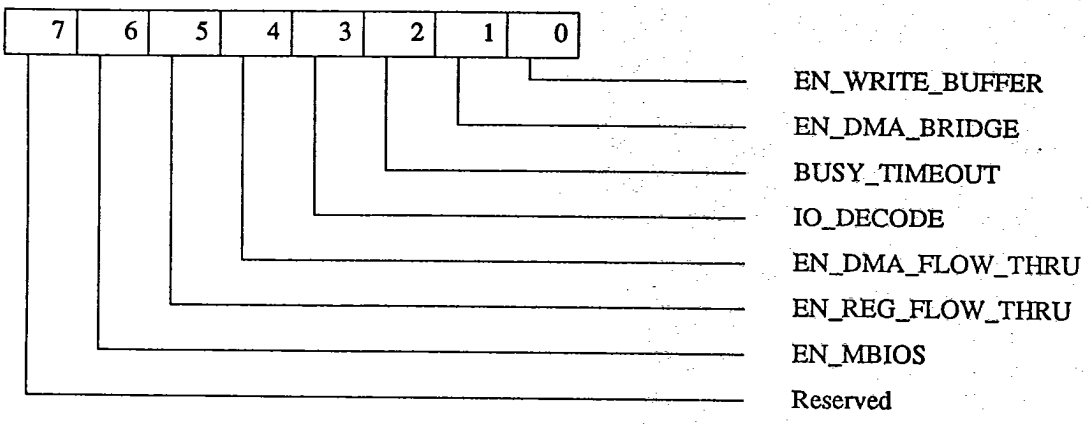
Reading this index port reads the data stored in the address register. Writing to the index port writes the value from the HD data bus to the address register.

Bit(s)	Value	Meaning
4:0		RAM address register contents
7:5		Reserved. Do not change contents.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Data Transfer Port

INDEX 2AH: (Reset State = 00H) R/W



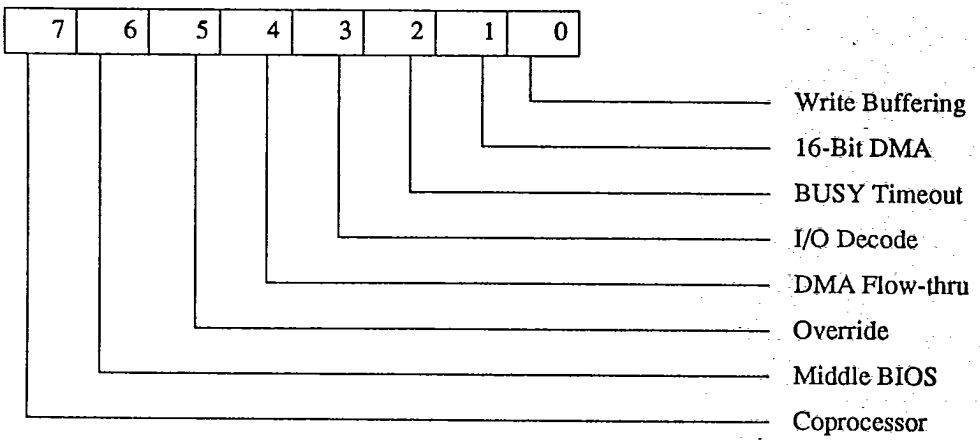
Reading this index port reads the data stored in the data register. Writing to the index port writes the value from the HD data bus to the register.

Bit(s)	Value	Meaning
7:0		Data register contents

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Other options

INDEX 002BH: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
0	0	Write buffering disabled
	1	Write buffering enabled
1	0	16-bit DMA bridge enabled
	1	16-bit DMA bridge disabled
2	0	BUSY timeout disabled
	1	BUSY timeout enabled
3	0	10-bit I/O Decode
	1	16-bit I/O Decode
4	0	DMA Flow-thru Mode is disabled
	1	DMA Flow-thru Mode is enabled
5	0	Regular Flow-thru Mode Override is disabled
	1	Regular Flow-thru Mode Override is enabled
6	0	Middle BIOS disabled
	1	Middle BIOS enabled
7	0	Coprocessor software reset enable
	1	Coprocessor software reset disable

WRITE Buffering

When enabled provides for early write cycle termination. when disabled will cause extended cycles.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

16-bit DMA Bridge.

This option disables 16-bit DMA internal data bridging. It should only be used with 32-bit DMA devices on the HTK320 Local Bus (if there are any installed).

BUSY Timeout.

BUSY Timeout is IBM PC compatible and should be turned on. It toggles the BUSY386 signal after finding no HADS* between two consecutive HREFRESH* signals.

DMA Flow-thru Mode Override.

This mode of operation affects DMA cycles only. It disables write buffering by shutting the entire stage of the pipeline off. The mode minimizes the latency of the DMA cycles and speeds the read cycles up during DMA. The bit enables special handshake mechanisms between the HT322 and HT321 controllers. Every time the CPU grants the bus to the HT321 controller, the grant is not passed to the ISA backplane until the HT322 signals its readiness with asserting HRDYN signal. The HT322 does that after offloading the write buffers and shutting the write buffering pipeline off. That is why both the HT322 and HT321 controllers should have the DMA flow-thru bits set for this mode to be operational.

Regular Flow-thru Override.

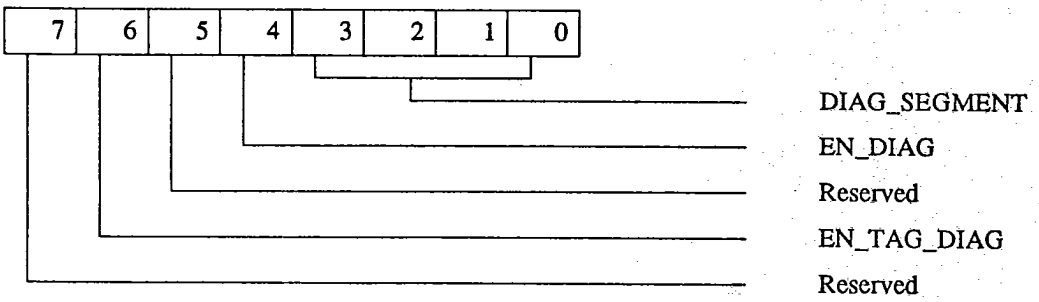
This mode shuts off write buffering and disables the write buffering pipeline completely.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Cache Diagnostic Options

Index 002CH: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
3:0	0 -FH	Diagnostic Segment Base Address on 64K boundary (bit 0 not used for 128K Cache)
4	0	Diagnostic Mode disabled
	1	Diagnostic Mode enabled
5		Reserved. Do not change contents.
6	0	TAG Diagnostic disabled
	1	TAG Diagnostic enabled
7		Reserved. Do not change contents.

When the Cache Diagnostic Option is enabled (by setting bit 4 of the index to 1), then a memory segment below 1 MB, equal to the cache size, is assigned directly to the data or TAG RAM. If the TAG diagnostic is disabled, the data RAM is mapped to the memory segment. Otherwise it is the TAG RAM that can be accessed by using the diagnostic memory segment.

The segment size depends on the cache size selected. The segment address (bits 19-16) is selected by bits 3:0 of the Cache Diagnostic Options port.

When one accesses the diagnostic segment and the diagnostic mode is enabled (no TAG Diagnostic), the cycle is treated as a cache hit. The main difference is that the DRAM memory is not updated during diagnostic write cycles at all. Way 0 is always mapped at the bottom half of the memory, way 1 at the top half.

On-chip TAG RAM can be accessed by using the TAG Diagnostic option. The TAG RAM gets mapped to the diagnostic segment and can be written to as well as read from. One can read location 0 of the TAG RAM at address offsets starting from 0 to 3FH/7FH/FFH, depending on the cache size (32K/64K/128K respectively), location 1 between offsets 40H/80H/100H - 7FH/FFH/1FFH, etc. The mapping aliases every dword within the offset range mentioned, which means that when accessing location 0 of the TAG RAM, one can reach it at address 0, 4, 8,. . ., 3CH/FCH/1FCH.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Bit 31 (highest) of the dword is where the LRU RAM is mapped. The bit aliases every 16K/32K/64K, depending on the cache size. This means that bit 31 of location 0 of the TAG RAM can be reached at offset ranges 0 to 3FH/FFH/1FFH, as well as 4000H/8000H/10000H to 403FH/80FFH/101FFH.

The TAG RAM should be read at d-word boundaries using 32-bit instructions.

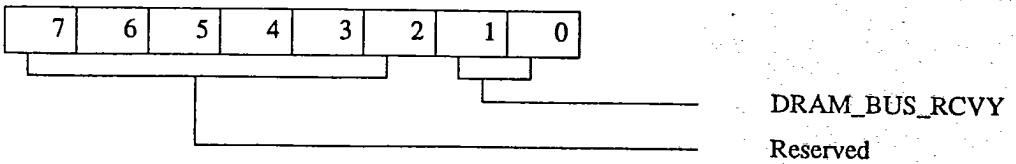
The write instructions writing to the TAG RAM MUST be 32-bit instructions and they MUST write all 4 bytes at a time.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

DRAM Options Port #5

INDEX 002DH: (Reset State = 03H) R/W



Bit(s)	Value	Meaning
1:0		BUS Recovery for DRAM cycles
	0 0	No recovery
	0 1	2 HCLK2
	1 0	1 HCLK2
	1 1	2 HCLK2
7:2		Reserved. Do not change contents.

Cacheability Registers

These registers are accessed via the standard Data Transfer Control Port mechanism. They are read/write registers.

NON_CACHEHIMEM Register

14 bit register. Reset State = 040H (points at 1MB boundary)

Bit(s)	Value	Meaning
13:0		Address bits 27:14 specifying the highest DRAM address +1 for which the cache controller should cache a memory cycle. Any DRAM cycle above the address should be considered non-cacheable.

NON_CACHE1MLO and NON_CACHE1MHI Registers

6 bit registers. Reset State = NON_CACHE1MLO = 0H (points at the beginning of the memory)

NON_CACHE1MHI = 28H (points at segment A000)

Bit(s)	Value	Meaning
5:0		Address bits 19:14 specifying boundaries for a window below 1MB of memory. Any DRAM cycle within the memory area should be considered non-cacheable. NON_CACHE1MLO specifies the low boundary, NON_CACHE1MHI the high one.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Memory Boundary Registers.

TOP_OF_REMAP_MEMORY Register

14 bit register. Reset State = 040H (points at 1MB boundary).

Bit(s)	Value	Meaning
13:0		Specifies the highest (+ 1) memory address (bits 27:14) which will be directed to the DRAM subsytem. The REMAP translation RAM contains the mapping scheme. This register value should be equal to TOP_OF_MEMORY + number of remapped EMS 16KB Blocks 16 KB.

TOP_OF_MEMORY Register

14 bit register. Reset State = 040H (points at 1MB boundary).

Bit(s)	Value	Meaning
13:0		Specifies the highest (+ 1) memory address (bits 27:14) which will be directed to the DRAM subsytem if there is no REMAPPING in the system (effectively , it specifies the total amount of contiguous memory installed) .

EMS Page Descriptor Registers

An EMS page is a 16KB Block of memory between 640K and 1MB address space. Therefore, there are 24 EMS pages in an IBM PC address space.

Every one of the pages has a 6-bit register associated with it called EMS Page Descriptor Register. These registers are stored in a RAM called EMS Page Descriptor RAM. Pages are numbered 0 - 23 and page 0 corresponds to the 16K chunk right above the 640K boundary. The page numbers address the Page Descriptors RAM when the writing to the RAM process occurs.

NOTE: PAGE 0 corresponds to RAM Address = 8

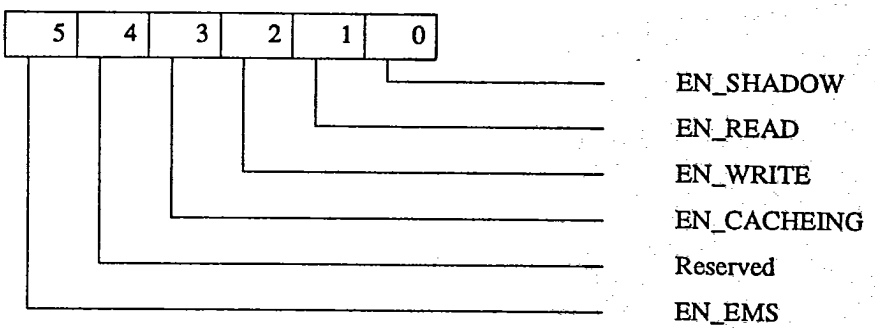
Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Register Descriptions

T-49-17-15

Outlined below is the content of an EMS Page Descriptor Register.

(Reset State = 00H)



Bit(s)	Value	Meaning
0	0	Shadowing is disabled
	1	Shadowing is enabled
1	0	Reading is disabled
	1	Reading is enabled
2	0	Writing is disabled
	1	Writing is enabled
3	0	Cacheing is disabled
	1	Cacheing is enabled
4	0	Reserved. Always program to 0
5	0	EMS translation is disabled
	1	EMS translation is enabled

A read cycle directed to the EMS page will be treated as a DRAM cycle if:
- EMS is enabled, or
- Shadowing is enabled and Reading is enabled.

A write cycle directed to the EMS page will be treated as a DRAM cycle if:
- EMS is enabled, or
- Shadowing is enabled and Writing is enabled.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Accessing HT322 Registers

Straight Indexing Scheme

The straight indexing scheme applies to all so-called static registers. They contain the static bits configuring the HT322 by enabling, disabling and setting chipset features.

The general scheme to access these registers is simple:

- IOW to address 28H sets an index of the register to be accessed,
- IOW/IOR to/from address 24H writes/reads the value to/from the indexed register.

Double Indexing Scheme

The HT322 contains many table-based Remapping, EMS and Cacheability Translations.

These translation tables are all accessed through the configuration registers. If there were an INDEX per table entry, there would be too many INDICES. Instead, there is a double indexing scheme. The normal Indices address the Data Transfer Port, RAM Address Register and Data Transfer Control Port. These registers are used to access the tables, thus only three indices are required for all of them.

The Data Transfer Port resides at index 2AH, RAM Address Register at index 29H and Data Transfer Port at index 28H. The bits are all defined in the HT322 Register Description Section of the Data Sheet.

Two categories of data storage are accessed via the Double Indexing Scheme:

- RAM locations containing Translation table Entries, and
- Static Registers called RAM-like Registers.

The only difference between the two categories is that RAM locations require a RAM Address Register to be filled in while transferring data to/from the location, and the RAM-like registers do not. Except for that, the access method is the same.

The sequence below describes how to write to a RAM location. For a RAM-like register, omit the step when the RAM Address Register is being set.

1. Set RAM Address Register
   - IOW to address 28H with value 29H
   - IOW to address 24H with RAM address value
2. Set Data Transfer Port
   - IOW to address 28H with value 2AH
   - IOW to address 24H with data of value to be transferred
3. Initiate the write transfer
   - IOW to address 28H with value 28H
   - IOW to address 24H with value:
     a) bits 3:0 specify the destination of the transfer
     b) bit 6 set
     c) bit 7 set

The sequence below describes how to read a RAM location. For a RAM-like register, omit the step when the RAM Address Register is being set.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

1. Set RAM Address Register
   - IOW to address 28H with value 29H
   - IOW to address 24H with RAM address value
2. Initiate the read transfer
   - IOW to address 28H with value 28H
   - IOW to address 24H with value:
     a) bits 3:0 specify the source of the transfer
     b) bit 6 reset
     c) bit 7 set
3. Read data from Data Transfer Port
   - IOW to address 28H with value 2AH
   - IOR from address 24H gives the data transferred value

Setting DRAM Memory Size and Remapping

Memory Address Range and Decoding

The range of memory to which this chip responds is directly related to the type and number of DRAM banks installed. It is up to the user to determine the upper boundary of memory to which the chip is to respond. The memory address decode section is affected by 2 operations: EMS, Remapping. There are two key registers which determine if the HT322 will respond to a processor memory cycle: TOP_OF_REMAP_MEMORY (TRM) and TOP_OF_MEMORY (TM). Register TM describes the total amount of DRAM in the system. If there were 4 banks of 1M DRAMs, totalling 16 Megabytes, then the TM register would contain the necessary bits to describe 16 Megabytes. Register TRM describes the Upper Address Limit to which the HT322 is to respond. This will be the same as the TM register except when Remap is enabled. Remap is enabled if TRM > TM. Selected blocks of the 384K of Memory between 640K and 1M will be remapped beyond the Total Physical Memory. The difference between TRM and TM is the amount of memory to be remapped. The Maximum, TRM - TM = 384K. The HT322 will respond to all addresses below the value set by TRM.

Note that it is possible to program TRM to be greater than TM + 384K. It is also possible to program TRM < TM. These errors will result in Aliasing of Memory Blocks. **THIS MUST BE AVOIDED.**

Representation

The basic memory block or page size has been set to 16K. Remapping, EMS and cacheability are all identified in this basic unit. The TRM and TM Registers are programmed for Address Comparison with those on the HA bus. The TM/TRM Bits are compared with HA[27:14]. Thus, both TRM and TM registers are 14 bits wide and hold values representing Address Bits [27:14]. For instance, values of 16, 17 and 18 Megabytes would be represented by 00010000000000Binary or 0400Hex; 00010001000000B or 0440H; 00010010000000B or 0480H respectively.

The EMS Translation Table Register, Cacheability and EMS Page Descriptor Registers also use this Structure. These other registers are described later.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Remap

In order to enable Remap of the Physical DRAM Memory between the 640K and 1MB space the TRM Register Value must exceed that of the TM Register. The REMAP RAM which contains the translation table setting the remapping scheme must also be programmed. The scheme implemented in the HT322 provides unlimited flexibility in remapping any of the 16K pages of DRAM between 640K to 1M above the Top of Physical Memory.

The EMS pages between 640K and 1M of the PC memory map are 16K size numbered 0 to 23. The Key is that Page 0 corresponds to RAM Address Location 8. In order to fill the REMAP RAM translation table, a Table assigning Virtual Pages above Top of Memory to physical EMS pages must be formed. When the REMAP RAM is loaded, the RAM Address Register contents correspond to the Virtual Page Number above Top of Memory for current translation, and the Data Transfer Register content corresponds to the physical EMS Page Number + 8 assigned to the Virtual Page.

For example: to Assign Virtual page 0 to Physical Page 0, Virtual Page 1 to Physical Page 1 , in progression.

In this case, the content of the RAM Address Register and Data Transfer Register, loaded in the REMAP RAM, would look like:

RAM Address Register	Data Transfer Register
0	8
1	9
2	A
3	B
4	C
...	...
17	1F

If the REMAP RAM was loaded as the Table above describes,all 24 EMS pages (384KB) of Memory would be Remapped above the Top of Memory.

The order of Physical Page numbers placed in the Data Transfer Register does not matter, they can be set in any order. The same applies to the number of pages remapped.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

By this method Remap,Shadowing and EMS can coexist. For example, 8 physical pages could be Shadowed (BIOS and Video BIOS), and the remaining 16 Pages Remapped above the Top of Memory or use one for an EMS page (by LIM EMS 4.0 Spec) assigned in available space between 640KB and 1MB.

Shadowing

Shadowing provides performance gain by duplication of "slower EPROM" in "faster DRAM".The HT322 supports shadowing for any of the 24 EMS pages. EMS Page Descriptor Registers have been defined for each of the 24 pages. Each Registers has 3 programmable Shadowing Attributes :

- Shadowing Enabled/Disabled (if this Bit is reset, the following two do not matter)
- Reading Enabled/Disabled (if the global shadowing Bit is set, this Bit determines whether a Read Cycle will Access the DRAM.
- Writing Enabled/Disabled (if the global shadowing Bit is set, this Bit determines whether a Write Cycle access the DRAM.

The sample source code below illustrates how Shadowing of the main 64KB BIOS might be achieved using the methods described above.

title Turn on the Shadow BIOS for the 386DX Design

SHDWBIOS 1.00 Copyright © LSI Logic Corporation of Canada Inc.
SHDWBIOS.ASM

```
COFFSET equ     0f000h          ; We want to shadow the system BIOS
PAGES   equ     4               ; We Want to shadow only four pages, ie 64k
code    segment public
        assume  cs:code,ds:code
initialize proc near
phinst:
; Setup DRAMS so that we read from EPROMs and write into DRAMS
    mov     ax,COFFSET          ; Get the code offset
    sub     ax,0a000h           ; Subtract 640k
    mov     dx,0                ; Setup for 16-bit divide
    mov     bx,400h             ; Divide this resultant by 16K
    idiv    bx                  ; Page offset is now in ax
    add     al,8                ; This is the 8 offset assigning page 0 to RAM location 8
    mov     dl,al               ; Save resultant
    mov     dh,dl               ; and keep one more copy
    mov     cx,PAGES            ; This is the number of pages to convert
wxfer_set:
    mov     al,29h              ; Get the Transfer address loaded
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        out     28h,al
        mov     al,dl           ; Get the address for this page
        out     24h,al
        inc     dl              ; Bump Page address for next time
        mov     al,2ah          ; Get the Transfer data loaded
        out     28h,al
        mov     al,5            ; Turn on shadowing with writing to DRAMS
        out     24h,al
        mov     al,28h          ; Initiate a write transfer
        out     28h,al
        mov     al,0c3h
        out     24h,al
        loop    wxfer_set       ; Continue definition of 16k pages
; Now block load the EPROM into the underlying DRAM
        mov     ax,COFFSET      ; Set pointer to the BIOS
        mov     ds,ax
        mov     dl,PAGES
xfer0:
        mov     bx,0            ; Start at the beginning of the BIOS
        mov     cx,2000h        ; Do a 16k data sweep
xfer1:
        mov     ax,[bx]         ; Read from EPROM
        mov     [bx],ax         ; Give to dynamic RAM
        inc     bx
        inc     bx              ; Bump pointer
        loop    xfer1           ; Loop until 64k is done
        dec     dl              ; Reduce number of pages to do
        jz      xfer2           ; Jump if all pages done
        mov     ax,ds           ; Bump Data Segment by 16K
        add     ax,400h
        mov     ds,ax           ; Resave new segment
        jmp     xfer0
; Setup DRAMS so that we read from DRAMS and write into EPROMs
xfer2:
        mov     dl,dh           ; Get back the page offset
        mov     cx,PAGES        ; This is the number of pages to convert
rxfer_set:
        mov     al,29h          ; Get the Transfer address loaded
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Register Access

T-49-17-15

```
        out     28h,al
        mov     al,dl           ; Get the address for this page
        out     24h,al
        inc     dl              ; Bump the page pointer
        mov     al,2ah          ; Get  the Transfer data loaded
        out     28h,al
        mov     al,0bh          ; Turn on shadowing with reading from DRAMS
        out     24h,al          ; and turn on the cache controller
        mov     al,28h          ; Initiate a write transfer
        out     28h,al
        mov     al,0c3h
        out     24h,al
        loop    rxfer_set
; Now get back to DOS
        mov     ah,0
        int     21h
initialize endp
code    ends
    end     phinst
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

EMS 4.0 Support

Any one of the 24 EMS pages can be used as an EMS page in the sense of the LIM EMS 4.0 Specification.

The HT322 provides unlimited flexibility for translation any of the 24 EMS Page Addresses ANYWHERE in Memory. This is achieved by means of enabling EMS Bit of the EMS Page Descriptor Register(this overrides shadowing) and loading the EMS Translation RAM (ETR) to point to the Translated Address.

The ETR is a 14-bit register representing Bits 27 to 14 of the target address for the current EMS Address Translation. In this way a Window that will point anywhere in Memory from EMS space may be set . Any one of the 24 EMS pages may be programmed.

In order to enable a 16KB EMS window using Page 0 (at Physical Address A000:0000) as an EMS page and access a 16KB Memory Block immediately above the 1MB boundary, do the following:

1. Set EMS Page Descriptor Register for page 0 (RAM address 8) to 20H - EMS bit on.

2. Set EMS Translation location MSB to 0 (RAM address 8).

3. Set EMS Translation location LSB to 40H (RAM address always set to page number + 8, which in this case is 8).

There will now be a 16K EMS window at A000:0000. Acccess to this Address+offset will result in access to the physical address 10000:0000+offset. The program example below will access Protected Memory above 15MB by using a 64KB EMS window.

EMSTEST

```
#include "stdio.h"
#include "conio.h"
#include "fcntl.h"
#include "io.h"
#include "math.h"
#define HOLE        0xd000          /* Location of the EMS Hole */
#define PAGES       4               /* Defines how much of a Hole exists */
main()
{
    unsigned int address_lo;
    unsigned int address_hi;
    unsigned int errstat;
    long address_pntr;
    unsigned int temp;
    long topmem,templ;              /* Top of Memory Register */
    unsigned int start_page;        /* Start page number of EMS Hole
    int num_blocks;                 /* Number of Blocks above 1 Meg Memory to test */
    int i,k;
    unsigned int j;
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

```
        long passno;
        system("cls");
        printf("\nEMS Testing");
    /* Locate the start page */
        start_page = HOLE - 0x8000;
        start_page = start_page / 0x400;
    /* Now calculate the number of blocks to test above the 1M boundary */
    /* First read TOP_OF_MEMORY register */
        outp(0x28,0x28);
        outp(0x24,0x8f);
        outp(0x28,0x2a);
        topmem = (long)inp(0x24);
        topmem = topmem * 16384L;
        outp(0x28,0x28);
        outp(0x24,0x8e);
        outp(0x28,0x2a);
        templ = (long)inp(0x24);
        templ = templ * 4194304L;
        topmem = topmem + templ;
        printf("\n\nTOP OF MEMORY set to %lx",topmem);
        templ = topmem - 0x100000L;                    /* Isolate how much memory to test */
        templ = templ / 0x4000L;                       /* Number of 16K blocks to test */
        templ = templ / (long)PAGES;                   /* number of 16K*PAGES blocks to test */
        num_blocks = (int)templ;
        printf("\nNumber of Pages to test per Block %d",PAGES);
        printf("\nNumber of Blocks to test %d\n",num_blocks);
    passno = 0;
    while(1)
    {
        address_pntr = 0x100000L;
        printf("\nPass == %ld\n",passno);
        j = (unsigned int)passno;
    /* Set up Cacheable Memory Hole */
        if(j & 1)
        {       printf("Cache On\n");
                for(i=0; i<PAGES; i++)
                {
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
outp(0x28,0x29);                    /* Get Transfer Address Setup */
outp(0x24,i+start_page);
outp(0x28,0x2a);                    /* Point to Data Transfer Register */
outp(0x24,0x28);                    /* Set the hole for this page */
outp(0x28,0x28);                    /* Point to Data Transfer Register */
outp(0x24,0xc3);                    /* Initiate a Write Xfer */
}
}
else
{
printf("Cache Off\n");
for(i=0; i<PAGES; i++)
{
outp(0x28,0x29);                    /* Get Transfer Address Setup */
outp(0x24,i+start_page);
outp(0x28,0x2a);                    /* Point to Data Transfer Register */
outp(0x24,0x20);                    /* Set the hole for this page */
outp(0x28,0x28);                    /* Point to Data Transfer Register */
outp(0x24,0xc3);                    /* Initiate a Write Xfer */
        }
}
for(i=0; i<num_blocks; i++)
{
printf("\rTesting Block %d Address %08lx",i+1,address_pntr);
/* Setup EMS Translation RAM */
for(j=0; j<PAGES; j++)
        {
outp(0x28,0x29);                    /* Put Page into RAM Address Register*/
outp(0x24,j+start_page);
templ = address_pntr > 14;
address_lo = (unsigned int)templ;
templ >= 8;
address_hi = (unsigned int)templ;
outp(0x28,0x2a);                    /* Put LSB of Xlat address into Data Transfer Register */
outp(0x24,address_lo);
outp(0x28,0x28);                    /* Get to Data Transfer Port */
outp(0x24,0xc1);                    /* Do a write Xfer to EMS LSB */
outp(0x28,0x2a);                    /* Put MSB of Xlat address into Data Transfer Register */
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        outp(0x24,address_hi);
        outp(0x28,0x28);                    /* Get to Data Transfer Port */
        outp(0x24,0xc0);                    /* Do a write Xfer to EMS LSB */
        address_pntr = address_pntr + 0x4000L;    /* Bump address to next page */
        }
    /* Do a 55 AA test into the Block of Memory */
    /* Then set the Block ID into it */
        if(errstat = mtest(PAGES,HOLE,i))
                {
        printf("\nTest Stopped because of Error == %x\n\n", errstat);
        exit(1);
        }
        }
    /* Now verify all the Block Numbers */
        printf("\n");
        address_pntr = 0x100000; /* Start testing at beginning of memory */
        for(i=0; i<num_blocks; i++)
        {
        printf("\rVerifying Block Number %d at Address %08lx",i+1, address_pntr);
    /* Set up EMS Translation RAM */
        for(j=0; j<PAGES; j++)
        {
        outp(0x28,0x29);                    /* Put Page into RAM Address Register */
        outp(0x24,j+start_page);
        templ = address_pntr > 14;
        address_lo = (unsigned int)templ;
        templ >= 8;
        address_hi = (unsigned int)templ;
        outp(0x28,0x2a);                    /* Put LSB of Xlat address into Data Transfer Register */
        outp(0x24,address_lo);
        outp(0x28,0x28);                    /* Get to Data Transfer Port */
        outp(0x24,0xc1);                    /* Do a write Xfer to EMS LSB */
        outp(0x28,0x2a);                    /* Put MSB of Xlat address into Data Transfer Register */
        outp(0x24,address_hi);
        outp(0x28,0x28);                    /* Get to Data Transfer Port */
        outp(0x24,0xc0);                    /* Do a write Xfer to EMS MSB */
    address_pntr = address_pntr + 0x4000L;    /* Bump address to next page */
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        }
    /* Flush the Cache Controller */
        outp(0x28,0x22);
        k = inp(0x24);
        k = 0x20;                              /* Set Flush bit */
        outp(0x24,k);
        k &= 0xdf;                             /* Reset Flush bit */
        outp(0x24,k);
        if(blkchk(PAGES,HOLE,i))
        {
        printf("\nBlock Number Failed. Testing Stopped\n\n");
    exit(1);
        }
        }
        passno = passno + 1;
        }
}
```

title **5555 AAAA Read Write Test Routine**

MTEST 1.00
MTEST.ASM

```
MTEST_TEXT      SEGMENT BYTE PUBLIC 'CODE'
MTEST_TEXT      ENDS
_DATA       SEGMENT WORD PUBLIC 'DATA'
_DATA       ENDS
CONST       SEGMENT WORD PUBLIC 'CONST'
CONST       ENDS
_BSS        SEGMENT WORD PUBLIC 'BSS'
_BSS        ENDS
DGROUP      GROUP CONST,_BSS,   _DATA
            ASSUME      CS: MTEST_TEXT, DS: DGROUP, SS: DGROUP, ES: DGROUP
MTEST_TEXT      SEGMENT
    PUBLIC _mtest
_mtest proc far
    push    bp
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        mov     bp,sp
        pushf
        push    ds
        push    bx
        push    cx
        push    dx
        push    di
; First Seed the memory with 5555H
        mov     di,[bp+10]          ; Get the current block number
        mov     bx,[bp+8]           ; Get the start location of the EMS hole
        mov     ds,bx
        mov     dx,[bp+6]           ; Get number of pages to test
        mov     ax,5555h
seed0:
        mov     bx,0
        mov     cx,2000h            ; Set loop counter to 16K
seed1:
        mov     [bx],ax
        inc     bx
        inc     bx
        loop    seed1
        dec     dx                  ; Reduce number of pages to check
        jz      seed2               ; Jump if all pages have been seeded
        mov     bx,ds               ; Get back data segment
        add     bx,400h             ; Bump segment by 16k
        mov     ds,bx
        jnz     seed0               ; Jump if not
; Now Check for 5555H and Write in AAAAH
seed2:
        mov     bx,[bp+8]           ; Get the start location of the EMS hole
        mov     ds,bx
        mov     dx,[bp+6]           ; Get number of pages to test
seed3:
        mov     bx,0
        mov     cx,2000h
seed4:
        mov     ax,[bx]             ; Now read back the data
        cmp     ax,5555h            ; Check for valid data
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        jnz     err1                    ; Jump if error detected
        mov     ax,0AAAAh               ; rewrite AAAA
        mov     [bx],ax
        inc     bx
        inc     bx
        loop    seed4
        dec     dx                      ; Reduce number of pages to check
        jz      seed5                   ; Jump if all pages have been seeded
        mov     bx,ds                   ; Get back data segment
        add     bx,400h                 ; Bump segment by 16k
        mov     ds,bx
        jnz     seed3                   ; Jump if not
; Now Check for AAAAH and Write in PAGE Number
seed5:
        mov     bx,[bp+8]               ; Get the start location of the EMS hole
        mov     ds,bx
        mov     dx,[bp+6]               ; Get number of pages to test
seed6:
        mov     bx,0
        mov     cx,2000h
seed7:
        mov     ax,[bx]                 ; Now read back the data
        cmp     ax,0AAAAh               ; Check for valid data
        jnz     err1                    ; Jump if error detected
        mov     [bx],di                 ; Write out the block number for this block
        inc     bx
        inc     bx
        loop    seed7
        dec     dx                      ; Reduce number of pages to check
        jz      seed8                   ; Jump if all pages have been seeded
        mov     bx,ds                   ; Get back data segment
        add     bx,400h                 ; Bump segment by 16k
        mov     ds,bx
        jmp     seed6                   ; Jump if not
; If we got this far the block tested positively
seed8:
        xor     ax,ax                   ; Clear the return status
        jmp     short mtest_exit
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
err1:
    mov     ax,ds
    jmp     short mtest_exit
err2:
    mov     ax,2
mtest_exit:
    pop     di
    pop     dx
    pop     cx
    pop     bx
    pop     ds
    popf
    mov     sp,bp                   ; That's it
    pop     bp
    ret
_mtest endp
    PUBLIC _blkchk
_blkchk proc far
    push    bp
    mov     bp,sp
    pushf
    push    ds
    push    bx
    push    cx
    push    dx
    push    di
    mov     di,[bp+10]              ; Get the current block number
    mov     bx,[bp+8]               ; Get the start location of the EMS hole
    mov     ds,bx
    mov     dx,[bp+6]               ; Get number of pages to test
bchk1:
    mov     bx,0
    mov     cx,2000h
bchk2:
    mov     ax,[bx]                 ; Now read back the data
    cmp     ax,di                   ; Check for valid data
    jnz     bcerr1                  ; Jump if error detected
    inc     bx
```


Powered by ICminer.com Electronic-Library Service CopyRight 2003

```
        inc     bx
        loop    bchk2
        dec     dx                      ; Reduce number of pages to check
        jz      bchk3                   ; Jump if all pages have been seeded
        mov     bx,ds                   ; Get back data segment
        add     bx,400h                 ; Bump segment by 16k
        mov     ds,bx
        jmp     bchk1                   ; Jump if not
; If we got this far the block tested positively
bchk3:
        xor     ax,ax                   ; Clear the return status
        jmp     short bchk_exit
bcerr1:
        mov     ax,ds
        jmp     short mtest_exit
bchk_exit:
        pop     di
        pop     dx
        pop     cx
        pop     bx
        pop     ds
        popf
        mov     sp,bp                   ; That's it
        pop     bp
        ret
_blkchk endp
MTEST_TEXT      ENDS
END
```

Notes :

EMS vs. remapped memory:

Remapped Memory cannot be accessed by means of an EMS window.

However, a DRAM memory within EMS space can be remapped.

EMS and shadow:

EMS takes precedence over Shadowing. That means if both EMS and Shadowing are enabled the Page will default to an EMS Page and Address Translation will be activated.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Cacheability

The Cacheability Registers referenced in previous paragraphs define non-cacheable regions of memory. 26 different regions may be described. A window below 1MB may be set by means of the NON_CACHE1MLO (NC1MLO) and NON_CACHE1MHI (NC1MHI) registers.

These registers will not effect cacheability if they contain equal values. NC1MLO sets the low boundary of a non-cacheable region below 1 MB and NC1MHI sets the high boundary of the region. A further register affecting cacheability is NON_CACHEHIMEM (NCHM). It sets a limit above which everything is non-cacheable. Normally this register's content equals that of the TRM register. It is possible to disable caching totally by loading MSB and LSB of this register with 0.

Each of the 24 EMS pages has an associated cacheability bit. This defines a further 24 regions of Cache Control.

Notes :

Caching and Remap:

Remapped space can be cached. Flush the cache, though, each time the REMAP Table is changed (usually this table is set only once; during the boot phase).

Caching and shadowing:

Shadowed space can be cached. No restrictions apply.

Caching and EMS:

EMS space can also be cached. Flush the cache, though, each time a context switch occurs. (Cacheing operates on physical untranslated addresses.)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

HTK320
386DX Chip Set

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
Local Bus Interface				
HA[31,27:2]	38-25, 22-10	I/O		Host Address Bus. Normally these lines are Inputs and they define the address of the device being accessed on the backplane. During DMA or Backplane MASTER cycles, these Address lines will be Outputs driven to the HA bus.
HADS*	44	I/O		Host Address Strobe, active low. This indicates that the address and status lines from the processor are stable and valid . They are valid from the Clock edge near the end of HADSN, or from the rising edge of HADSN. During DMA or Backplane MASTER cycles this signal will be an Output and will be strobed when the HA, HBEN and status lines are stable.
HBEN[3:0]	40-43	I/O		Host Byte Enables, active low. These signals define onto which byte the data will be transfered. During DMA or Backplane MASTER cycles, these lines will be driven by the HT321.
HCLK2	163	I		Host Clock. This is a single phase clock that drives the entire system. This clock drives the entire HT321.(used to create the INTERNAL Phase clock HCLK)
HD[15:0]	176-183,2-9	I/O		Host Data Bus. When configuration registers are Read/Written, data will pass over the data bus. All backplane accesses are also passed via the ISA controller to/from the Local Host Data Bus.
HHLDA	168	I		Host Hold Acknowledge, active high. This signal from the CPU, indicates the Host Bus has been released and is free for use.
HLOCAL*	167	I		Host Local Cycle, active low. This is asserted as result of a LOCAL Bus Device decoding a Valid Address for it's operation (normally the HT322 Controller). It will be active one clock after HADSN and will remain low for 2 HCLK2's. It will then be driven high, then tri-stated. If this signal is not detected 2 HCLK2 cycles after HADS*, then the HT321 will operate as the CPU Default Access, and initiate the sequence for the Backplane
HMIO HDC HWR	175,174,173	I/O		Host Status Lines: HMIO, HDC and HWR.(Host Memory I/O, Host Data Code and Host Write Read) These signals,validated at HADS*, define the type of CPU access. During DMA or Backplane MASTER accesses these lines will be driven by the HT321.

(1) For Internal PU/PD Resistance Range see DC Specs.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
HNA*/EADS*	172	O		Host Next Address, active low. This signal is normally at tri-state, but will be asserted when the current cycle is to the HT321 and the Processor has entered a T2 state. This signal requests Pipeline Operation. When the Pipeline sequence has ended, the signal will be driven high and tri-stated. During 486 mode, this pin is used as the EADS* connection, indicating that the HT321 has applied a valid address onto the local bus.
HRDYI*	165	I		Host Ready In, active low. During all cycles this signal going inactive signifies termination of the cycle.
HRDY*	39	I/O		Host Ready , active low. This signal goes active to indicate the readyness to end the cycle. The Signal duration will be one HCLK2, then will be driven high and tristated.
HREFRESH*	171	O		Host Refresh, active low. This signal indicates a Refresh Cycle to the DRAM Controller and Backplane. This signal is initiated from Internal Timer Channel 1.During MASTER mode this signal is an Input and a Refresh cycle can be initiated by asserting it low.
HRESCPU	170	O		Host reset, active high. When this signal is active, the processor is being reset. This signal will be asserted by the ISA Controller when a System Reset occurs, or a Shutdown is detected, or RC occurs, or when Port 92 FAST_RC occurs.
KB_CLAMPA20*	166	I		KeyBoard Clamp A20, active low. When active, HA20 should be treated as low regardless of what the real level of the line is. When high, HA20 should be treated normally.
PARITY*	169	I		Parity Check, active low. This is activated by a Memory Device on the Local Bus when it detects a Parity Error. It remains active for HCLK2's, then is de-asserted and tri-stated. Once active, if the internal Parity Mask is open, an NMI will occur.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HTK320
386DX Chip Set

T-49-17-15

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
CPU Interface				
BS16*	45	O		Bus Size 16, active low.The HT321 indicates to the CPU that it can only accept data on HD[0:15]. If more than two bytes of data are required for the cycle, the CPU must perform a second cycle to acquire/present all the Data.
HOLDREQ	48	O		Host Hold Request, active high. This signal is asserted when a DMA (or MASTER DMA)request occurs. It will remain high until the Temporary Bus master completes it's Cycle(s).
INT	50	O		Host Interrupt, active high. When asserted, the HT321 is requesting the CPU execute an Interrupt cycle. The signal source is the Internal 8259 Interrupt Controller.
NMI	49	O		Non-Maskable Interrupt, active high. When active, the HT321 is requesting that the CPU execute a Non Maskable Interrupt sequence. This is usually the result of a PARITY* check or IOCHCK* asserted during a Backplane cycle.
RESET387	51	O		RESET Co-Processor. This line, active high, Resets a Co-processor device on the Local Bus.Connect it to the RESETI line of the Co-Processor.
Backplane Interface				
AEN	164	O		Address Enable, active high. When high during a DMA cycle, either 8 or 16 bit, I/O devices other than the Active DACK should not activate decode. Used in conjunction with HHLDA it can determine which type of access is currently in progress.

AEN	HHLDA	Cycle
0	0	CPU
0	1	MASTER
1	0	Refresh
1	1	DMA

BALE	75	O		Bus Address Latch Enable. When high, the Address on the SA values may be changing. At the falling edge, all Address lines will be guaranteed stable. This signal is normally low for all non-backplane accesses. During MASTER, Refresh or DMA, Cycles this signal will remain high.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT321 Pin Descriptions

T-49-17-15

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
BCLK	68	O		Backplane System Clock. This Clock to the backplane is synchronized with the Commands of the HT321 and has a Frequency of 8.00 - 8.33 MHz.
DACK*[7:5],[3:0]	65-59	O		DMA Acknowledges. These signals are the respective Bus Grant Signals to DRQ requests.
DRQ[7:5],[3:0]	58-52	I		DMA Requests. These signals are used by Backplane DMA or Master DMA devices. Priorities decrease from 0 to 7. DMA Channels 0 to 3, perform 8-bit cycles, Channels 5 to 7, 16-bit cycles.
IOCHK*	159	I		I/O Channel Check, active low. When asserted, it indicates that a fatal system failure at a Backplane device. If enabled, the result is an NMI
IOCHRDY	144	I/O		I/O Channel Ready, active high. This signal indicates that no wait state insertion is necessary for the current backplane cycle. Slow I/O devices can Negate this Signal to Suspend the Cycle until Ready for completion.
IOCS16*	142	I		I/O Chip Select is 16-bits, active low.Asserted by the respondant Backplane Device, it indicates Acceptance of a 16-bit transfer for the Current I/O Cycle .
IOR*	66	I/O		I/O Read, active low. This signal indicates an I/O read operation is in progress on the backplane. For CPU and DMA cycles, this signal is an Output; for MASTER Mode cycles it is an input.
IOW*	67	I/O		I/O Write, active low. This signal indicates when an I/O Write operation is in progress. During Local Host Bus I*/O Memory access, this signal will not be active. Normally an output, during Master mode accesses this signal will be an input.
IRQ1	158	I		Interrupt Request 1. Interrupt from the 8042 Keyboard Controller, called by pseudonym "OPTBUFULL".
IRQ15,14,[12:9], [7:3]	145-146, 148-151, 153-157	I		Interrupt Requests. Interrupts from the I/O Channel indicate that an Peripheral on the Backplane is requesting service by the CPU. Inputs to the 8259 Interrupt Controller of the HT321. Priorities decrease from IRQ[9:15] and then from IRQ3 down to IRQ 7. An interrupt request is generated on the rising edge of an IRQ which must be maintained high until acknowledged by the INTA cycle.
IRQ8*	152	I		Interrupt Request 8. Real Time Clock interrupt.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HTK320
386DX Chip Set

T-49-17-15

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
IRQ13	147	I		Interrupt Request 13. When high, the Numerical Co-Processor has detected an Exception and requests Interrupt Service.
LA[23:17]	112-106	I/O		Backplane Address Bits 23 to 17. These signals are flow- thru Addresses to the Backplane.These signals are Outputs during all cycles except MASTER cycles when they are Inputs.
LBHEN	137	I/O		Latched Bus High Enable.This signal will be an Output during Backplane cycles initiated by the HT321 (both CPU and DMA).This signal will be an input during MASTER Mode accesses.
MASTER*	140	I		The ISA Backplane Master cycle indicator, active low. When active at the DRQ/DACK exchange, it indicates that a Backplane Master device owns the local bus using the HT321 as a Synchronizer/Interface chip between the ISA and Local Bus.
MEMCS16*	141	I		Memory Chip Select is 16 bits, active low. Asserted by the respondant Backplane Device, it indicates Acceptance of a 16-bit transfer for the Current Cycle.
MEMR*	71	I/O		Memory Read, active low. When active, this signal indicates that a Memory Read Cycle is in progress on the backplane. This signal will be active for all backplane accesses below 16 Mbytes. Normally an Output,during a MASTER Mode Cycle, this signal will be an Input.
MEMW*	72	I/O		Memory Write, active low.When active, this signal indicates that a Memory Write Cycle is in progress on the backplane. This signal will be active for all memory backplane accesses below 16 Mbytes. Normally an Output,during a MASTER Mode Cycle, this signal will be an Input.
OSC	160	I		Oscillator (14.31818 MHz),to the backplane.The HT321 divides this by twelve to produce 1.19MHz for the Internal 8254 equivalent.(equal to T.V. Colourburst Frequency)
RESETDRV	76	O		Backplane Reset, active high. When active, all devices on the backplane should initialise. This signal is activated by a power on reset.
SA[19:0]	136-129, 126-117, 114,113	I/O		System Address 0 to 19. These signals are the latched addresses to the backplane. SA0 and SA1 are calculated from the HBENs during non-refresh cycles. During Refresh Cycles, these lines contain the Refresh Address. During all cycles except MASTER these lines are Outputs.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
SD[15:0]	103-94,91-86	I/O		System Data Bus 0 to 15. This data bus connects directly to the ISA backplane and is used to transfer information to/from the HT321 and the ISA Backplane peripherals. The direction of data flow depends on the type of cycle and the originator. (i.e. ISA Bus MASTER, CPU or HT321).
SMEMR*	73	O		System Memory Read, active low. This backplane signal is similar in timing to the MEMR signal except that it is only active for accesses to the backplane below 1 Mbyte and is always an Output.
SMEMW*	74	O		System Memory Write, active low. This backplane signal indicates that a Memory Write is in progress to an Address below 1 Mbyte. This signal is derived from MEMW so has the same timing, but is always an Output.
TC	85	O		Terminal Count, active high. When active, it indicates the DMA controller has reached the end of its Address Increment/Decrement Count.
0WS*	143	I		Zero Wait State, active low.Asserted by the respondant Backplane Device, this signal indicates that the slave device requests early Termination of the Backplane Cycle or is capable of a Zero Wait State Cycle.

Peripheral Interface

KBDCS*	80	O		Chip select for the system Keyboard Controller.
RC	77	I		Keyboard reset, active low. When asserted, the 8042 keyboard controller is requesting a "warm Local Bus Reset".
ROMEN	79	O		Output Enable for the System BIOS ROM.
RTCCS*/MODE	81	O		Chip select for the system RTC.During POR this line is read to determine which CPU is connected in the system. If this line is pulled high, 386 mode is selected, if low, 486 mode.
SPKR	78	O		Speaker output signal to drive an external speaker. It is generated by Counter 2 of the 8254 Timer and gated by Bit 1 of Port_B register.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
Other signals				
CLAMPA20*/ ROMWIDTH	84	I/O		CLAMP A20, active low. When active, HA20 should be treated as ZERO regardless of what the real Value is. When high, HA20's Value passed as normal. During POR this line is READ to determine whether an 8 or 16-bit EPROM is installed in the system. Low during POR, then ROM accesses are 16-Bit, high ROM is 8-Bit.
POR	82	I		Power On Reset, active low. This is the Power-on Reset that indicates Reset the entire System.
TESTIN	83	I		Input for test patterns or other tests activation. When it is asserted high, all outputs are tri-stated. This may be used by In Circuit Testers.Low for Normal Operation.
VCC	23,46,69,93, 105,116, 127,139,161, 184			Power
GND	1,24,47,70, 92,104, 115,128,138, 162			Ground

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Pin Names and Numbers in Alphabetical Order

AEN	164	IOR*	66
BALE	75	IOW*	67
BCLK	68	IRQ1	158
BS16*	45	IRQ[15:3]	145-157
CLAMPA20*	84	KBCS*	80
DRQ*[3:0]	55-52	KB_CLMPA20*	166
DRQ*[7:5]	58-56	LA[23:17]	112-106
DACK*[3:0]	62-59	LBHEN	137
DACK*[7:5]	65-63	MASTER*	140
GND	1,24,47,70,92,104, 115,128,138,162	MEMCS16*	141
		MEMR*	71
HA[31:2]	38-25,22-10	MEMW*	72
HADS*	44	NMI	49
HBEN[3:0]	43-40	OSC	160
HCLK2	163	PARITY*	169
HD[15:0]	183-176,9-2	POR	82
HDC	174	RC	77
HHLDA	168	RESETDRV	76
HLOCAL*	167	RESET387	51
HMIO	175	ROMEN	79
HNA*	172	RTCCS*	81
HOLDREQ	48	SA[19:0]	136-129,126-117, 114-113
HRDY*	39	SD[15:0]	103-94,91-86
HRDYI*	165	SMEMR*	73
HREFRESH*	171	SMEMW*	74
HRESCPU	170	SPKR	78
HWR	173	TC	85
INT	50	0WS*	143
IOCHK*	159	VCC	23,46,69,93,105,116, 127, 139,161, 184
IOCHRDY	144		
IOCS16*	142		

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Pin Names and Numbers in Numerical Order

001 GND	047 GND	093 VCC	139 VCC
002 HD7	048 HOLDREQ	094 SD6	140 MASTER*
003 HD6	049 NMI	095 SD7	141 MEMCS16*
004 HD5	050 INT	096 SD8	142 IOCS16*
005 HD4	051 RESET387	097 SD9	143 0WS*
006 HD3	052 DRQ0	098 SD10	144 IOCHRDY
007 HD2	053 DRQ1	099 SD11	145 IRQ15
008 HD1	054 DRQ2	100 SD12	146 IRQ14
009 HD0	055 DRQ3	101 SD13	147 IRQ13
010 HA2	056 DRQ5	102 SD14	148 IRQ12
011 HA3	057 DRQ6	103 SD15	149 IRQ11
012 HA4	058 DRQ7	104 GND	150 IRQ10
013 HA5	059 DACK0*	105 VCC	151 IRQ9
014 HA6	060 DACK1*	106 LA17	152 IRQ8*
015 HA7	061 DACK2*	107 LA18	153 IRQ7
016 HA8	062 DACK3*	108 LA19	154 IRQ6
017 HA9	063 DACK5*	109 LA20	155 IRQ5
018 HA10	064 DACK6*	110 LA21	156 IRQ4
019 HA11	065 DACK7*	111 LA22	157 IRQ3
020 HA12	066 IOR*	112 LA23	158 IRQ1
021 HA13	067 IOW*	113 SA0	159 IOCHK*
022 HA14	068 BCLK	114 SA1	160 OSC
023 VCC	069 VCC	115 GND	161 VCC
024 GND	070 GND	116 VCC	162 GND
025 HA15	071 MEMR*	117 SA2	163 HCLK2
026 HA16	072 MEMW*	118 SA3	164 AEN
027 HA17	073 SMEMR*	119 SA4	165 HRDYI*
028 HA18	074 SMEMW*	120 SA5	166 KB_CLMPA20*
029 HA19	075 BALE	121 SA6	167 HLOCAL*
030 HA20	076 RESETDRV	122 SA7	168 HHLDA
031 HA21	077 RC	123 SA8	169 PARITY*
032 HA22	078 SPKR	124 SA9	170 HRESCPU
033 HA23	079 ROMEN	125 SA10	171 HREFRESH*
034 HA24	080 KBCS*	126 SA11	172 HNA*
035 HA25	081 RTCCS*	127 VCC	173 HWR
036 HA26	082 POR	128 GND	174 HDC
037 HA27	083 TESTIN	129 SA12	175 HMIO
038 HA31	084 CLAMPA20*	130 SA13	176 HD15
039 HRDY*	085 TC	131 SA14	177 HD14
040 HBEN3	086 SD0	132 SA15	178 HD13
041 HBEN2	087 SD1	133 SA16	179 HD12
042 HBEN1	088 SD2	134 SA17	180 HD11
043 HBEN0	089 SD3	135 SA18	181 HD10
044 HADS*	090 SD4	136 SA19	182 HD9
045 BS16*	091 SD5	137 LBHEN	183 HD8
046 VCC	092 GND	138 GND	184 VCC

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Local Bus Interface

CLAMPA20*	35	I	Gate A20, active low. When Active, HA20 should be asserted as low regardless of what the real level of the line is.When high, HA20 should be unchanged.
HA31,HA[31:17] [16:2]	172-183, 1-15	I	Host Address Bus. These lines are inputs and are used to determine if the address of a device currently accessed is a DRAM "hit", meaning if the cycle belongs to the DRAM controller. Usually, these lines are driven by the CPU except forDMA Cycles when they are driven by the HT321.
HADS*	34	I	Host Address Strobe, active low. Defines the beginning of the cycle or pipelined cycle.
HBEN[3:0]	158-155	I	Host Byte Enables, active low. These signals define which bytes contain Valid transfer Data.During DAM Cycles they will be driven by the HT321.During DRAM Read Cacheable Cycles the state of these signals has no meaning. All four(4) Bytes must be presented to the Host Data Bus.
HCLK2	163	I	Host Clock. This clock drives the entire chip.
HD[31:0]	57-48, 44-39, 33-25,22-16	I/O	Host data bus. Data from the DRAM/Cache Controller is driven to the Bus during Reads and accepted from the Bus during Writes.
HHLDA	37	I	Hold acknowledge. This signal is used only to determine the real value of HA and DMA bridge path. Active high signal.
HLOCAL*	166	I/O	Host Local, active level. Asserted when the DRAM Controller decodes a Valid address for a DRAM Operation (memory cycles) or configuration operation (I/O cycles). Aserted one clock after HADS* and will remain low for one clock. It will then be driven high and tri-stated. data will be transfered. During DMA these lines will be driven by the HT321.
HLOCRDY*	75	I	Local Ready In,active low. Provides for a Direct Local Ready Path.Allows for connection of less flexible Local Bus Devices.
HMIO, HDC, HWR	160, 165, 164	I	Host Status Line bus: HMIO, HDC, HWR. Host Memory I/O, Host Data Code, Host Write Read. These signals, qualified at HADS*, define the type of CPU access. During DMA or Backplane MASTER accesses,these lines will be driven by the HT321.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
HRDYI*	36	I		Host Ready In, active low. This is the signal that terminates any cycle on the Local Bus. It comes from an external combinatorial logic and is the READY that goes to the host and terminates the cycle.
HRDY*	167	I/O		Host Ready, active low. This signal is active to indicate readiness to terminate the cycle. This signal will last one HCLK2, then will be driven high and tri-stated.
HREFRESH*	38	I/O		Host Refresh, active low. This signal indicates to the DRAM Controller and Backplane that a Refresh should occur.
HRESCPU	159	I		Host reset, active high. When this signal occurs, the processor is being reset. This signal will be asserted by the HT321 when a System Reset occurs, when a Shutdown is detected, when RC occurs, and when Fast Reset occurs.
PARITY*	58	I/O		Parity Check, active low. This signal goes active when a memory device on the Local Bus detects a parity error. It remains active for 1 HCLK2 then is driven high and tri-stated. The DRAM controller will generate the signal when it detects a Parity Error during a DRAM cycle.
POR	171	I		Power On Reset, active low. This is the Power on Reset that indicates the entire system is being reset.
TESTIN	45	I		Input for Test Patterns or other Test Activation. As a default it is a Tri-State enable pin. When it is asserted low in its default state, all outputs are tri-stated. This may be used by In Circuit Testers to synchronise Test Phases and Data.

DRAM Interface

BANKSELEVN	84	O		This line selects the Bank Accessed in the even group of Banks. It is used to multiplex CASEVN*[0:3] directing them to the appropriate bank.
BANKSELODD	85	O		This line selects the Bank currently Accessed in the Odd group of Banks. It is used to multiplex CASODD*[0:3] directing them to the appropriate bank.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Pin Descriptions

T-49-17-15

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
CASEVN*[3:0]	111-108	O		Four CAS signals for each Even Bank of the DRAM memory. There is one CAS line per byte. These signals should be multiplexed using BANKSELEVN signals to access the selected bank. Active low signals.
CASODD*[3:0]	107-104	O		Four CAS signals for each Odd Bank of the DRAM Memory. There is one CAS line per byte. These signals should be multiplexed using BANKSELODD signal in order to access the selected bank.Active low signals.
MA[11:1]	100-94, 91-88	O		These are address lines connecting to the memory address lines of the DRAMs.
MAEVN0	87	O		This is the Lower Address line connected to the Least Significant Memory Address line of the Even Banks of DRAM.
MAODD0*	101	O		This is the Lower Address line connected to the Least Significant Memory Address line of the Odd Banks of DRAM.
MD[31:0]	168-170, 154-140, 137-126, 123-122	I/O		This is the dedicated 32-bit Data Bus for the DRAM.
PARD[3:0]	121-118	I/O		These are Parity Data lines of the DRAM. One Bit per Byte of DRAMs.
RAS*[3:0]	117,114-112	O		RAS signals to each of the four banks of DRAM Memory. RAS0 corresponds to the first bank, RAS1 to the second, etc. Active low signals.
WEN	86	O		Write Enable. The signal to drive all WE pins of the Banks of DRAM.

Cache Control Signals

CA0	74	O		This is the Least Significant Address line to the Data Cache SRAM. It is required for Address Prediction and Interleaving during bursting.
CA1	83	O		This is the second Lowest Address line to both of the Data Cache SRAM Banks A and B. It is required for Address Prediction.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HTK320
386DX Chip Set

T-49-17-15

HT322 Pin Descriptions

Pin Name	Pin Number	Pin Type	Internal Pull Up/Dn	Description
CALE	80	O		This signal is used to latch addresses for certain types of SRAM in Cache Configuration.
CHIPSEL*[3:0]	79-76	O		These are Byte Selects connected to CS lines of SRAM, enabling individual Bytes during Write hit/miss updates.
FLUSH*	66	I		Active low. This signal flushes the entire Cache Directory Invalidating all Tags.
NON_CACHE*	67	I		Active low. This signal provides for external control of the Cacheability of a Cycle.
OEA*,OEB*	71	O		These are output enables for two Banks of Data Cache SRAM.
WEA*,WEB*	72,73	O		These are write enables for two Banks of Data Cache SRAM.

NPU Interface

BUSY387*	61	I		BUSY 387. Connects to the "BUSY" line of the 80387 Co-processor.
BUSY386*	62	O		BUSY 386. Connects to the "BUSY" line of the 80386 processor.
ERROR387*	63	I		ERROR (Co-processor). This line signals a Co-processor Error has occured and connects to the ERROR line of the 80387.
ERROR386*	64	O		ERROR (Co-processor). This line signals to the CPU that a Co-processor Error has occurred.
IRQ13	65	O		Interrupt line 13 for Coprocessor error reporting.
PEREQ387	59	I		Processor Extension Request. Connect to the "PEREQ" line of the 80387 NPU.
PEREQ386	60	O		Processor Extension Request. Connect to the "PEREQ" line of the 80386 CPU.
VCC	24,46,70,82,93 102,115,125, 138,161,184			Power
GND	23,47,69,81, 92,103,116, 124,139,162			Ground

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

Pin Names in Alphabetical Order

BANKSELEVN	84
BANKSELODD	85
BUSY386*	62
BUSY387*	61
CA1	83
CA0	74
CALE	80
CASEVN*[3:0]	111-108
CASODD*[3:0]	107-104
CHIPSEL*[3:0]	79-76
CLAMPA20*	35
ERROR386*	64
ERROR387*	63
FLUSH*	66
GND	23,47,69,81,92,103, 116,124,139,162
HA[2:31]	15-1,183-172
HADS*	34
HBEN[3:0]	158-155
HCLK2	163
HDC	165
HD[31:0]	57-48,44-39,33-25,22-16
HHLDA	37
HLOCAL*	166
HLOCRDY*	75
HMIO	160
HREFRESH*	38
HRESCPU	159
HRDY*	167
HRDYI*	36
HWR	164
IRQ13	65
MA[11:1]	100-94,91-88
MAEVN0	87
MAODD0	101
MD[31:0]	168-170,154-140,137-126, 123-122
NON-CACHEN	67
OEA*	71
OEB*	68
PARD[3:0]	121-118
PARITY*	58
PEREQ386	60
PEREQ387	59
POR	171
RASN[3:0]	117,114-112
TESTIN	45
VCC	24,4670,82,93,102, 115,125,138,161,184
WEN	86
WEA*	72
WEB*	73

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Pin Names and Numbers in Numerical Order

001 HA16	047 GND	093 VCC	139 GND
002 HA15	048 HD22	094 MA5	140 MD14
003 HA14	049 HD23	095 MA6	141 MD15
004 HA13	050 HD24	096 MA7	142 MD16
005 HA12	051 HD25	097 MA8	143 MD17
006 HA11	052 HD26	098 MA9	144 MD18
007 HA10	053 HD27	099 MA10	145 MD19
008 HA9	054 HD28	100 MA11	146 MD20
009 HA8	055 HD29	101 MAODD0	147 MD21
010 HA7	056 HD30	102 VCC	148 MD22
011 HA6	057 HD31	103 GND	149 MD23
012 HA5	058 PARITY*	104 CASODD0*	150 MD24
013 HA4	059 PEREQ387	105 CASODD1*	151 MD25
014 HA3	060 PEREQ386	106 CASODD2*	152 MD26
015 HA2	061 BUSY387*	107 CASODD3*	153 MD27
016 HD0	062 BUSY386*	108 CASEVN0*	154 MD28
017 HD1	063 ERROR387*	109 CASEVN1*	155 HBEN0
018 HD2	064 ERROR386*	110 CASEVN2*	156 HBEN1
019 HD3	065 IRQ13	111 CASEVN3*	157 HBEN2
020 HD4	066 FLUSH*	112 RAS0*	158 HBEN3
021 HD5	067 NON-CACHEN	113 RAS1*	159 HRESCPU
022 HD6	068 OEB*	114 RAS2*	160 HMIO
023 GND	069 GND	115 VCC	161 VCC
024 VCC	070 VCC	116 GND	162 GND
025 HD7	071 OEA*	117 RAS3*	163 HCLK2
026 HD8	072 WEA*	118 PARD0	164 HWR
027 HD9	073 WEB*	119 PARD1	165 HDC
028 HD10	074 CA0	120 PARD2	166 HLOCAL*
029 HD11	075 HLOCRDY*	121 PARD3	167 HRDY*
030 HD12	076 CHIPSEL0*	122 MD0	168 MD31
031 HD13	077 CHIPSEL1*	123 MD1	169 MD30
032 HD14	078 CHIPSEL2*	124 GND	170 MD29
033 HD15	079 CHIPSEL3*	125 VCC	171 POR
034 HADS*	080 CALE	126 MD2	172 HA31
035 CLAMPA20*	081 GND	127 MD3	173 HA27
036 HRDYI*	082 VCC	128 MD4	174 HA26
037 HHLDA	083 CA1	129 MD5	175 HA25
038 HREFRESH*	084 BANKSELEVN	130 MD6	176 HA24
039 HD16	085 BANKSELODD	131 MD7	177 HA23
040 HD17	086 WEN	132 MD8	178 HA22
041 HD18	087 MAEVN0	133 MD9	179 HA21
042 HD19	088 MA1	134 MD10	180 HA20
043 HD20	089 MA2	135 MD11	181 HA19
044 HD21	090 MA3	136 MD12	182 HA18
045 TESTIN	091 MA4	137 MD13	183 HA17
046 VCC	092 GND	138 VCC	184 VCC

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD + 0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Ambient Temperature Range (Commercial)	TA	0 to +70	C

DC Characteristics: VDD = 5V +/- 5%, TA = 0C to 70C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High HADS*,HD[15:0],HREFRESH*,LBHEN,LA[23:17] SA[19:0],SD[15:0],BCLK,BALE,RESETDRV,MEMR* MEMW*,SMEMR*,SMEMW*,IOW*,IOR*,AEN DACK*[7:5,3:0],TC,IOCHRDY	VOH	IOH = 8mA	2.4	4.5		V
HA[31,27:2],HBEN[3:0],HRDY*,HMIO,HDC,HWR HNA*,HRESCPU,BS16*,HOLDREQ,NMI,INT RESET387,SPKR,ROMEN,KBCS*,RTCCS* CLAMPA20*		IOH= 4mA	2.4	4.5		
Voltage Output Low HADS*,HREFRESH*,LBHEN,LA[23:17],SA[19:0] SD[15:0],BCLK,BALE,RESETDRV,MEMR*, MEMW*,SMEMR*,SMEMW*,IOW*,IOR*,AEN, DACK*[7:5,3:0],TC,IOCHRDY,HD[15:0]	VOL	IOL= 16mA	0.4	0.8		
HA[31,27:2],HBEN[3:0],HRDY*,HMIO,HDC,HWR, HNA*,HRESCPU,BS16*,HOLDREQ,NMI,INT RESET387,SPKR,ROMEN,KBCS*,RTCCS* CLAMPA20*		IOL = 8mA	0.4	0.8		
Tri-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	1	10	uA
Output Short Circuit Current	IOS	VDD=Max, VO=VDD VDD=Max, VO=0V	20 -10	110 -90	220 -190	mA mA
Supply Current	IDD	CLK= 25 MHz CL=50pF				mA

Note: Not more than one Output may be shorted at a time, for a maximum duration of ONE SECOND.

Figure 5.1 - HT321 DC Specifications

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Absolute Maximum Ratings (Referenced to

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD + 0.	V
DC Input Current	IIN	10	mA
Storage Temperature Range (plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Ambient Temperature Range (Commercial)	TA	0 to +70	C

DC Characteristics: VDD = 5V +/- 5%, TA = OC to 70C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High	VOH		2.4	4.5		V
CA1 , CA0		IOH = 12mA	2.4	4.5		
HD[31:0] ,RAS*{1;0] MA[1:11] OEA* , OEBN*, WEA* , WEB*, CALE		IOH = 8mA				
HRDY*,HLOCAL*,HLOCRDY,PARITY*,RAS*[3:2] CASEVN*[3:0],CASODD*[3:0],MAEVNO,MAODDO BANKSELEVN,BANKSELODD,WEN,PARD[3:0] MD[31:0],CHIPSEL*[3:0],PEREQ386,BUSY386 ERROR386,IRQ13		IOH= 4mA				
Voltage Output Low	VOL					
CA1 , CA0		IOL = 12mA				
HD[31:0] ,RAS*{1;0] MA[1:11] OEA* , OEB* , WEA* , WEB*, CALE		IOL= 8mA	0.4	0.8		
HRDY*,HLOCAL*HLOCRDY,PARITY*,RAS*[3:2] CASEVN*[3:0],CASODD*[3:0],MAEVNO,MAODDO BANKSELEVN,BANKSELODD,WEN,PARD[3:0] MD[31:0],CHIPSELN[3:0],PEREQ386,BUSY386 ERROR386,IRQ13		IOL = 4mA	0.4	0.8		
Tri-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	1	10	uA
Output Short Circuit Current	IOS	VDD=Max, VO=VDD	20	110	220	mA
Supply Current	IDD	CLK= 25 MHz CL=50pF		???		mA

Note: Not more than one Output may be shorted at a time, for a maximum duration of ONE SECOND.

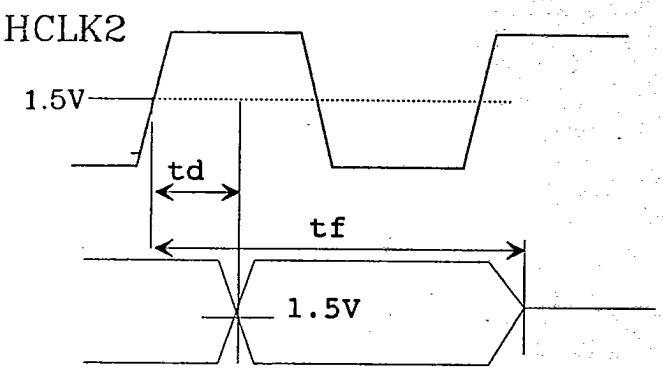
Figure 5.2 - HT322 DC Specifications

Powered by ICminer.com Electronic-Library Service CopyRight 2003

SYMBOL	Parameter	Min	Max	Unit	Fig Ref	Notes
t201	HCLK2		80	MHz		Duty Cycle 50%+/-5%
t202	HRESCPU Setup	4		nS		
t203	HRESCPU Hold	2	0	nS		
t204	HMIO,HWR,HDC,HBEN[3:0],HHLDA Setup	10		nS		Note 2
t205	HMIO,HWR,HDC,HBEN[3:0],HHLDA, Hold	4		nS		
t206	HA31,HA[27:2], CLAMPA20* Setup	10		nS		
t207	HA31,HA[27:2], CLAMPA20* Hold	4		nS		
t208	HADS* Setup	10		nS		Note 2
t209	HADS* Hold	4		nS		Note 2
t210	HRDYI* Setup	10		nS		Note 2
t211	HRDYI* Hold	2		nS		Note 2
t212	POR,HREFRESH*,FLUSH* Setup	10		nS		Note 1
t213	POR,HREFRESH*,FLUSH* Hold	4		nS		Note 1
t214	NON-CACHE* Setup	6		nS		Note 7
t215	NON-CACHE* Hold	3		nS		Note 3
t216	PEREQ387,BUSY387,ERROR387 Setup	4		nS		Note 2
t217	PEREQ387,BUSY387,ERROR387 Hold	3		nS		Note 2
t218	HD[31:0] Write Setup	10		nS		Note 2
t219	HD[31:0] Write Hold	4		nS		Note 2
t220	HD[31:0]Read Delay		10	nS		Note 2
t221	HD[31:0] Read Float Delay		15	nS		Note 3
t222	PARD,MD[31:0] Read Setup	3		nS		Note 2
t223	PARD,MD[31:0] Read Hold	3		nS		Note 2
t224	PARD,MD[31:0] Write Valid Delay		15	nS		Note 2
t225	PARD,MD[31:0] Write Float Delay		15	nS		Note 2
t226	HRDY* Valid Delay		10	nS		Note 2
t227	HRDY* Float Delay		15	nS		Note 2
t228	HLOCAL* Valid Delay		10	nS		Note 2
t229	HLOCAL* Float Delay		15	nS		Note 3
t230	PARITY* Valid Delay		8	nS		Note 2
t231	PARITY* Float Delay		15	nS		Note 3
t232	RAS* Delay CASEVN*[3:0] Delay CASODD*[3:0] Delay WEN,BANKSEL-EVN/ODD Delay	5 7 7 5	15 20 20 15	nS		Note 2
t233	MA[11:1],MAEVNO, MAODDO Delay	8	21	nS		Note 4
t234	OEA*,OEB*,WAE*,WEB* Delay	8	10	nS		Note 5
t235	CALE Delay		15	nS		Note 6
t236	CA!,CAO,CHIPSEL*[3:0] Delay		10	nS		Note 8
t237	PEREQ386,BUSY386,ERROR386 Delay	4	8	nS		Note9
t238	PEREQ386,BUSY386,ERROR386 Valid Delay		8	nS		Note 2

Figure 5.3 - HT321 AC Characteristics

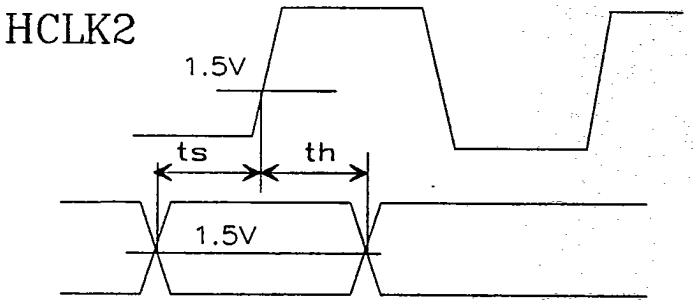
Powered by ICminer.com Electronic-Library Service CopyRight 2003




```
td = t224,t226,t228,t230,t232,t233,t234,t235,t238
tf = t221,t225.t227.t229.t231
```

Note 1: The requirement specified is non-linked. It should be fulfilled for the clock edge where it is to be recognised.

Figure 5.4




```
ts = t202,t204,t206,t208,t210,t212,t214,t216,t218,t222
th = t203,t205,t207,t209,t211,t213,t215,t217,t219,t223
```

Note 2: The parameters relate to HCLK2 clock beginning PUI1 of the CPU.

Note 3: The parameters releate to HCLK2 clock beginning PHI of the CPU

Note 4: The parameters relate to either the clock edge beginning PHI1 or PHI2 dependant upon the timing shown.

Note 5: OEA*, OEB* always relate to the clock edge beginning PHI1, WEA*, WEB* to both, dependant on the timing option.

Note 6: Falling edge of CALE relates to the clock edge beginning PHI1, Rising edge to PHI2.

Figure 5.5

Powered by ICminer.com Electronic-Library Service CopyRight 2003

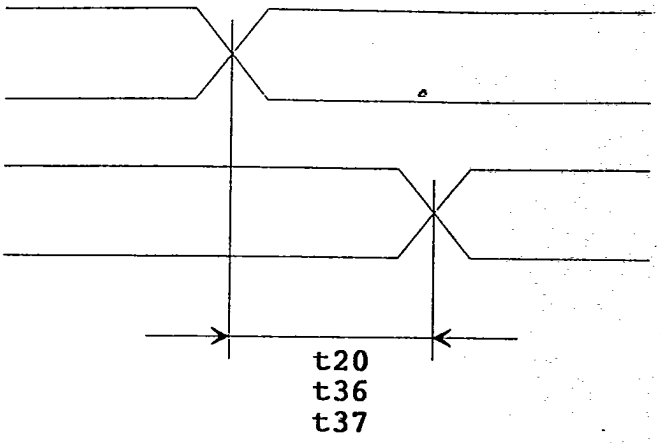


Figure 5.6 - Asynchronous Delays

Note 7: HD[31:0] Read Delay is an asynchronous delay from the MD[31:0] bus.

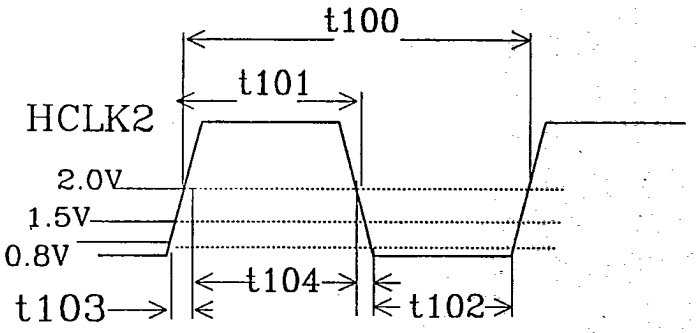
Note8: CA1, CA0 delays are both asynchronous delays from HA2, HA3 and HCLK2 clock edge beginning PHI1. CHIPSEL* delay is an asynchronous delay from HBEN[3:0] and HWR.

Note 9: Pereq386, BUST386, ERROR386 delays are asynchronous delays from PEREQ387, BUSY387, ERROR387 respectively.

SYMBOL	Parameter	Min	Max	Unit	Fig Ref	Notes
HCLK2	Frequency	0	80	MHz		1x Clock Driven to ??
t100	HCLK2 Period	12.5		nS		
t101	HCLK2 High Time	5		nS		At +2.0 Volts
t102	HCLK2 Low Time	5		nS		At 0.8 Volts
t103,t104	HCLK2 Rise/Fall Time		3	nS		
t105	HA[31,27:2],HADS*,HRDY*,BS16*,HBEN[3:0] REFRESH*,HNA*,HMIO,HDC,HWR Valid Delay		13	nS		
t106	RESET387,HRESCPU Valid Delay		7	nS		
t107	HOLDREQ,BCLK Valid Delay		10	nS		
t108	HADS*,HRDYI*,HBEN[3:0],HMIO,HDC,HWR HHLDA,MASTER*,HLOCAL*,POR,HA[31,27:2] HD[15:0],(for Writes) SETUP	6		nS		
t109	HADS*,HRDYI*,HBEN[3:0],HMIO,HDC,HWR HHLDA,MASTER*,HLOCAL*,POR,HA[31,27:2] HD[15:0],(for Writes) HOLD	4		nS		
t110	SD to HD for CPU Reads SETUP		13	nS		
t111	PARITY* to NMI DELAY		15	nS		
t112	KB_CLAMPA20* to CLAMPA20* DELAY		14	nS		NMI Mask is OFF

Figure 5.7 Local Bus Interface

Powered by ICminer.com Electronic-Library Service CopyRight 2003



HCLK2

Figure 5.8

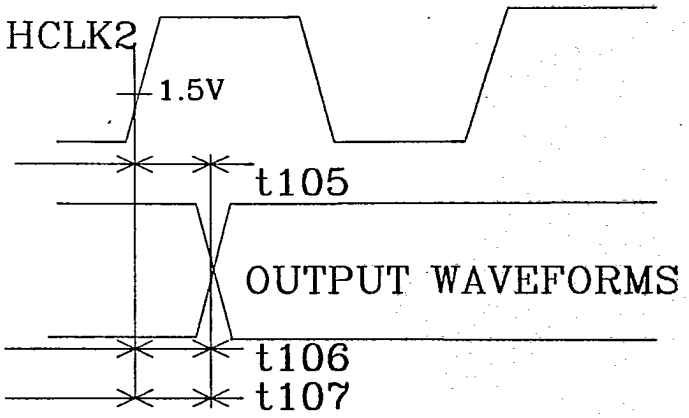
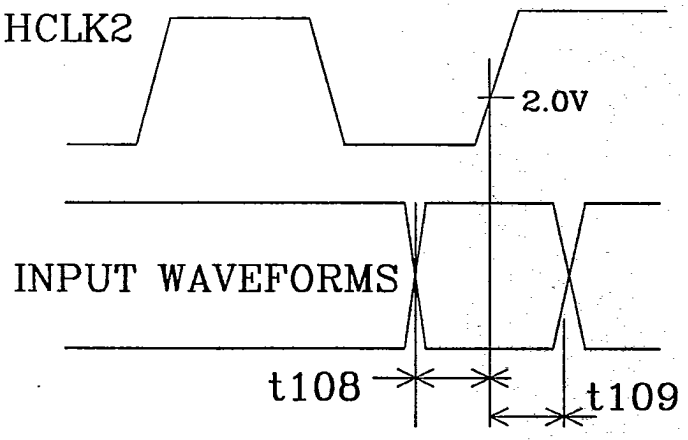


Figure 5.9



INPUT WAVEFORMS

Figure 5.10

Powered by ICminer.com Electronic-Library Service CopyRight 2003

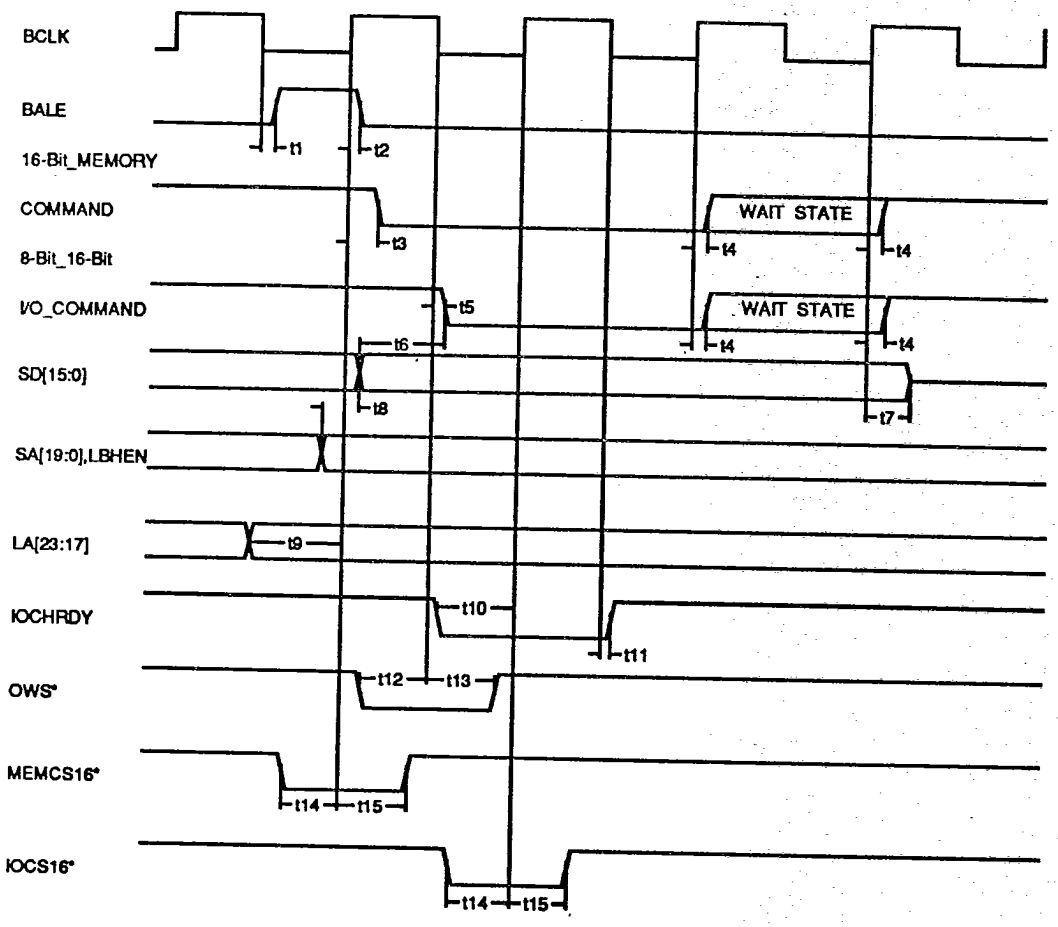


Figure 5.11 - ISA Backplane Interface

Powered by ICminer.com Electronic-Library Service CopyRight 2003

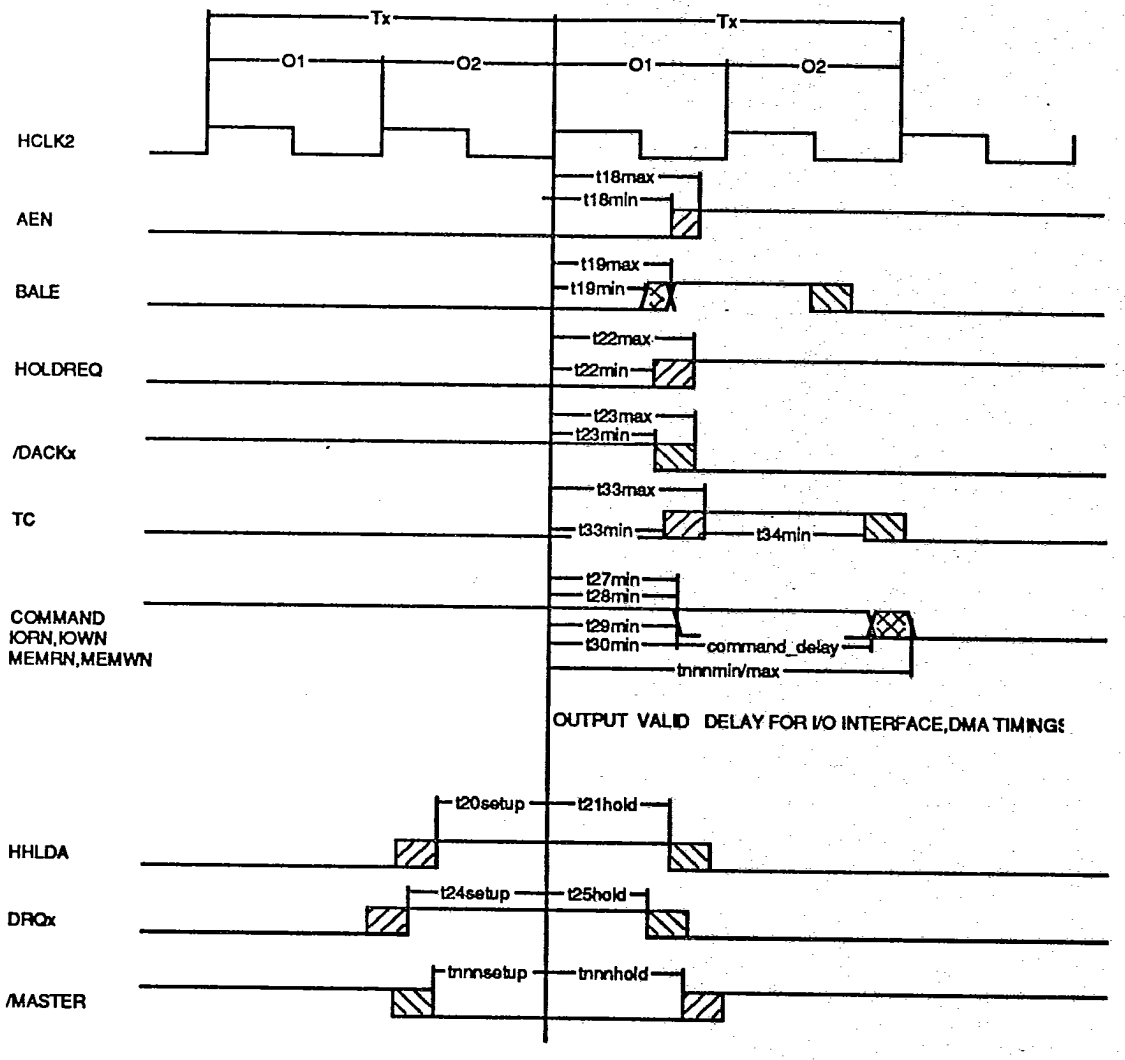


Figure 5.12 SETUP and HOLD Timing

Powered by ICminer.com Electronic-Library Service CopyRight 2003

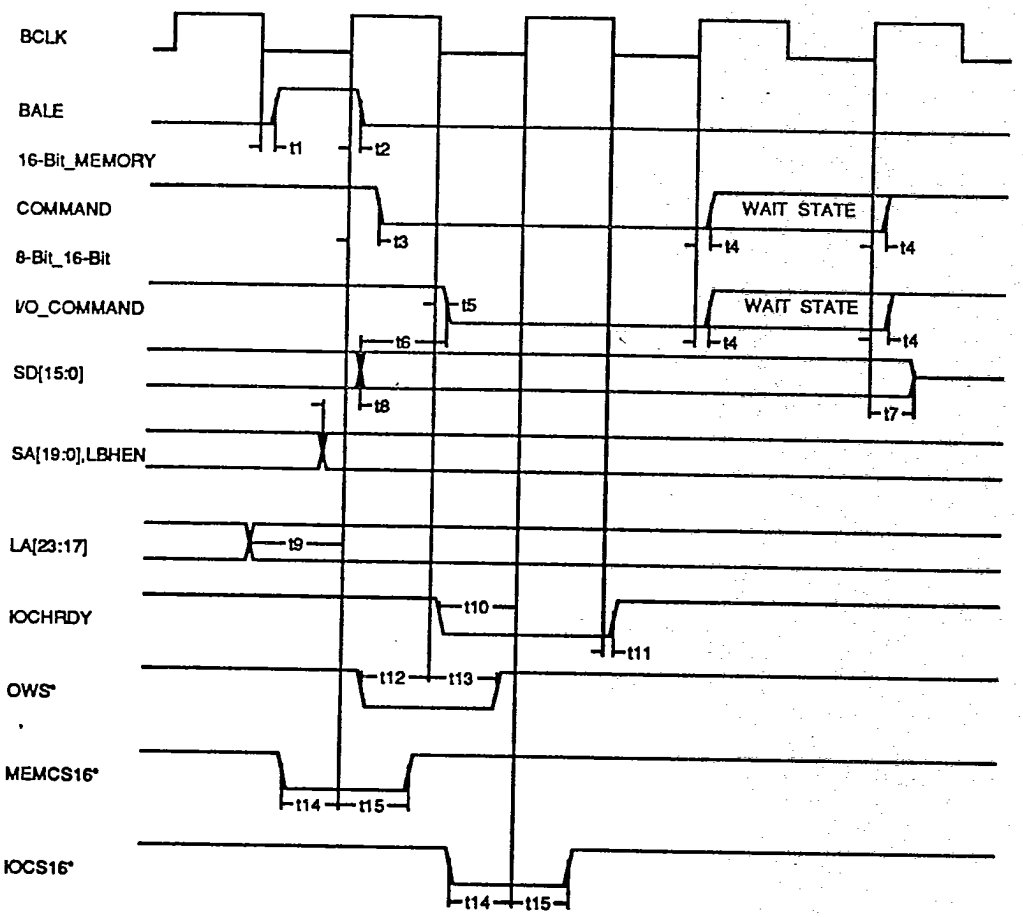


Figure 5.13 ISA Backplane Interface

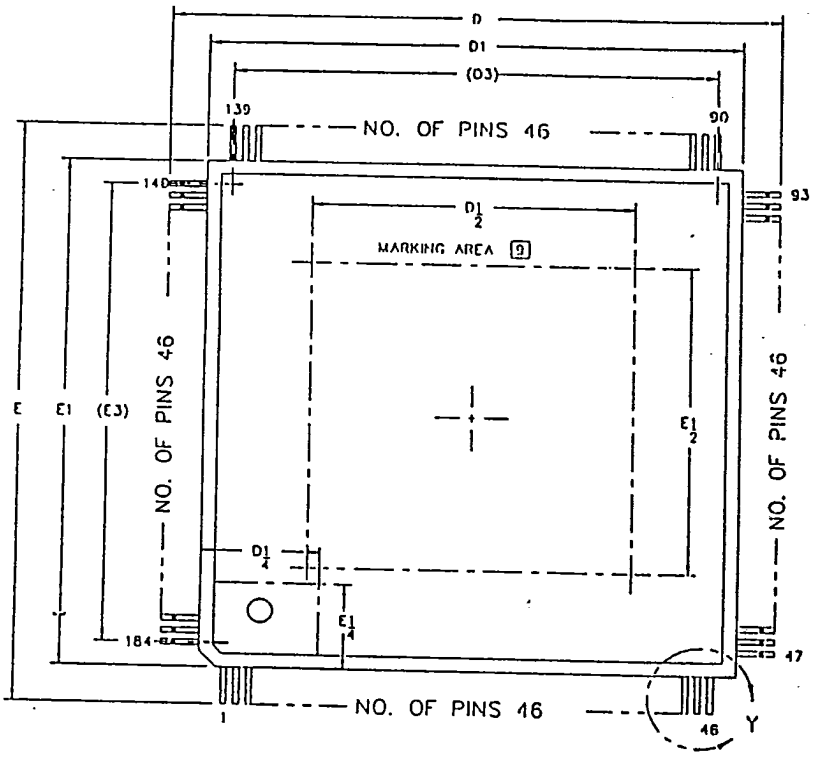
Powered by ICminer.com Electronic-Library Service CopyRight 2003

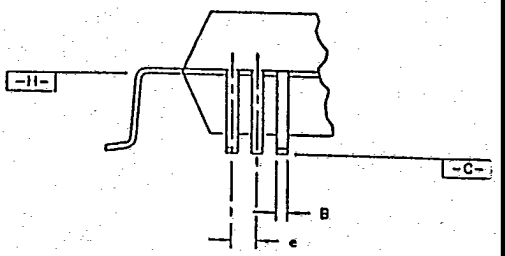
T-49-17-15

HTK320

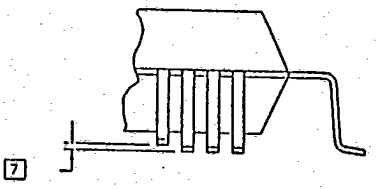
386DX Chip Set

Package Outline

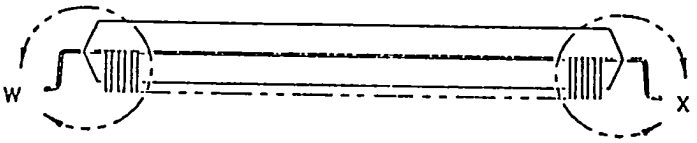


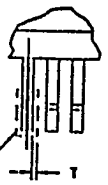


DETAIL W



DETAIL X





Tolerance window for lead skew from theroetical true position

DETAIL Y

*See notes next page

Dimensions in MM			
Sym	Minimum	Maximum	Note*
A1	0.25	0.36	
A2	3.40 + / - 0.10		
A3	1.60 + / - 0.05		
A4	1.60Ref.		
B	0.30 + / - 0.05		6, 10
C1	0.15 + / - 0.03		10
D	36.00 + / - 0.20		2
D1	32.00 + / - 0.10		3
D3	29.25 Ref.		11
E	36.00 + / - 0.20		2
E1	32.00 + / - 0.10		3
E3	29.25 Ref		11
e	0.65 Basc.		8
L	0.80 + / - 0.10		
M	1.60 Ref.		
R	0.19 + / - 0.06		
R1	0.13	-	
S	0.40	-	
T	-	0.1	12
Θ	2.5 + / - 2.5 Deg.		
Θ1	4 +/ - 4 Deg		
Θ2	10 + / - 2 Deg.		
Θ3	10 + / - 2 Deg.		
X	2.25 Ref.		
Y	0.38 + / - 0.1		
Z1	37.0 + / - 0.1		
Z2	32.0 + / - 0.1		
Total No of Pins	184		

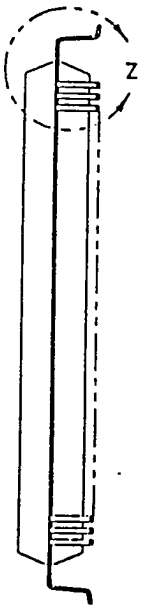
Powered by ICminer.com Electronic-Library Service CopyRight 2003

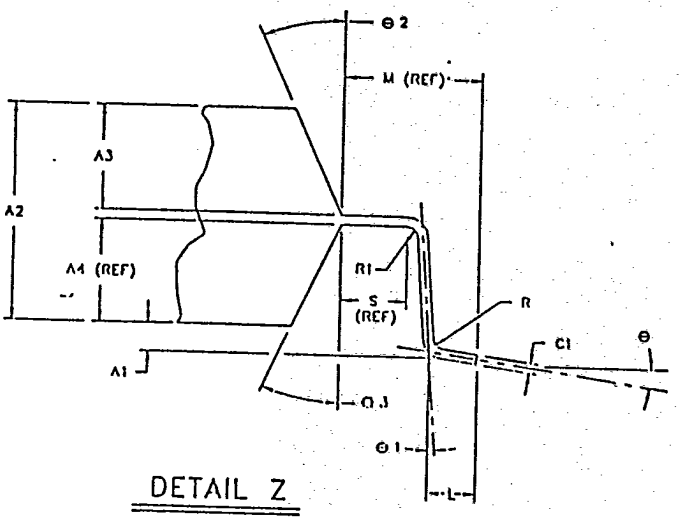
T-49-17-15

HTK320

Package Outline

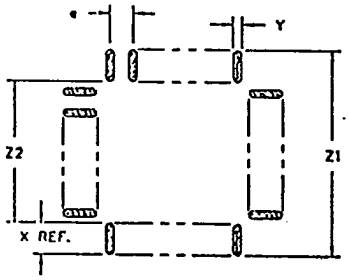
386DX Chip Set





DETAIL Z

SUBSTRATE RECOMENDED LAND PATTERN



NOTES: Unless otherwise specifies

1. Datum plane - H - located at mold parting line and is coincident with the bottom of lead, where the lead exits the plastic body.
2. To be determined at seating plane - C -.
3. Dimension D1 and E1 do not include mold protusion. Allowable protusion is .25mm per side.
4. These dimensions to be determined at datum plane - H -.
5. All dimensions in milimeters. Controlling dimension in milimeters. Inches shall be rounded to nearest .001 inch.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot minimum space between adjacent leads to be 0.07.
7. Coplanarity of all leads shall be within 0.076mm. Difference between highest and lowest lead with seating plane - C - as reference.
8. Lead pitch determined at datum - H -.
9. Marking area free of protrusion and intrusion.
10. Plating thickness included. Plating thickness to be 0.005mm Minimum; 0.020mm Maximum.
11. Dimension D3 and E3 to centered relative to dimension D1 and E1 within + / - 0.15mm respectively.
12. From true lead location measured at seating plane - C -

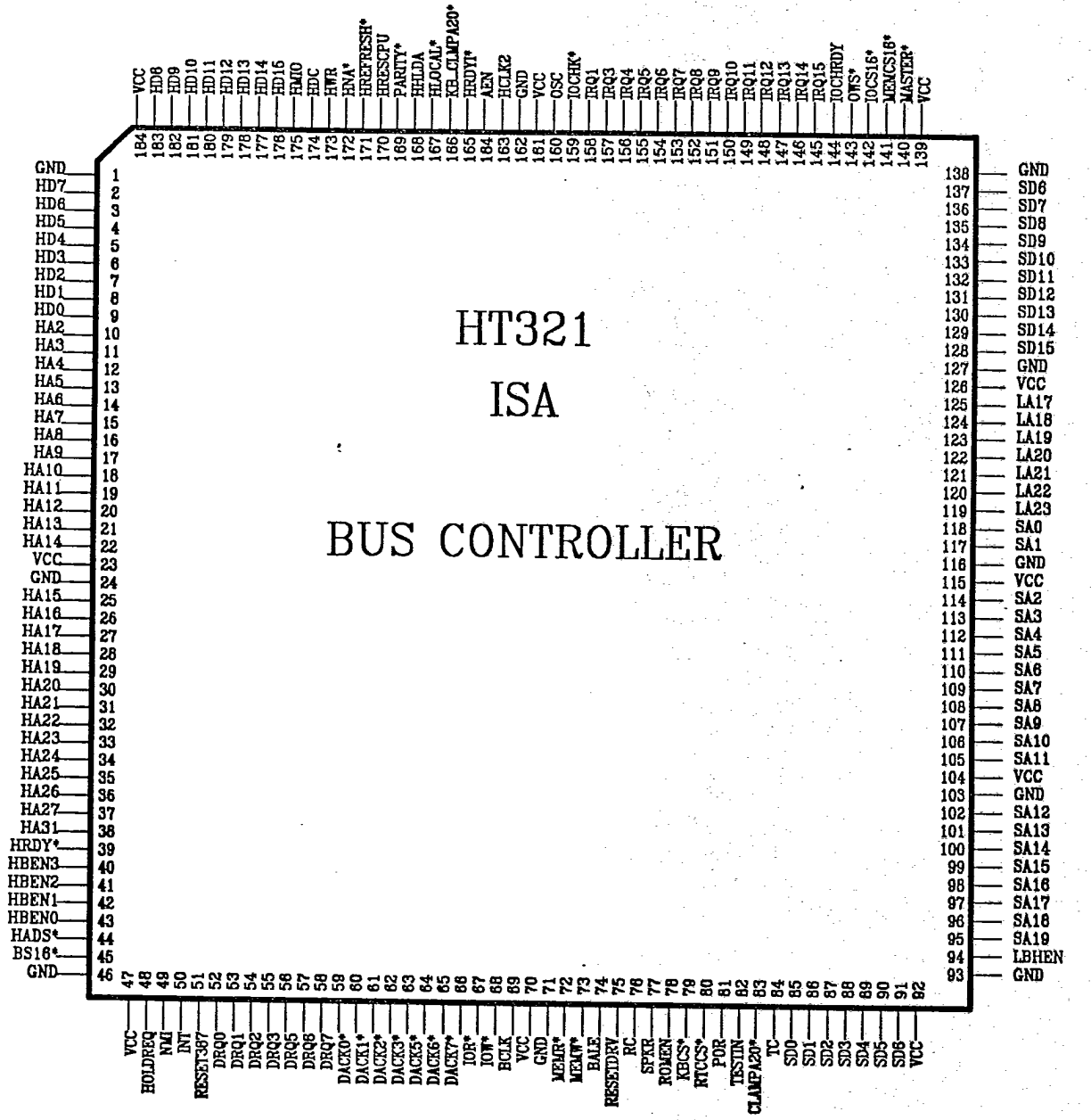
Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

HTK320

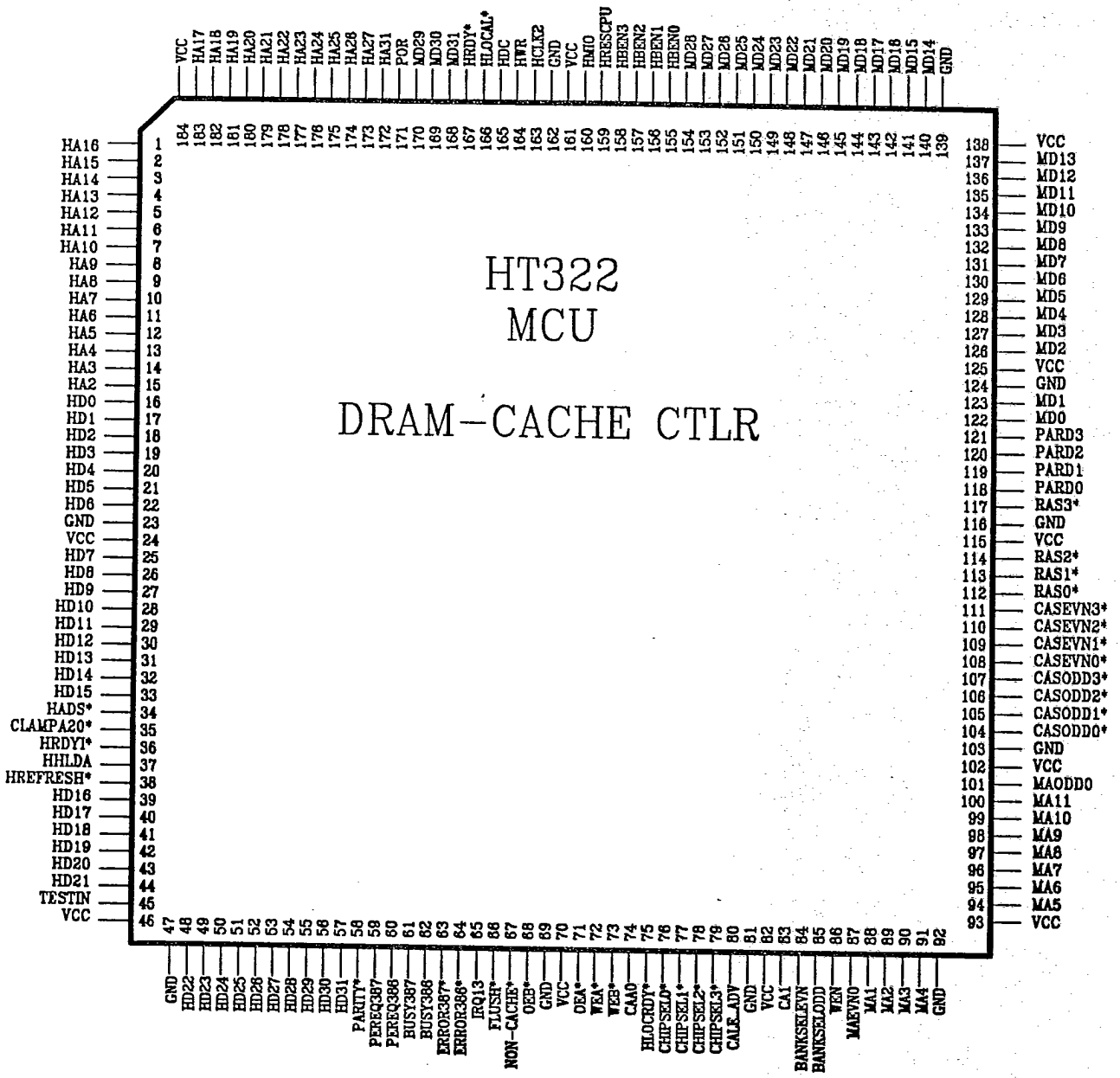
386DX Chip Set

HT321 Pin Package



Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 Pin Package



Powered by ICminer.com Electronic-Library Service CopyRight 2003

NANDTREE Test of the HTK320 Chip Set

Testing features are included in the design of the chip set. An outline of these features follows along with the information which will support their use.Most of the active pins of the HT321 (84%) and HT322 (70%) can be tri-stated. PCB connection to the device pins can be confirmed by use of NANDtree control and toggling of output pins. If a Manufacturing Test Strategy is incorporated into the overall PCB design along with necessary Test Tools high functional integrity may be achieved. Systems and Chip level simulation testing are possible since the chip set was developed utilizing high level VHDL tools. VHDL allows for complete systems, backplane and peripheral device simulation testing before prototyping.

Tri-stateability

The HT321 and HT322 can be isolated from the rest of a PCB by placing them in their test mode. This will allow use of test tools such as Bed-of-Nails to probe and isolate circuit faults on a PCB.

HT321 NANDTREE Sequence

(1) Set the tri-stateable bi-directional pins to Z state and the other input pins to any logical state.(see list B for definition of tri-state pins and their numbers.) These values simulate the device at Power-up.

(2) After the network is settled, set the following inputs to the specified states.

A: Set the following inputs to a Logical 0 : POR(82)

B: Set the following inputs to a Logical 1 :

MASTER*(14), MEMCS16*(141), IOCS16*(142), 0WS*(143), IOCHRDY(144), IRQ15(145), IRQ14(146), IRQ13(147), IRQ11(149), IRQ10(150), IRQ9(151), IRQ8(152),IRQ7(153), IRQ6(154), IRQ5(155), IRQ4(156), IRQ3(157), IRQ1(158), IOCHK*(159), OSC(160), HRDYI*(165), KB_CLAM-PA20*(166), HLOCAL(167), HHLDA(168), PARITY*(169), DRQ0(52), DRQ1(53), DRQ2(54), DRQ3(55), DRQ5(56), DRQ6(57), DRQ7(58), RC(77), TESTIN(83)

C: Set the tri-stateable inputs to Z state, per LIST B

The bi-directional Pins are "inputs " only when the TESTIN(83) input is set to a Logical 1 (3) After the network is settled set all inputs in their NANDtree initialization states as follows :

A: Set POR(82) to Logical 0 .

B: Set all other inputs to Logical 1 .

(4) With the inputs set as in (3)

A: Set POR(82) to Logical 1 for two complete Test Cycles.

B: Set POR(82) to Logical 0 for one complete Test Cycle.

C: Set POR(82) to Logical 1 for the start of the NANDtree sequence.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

(5) One at a time, change the state of the inputs from a Logical 1 to 0 , as per LIST A sequence .

The sample results of NANDtree test at the NANDtree output Pin KBCS*(80). The output at this pin will toggle Logical value with each cycle of state change of the input from Logical 1 to 0.

LIST A : The NANDtree sequence.

CLAMPA20*(84),SD0(86),SD1(87),SD2(88),SD3(89),SD4(90),SD5(91),SD6(94),SD7(95), SD8(96),SD9(97),SD10(98),SD11(99),SD12(100),SD13(101),SD14(102),SD15(103),LA17(106), LA18(107),LA19(108),LA20(109),LA21(110),LA22(111),LA23(112),SA0(113),SA1(114),SA2(117), SA3(118),SA4(119),SA5(120),SA6(121),SA7(122),SA8(123),SA9(124),SA10(125),SA11(126),SA12(129), SA13(130),SA14(131),SA15(132),SA16(133),SA17(134),SA18(135),SA19(136),LBHE(137),MASTER*(1 40),MEMCS16*(141),IOCS16*(142),0WS*(143),IOCHRDY(144),IRQ15(145),IRQ14(146), IRQ13(147),IRQ11(149),IRQ10(150),IRQ9(151),IRQ8(152),IRQ7(153),IRQ6(154),IRQ5(155),IRQ4(156), IRQ3(157),IRQ1(158),OSC(160),HRDYI*(165),KB_CLAMPA20*(166),HLOCAL(167),HHLDA(168),PA RITY*(169),HREFRESH*(171),HWR(173),HDC(174),HMIO(175),HD15(176),HD14(177),HD13(178), HD12(179),HD11(180),HD10(181),HD9(182),HD8(183),HD7(2),HD6(3),HD5(4),HD4(5),HD3(6),HD2(7), HD1(8),HD0(9),HA2(10),HA3(11),HA4(12),HA5(13),HA6(14),HA7(15),HA8(16),HA9(17),HA10(18), HA11(19),HA12(20),HA13(21),HA14(22),HA15(25),HA16(26),HA17(27),HA18(28),HA19(29),HA20(30), HA21(31),HA22(32),HA23(33),HA24(34),HA25(35),HA26(36),HA27(37),HA31(38),HRDY*(39), HBEN3(40),HBEN2(41).HBEN1(42),HBEN0(43),HADS*(44),DRQ0(52),DRQ1(53),DRQ2(54),DRQ3(55), DRQ5(56),DRQ6(57),DRQ7(58),IOR*(66),IOW*(67), MEMR*(71),MEMW*(72), RC(77),POR(82), TESTIN(83) .

The NANDtree output Pin is:KBCS*(80)

LIST B : The tri-stateable bi-directional Pins

CLAMPA20*(84),SD0(86),SD1(87),SD2(88),SD3(89),SD4(90),SD5(91),SD6(94),SD7(95),SD8(96), SD9(97),SD10(98),SD11(99),SD12(100),SD13(101),SD14(102),SD15(103),LA17(106),LA18(107), LA19(108),LA20(109),LA21(110),LA22(111),LA23(112),SA0(113),SA1(114),SA2(117),SA3(118), SA 4(119) ,SA5(120),SA6(121),SA7(122),SA8(123),SA9(124),SA10(125),SA1 1(126),SA12(129) ,SA13(130),SA14(131),SA15(132),SA16(133),SA17(134),SA18(135),SA19(136),LBHE(137),RMASTER* (140),MEMCS16*(141),IOCS16*(142),0WS*(143),IOCHRDY(144),HREFRESH*(171), HWR(173),HDC(174),HMIO(175),HD15(176),HD14(177),HD13(178),HD12(179),HD11(180),HD10(181), HD9(182),HD8(183),HD7(2),HD6(3),HD5(4),HD4(5),HD3(6),HD2(7),HD 1(8),HD0(9),HA2(10),HA3(11), HA4(12), HA5(13),HA6(14), HA7(15),HA8(1 6),HA9(17),HA10(18),HA11(19), HA12(20),HA13(21), HA14(22),HA15(25),HA16(26),HA17(27),HA18(28),HA19(29),HA20(30),HA21(31),HA22(32), HA23(33),HA24(34),HA25(35),HA26(36),HA27(37),HA31(38),HRDY*(39),HBEN3(40),HBEN2(41), HBEN1(42), HBEN0(43), HADS*(44), IOR*(66), IOW*(67), MEMR*(71),MEMW*(72)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

HT322 NANDTREE Sequence

(1) Set the tri-stateable bi-directional Pins to Z state and the other input Pins to any Logical state.(see List B for definition of tri-state Pins and their numbers.) These values simulate the device at Power-up.

(2) After the network is settled, set the following inputs to the specified states.

A: Set the following inputs to a Logical 0 : POR(171),HRESCPU(159)

B: Set the following inputs to a Logical 1 :

HREFRESH*(38),HHLDA(37),HRDYI*(36),CLAMPA20*(35),HADS*(34),HA2(15),HA3(14), HA4(13),HA5(12),HA6(11),HA7(10),HA8(9),HA9(8),HA10(7),HA11(6),HA12(5),HA13(4),HA14(3), HA15(2),HA16(1),HA17(183),HA18(182),HA19(181),HA20(180),HA21(179),HA22(178),HA23(177), HA24(176),HA2 5(175),HA26(174),HA27(173),HA31(172),HDC(165),HWR(164),HMIO(163), HBEN3(158),HBEN2(157),HBEN1(156),HBEN0(155),NON_CACHEN(67),FLUSH*(66),ERROR387(63), BUSY387(61),PEREQ387(59),TESTIN(45)

C: Set the Tri-stateable inputs to Z state,as per LIST B (as set in step 1) The bi-directional Pins are inputs only when the TESTIN(45) input is set to a Logical 1 .

(3) After the network is settled, set all inputs in their NANDtree initialization states, as follows:

A: Set POR(171) and HRESCPU(159) to Logical 0 .

B: Set all other input pins to Logical 1 .

(4) Then with inputs set as in (3):

A:Set POR(171) to Logical 1 and HRESCPU(159) to Logical 0 for one Test Cycle.

B:Set POR(171) to Logical 1 and HRESCPU(159) to Logical 1 for one Test Cycle.

C:Set POR(171) to Logical 0 and HRESCPU(159) to Logical 0 for one Test Cycle.

D:Set POR(171) to Logical 1 and HRESCPU(159) to Logical 1 for the start of the NANDtree sequence.

(5) One at a time,change the state of the inputs from Logical 1 to 0 according to the sequence in LIST A .

Sample results of each NANDtree test at the NAND tree output pin IRQ1(65). The output will toggle logical values with each cycle of state change at the input from logical 1 to 0 .

Powered by ICminer.com Electronic-Library Service CopyRight 2003

T-49-17-15

LIST A:

HD21(44),HD20(43),HD19(42),HD18(41),HD17(40),HD16(39),HREFRESH*(38),HHLDA(37), HRDYI*(36),CLAMPA20*(35),HADS*(34),HD15(33),HD14(32),HD13(31),HD12(30),HD11(29), HD10(28),HD9(27),HD8(26),HD7(25),HD6(22),HD5(21),HD4(20),HD3(19),HD2(18),HD1(17),HD0(16), HA2(15),HA3(1 4),HA4(13),HA5(12),HA6(11),HA7(10),HA8(9),HA9(8),HA10(7),HA11(6), HA12(5),HA13(4),HA14(3),HA15(2),HA16(1),HA17(183),HA18(182),HA19(181),HA20(180),HA21(179), HA22(178),HA23(177),HA24(176),HA25(175),HA26(174),HA27(173),HA31(172),POR(171),MD29(170), MD30(169),MD31(1 68),HDC(165),HWR(164),HMIO(160),HRESCPU(159),HBEN3(158),HBEN2(157), HBEN1(156),HBEN0(155),MD28(154),MD27(153),MD26(152),MD25(151),MD24(150),MD23(149), MD22(148),MD21(147),MD20(146),MD19(145),MD18(144),MD17(143),MD16(142),MD15(141), MD14(140),MD13(137), MD12(136),MD11(135),MD10(134),MD9(133),MD8(132),MD7(131),MD6(130), MD5(129),MD4(128), MD3(127),MD2(126),MD1(123),MD0(122),PARD3(121),PARD2(120), PARD1(119),PARD0(118),NON_CACHEN(67),FLUSH*(66),ERROR387(63),BUSY387(61),RPEREQ38 7(59),HD31(57),HD30(56),HD29(55),HD28(54),HD27(53),HD26(52),HD25(51),HD24(50), HD23(49),HD22(48),TESTIN(45)

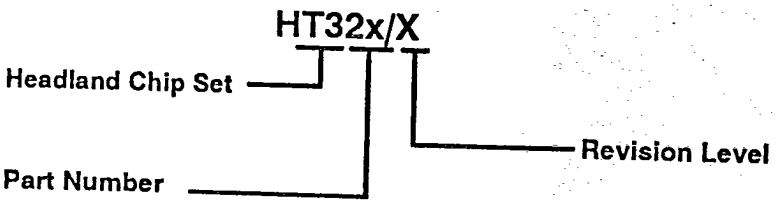
The NAND tree output pin is:IRQ13(65) .

LIST B: The tri-stateable bi-directional pins included in the NAND tree:

HD21(44),HD20(43),HD19(42),HD18(41),HD17(40),HD16(39),HD15(33),HD14(32),HD13(31), HD12(30),HD11(29),HD10(28),HD9(27),HD8(26),HD7(25),HD6(22),HD5(21),HD4(20),HD3(19), HD2(18), HD1(17),HD0(16),MD29(170),MD30(169),MD31(168),MD28(154),MD27(153), MD26(152),MD25(151),MD24(150),MD23(149),MD22(148),MD21(147),MD20(146), MD19(145), MD18(144), MD17(143),MD16(142),MD15(141),MD14(140),MD13(137),MD12(136), MD11(135), MD10(134), MD9(133),MD8(132),MD7(131),MD6(130),MD5(129),MD 4(128),MD3(127), MD2(126),MD1(123),MD0(122),PARD3(121),PARD2(120),PARD1(119),PARD0(118),HD31(57), HD30(56), HD29(55), HD28(54),HD27(53),HD26(52),HD25(51),HD24(50),HD23(49),HD22(48)

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Product Order Information



IMPORTANT: Contact your local sales office for the current Order Code/Part Number

Powered by ICminer.com Electronic-Library Service CopyRight 2003