Preliminary Technical Manual

FE3600 Chip Set

WESTERN DIGITAL

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GENERAL PRODUCT DESCRIPTION

1.0 Introduction

This document is the Technical Specification/OEM Manual for Western Digital ® Corporation's FE3600 chip set. This manual describes the electrical, physical, and functional features in detail.

Applications

The FE3600 is a highly-integrated chip set that allows designers to reduce chip count, increase flexibility, and provide improved operating speed and functionality for a 16 MHz IBM * PC/AT * compatible system board. The FE3600 chip set is extremely cost effective because it replaces approximately 60% of the components on a typical IBM AT motherboard and results in decreased size and power consumption. In addition, the FE3600 chip set devices are manufactured in surface-mountable packages which allows for a higher level of logic integration resulting in an extremely reliable device that occupies much less space.

1.1 Product Overview

The FE3600 chip set provides all necessary core logic to build a totally integrated IBM AT compatible motherboard using the 16-bit Intel * 80286 Central Processing Unit (CPU). The FE3600 chip set is 100% hardware (register level) and software compatible with the IBM PC/AT.

The FE3600 chip set consists of four devices:

- FE3001 AT CPU Control Logic
- FE3010B AT Peripheral Control Logic
- FE3021 AT Address Bus Buffer
- FE3031 AT Data Bus Buffer

Each of the four chips are covered in separate sections of this manual. A separate section is also provided to describe applications with the four chips working in tandem to provide a 100% PC/AT compatible solution.

1.2 Features

FE3001:

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an AT compatible computer. It's features include programmable CPU and DMA clock generation, system clock generation, programmable bus timing, programmable wait state generator, refresh and DMA controls, bus arbitration logic, NMI generator and parity error logic, reset/shutdown control, sleep mode, 80286 interface logic, and 84-pin PLCC design.

FE3010B:

The FE3010B AT peripheral control logic is a highly integrated 84-pin J-type chip with various control and peripheral functions. The FE3010B contains the functional equivalent of two 8237 DMA Controllers in cascade mode. This block improves the performance of a system by allowing external devices to transfer data directly from the system's memory. The FE3010B also contains the functional equivalent of two 8259 Interrupt Controllers in cascade mode. Additional features include 15 interrupt channels, 3 timer channels, 7 DMA channels, DMA page registers, 8 MHz DMA, and TTL compatibility. The FE3010B is designed to be upward-compatible with the Intel 80386 processor.

FE3021:

The FE3021 is a 16 MHz AT address buffer and memory controller in a 132-pin JEDEC package. Chip count is significantly reduced by integrating the memory controller, AT bus address buffers, and I/O into one chip. The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM. A maximum of 4 banks of DRAM can be controlled allowing a maximum of 8 MB of memory to be controlled by the FE3021. The DRAM bank locations are programmable on 64K byte boundries. One memory bank allows split addressing, so that one portion may be placed in real memory with the remainder in extended memory. FE3600 additional features include EMS 4.0 support, on-chip address and control signal buffers for directly driving the AT bus, zero wait state access at 16 MHz using 100 ns DRAM with page mode access, generation of chip selects for floppy controller, 8042, 80287, and NMI, and mapping main and EGA BIOS into one physical PROM.

FE3031:

The FE3031 is an AT data buffer and parity generator/checker in a 100-pin PLCC package that contains all of the data buffers necessary to implement an AT compatible computer. The FE3031 functions as a peripheral data bus buffer, memory data bus buffer, a parity/generator/checker, and PC/AT data bus buffer.

Figure 1.1 illustrates a functional block diagram of the FE3600 chip set.

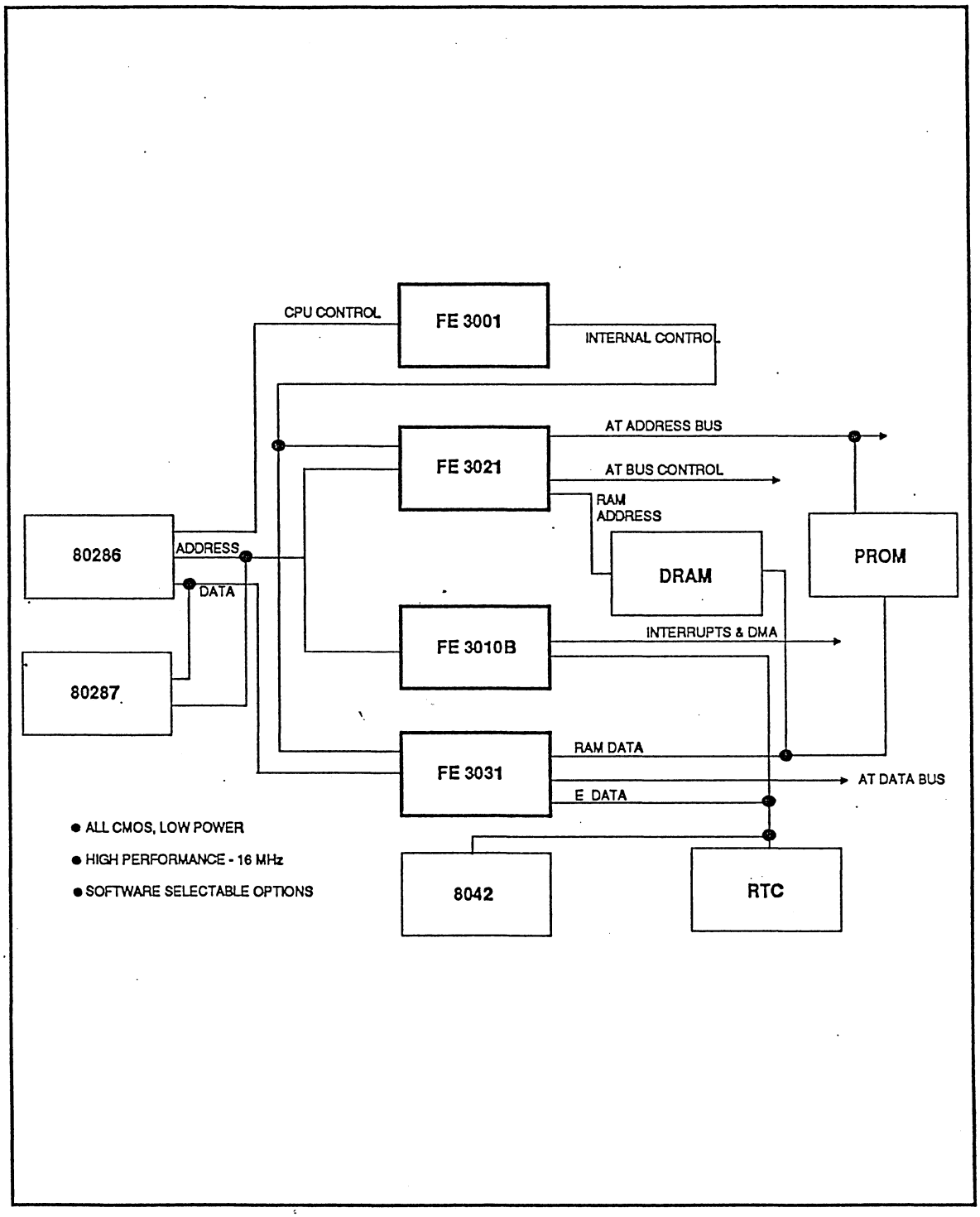

Figure 1.1 FE3600 Functional Block Diagram

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CHIP SET OVERVIEW

2.0 Introduction

The Western Digital 3600 chip set is a four - chip VLSI implementation of most of the system logic to implement a high performance IBM PC AT. The chip set is designed to offer a 100% PC AT compatible solution using only 27 components in addition to memory.

This section details how the four chips work in unison to provide 100% PC AT compatible solutions. It also provides an overview of the four chips: FE3001, FE3010B, FE3021, and FE3031. Sections 2.6 through 2.10 detail clock generation, clock programming, bus programming, wait states programming, and control registers. These topics are also aided by chip set system timing diagrams which follow the text..

2.1 Overview

The major components of an IBM PC AT compatible system using the FE3001, FE3010B, FE3021, and FE3031 are:

- Intel 80286 CPU
- Intel 80287 Math Coprocessor
- W.D. CPU Control Logic (FE3001)
- W.D. AT Peripheral Logic (FE3010B)
- W.D. Address Buffer & Memory Controller (FE3021)
- W.D. Data Buffer (FE3031)
- Keyboard Controller (Intel 8042)
- Real Time Clock

The design presented is fully compatible with the IBM PC AT system. The CPU Bus, the Expansion Bus, the Memory Bus, and I/O Bus are implemented in the same manner as in the IBM PC AT systems. All the peripherals and memories are decoded to match an IBM PC AT. To complete the overview, a brief description of each of the devices is presented.

2.2 FE3001 AT Control Logic IC

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an AT compatible computer. The salient features of the FE3001 are:

- Programmable CPU, DMA, and system clock generation
- Programmable bus timing
- Programmable wait state generator
- Refresh and DMA controls
- Bus arbitration logic
- NMI generator and Parity error logic
- Reset/shutdown control
- Sleep mode
- 80286 interface logic

The FE3001 is also detailed in Section 2.6.

2.3 FE3010B AT Peripheral Control Logic

The Western Digital FE3010B AT and peripheral controller is a highly integrated chip with various control and peripheral functions. The FE3010B contains the functional equivalent of two 8237 DMA Controllers in cascade mode. This block improves the performance of the system by allowing external devices to transfer data directly from the system's memory.

The FE3010B also contains the functional equivalent of two 8259 Interrupt Controllers in cascade mode. A total of 15 interrupts are supported including one from the time block. In addition, the FE3010B includes a functional equivalent of an 8254 timer. One channel is used to generate refresh request, one to generate sound for the speaker, and the other is tied to interrupt 0.

The FE3010B also contains a page register. It is used to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers and refresh cycles.

2.4 FE3021 Address Buffer & Memory Controller

The FE3021 is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001, FE3010B, and FE3031 to implement a low cost, high performance AT compatible computer. Chip count is reduced by integrating the memory controller, AT bus address buffers and I/O manager functions into one chip.

The memory controller is a high performance design with programmable modes of operation. It generates RAS and CAS signals for DRAM chips. It also provides control signals for Page Mode DRAM operation.

The Memory Controller portion has the capability to control page interleaved memory systems. It controls up to 4 banks of DRAM (up to 8 Mbytes) of memory. The DRAM bank locations

are programmable on 64K boundaries. One memory bank allows split addressing so that one portion may be placed in real memory with the remainder in extended memory.

An additional major function of the FE3021 is to generate chip select decodes for peripheral chips on the system board; the floppy controller, hard disk controller, serial and parallel port chips. System operating speed may be optimized by tailoring the number of process wait states to each individual peripheral device.

To reduce chip count and improve performance (particularly on EGA), the graphics controller is placed on the system board. Separate blocks of ROM may be mapped into a single physical ROM. The EGA BIOS and standard BIOS may be placed into a single 16-bit wide ROM. In addition to reduction of chip count, EGA operating speed will be increased since the EGA BIOS will be accessed at 16-bits at a time.

2.5 FE3031 AT Data Buffer

The FE3031 AT Data Buffer contains all of the data buffers necessary to implement an AT compatible computer. Its features include:

- 100 Pin PLCC design
- PC/AT Data Bus Buffers
- Peripheral Data Bus Buffer
- Memory Data Bus Buffers
- Parity Generator/Checker
- 1.25 Micron CMOS Technology

2.6 Programming Of The IBM PC/AT Bus

CLOCK GENERATION:

The FE3001 generates clock signals for the 80286, 80287 numeric processor, DMA, FE3010B, and the 8042 keyboard controller. There are three clock inputs to the FE3001: CLK16, CLKHS, and CLK14. The CLK16 is for 16 MHz oscillators, CLKHS is for 32 MHz or 40 MHz oscillators, and CLK14 is for 14.31 MHz oscillator inputs. The FE3001 generates six different clock signals: CPUCLK, DMACLK, PCLK, SYSCLK, TMRCLK, and 287CLK.

The user may select (with software) either CLK16 or CLKHS. As a result, CPUCLK and SYSCLK will change. The remaining four clocks will not change.

The CLK16 and CLKHS are provided to enable the 80286 to operate at up to 20 MHz while plug-in boards to the PC AT bus run up to 10 MHz. In essence, a motherboard designed with the FE3600 chipset (FE3001, FE3010B, FE3021 and FE3031) may be used with slower peripheral boards.

Although the FE3001 has two clock inputs, two oscillators are not necessary. The CLK16 is tied high with a pull-up resistor and the oscillator is connected to CLKHS. In this case, CLKHS + 2 will be used for the CLK16 input (done internally). It is not possible to connect CLKHS high and connect CLK16 to an oscillator. The frequency of CPUCLK is either CLK16 or CLKHS depending on whether CLK16 or CLKHS is chosen.

The SYSCLK clock is not used on the motherboard and is available on a PC AT Bus (B-20). The frequency of SYSCLK clock is either CLK16 + 2 or CLKHS + 4 depending on whether CLK16 or CLKHS is selected.

When CLKHS is selected, the phase of SYSCLK is dependent on ALE. When ALE is low, SYSCLK is equal to CPUCLK + 4. When ALE is high, SYSCLK goes low when CPUCLK makes the high to low transition. When CLK16 is selected, SYSCLK is equal to CPUCLK + 2, and does not depend on ALE. This scheme is used to insure that SYSCLK is synchronous to the command strobes and other bus signals.

The clock input CLK14 is a 14.31818 MHz input used to derive clock signals for the 8042 and FE3010 timer. The 8042 clock (PCLK and NPCLK) is fixed at 7.15 MHz and the timer clock is fixed at 1.19 MHz.

The DMA clock is programmable and is derived from CLKHS and CLK16. By writing in a register, the DMA clock can be set to either low or high speed. When CLKHS is selected for the CPU, the DMA CLK is CLKHS + 8 or CLKHS + 4. The user can choose between CLKHS + 8 and CLKHSS + 4 by writing in a register. When CLK16 is selected for the CPU, DMACLK is CLK16 + 4 and CLK16 + 2. The user can choose between CLK16 + 4 and CLK16 + 2 by writing in a register.

The clock for the 80287 (CLK287) is also generated by the FE3001. If CLKHS is chosen for CPU operation and CLK16 is tied to 5V through a pull up resistor, then CLK = CLKHS + 2. If CLK16 is not connected to 5V and is selected, then CLK287 = CLK16. For example, if CLKHS = 32 MHz and CLK16 = 16 MHz, and CLK16 is selected, then CLK287 = 16 MHz. However, the 80287 does not function beyond 10 MHz so a divide-by-three method must be used resulting in roughly 5 MHz 80287 operation.

To use the 80287 at 10 MHz, the CPUCLK from the FE3001 may be more suitable than CLK287 as it can be divided down to 8 or 10 MHz. For power consumption when the system is temporarily not in use, the FE3001 can be put in a sleep mode (bit 6 of port 063H high). In this mode, all clocks will be off except the 8042 and FE3010B timer clocks. These clocks are used for refresh timing and keyboard interface logic. Sleep mode is exited by pulsing the CPURES input of the FE3001.

2.7 Programming Clocks:

The speed select register controls the speed of the CPU and DMA clocks. This speed select register resides in I/O space and is an 8-bit with address 063H. It is a write-only register and can be written with an I/O command. The address 063H is defined to accomplish this task. Bits 0, 1, 4, and 5 are not used. When bit 2 is low, CLK16 is selected; otherwise CLKHS is selected. When bit 3 is low, the DMA clock is at 4 MHz, otherwise it is 8 MHz. The speed selector register is used to initiate the sleep mode. When bit 6 is at logic high, all of the clocks (except the timer clock) are stopped, allowing refresh to continue. Bit 7 is used to unlock and write other registers in the FE3000A. The speed select register is cleared by a system reset. To exit the sleep mode, the pulsing of the CPURES input of the FE3001 (by external hardware) is required.

2.8 Bus Programming

PC AT Bus programming is required due to the CPU 80286 running at up to 16 MHz and the fact that the PC AT Bus is designed for up to 8 MHz operations. The control/command signals from the motherboard should be delayed to conform up to 8 MHz specifications.

The programmed signals are BALE, IOW, IOR, MEWR, and the number of wait states. All programming is handled through registers in the FE3001. Figure 2.3 illustrates various program-

mable signals. The lower three signals: CPU CLK (32 MHz), ALE, and COMMANDX are signals present on the motherboard. The 32 MHz CPU CLK indicates that the 80286 is running at 16 MHz. The lower two signals BALE and COMMANDY are signals present on the PC AT Bus. These signals should meet 8 MHz Bus specifications.

To establish a relationship between ALE and BALE, COMMANDX and COMMANDY, refer to the timing diagram of ALE and COMMANDX with a 32 MHz CPU CLK, figure 2.3. The BALE and COMMANDY timing with respect to a 16 MHz CPU CLK is also shown in figure 2.3. The 16 MHz CPU CLK will generate 8 MHz BUS signals.

In figure 2.3, A represents the delay between the leading edge of ALE and the leading edge of BALE. B represents the width of BALE, and C is the delay between the trailing edge of ALE and beginning of COMMANDY. All delays are measured with respect to ALE and are expressed in terms of CPU CLK cycle. Delay A is 1 CPU clock, B and C are 2 CPU clock's. The minimum resolution is 1 CPU clock.

2.9 Programmable Registers

Table 2.1 contains registers, functions, waveforms, and default parameters. There are 13 registers (R0 to R12) which handle the programming of various bus signals. These registers are controlled through two registers; point register, address 072H, and data register, address 073H. Both are write-only registers, located in I/O space

The pointer register contains the address of one of 14 registers. Not all 8 bits in the pointer are used (bit 0, 1, 4, and 5 are unused). The remaining four bits (bit 2, 3, 6, and 7) form the address with bit 7 as MSB and bit 2 as LSB.

EXAMPLE: If bits 2, 3, 6, and 7 are 0, 1, 0, and 1 respectively, the address is 10 (decimal). It is pointing to register R (see Table 2.1). If all four bits are zero, R is being pointed at 0.

The data register, address 073H, contains data to be written into one of Ro-12 register. Not all eight bits of the data registers are used (bits 0, 1, 4, and 5 are not used). Bits 2, 3, 6, and 7 form 4-bit data with bit 2 as LSB and bit 7 as MSB.

REG	FUNCTION	DEFAULT
R_0	BALE delay from ALE leading edge	0
R_1	BALE width	1
R_2	NOT USED	
R_3	8-bit memory, 8/16-bit I/O - cmd delay	1
R_4	8-bit operation - wait states	4
R_5	16-bit I/O operation - wait states	1
R_6	16-bit memory operation - command delay	0
R_7	16-bit memory operation - wait states	1
R_8	16-bit memory operation - wait states	0
R_9	Local DRAM read operation - wait states	0
R_{10}	Local DRAM write operation - wait states	1
R_{11}	Local DRAM write operation - cmd delay	0
R_{12}	On-board I/O operation - command delay	1

Table 2.1 SUMMARY OF COMMAND TIMING REFERENCE

2.10 Wait States

As shown in figure 2.3, 4 wait states on the motherboard must appear as 1 wait state on the PC AT BUS. A simple formula exists to calculate the number of wait states at the PC/AT BUS from the number of wait states at the motherboard.

Number of wait states at the PC/AT BUS =

$$\frac{\text{Number of wait states in the CPU clock} - 2}{2}$$

2.11 16 MHz CPU - 8 MHz PC/AT Bus Emulator

This section describes how to find delays, signal widths, number of wait states, and register values for a 16 MHz CPU to generate 8 MHz Bus signals.

Refer to figures 2.1 and 2.2 for the timing diagrams of the 32 MHz CPU clock and the 8 MHz SYSCLK. It is then possible to find the relationship between corresponding signals; for example, ALE and BALE, number of wait states, and command signals. The MEWR, memory write is the command seen in Figure 2.5. Figure 2.4 describes a 16-bit I/O operation. The delay between the leading edge of ALE and the leading edge of BALE is 1 CPU clock, and the value of register R 0 is 1. The width of BALE is two CPU clocks, and the value of register R 1 is 2. The command delay is 2 CPU clocks, and the value of register R 6 is 2. The number of wait states in terms of the CPU clock is 4. Therefore, the value of register R 7 is 4. The ready signals need not be programmed, due to wait state programming.

The 16-bit I/O operation is illustrated in Figure 2.4

Note: The numbers listed in the DEFAULT column are CPU clocks. Default is considered a 16 MHz CPU clock and an 8 MHz 80286 device.

2.12 System Timing Diagrams

Figures 2.7 through 2.12 illustrate the timing information for various page and non-page modes, CPU CLK speeds, DRAMS, and wait states.

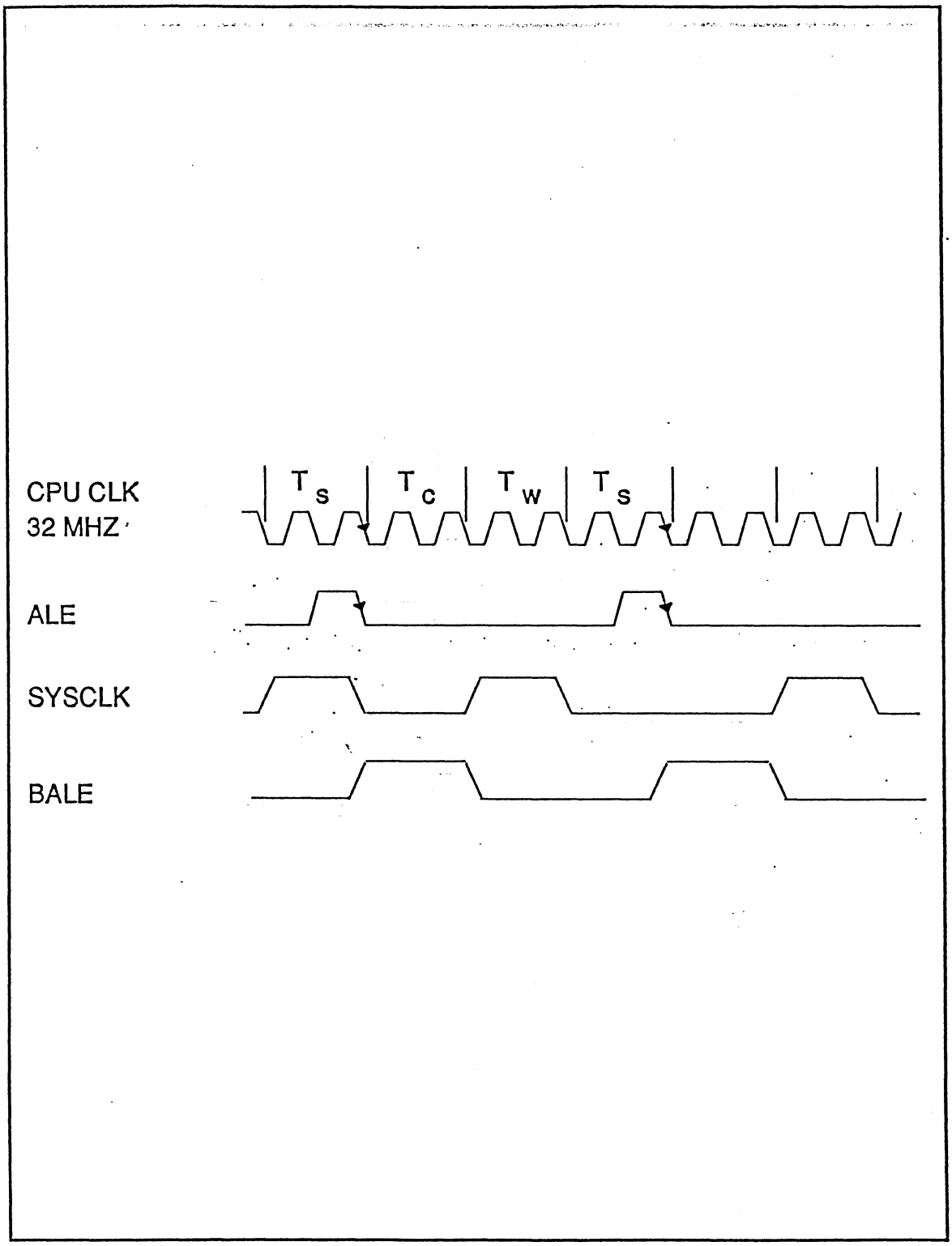


Figure 2.1 CLKHS IS SELECTED, SYSCLK = CPUCLK/4

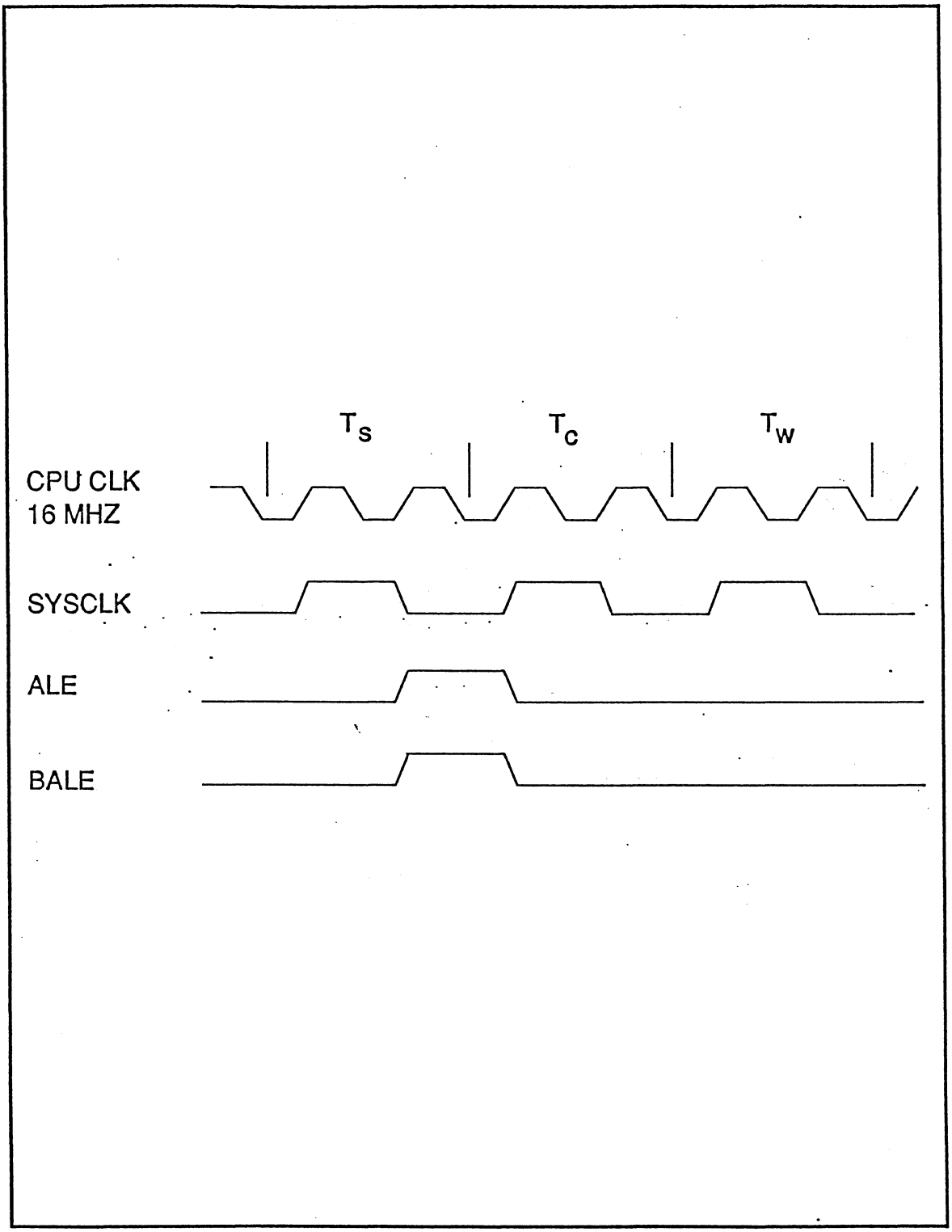


Figure 2.2 CLK16 IS SELECTED, SYSCLK = CPUCLK/2

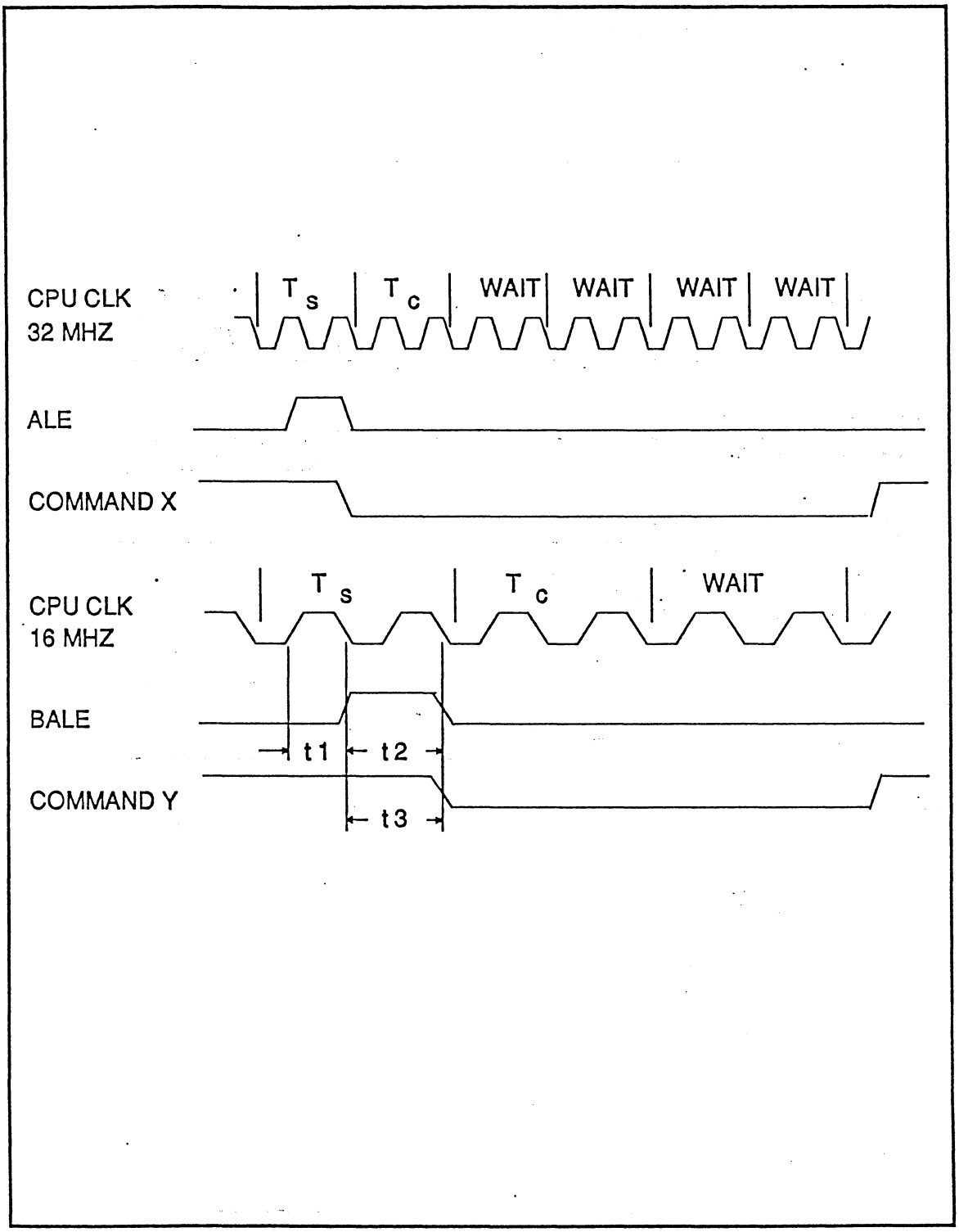


Figure 2.3 32 MHz/16 MHz CPU CLK TIMING DIAGRAM

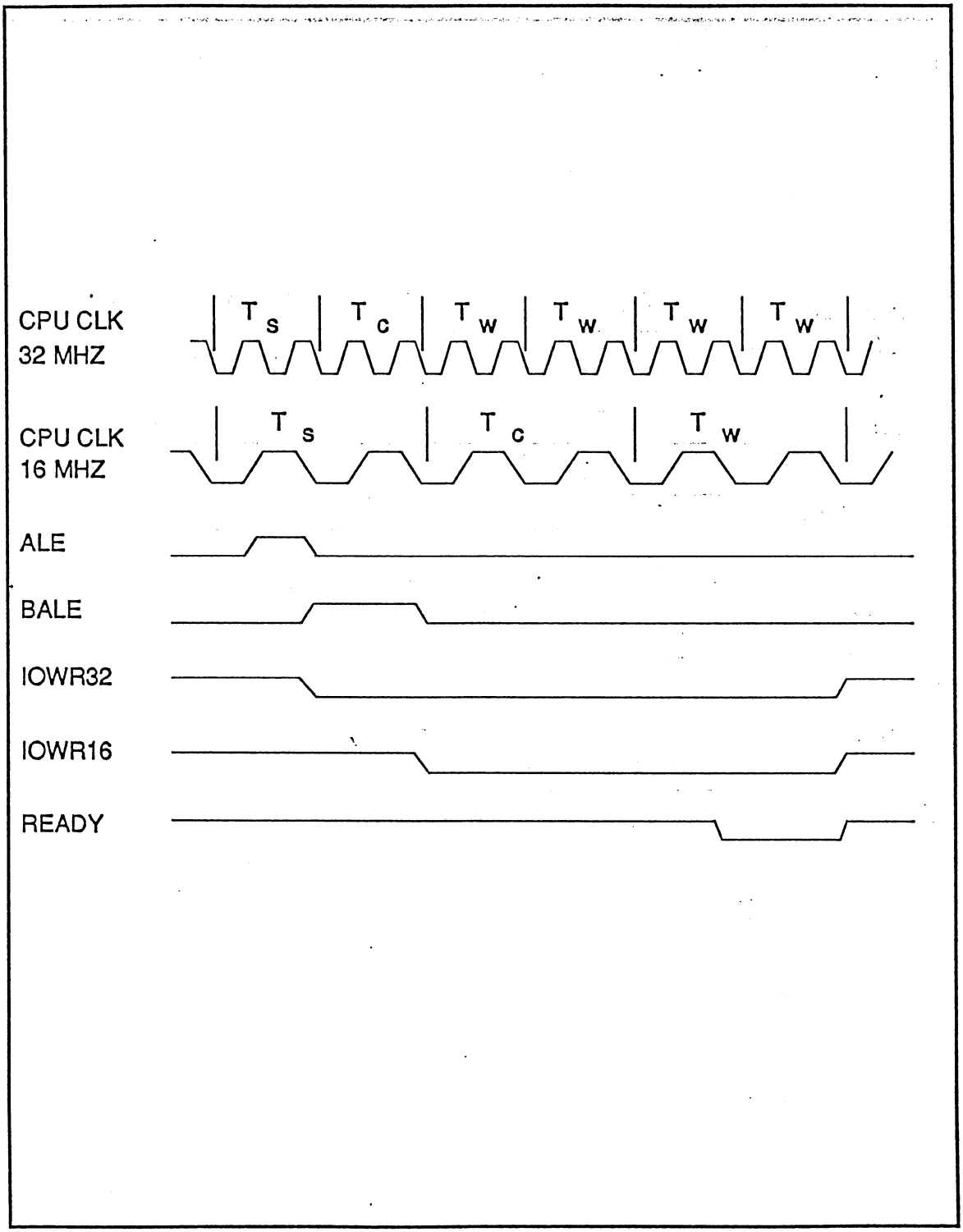


Figure 2.4 16 BIT I/O READ OPERATION

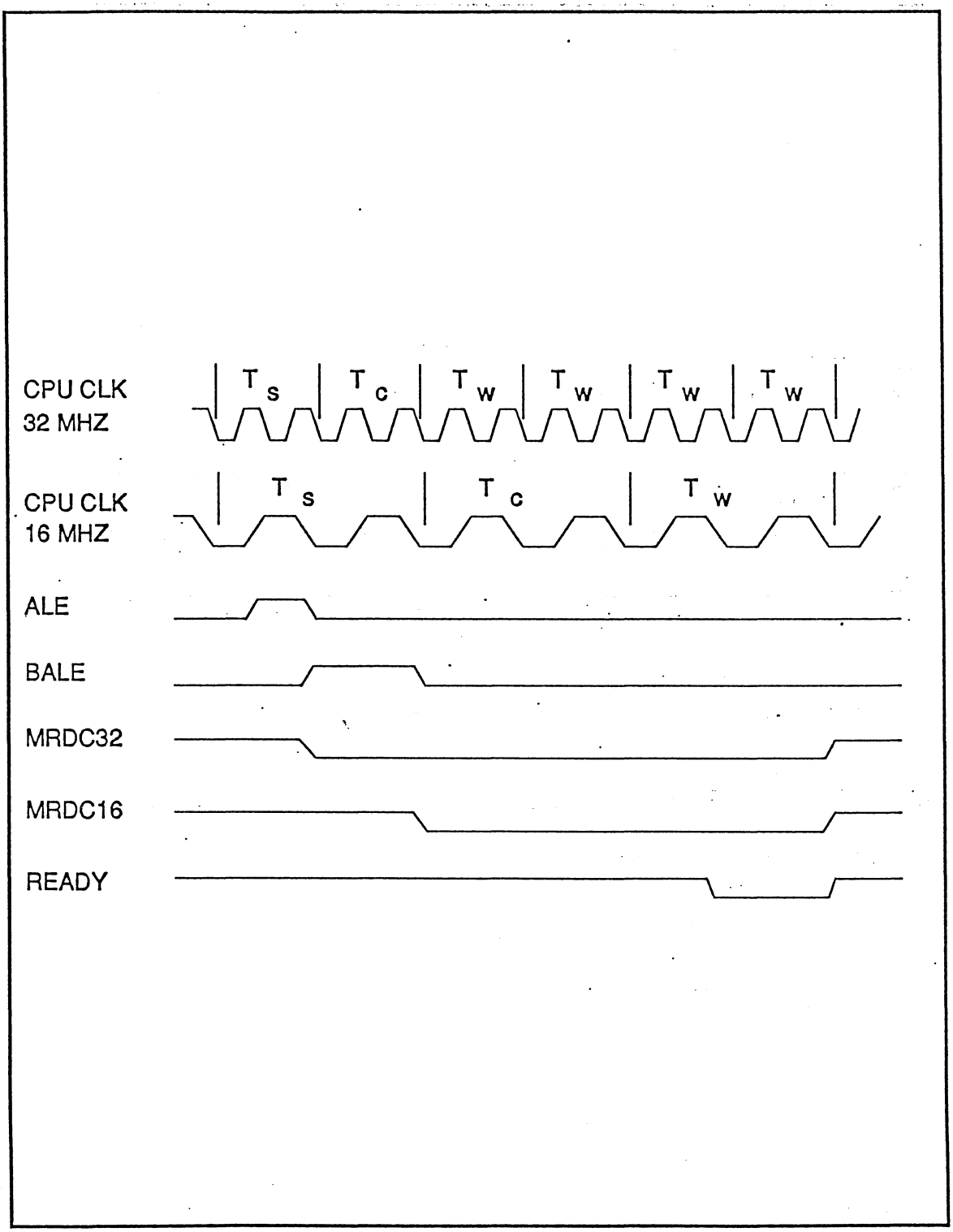


Figure 2.5 16 BIT MEMORY READ OPERATION

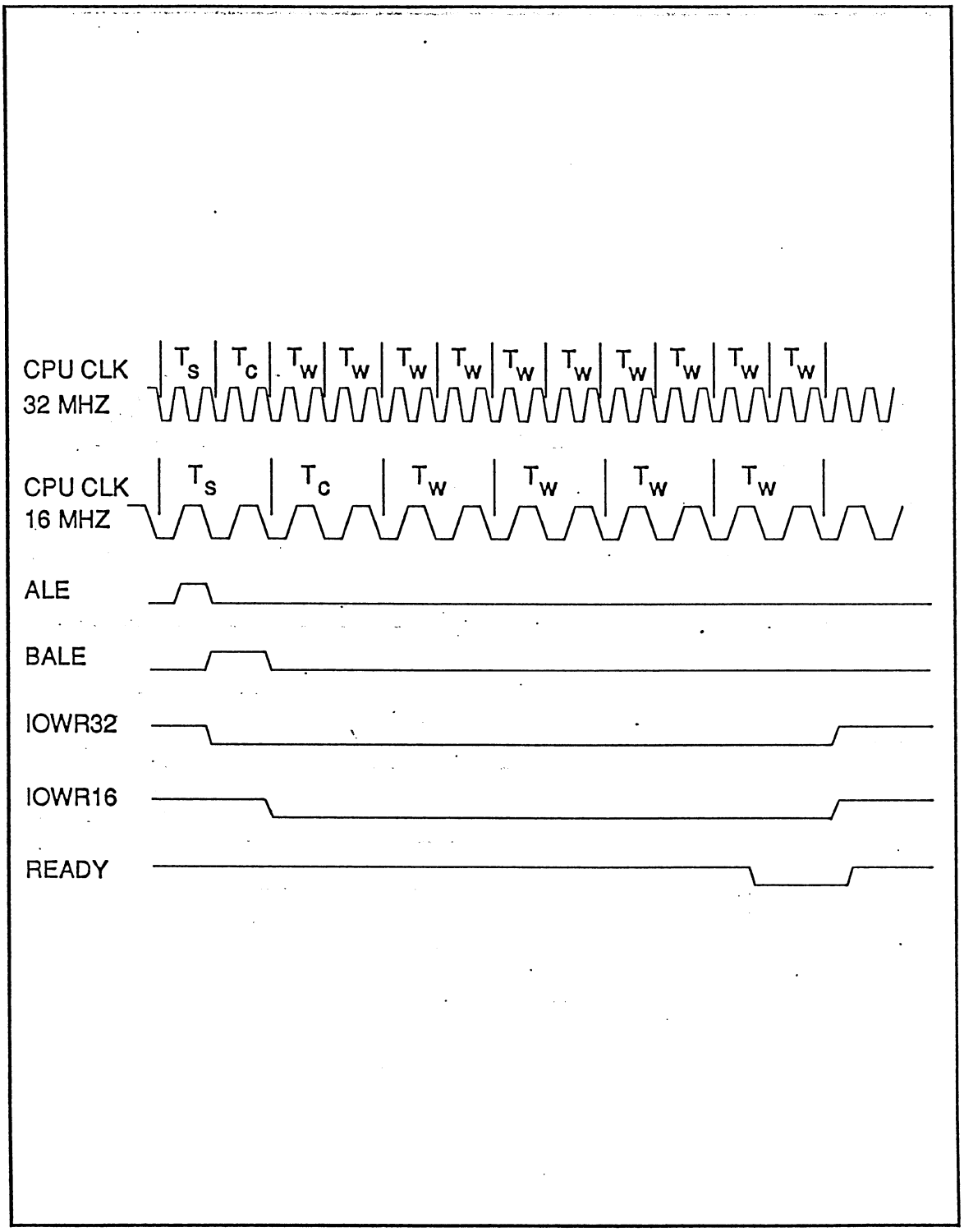


Figure 2.6 8 BIT I/O READ OPERATION TO 8 BIT DEVICE

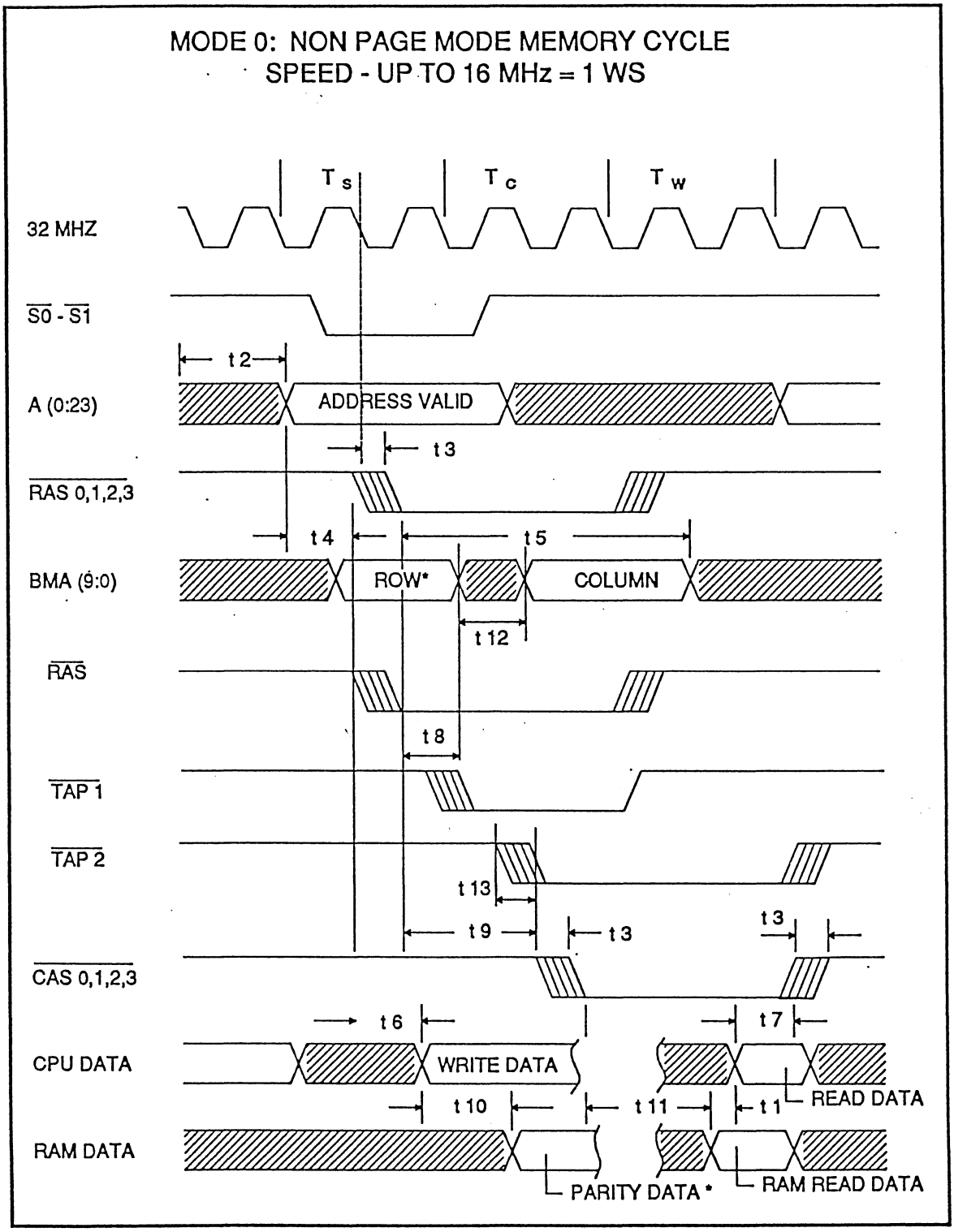


Figure 2.7 MODE 0 TIMING DIAGRAM

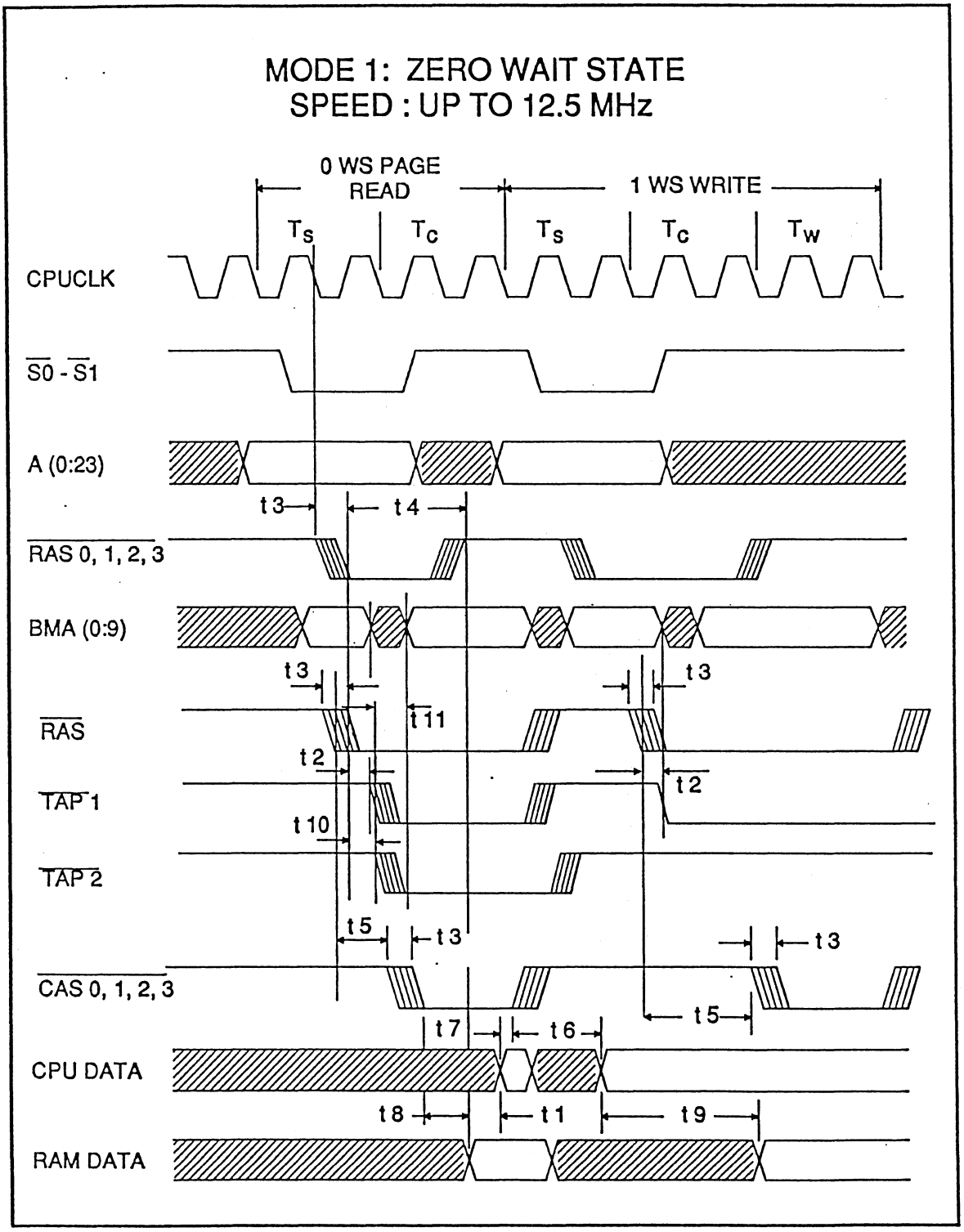


Figure 2.8 MODE 1 TIMING DIAGRAM

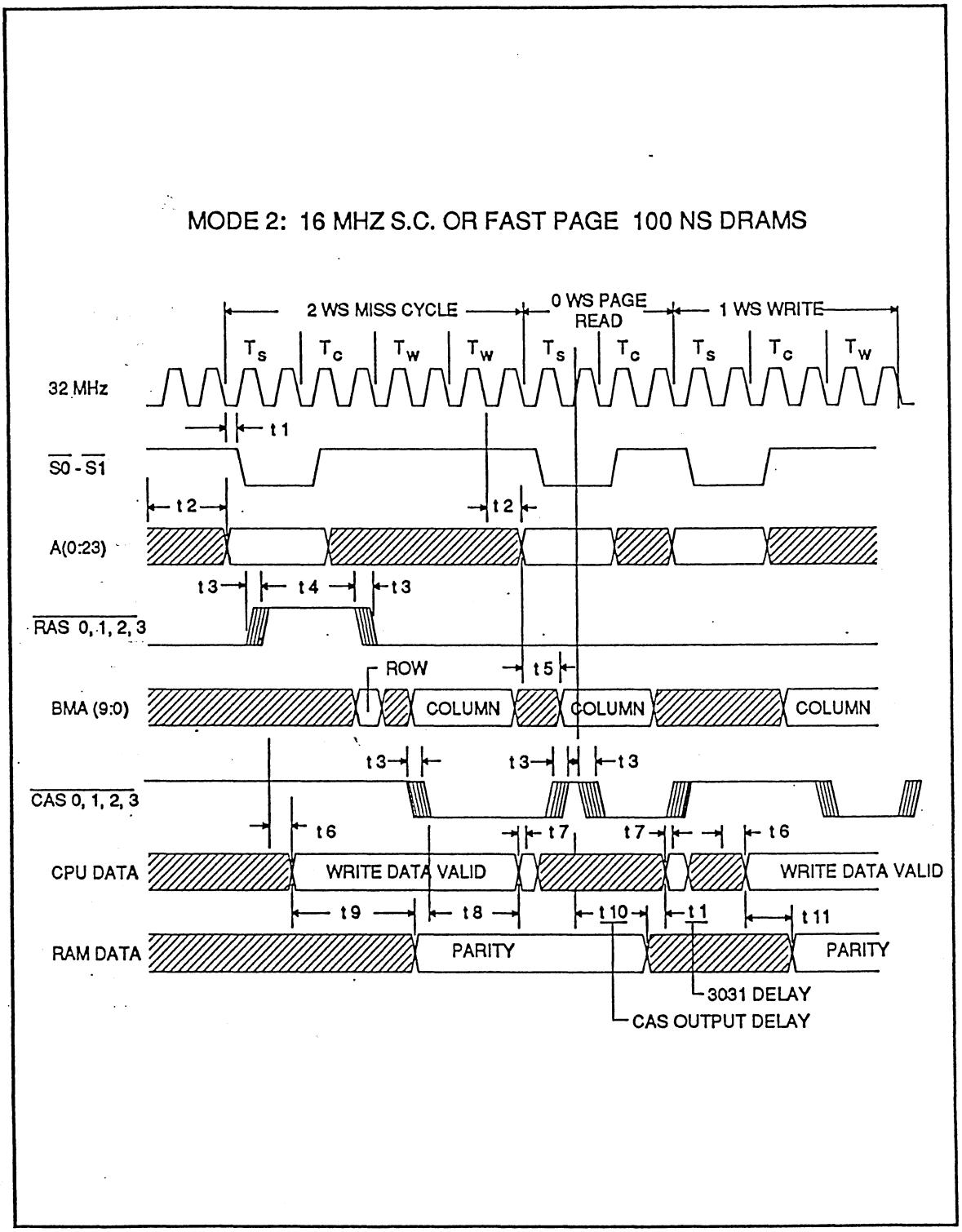


Figure 2.9 MODE 2 TIMING DIAGRAM

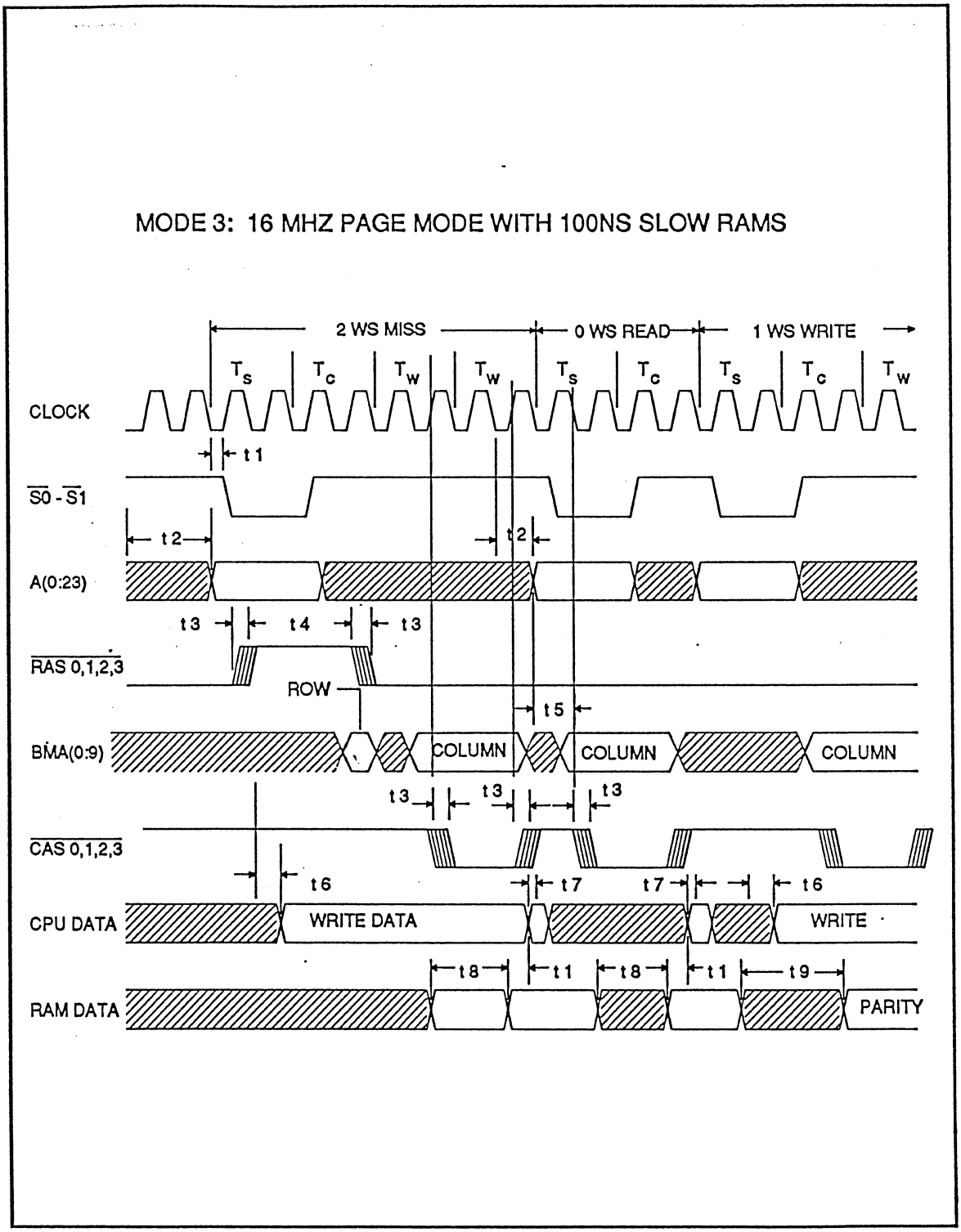


Figure 2.10 MODE 3 TIMING DIAGRAM

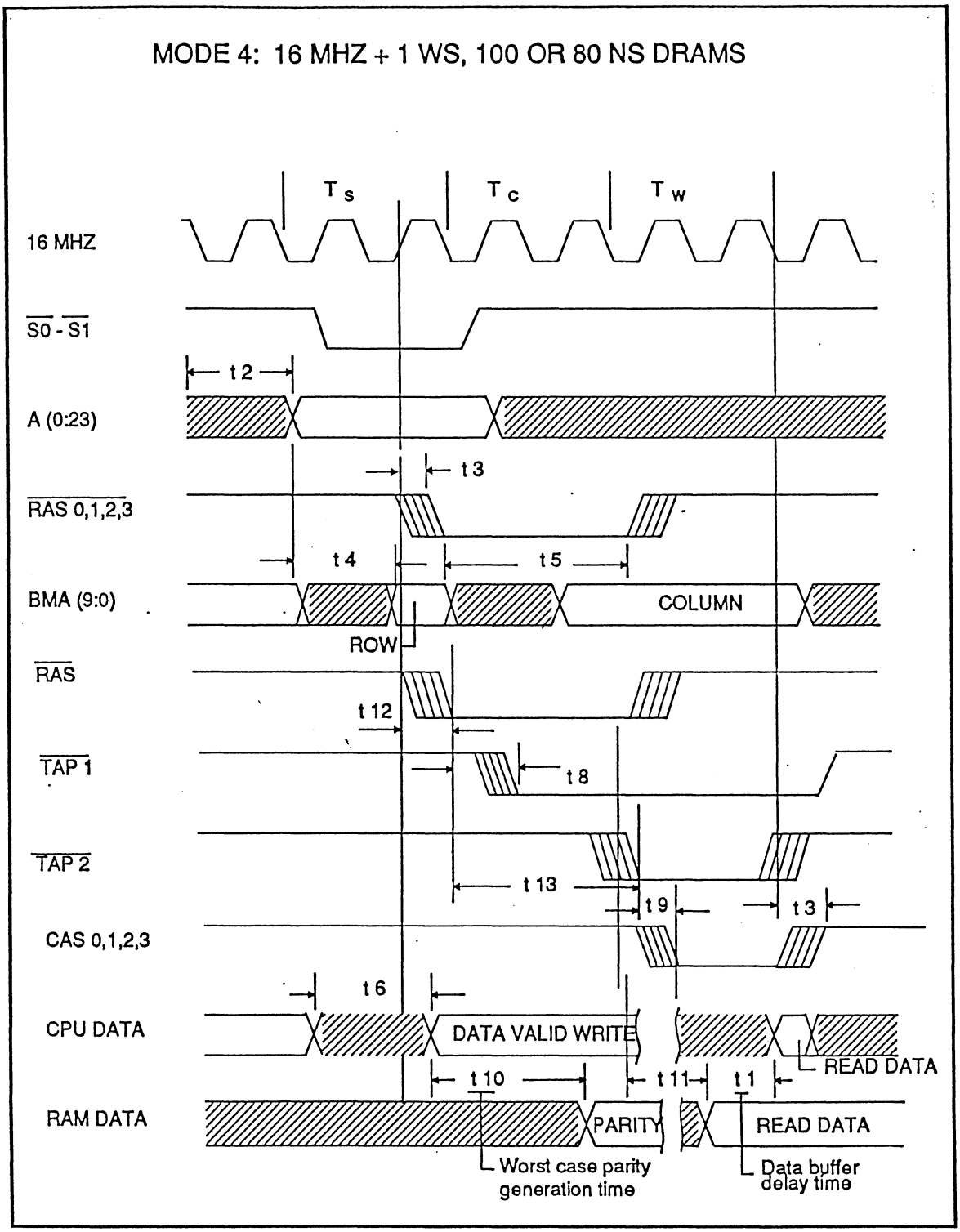


Figure 2.11 MODE 4 TIMING DIAGRAM

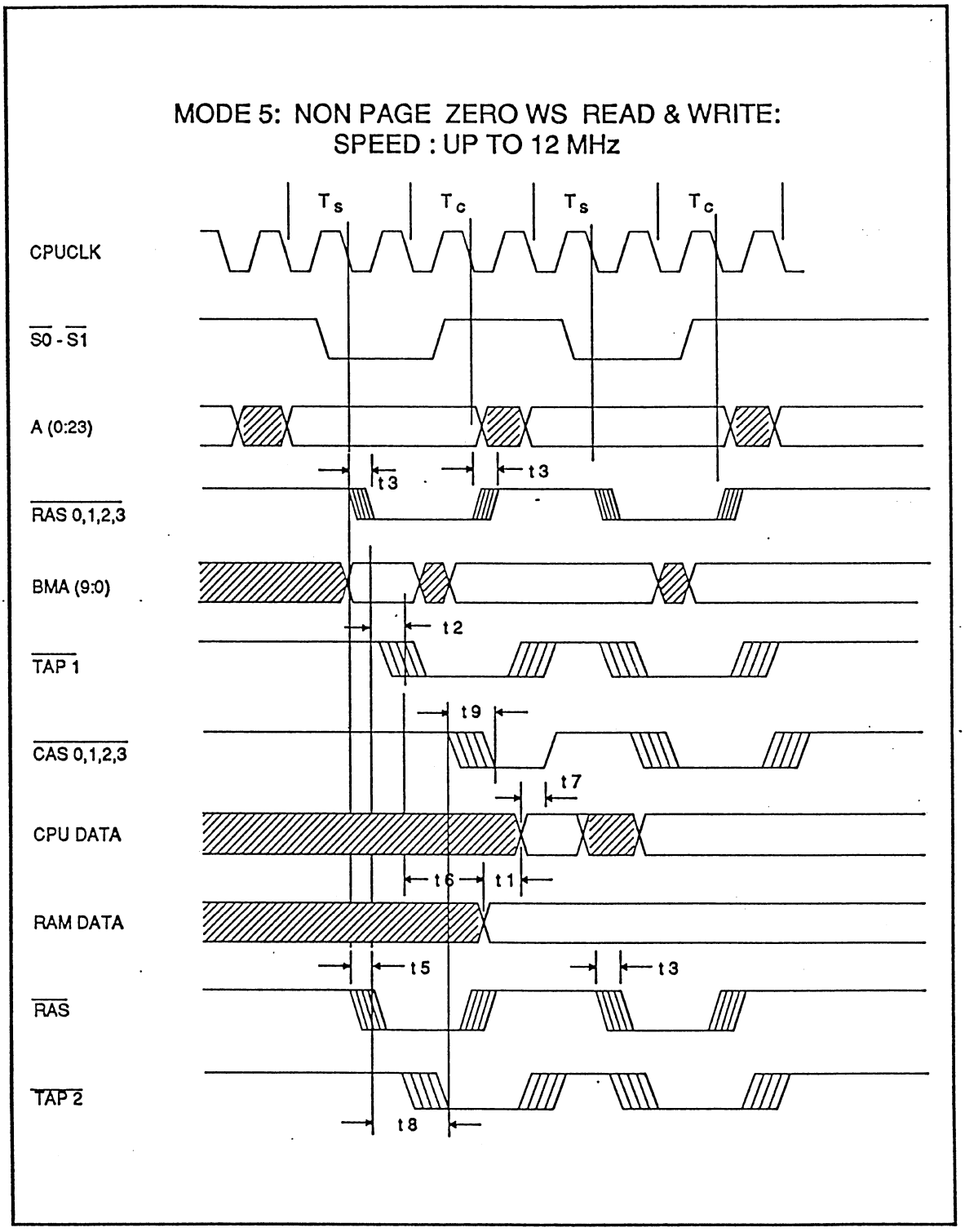


Figure 2.12 MODE 5 TIMING DIAGRAM

FE3001 AT CONTROL LOGIC

3.0 Introduction

This section describes the functions, pinouts, signals, timing and electrical specifications of the FE3001 AT Control Logic IC.

3.1 Overview

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an AT compatible computer. It is part of the FE3600 chip set intended to simplify the design of 16 MHz 80286 based AT computers.

A block diagram of the FE3001 is shown in Figure 3.1. For more information on the FE3010B, FE3021, and FE3031 refer to the Table of Contents for the appropriate section.

3.2 Features

The FE3001 contains all of the clock generation and cycle control logic necessary to implement an AT compatible computer. The following features are incorporated into the FE3001:

- 84 Pin PLCC
- Programmable CPU and DMA clock generator
- System clock generator
- Programmable bus timing
- Programmable wait state generator
- Refresh and DMA controls
- Bus arbitration logic
- NMI generator and Parity error logic
- Reset/shutdown control
- Sleep mode
- 80286 interface logic
- 1.25 micron HCMOS technology

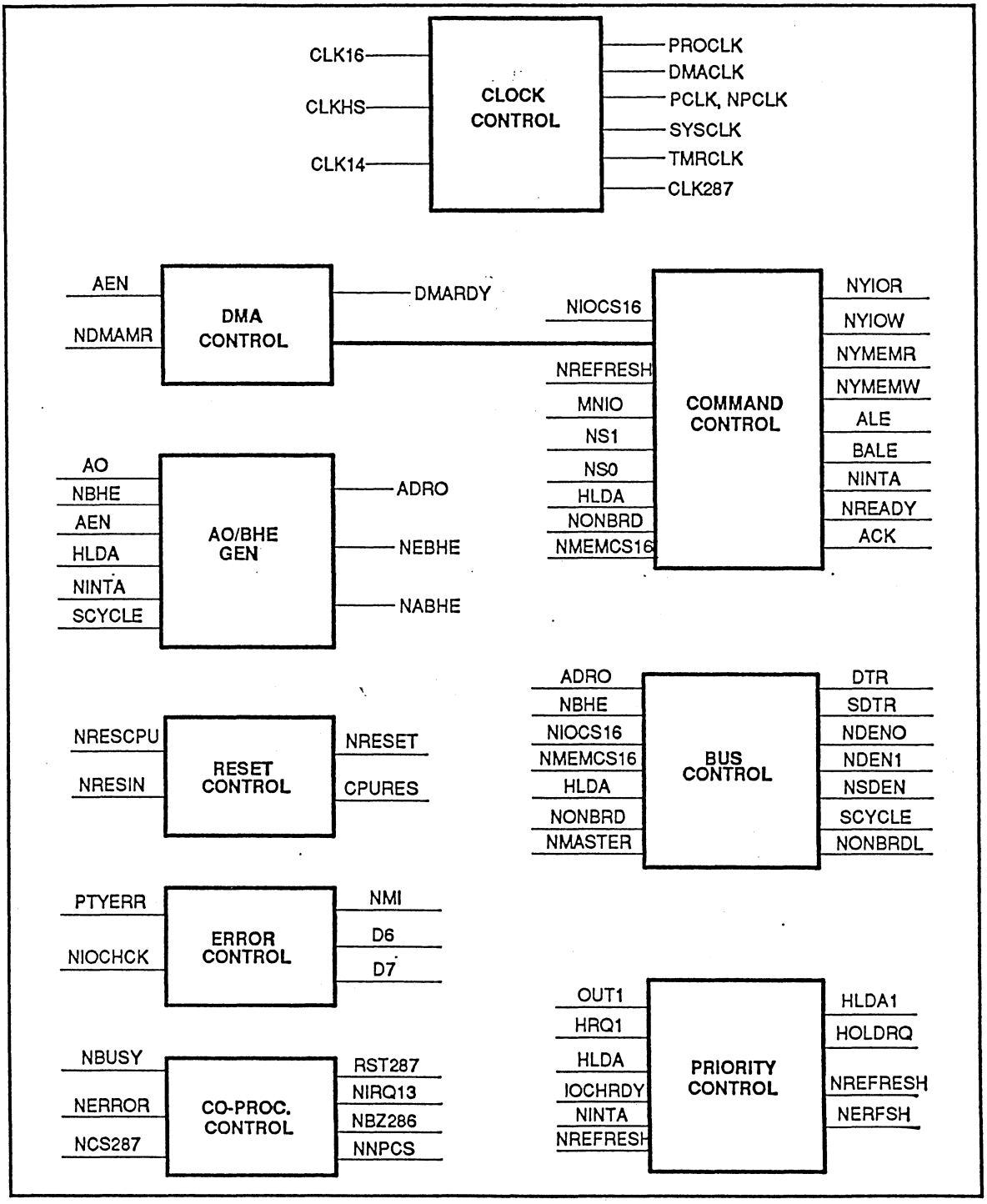


Figure 3.1 FE3001 Block Diagram

3.3 FE3001 Pinouts

The FE3001 pinouts are shown in Figure 3.2.

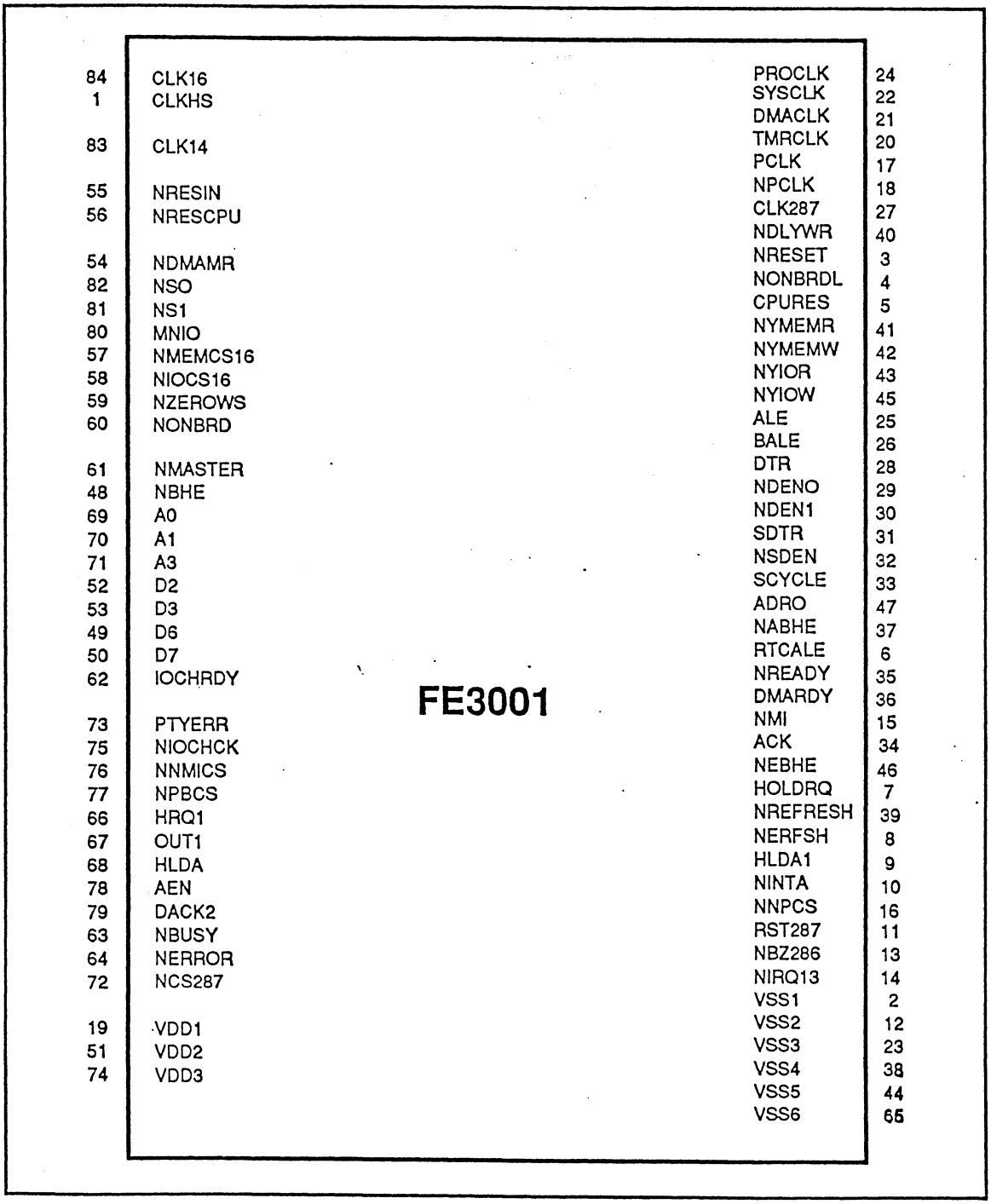


Figure 3.2 FE3001 Pin Assignments

3.4 Signal Descriptions

PIN#	SIGNAL	TYPE	DESCRIPTION
1	CLKHS	I	High speed clock input (40MHz max). This provides the high speed clock when selected. When CLK16 (pin 84) is pulled high, this input (divided by two) is used as the low speed clock.
2	VSS1		Ground.
3	NRESET	O	Reset to the system.
4	NONBRDL	O	NONBRD input latched by ALE internally.
5	CPURES	O	Reset to 80286.
6	RTCALE	O	Real Time Clock Address Latch Enable (I/O address 70H).
7	HOLDRQ	O	Hold request to 80286 for DMA or Refresh.
8	NERFSH	O	Enable refresh address signal to FE3010. Puts refresh address on address bus.
9	HLDA1	O	DMA hold acknowledge signal to FE3010.
10	NINTA	O	Interrupt acknowledge to FE3010.
11	RST287	O	Reset to 80287 (Write to I/O address F1H or system reset).
12	VSS2		Ground.
13	NBZ286	O	80287 busy signal to 80286.
14	NIRQ13	O	Interrupt request 13 for 80287 error to FE3010.
15	NMI	O	Non-Maskable Interrupt to 80286. Generated in response to a parity error or bus IOCHCK.
16	NNPCS	O	80287 Co-processor chip select (F8).
17	PCLK	O	7.16 MHz clock for keyboard controller.
18	NPCLK	O	Inverted PCLK.
19	VDD1		+5V VDD.
20	TMRCLK	O	1.19 MHz timer clock to FE3010.
21	DMACLK	O	Software selectable clock for DMA to FE3010.
22	SYSCLK	O	System clock needed for bus timing. See description in synchronization section.
23	VSS3		Ground.
24	PROCLK	O	Software selectable 80286 clock.
25	ALE	O	Local Address Latch Enable. 3
26	BALE	O	Bus Address Latch Enable. (Programmable)
27	CLK287	O	Clock for 80287. See clock section for details.
28	DTR	O	Data direction to data buffers.
29	NDEN0	O	Low byte data enable to data buffers.
30	NDEN1	O	High byte data enable to data buffers.
31	SDTR	O	Byte swap data direction to data buffers.
32	NSDEN	O	Byte swap data enable to data buffers.
33	SCYCLE	O	Latch low byte during byte swap read.

Table 3.1 Signal Descriptions

PIN	SIGNAL	TYPE	DESCRIPTION
34	ACK	O	DMA Acknowledge signal to the PC/AT bus.
35	NREADY	O	Ready to CPU.
36	DMARDY	O	End DMA cycle to FE3010.
37	NABHE	O	High byte enable for devices on local bus.
38	VSS4		Ground.
39	NREFRESH	I/O	Refresh cycle. Generated from timer OUT1 or externally from the bus.
40	NDLYWR	I/O	NYIOW delayed to the FE3010, active edge delayed one PROCLK. Input from FE3010 in during DMA to generate NYIOW.
41	NYMEMR	I/O	Memory read. Input during Master cycle.
42	NYMEMW	I/O	Memory write. Input during HLDA cycle.
43	NYIOR	I/O	I/O read. Input during HLDA cycle.
44	VSS5		Ground.
45	NYIOW	I/O	I/O write. Input during Master cycle.
46	NEBHE	I/O	High byte enable to expansion bus.
47	ADR0	I/O	Low byte enable. During a CPU cycle, is A0 latched with ALE.
48	NBHE	I/O	High byte enable from the 80286. Output during MASTER and DMA cycles for memory control use.
49	D6	I/O	Peripheral data bus bit 6.
50	D7	I/O	Peripheral data bus bit 7.
51	VDD2		+5V VDD.
52	D2	I	Peripheral data bus bit 2.
53	D3	I	Peripheral data bus bit 3.
54	NDMAMR	I	DMA memory read from DMA controller.
55	NRESIN	I	System reset input.
56	NRESCPU	I	CPU reset input from keyboard controller.
57	NMEMCS16	I	16 bit memory transfer on the PC/AT bus.
58	NIOCS16	I	16 bit I/O transfer on the PC/AT bus.
59	NZEROWS	I	Zero wait state bus cycle. See description for more details.
60	NONBRD	I	16 bit On Board DRAM memory or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles.
61	NMASTER	I	Master on PC bus has control of the bus.
62	IOCHRDY	I	Current bus cycle may complete. May be used to extend CPU, DMA, or refresh cycles.
63	NBUSY	I	80287 co-processor busy.
64	NERROR	I	Error from 80287.
65	VSS6		Ground.
66	HRQ1	I	Hold request from DMA controller in FE3010.
67	OUT1	I	Refresh timer input from FE3010.

Table 3.1 Signal Descriptions (Continued)

PIN	SIGNAL	TYPE	DESCRIPTION
68	HLDA	I	Hold acknowledge from 80286.
69	A0	I	Local 80286 address bus 0.
70	A1	I	Local 80286 address bus 1.
71	A3	I	Local 80286 address bus 3.
72	NCS287	I	80287 select decode (0FXH).
73	PTYERR	I	Onboard RAM parity error.
74	VDD3		+5V VDD.
75	NIOCHCK	I	Error from PC/AT bus.
76	NNMICS	I	NMI port enable decode (07XH). Also used for programming bus control registers.
77	NPBCS	I	Port B chip select decode (061H,063H). See register description for decode definitions.
78	AEN	I	DMA cycle enable from FE3010.
79	DACK2	I	16 bit DMA acknowledge from FE3010.
80	MNIO	I	80286 memory/IO select. High indicates memory cycle, low indicates I/O cycle.
81	NS1	I	80286 Status 1.
82	NS0	I	80286 Status 0.
83	CLK14	I	14.318 MHz clock input used to derive TMRCLK, PCLK, and NPCLK.
84	CLK16	I	16MHz clock input. This provides the low speed CPU clock for 8 MHz operation. When this pin is pulled high, CLKHS 2 is used

Table 3.1 Signal Descriptions (Continued)

NOTE: Signals beginning with the letter "N" are active low, other signals are active high.

3.5 Functional Description

3.5.1 Functional Overview

The FE3001 is designed to run with the FE3010 peripheral controller, and the FE3021 and FE3031 buffers/memory controls to create a 16MHz or 20MHz PC/AT compatible system. The FE3001 and FE3010 can, however, be used with discrete logic to also produce a 16MHz or 20MHz PC/AT system. The basic architecture of an AT compatible system using the FE3600 chip set involves putting the system DRAM on the local data and command bus, allowing the RAM to use the full 20MHz capabilities of the system. The BIOS ROM can be put on the local bus or expansion bus; the FE3021 has provisions especially to use the ROM on the higher speed bus. During accesses to local memory, the data buffer controls in the FE3001 prevent data collisions between the local and expansion buses. The FE3021 and FE3031 also inhibit memory read and write signals to the expansion bus for the local memory accesses.

The FE3001 generates all of the clocks needed in the system. The CPU clock to the 80286 processor (PROCLK) is programmable, as is the DMA clock for the DMA controller in the FE3010 (DMACLK). The expansion bus clock (SYSCLK) and coprocessor clock for the 80287 (CLK287) are not programmable but depend on the current operating configuration. These clocks are described

in more detail below. The clock for the timers in the FE3010 (TMRCLK) is fixed at 1.19MHz, and the clocks for the keyboard controller (PCLK and NPCLK) are fixed at 7.16MHz.

On power-up, the FE3001 will boot the system using the low speed clock (CLK16) as PROCLK, designed to be a 16MHz clock to run the PC/AT at 8MHz and keep the bus fully compatible with the standard AT bus. If CLK16 is pulled high, the high speed clock (CLKHS) is divided by two and used as PROCLK in the low speed mode. This enables an 8/16MHz system to be constructed with only one 32MHz clock (of course CLK14 is still needed, but a 7/14MHz system can be built by using the 14.3MHz clock also as CLKHS and pulling CLK16 high). For running at 20MHz, it is recommended that CLK16 be used; otherwise, the system will boot the bus at 10Mhz, causing potential incompatibilities with add-in cards designed for the 8 Mhz bus. DMACLK initially is the low speed clock divided by 4, synchronized in the same manner as on the PC/AT. SYSCLK is initially the low speed clock divided by 2, also synchronized in the same manner as on the PC/AT. CLK287 is always identical to the low speed clock, so is CLK16 if present or CLKHS divided by 2 if CLK16 is pulled high (i.e. CLK287 will be 16MHz in most applications).

The FE3001 has registers to delay the five commands (memory read and write, I/O read and write, interrupt acknowledge) during a CPU cycle and control the length of the commands based on various input signals (16 bit memory, 16 bit I/O, on board memory, fast 16 bit I/O device, and zero wait state device). On power-up, these registers are loaded with values to run the system with a 16MHz PROCLK (8MHz system) with full AT compatibility and no register programming necessary. Before switching to high speed operation, it is necessary to program the registers for proper bus emulation. These registers completely eliminate the need to either slow down the processor for expansion bus operations or run the bus asynchronously. Note that a 16MHz system can be made to exactly match the bus timing of an 8MHz system and remain truly compatible. Since programming the registers is performing an I/O write to an 8-bit device, it is recommended that the last four registers to get changed are 8-bit wait states, 8-bit command delay, BALE width, and BALE delay, respectively. Basic bus programming first involves clearing the lock bit, writing the register number to be changed to I/O address 072H, then writing the data into I/O address 073H. After all registers are programmed with proper values for high speed operation, the clock speed can be changed. Internal circuitry is present to assure glitch-free clock switching. It is then recommended that the lock bit be set to avoid inadvertent writes to the registers. When switching back to the lower clock speed, the process is simply reversed. Note that a system reset will automatically reboot at the lower speed, while a CPU reset (Ctl-Alt-Del) or shutdown will not affect the clock speed or register contents. In high speed operation, DMACLK operates at high speed clock divided by 8 for low speed DMA or high speed clock divided by 4 for high speed DMA. In low speed operation, DMACLK operates at low speed clock divided by 4 for low speed DMA or low speed clock divided by 2 for high speed DMA. Thus for an 8MHz system, the DMA can be performed at 4MHz or 8MHz, selectable by setting the appropriate bit in the clock select register.

Synchronization is trivial at low speed operation, since SYSCLK is one half the speed of PROCLK, and all synchronization is the same as on the PC/AT. At high speed operation, synchronization becomes very important, since now SYSCLK runs at one fourth the speed of PROCLK. This allows the cards on the bus to count wait states and synchronize signals totally oblivious to the actual speed at which the CPU is running. So if PROCLK is running at 32MHz, SYSCLK still runs on the bus at 8MHz. In order to properly synchronize SYSCLK to BALE and the commands, logic was used to make the clock perform as shown in figure 3.3. Also, DMACLK synchronization at 8MHz DMA operations is not performed, since no standards currently support 8Mhz DMA on the PC/AT system. Also to guarantee that NREADY is generated in the middle of a Tc cycle and that bus commands terminate on a rising edge of SYSCLK, logic is present to

do so. Hence if an odd number of wait states is programmed for any bus mode in high speed operation, or if IOCHRDY would cause the command to end on the wrong phase of the clock, one additional wait state will be added for synchronization. The command delays for 16 bit memory and onboard I/O devices can differ from the default setting (which is used for 16 bit I/O devices and all 8 bit devices). The necessary NMEMCS16 and NONBRD signals need to be present before the commands should go active by the setup time in the AC spec. If this does not occur, the command may not be generated for the current cycle. All onboard memory accesses (memory cycles with NONBRD active) have a command delay of zero. The logic to generate NREADY to the processor and terminate the commands requires that the control signal NIOCS16 be present before NREADY is to go active by the setup time shown in the AC spec. In the PC/AT, NZEROWS is used to override the default one wait state for 16 bit memory or I/O, or terminate an 8 bit memory cycle early (before its four wait states are complete). The FE3001 contains a register to terminate any cycle after a programmed minimum number of wait states is complete, allowing one extra wait state for synchronization if needed as described above. The default value for the NZEROWS register is zero, so any cycle in which NZEROWS is activated will terminate at the end of the next Tc. For high speed operation, this register needs to be non-zero to maintain compatibility with the AT bus.

The major logic modules that make up the FE3001 are described in this section. The following discussion assumes CLK16 is 16MHz and CLKHS is 32 MHz.

3.5.2 Clock Generator

This module generates clocks for the CPU, DMA, 8042 keyboard controller, timer and 80287 Numeric Processor. The CPU clock is software selectable for standard speed or high speed CPU operation. The DMA clock is software selectable between 4 MHz and 8 MHz. The 80287 clock is fixed at the low speed CPU clock (16MHz).

There are three input clocks to the FE3001. CLK16 is a 16 MHz clock to be used for 8 MHz CPU operation. CLKHS is the high speed clock for 16 or 20 MHz CPU operation. If the CLK16 input is tied high with a pull-up resistor then CLKHS + 2 will be used in place of CLK16 as the low speed clock. CLK287 is fixed at the lower speed clock.

When the lower speed clock is selected, SYSCLK is PROCLK + 2. During high speed operation, SYSCLK is PROCLK + 4. In the high speed case, SYSCLK is brought into sync with the PC/AT bus at the end of ALE. See Figure 3.3 for SYSCLK functional timing.

The CLK14 input is a 14.31818 MHz input used to derive the 8042 clock and FE3010 timer clock. The 8042 clock (PCLK, NPCLK) is fixed at 7.16MHz and the timer clock is fixed at 1.19 MHz.

Software may put the FE3001 in sleep mode by setting port 063H bit 6. In this mode all the clocks will be stopped except for TMRCLK, PCLK, NPCLK, and CLK287 on the next HLDA rising edge. These clocks are used for refresh timing keyboard interface logic, and coprocessor. This mode allows systems using a CMOS 80286 to go into a low power mode for battery operation while on "stand-by". Refer to Application Note for external logic needed for complete sleep mode implementation.

3.5.3 Command Control

This module generates the I/O read and write commands, memory read and write commands, ALE and BALE from NS1, NS0, and MNIO. It also controls the number of wait states used during each CPU cycle. See the register descriptions for programming information. For information on the emulation of an 8MHz PC/AT refer to section 3.11.

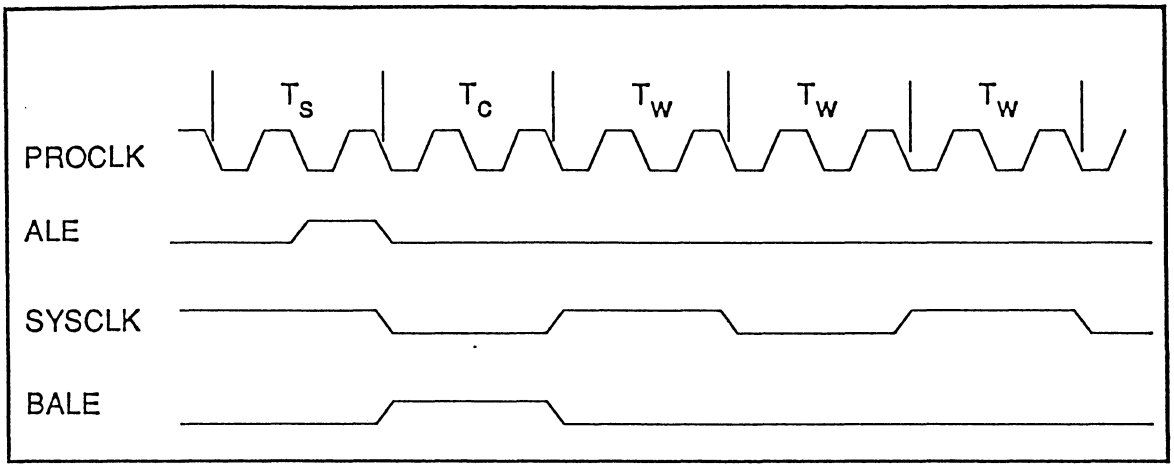


Figure 3.3 SYSCLK TIMING DURING HIGH SPEED OPERATION

3.5.4 Bus Control

This module generates the data buffer controls for CPU, DMA, and refresh cycles. The operation of the bus controls for each PC/AT CPU, DMA and BUS MASTER cycle is described in detail in section 3.11.

The NONBRD signal is used to indicate on board DRAM and I/O operations. The system DRAM and fast on-board I/O devices are assumed to be 16 bit devices. During CPU cycles which access the DRAM, the system data buffers will be disabled. For Bus Master and DMA cycles, NONBRD must be decoded only for on board memory.

3.5.5 A0/BHE Generator

This module generates the system ADR0, NABHE and NEBHE using A0 and NBHE from the 80286 CPU and AEN and DACK2 from the DMA controller in the FE3010.

During CPU cycles A0 from the 80286 is latched with ALE to produce ADR0. For 16 bit DMA transfers and interrupt acknowledge cycles, ADR0 is forced low so that the low byte of the data bus is activated. For all other CPU hold conditions ADR0 is in the tri-state mode for bus master control of ADR0. The FE3001 performs two cycles when an instruction is received to attempt a 16 bit operation to an 8-bit device on an even address boundary. ADR0 is automatically forced to one at the start of the second cycle to insure proper addressing.

During CPU cycles NBHE from the 80286 is latched with ALE to produce NABHE. NEBHE is NABHE latched with BALE. For 16 bit DMA transfers NABHE is forced low so that the low byte of the data bus is activated. ADR0 from the DMA controller is inverted to produce NABHE during an 8 bit DMA transfer. For all other CPU hold conditions NEBHE is in the tri-state mode for bus master control of NEBHE. In bus master mode, NEBHE is used as an input to generate NABHE. In DMA or bus master mode, NBHE becomes an output echoing NEBHE.

3.5.6 Priority Control

The Priority Control module generates the hold request signal to the CPU in response to a request from the DMA controller or refresh timer. For a refresh request, the module generates controls for a refresh cycle. For a DMA operation, this module generates the DMA hold acknowledge (HLDA1).

3.5.7 DMA Control

This module generates the DMARDY signal for the FE3010 peripheral controller. This signal indicates that the DMA may complete its cycle. The module also generates the memory read during DMA by delaying the leading (falling) edge of the FE3010 DMA memory read by one DMA clock.

3.5.8 Error Control

This module generates a non-maskable interrupt (NMI) to the 80286 when a parity error or system bus error is encountered. Parity error, system bus error or NMI can be enabled or disabled from software. They are all disabled on system reset.

3.5.9 Coprocessor Interface

The Coprocessor Interface module provides the system interface to the 80287 Numeric Processor Extension. The reset and chip select to the 80287 are generated in this module in addition to the busy signal to the CPU and interrupt 13 to the interrupt controller.

Interrupt 13 is generated whenever an error is received from the 80287. The busy signal is sent to the 80286 during a busy signal from the 80287 or during an error condition. A reset to the 80287 is generated in response to a system reset or a CPU write to I/O location 0F1.

3.5.10 Reset Control

This module generates the RESCPU signal to bring the 80286 to a known reset state during a power on reset or a CPU reset signal from the keyboard controller. It also generates the NRESET signal for the system. NRESET is held active (low) a minimum of 30 clock cycles on any NRESIN to insure minimum reset time to 80286.

3.5.11 General Notes

* *NIOCS16 must remain valid throughout the cycle.*
* *NONBRD must only be decoded for memory cycles during DMA and bus master cycles and must not be active during interrupt acknowledge cycles.*
* *For memory cycles with NONBRD asserted, the system will use the MDATA bus of the FE3031 for data transfers. For I/O cycles with NONBRD asserted, the system will use the expansion bus (DATA) of the FE3031 for data transfers.*
* *Input clocks should have 50% duty cycle, although duty cycle for CLKHS at 40Mhz depends on the final 20Mhz 80286 spec and FE3001 clock skew.*
* *Inputs CLK16, NBUSY, NERROR, and NCS287 have internal 100k Ω (approx.) pull-up resistors.*

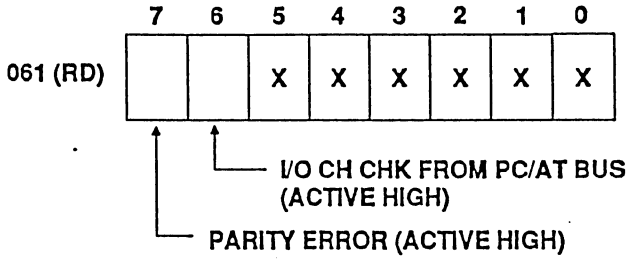
MNIO	NS1	NS0	TYPE OF BUS CYCLE
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None, not a status cycle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None, not a status cycle

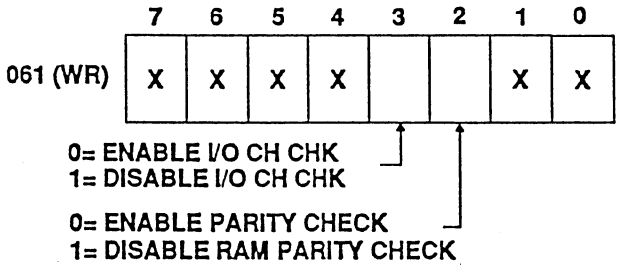
Table 3.2 BUS CYCLES

3.6 FE3001 Registers

3.6.1 Error Control Register (061H), Read/Write

The error control register contains the mask for the parity check and I/O channel check signals. It also provides read port for these signals.

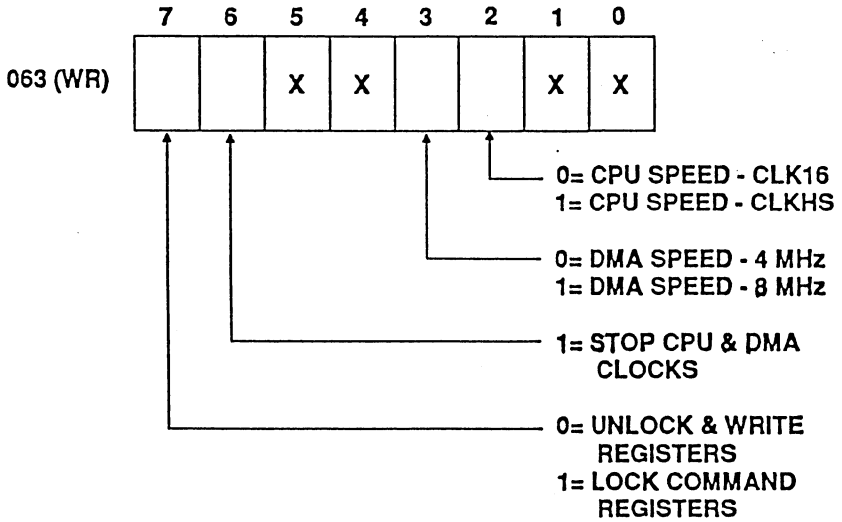




3.6.2 Speed Select (063H), Write

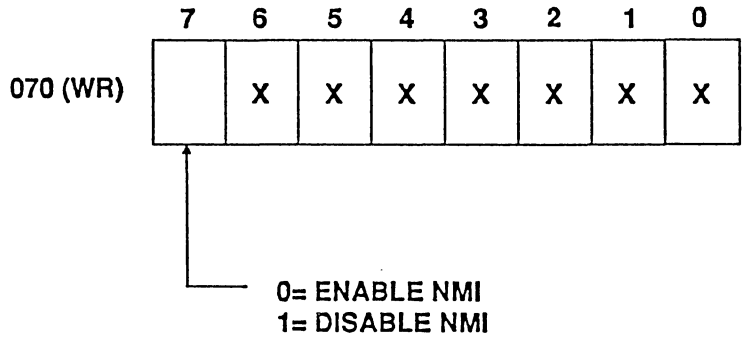
The speed select register controls the speed of the CPU and DMA clocks. This register is also used to stop the CPU (sleep mode) and unlock the command control and speed select registers for access. The lock bit must be reset and D7 must be low to change speed or stop clocks.

The Stop Clock bit stops all the clocks except for the timer clock, coprocessor clock, and keyboard controller clocks. This allows refresh to continue. Bits 2,3, and 6 in the register are cleared and bit 7 is set by system reset.



3.6.3 NMI Enable (070H), Write

The NMI enable register contains the mask for NMI to the 80286. Bit 7 is set on power-up.



3.6.4 Command Control Registers (072H,073H), Write

The timing of the command controls on the expansion bus is programmable via the Command Control Registers. These registers control the timing of BALE, NYMEMR, NYMEMW, NYIOR, NYIOW and the number of wait states in a CPU cycle. This section describes the programming of these registers. Emulation of an 8MHz expansion bus with CPU clock speeds of 16, 24 and 32 MHz is detailed in section 3.11.

The programmable bus signals are shown in Figure 3.4. A summary of the timing registers is shown in Table 3.3.

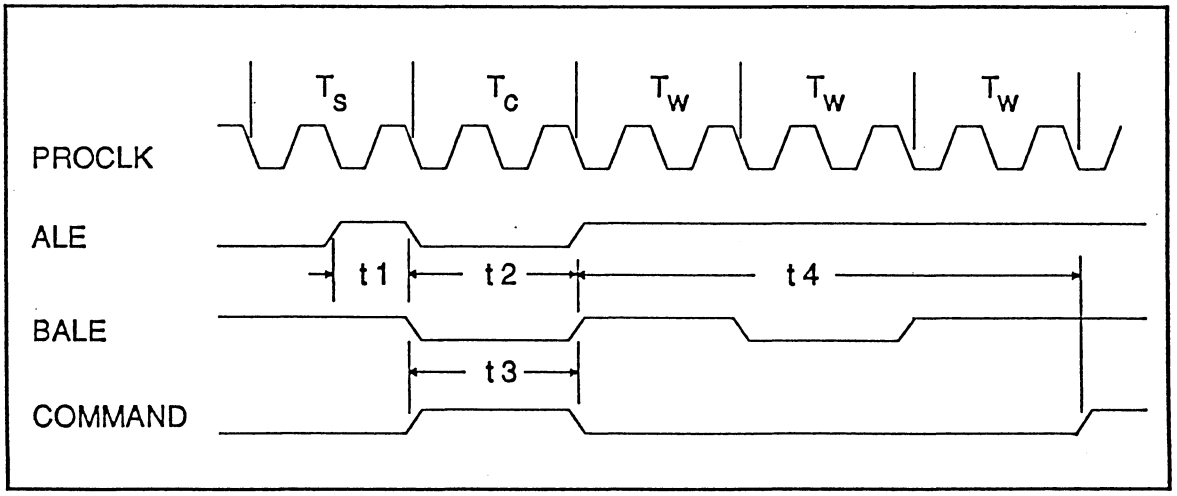


Figure 3.4 PROGRAMMABLE COMMAND TIMING

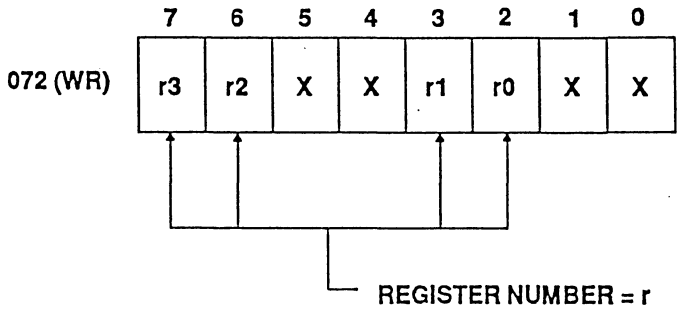
REG	BITS	FUNCTION	WAVEFORM	DEFAULT
R_0	2	BALE delay from ALE leading edge	A	0
R_1	2	BALE width	B	1
R_2		Not used		
R_3	4	8 bit memory, 8/16 bit I/O - cmd delay	C	1
R_4	4	8 bit operation - wait states	D	4
R_5	4	16 bit I/O operation - wait states	D	1
R_6	4	16 bit memory operation - command delay	C	0
R_7	4	16 bit memory operation - wait states	D	1
R_8	4	Minimum number of wait states when NZEROWS is asserted - wait states	D	0
R_9	4	Onboard 16 bit read cycle - wait states	D	1
R_{10}	4	Onboard 16 bit write cycle - wait states	D	1
R_{11}		Not used		
R_{12}	4	On Board I/O operation - command delay	C	1

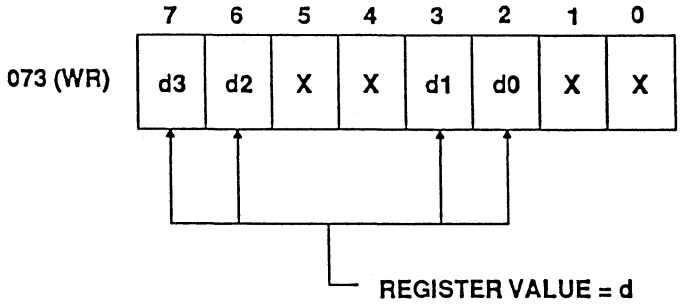
Table 3.3 SUMMARY OF COMMAND TIMING REGISTERS

* *Command delay is number of PROCLKs from end of T_3*
* *Each wait state is two PROCLKs.*
* *One wait state may be added in high speed mode for synchronization.*

3.6.5 Command Register Pointer (072H)

The Command Register Pointer points to one of 11 registers at location 073H. Each register contains a command timing parameter based on the selected CPU clock. Whichever register number is loaded in bits 7,6,3, and 2 in location 072H is the register which is loaded with the next write to address 073H. Refer to Table 3.3 for details.





3.6.6 BALE Timing (R_0,R_1)

The leading edge and width of BALE are controlled by these two registers. BALE delay is defined as the number of PROCLK cycles from the leading edge of ALE. BALE width is the width in PROCLK cycles.

Default values: Delay (R_0) - 0
Width (R_1) - 1

3.6.7 8 Bit Memory and 8/16 bit I/O Command Delay (R_3)

This register controls the command delay for 8 bit memory and 8/16 bit I/O operations. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE to the start of the command.

Default value: Command Delay (R_3) - 1

3.6.8 8 Bit Memory and I/O Wait States (R_4)

This register controls the number of wait states 8 bit operations. The number of wait states is the number of CPU wait states required for these operations.

Default value: Wait States (R_4) - 4

3.6.9 16 Bit I/O Wait States (R_5)

This register controls the number of wait states for 16 bit I/O cycles. These cycles are indicated by the assertion of NIOCS16. The number of wait states is the number of CPU wait states required for this operation.

Default values: Wait States (R_5) - 1

3.6.10 16 Bit AT Bus Memory Timing (R_6,R_7,R_8)

These registers control the command delay and number of wait states for 16 bit memory operations. These cycles are indicated by the assertion of NMEMCS16. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states is the number of CPU wait states required for this operation. The number of wait states for operations with NZEROWS asserted is the number of CPU wait states required to emulate slow speed zero wait state bus operation.

Default values: Command Delay (R_6) - 0
Wait States (R_7) - 1
Wait States,NZWS (R_8) - 0

3.6.11 On Board Memory Timing (R_9,R_{10})

These two registers control the number of wait states for on board operations. These cycles are indicated by the assertion of NONBRD during CPU cycles. Command delay is zero for all on board memory operations. The number of wait states is the number of CPU wait states required for this operation. There are separate registers to program the number of wait states for read and write operations to give the system designer added flexibility and potential for greater speed.

Default values: Wait States,Read (R_9) - 1
Wait States,Write (R_{10}) - 1

3.6.12 On Board I/O Timing (R_{12})

This register controls the command delay for 16 bit on board I/O operations. These cycles are indicated by the assertion of NONBRD during CPU I/O cycles. Command delay is defined as the number of PROCLK cycles from the trailing edge of ALE. The number of wait states for on board I/O is defined by the on board memory registers described above. Additional wait states can be added by using the IOCHRDY signal.

Default values: Command Delay (R_{12}) - 1

3.6.13 CLEAR 80287 BUSY (0F0H), Write

When an error signal is received from the 80287 the NBUSY signal is latched in the ON (0) state. This signal is cleared by an OUT instruction to this port. The output data is don't care.

3.6.14 RESET 80287 (0F1H), Write

An OUT instruction to this port generates a reset to the 80287.

3.7 Package

The FE3001 is packaged in a 84 pin PLCC.

3.8 Absolute Maximum Ratings

Ambient Temperature (operating):	0° to + 70° C
Storage Temperature:	-40° to +125° C
Voltage on any pin to ground:	- .5 V to +7 V
Power Dissipation:	400 mW

3.9 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1]	4		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[1]	-4		mA	V_{OH}= 2.4 V
I_{OL}	LOW V Output Current[2,3]	8		mA	V_{OL}= 0.4 V
I_{OH}	HIGH V Output Current[2,3]	-8		mA	V_{OH}= 2.4 V
V_{OHC}	PROCLK Out HIGH Volt	3.8		V	I_{OH}= -2 mA
V_{DD}	Supply Voltage (Any V_{DD})	4.5	5.5	V	
I_{DD}	Supply Current (Total)			mA	

Table 3.4 DC CHARACTERISTICS

* *1. Output currents are for PROCLK, DMACLK, TMRCLK, PCLK, NPCLK, CLK287, CPURES, ALE, RT-CALE, DTR, SDTR, NDEN0, NDEN1, NSDEN, SCYCLE, NREADY, DMARDY, NNPCS, RST287, NBZ286, NIRQ13, NMI, HOLDRQ, NERFSH, HLDA1, NINTA, NDLYWR, NABHE, NBHE, NON-BRDL.*
* *2. Output currents are for NRESET, NYMEMR, NYMEMW, NYIOR, NYIOW, D6, D7, ADR0, SYSCLK, BALE, NEBHE, ACK.*
* *3. Output current for NREFRESH. This is an I/O pin which is only driven low in output mode. It is in a tri-state condition otherwise. A pull-up resistor is needed to bring the output high.*
* *4. Input buffers for NREFRESH and NRESIN have hysteresis to compensate for extremely long rise times on the inputs.*

3.10 AC Characteristics (T_a=0° to 70°C, V_{dd}=4.5 to 5.5V, C_L=50pf)

SYMBOL	MIN	MAX	UNIT	PARAMETER
t_1		12	ns	ALE active delay from PROCLK
t_2		15	ns	ALE inactive delay from PROCLK
t_3		17	ns	BALE active delay from PROCLK, BALE delay = 0 (R_1)
t_3		13	ns	BALE active delay from PROCLK, BALE delay 0 (R_1)
t_4		20	ns	BALE inactive delay from PROCLK
t_5		21	ns	NYMEMR,NYMEMW active delay from PROCLK
t_6		20	ns	NYMEMR,NYMEMW inactive delay from PROCLK
t_7		20	ns	NYIOR,NYIOW active delay from PROCLK
t_8		16	ns	NYIOR,NYIOW inactive delay from PROCLK
t_9		20	ns	ADR0 delay from ALE active
t_{10}		20	ns	NABHE delay from ALE active
t_{11}		16	ns	NREADY active delay from PROCLK
t_{12}	25		ns	NREADY inactive delay from PROCLK (PROCLK at end of T_c)
t_{13}		20	ns	DTR low delay from PROCLK (RD)
t_{14}	0	18	ns	DTR high delay from NDEN0,1 inactive (RD)
t_{15}	0	20	ns	NDEN0,1 active delay from DTR low (RD)
t_{16}	3	19	ns	NDEN0,1 inactive delay from PROCLK (RD)
t_{17}		20	ns	NDEN0,1 active delay from PROCLK (WR)
t_{18}		20	ns	NDEN0,1 inactive delay from PROCLK (WR)
t_{21}	13		ns	NS1,NS0 setup time to PROCLK
t_{22}	30		ns	NZEROWS setup time to PROCLK
t_{23}	24		ns	NONBRD setup time to PROCLK (Memory)
t_{24}	32		ns	NONBRD setup time to PROCLK (I/O)
t_{25}	32		ns	NMEMCS16 setup time to PROCLK
t_{26}	36		ns	NIOCS16 setup time to PROCLK
t_{27}	12		ns	IOCHRDY setup time to PROCLK

Table 3.5 AC CHARACTERISTICS

NOTE:

All delays with respect to PROCLK are with respect to the falling edge of PROCLK.

The following describes at which falling edge of PROCLK that t_{22}, t_{25}, t_{26}, and t_{27} is referenced.

t_{22} : NZEROWS SET-UP TIME TO PROCLK:

This signal must be set-up prior to the falling edge of PROCLK that would normally end the bus cycle. For example, if Register R_8 in the FE3001 is set so that two wait states will be inserted for a 16-bit cycle with NZEROWS asserted, then the NZEROWS line must be set-up t_{22} before the falling edge of PROCLK that marks the middle of the second wait state.

t_{25} :NMEMCS16 SET-UP TIME TO PORCLK:

t_{26} :NIOCS16 SET-UP TIME TO PROCLK:

These signals must be set-up prior to the falling edge of PROCLK that marks the beginning of the command being asserted.

t_{27} :IOCHRDY SET-UP TIME TO PROLK:

This signal must be set-up prior to the falling edge of PROCLK that is two PROCLKs before the falling edge that would normally mark the end of the bus cycle if it was not going to be extended.

3.11 FE3001 Bus Cycle Programming

3.11.1 Overview

This section describes the FE3001 programmable bus timing registers and the default values necessary for 8 MHz bus emulation on 8 MHz, 12 MHz, and 16 MHz PC/AT systems. The FE3001 AT Control Logic IC contains a set of programmable registers which determine the AT bus timing. This allows the CPU to operate at a high speed while communicating with low speed (8 MHz) peripheral boards. This also makes switching the CPU clock for each bus access unnecessary.

3.11.2 Register Descriptions

The timing of the command controls on the expansion bus is programmable via the Command Control Registers. These registers control the bus timing parameters BALE, NYMEMR, NYMEMW, NYIOR, NYIOW and the number of wait states in a CPU cycle.

The programmable bus signals are shown in Figure 3.5. A summary of the timing registers is shown in Table 3.6.

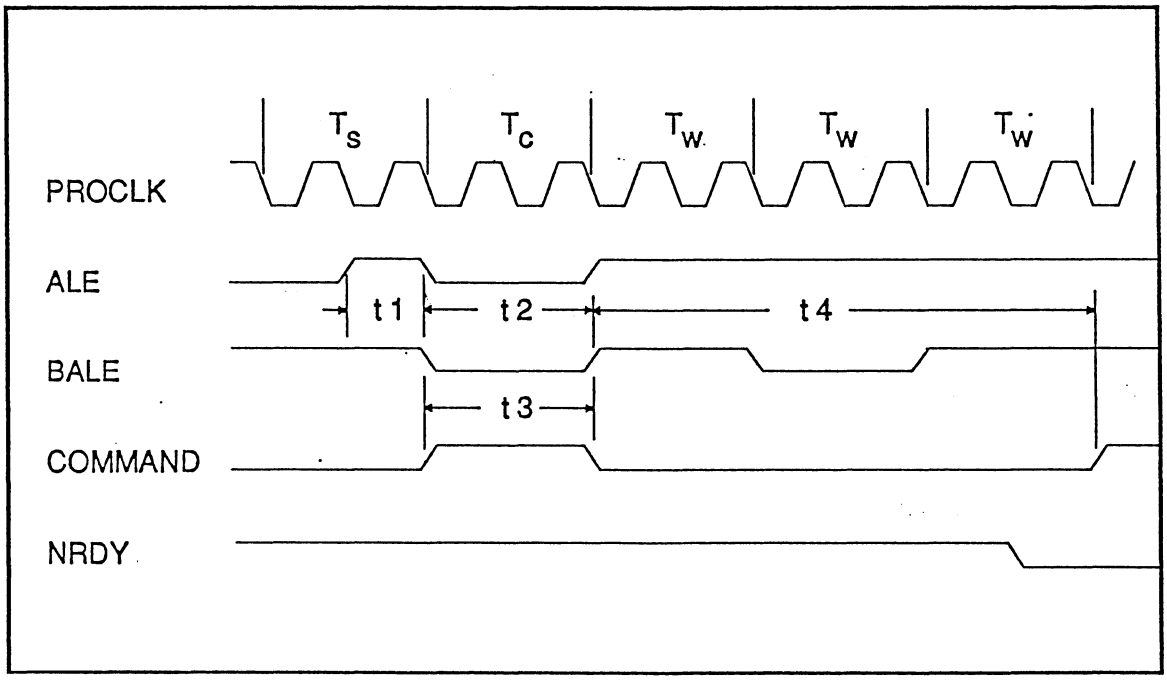


Figure 3.5 PROGRAMMABLE COMMAND TIMING

REG	SIZE	FUNCTION	WAVEFORM	DEFAULT
R_0	2	BALE delay from ALE leading edge	A	0
R_1	2	BALE width	B	1
R_2		Not Used		
R_3	4	8 bit memory, 8/16 bit I/O - cmd delay	C	1
R_4	4	8 bit operation - wait states	D	4
R_5	4	16 bit I/O operation - wait states	D	1
R_6	4	16 bit memory operation - command delay	C	0
R_7	4	16 bit memory operation - wait states	D	1
R_8	4	16 bit memory operation ZWS - wait states	D	0
R_9	4	Local DRAM read operation - wait states	D	1
R_{10}	4	Local DRAM write operation - wait states	D	1
R_{11}	4	Local DRAM write operation - cmd delay	C	0
R_{12}	4	On Board I/O operation - command delay	C	1

Table 3.6 SUMMARY OF COMMAND TIMING REGISTERS

3.12 On Board I/O and Memory operations (R_9,R_{10},R_{11})

These registers control the timing of non-bus operations and not discussed in this section.

3.13 8 MHz System clock - 8 MHz bus emulation

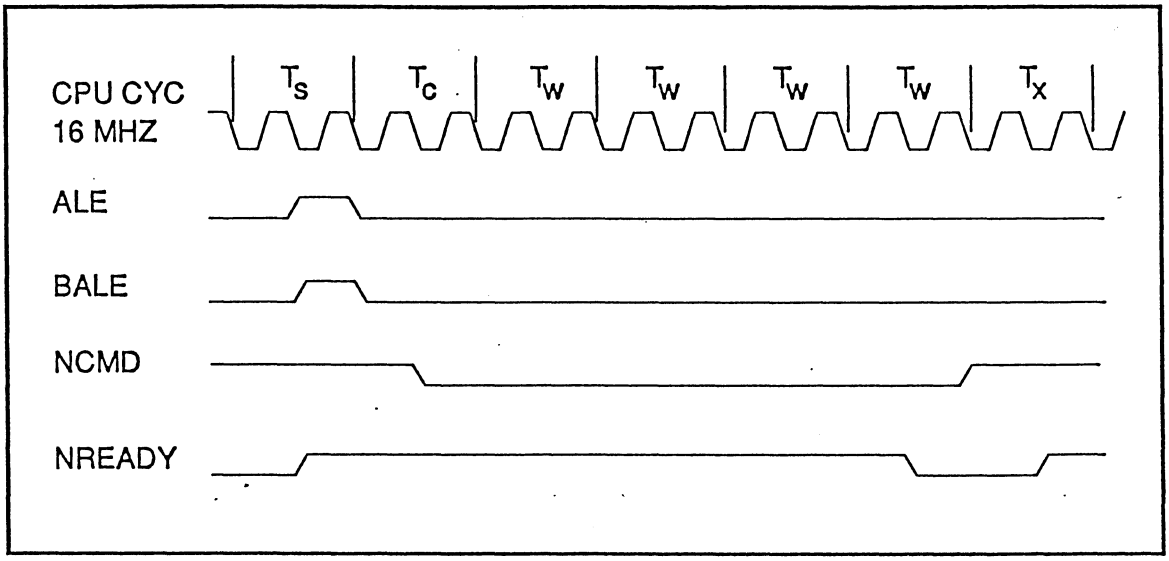
This section defines the default values for the programmable bus timing registers in the FE3001. These values are for an 8 MHz system clock with the system emulating an 8MHz bus.

For all bus cycles the values for R0 and R1 are shown below.

REG	DEFAULT	FUNCTION
R_0	0	BALE delay from ALE leading edge
R_1	1	BALE width

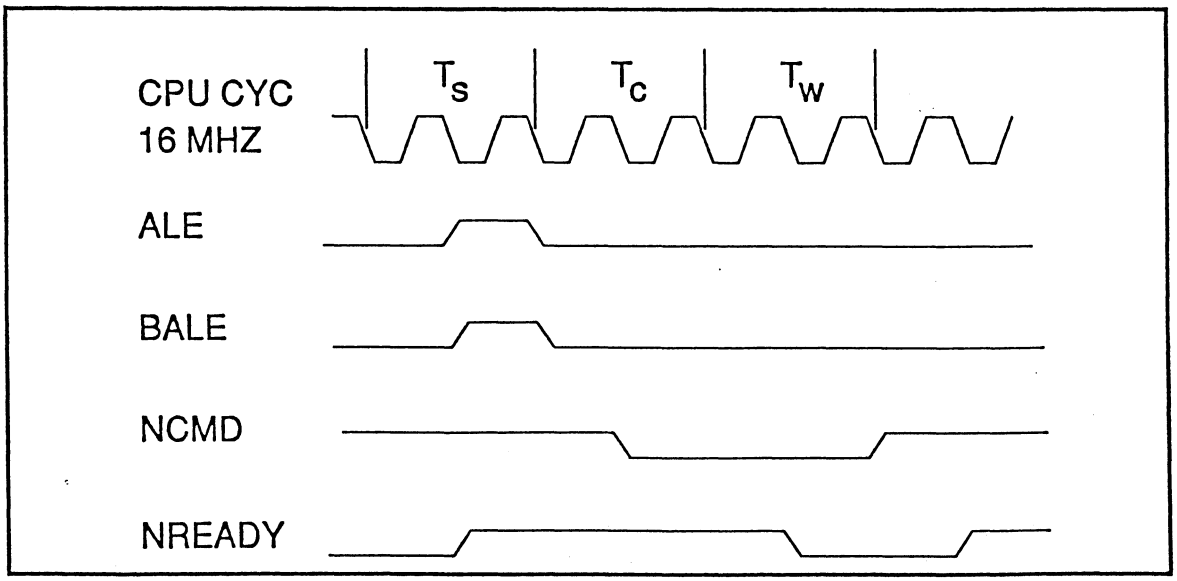
3.14 8 bit memory or I/O operation

REG	DEFAULT	FUNCTION
R3	1	8 bit memory, 8/16 bit I/O - cmd delay
R4	4	8 bit operation - wait states



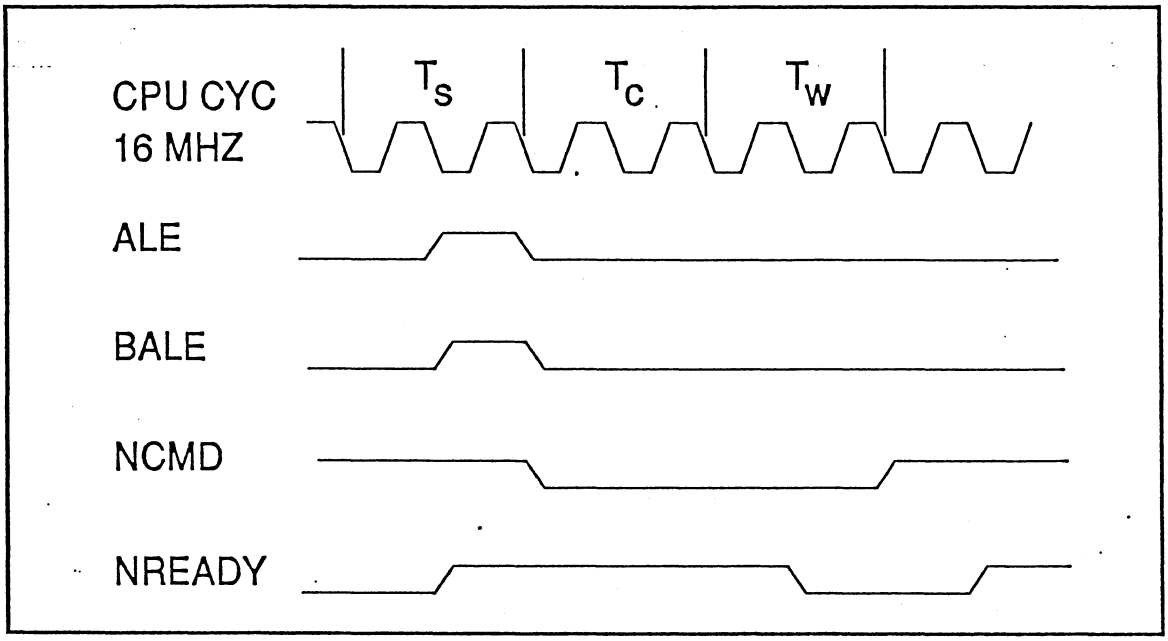
3.15 16 bit I/O operation

REG	DEFAULT	FUNCTION
R3	1	8 bit memory, 8/16 bit I/O - cmd dly
R5	1	16 bit I/O operation - wait states



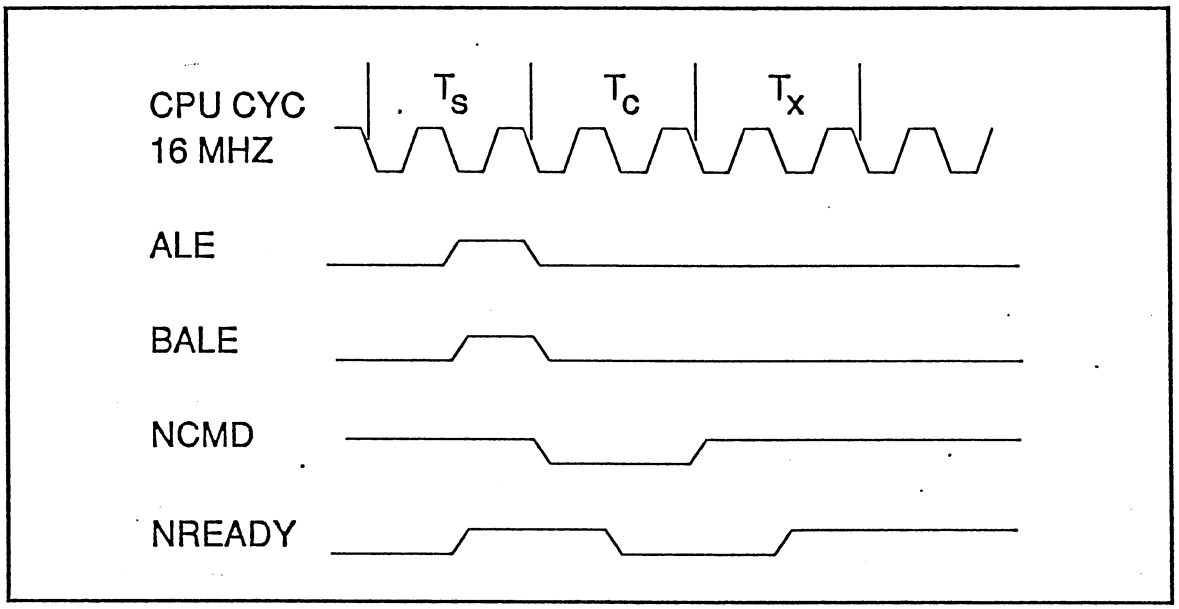
3.16 16 bit memory operation

REG	VALUE	FUNCTION
R6	0	16 bit memory operation - command delay
R7	1	16 bit memory operation - wait states



3.17 16 bit memory operation - ZWS asserted

REG	DEFAULT	FUNCTION
R_6	0	16 bit memory operation - command delay
R_8	0	16 bit memory operation (ZWS) - wait states



3.18 12 MHz System clock - 8 MHz bus emulation

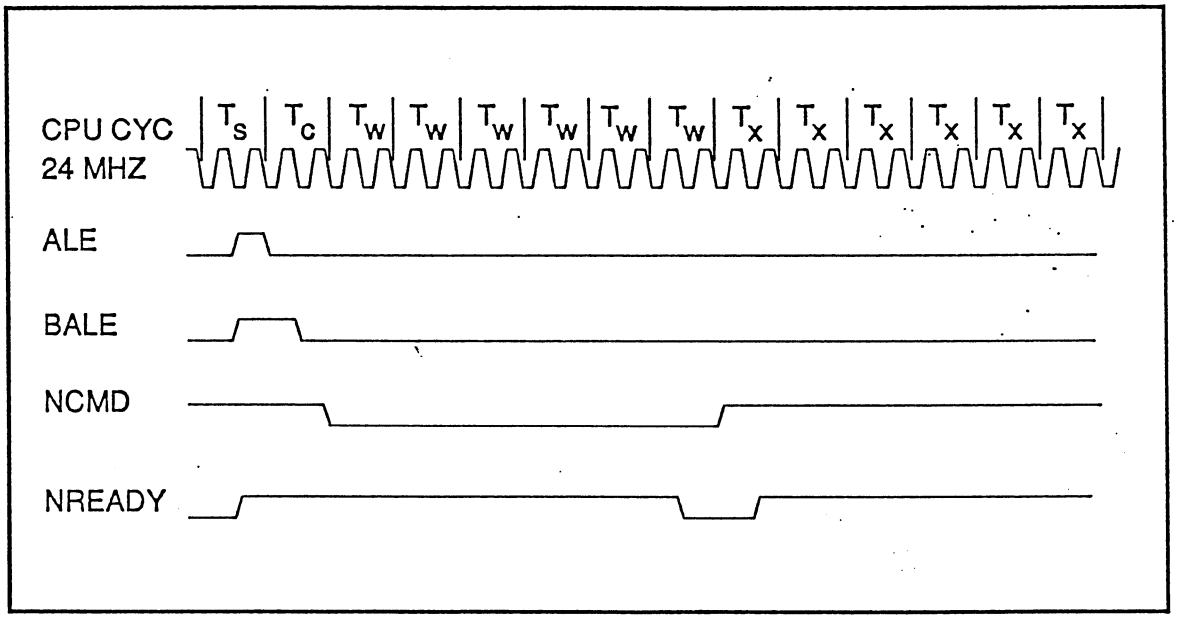
This section describes the register values necessary for a 12 MHz system to emulate an 8 MHz PC/AT bus.

For all bus cycles the values for R0 and R1 are shown below.

REG	VALUE	FUNCTION
R_0	0	BALE delay from ALE leading edge
R_1	2	BALE width

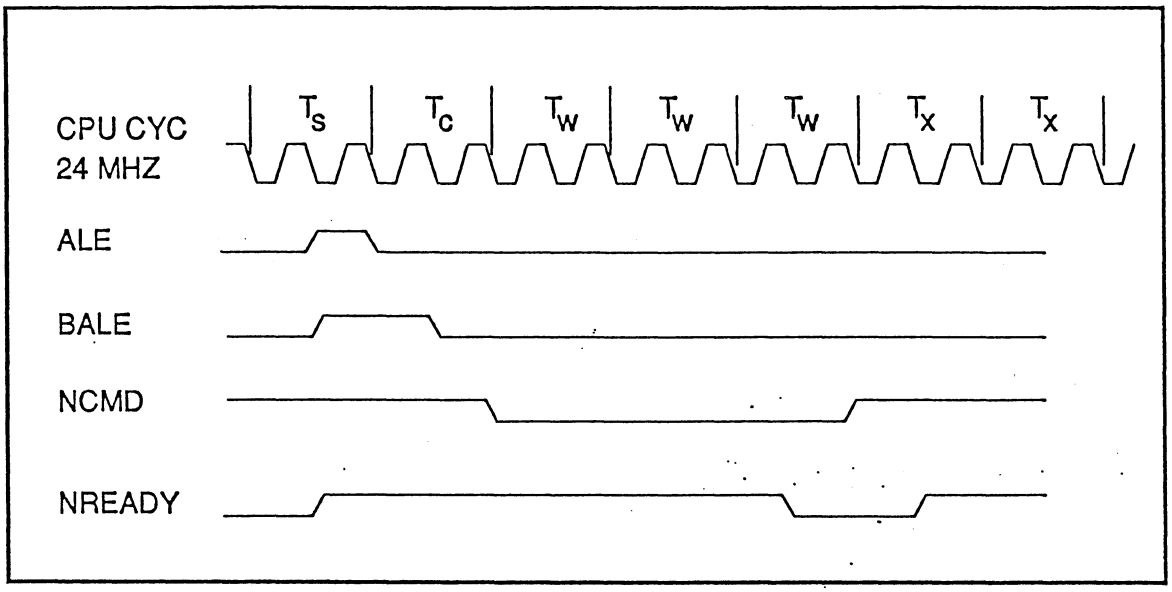
3.19 8 bit memory or I/O operation

REG	VALUE	FUNCTION
R_3	1	8 bit memory, 8/16 bit I/O - cmd delay
R_4	7	8 bit operation - wait states



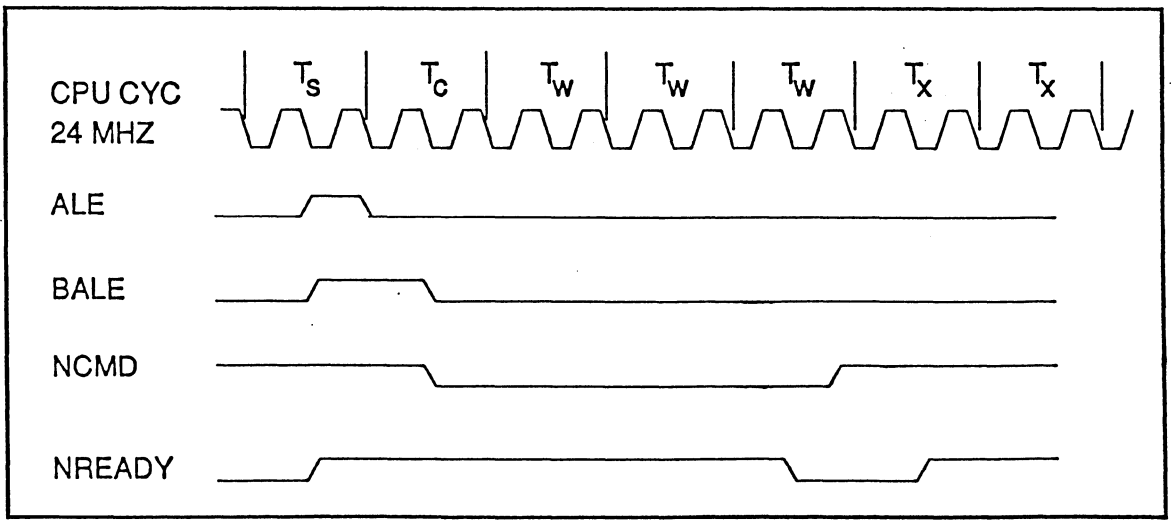
3.20 16 bit I/O operation

REG	VALUE	FUNCTION
R3	1	8 bit memory, 8/16 bit I/O - cmd dly
R5	3	16 bit I/O operation - wait states



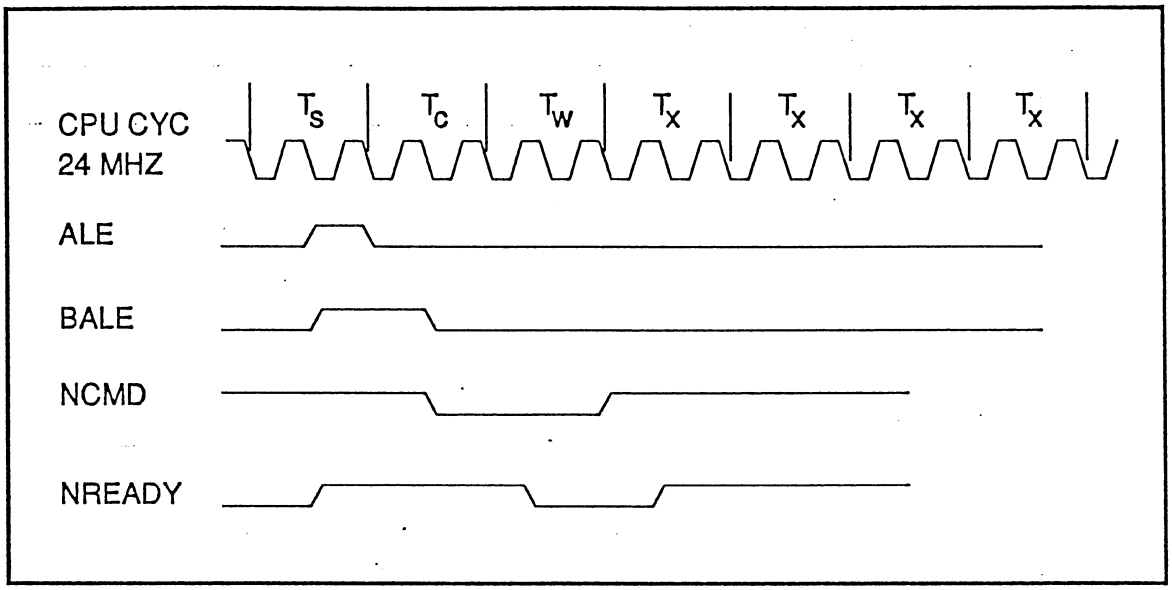
3.21 16 bit memory operation- 24 MHz

REG	VALUE	FUNCTION
R6	0	16 bit memory operation - command delay
R7	3	16 bit memory operation - wait states



3.22 16 bit memory operation - ZWS asserted

REG	VALUE	FUNCTION
R_6	0	16 bit memory operation - command delay
R_8	1	16 bit memory operation (ZWS) - wait states



3.23 16 MHz System clock - 8 MHz bus emulation

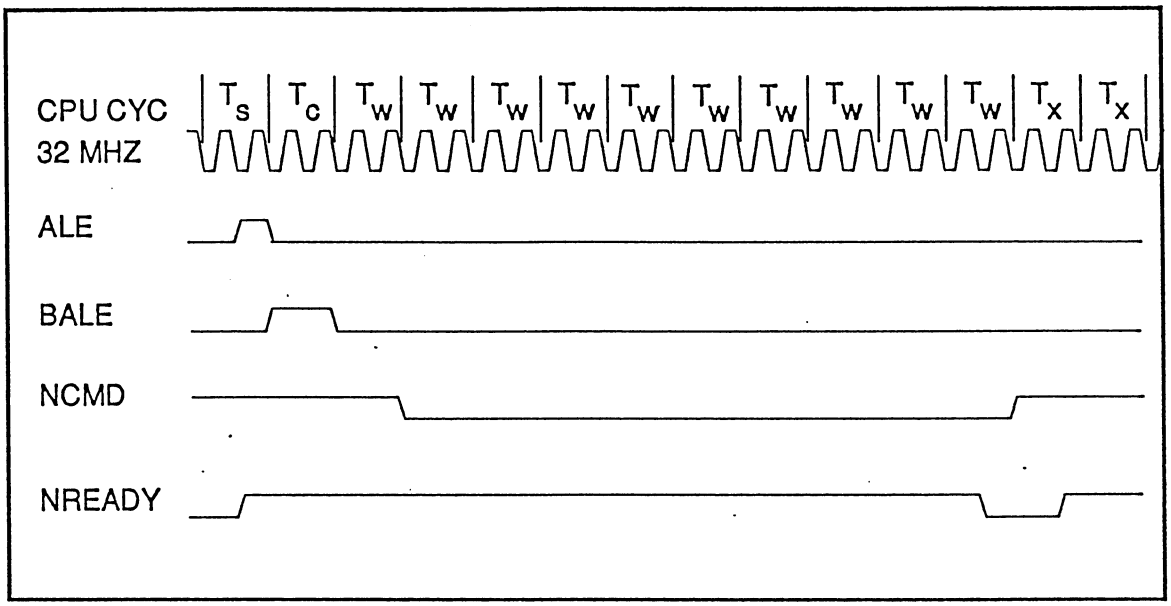
This section describes the register values necessary for a 16 MHz system to emulate an 8 MHz PC/AT bus.

For all bus cycles the values for R0 and R1 are shown below.

REG	VALUE	FUNCTION
R_0	1	BALE delay from ALE leading edge
R_1	2	BALE width

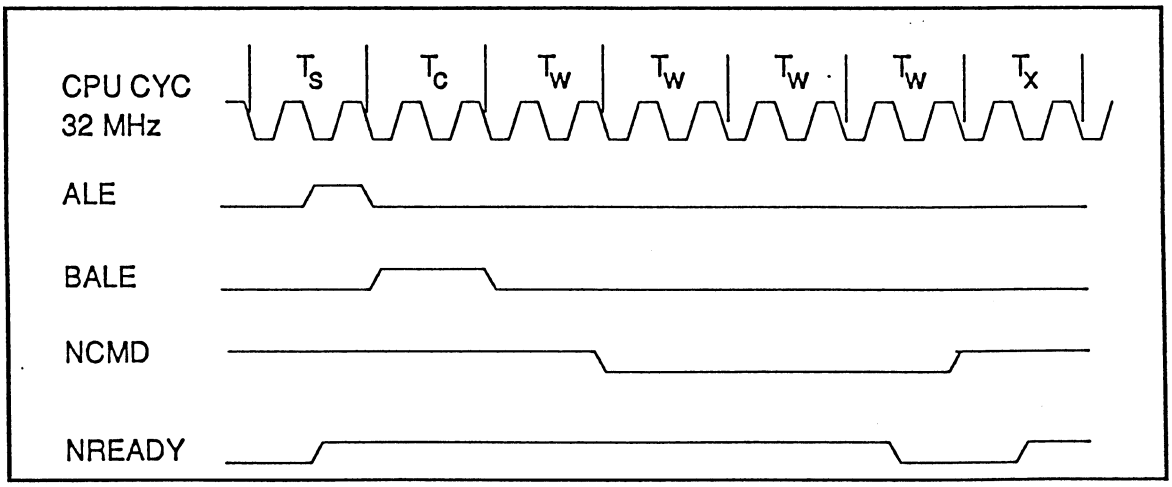
3.24 8 bit memory or I/O operation

REG	VALUE	FUNCTION
R3	4	8 bit memory, 8/16 bit I/O - cmd delay
R4	10	8 bit operation - wait states



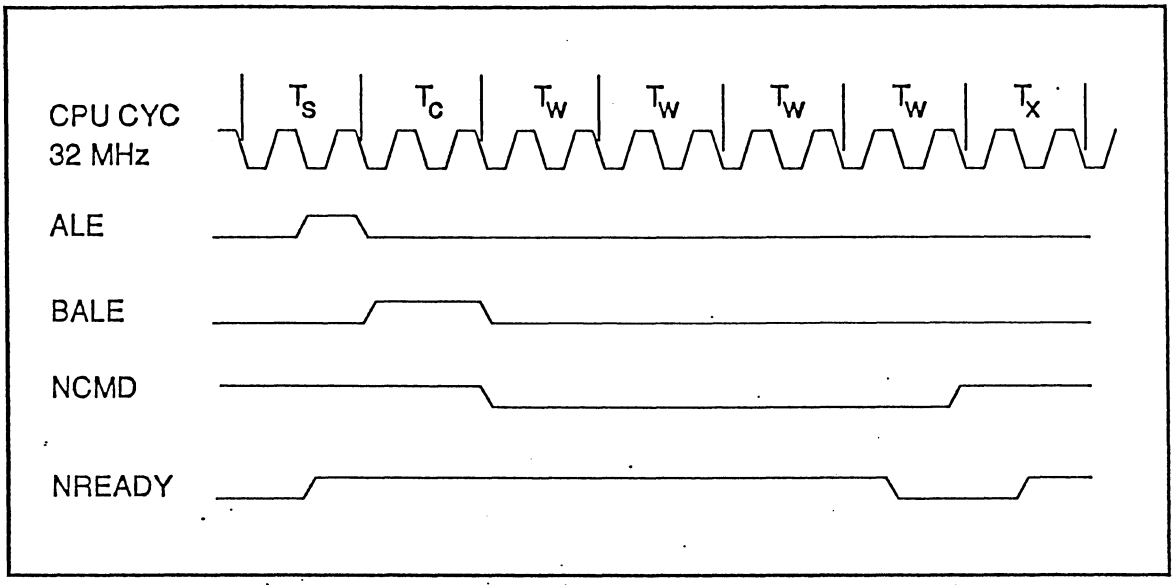
3.25 16 bit I/O operation

REG	VALUE	FUNCTION
R3	4	8 bit memory, 8/16 bit I/O - cmd dly
R5	4	16 bit I/O operation - wait states



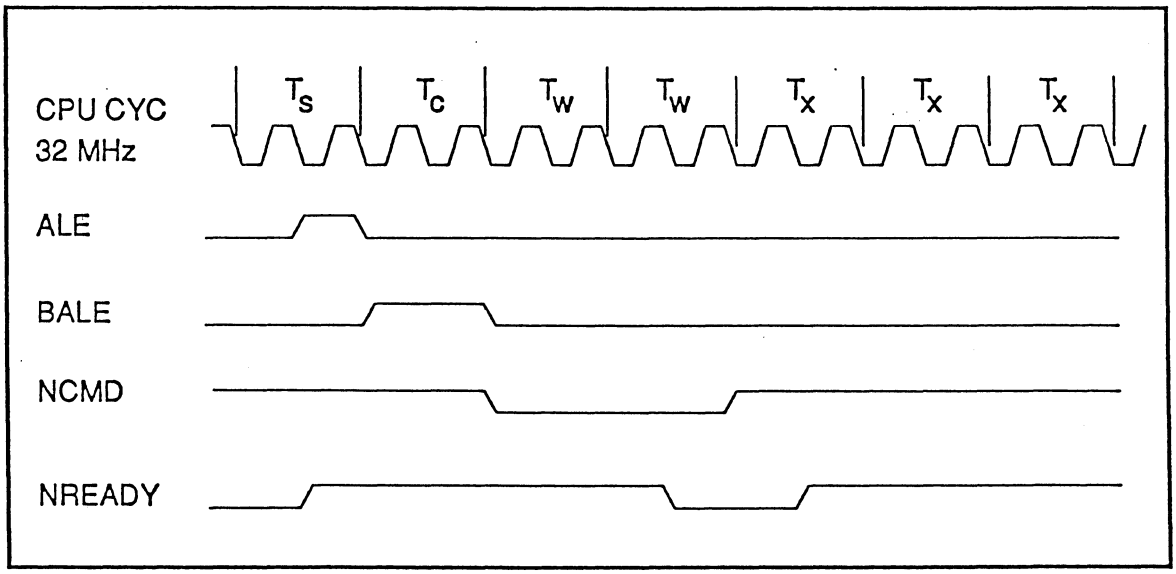
3.26 16 bit memory operation

REG	VALUE	FUNCTION
R_6	2	16 bit memory operation - command delay
R_7	4	16 bit memory operation - wait states



3.27 16 bit memory operation - ZWS asserted

REG	VALUE	FUNCTION
R_6	2	16 bit memory operation - command delay
R_8	2	16 bit memory operation (ZWS) - wait states



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FE3010B AT PERIPHERAL CONTROL LOGIC

4.0 Introduction

The FE3010B AT peripheral controller is a highly integrated chip with various control and peripheral functions. The FE3010B has been designed to enhance the IBM PC AT while being extremely flexible. The FE3010B incorporates the following features:

- 100% hardware and software compatible to the IBM PC-AT
- 15 interrupt channels
- 3 timer channels
- 7 DMA channels
- TTL compatible
- 84-pin, J-type leaded surface mount plastic chip carrier
- DMA clock rate up to 8 MHz
- HCMOS technology
- Refresh circuitry for 256K or 1 MB RAM Chips
- DMA page registers

The FE3010B is used in conjunction with the FE3000A, the PC AT CPU controller, the FE3020 address buffer, and the FE3030 data buffer to reduce the size of a typical PC AT motherboard by 80%, power by 70%, and the component count by 62%. The FE3010B has designed to be upward-compatible with the Intel 80386 processor.

Figure 4.1 illustrates a block diagram of the FE3010B AT peripheral logic control integrated circuit. Refer to Table 4.1 for the pin descriptions shown in Figure 4.2.

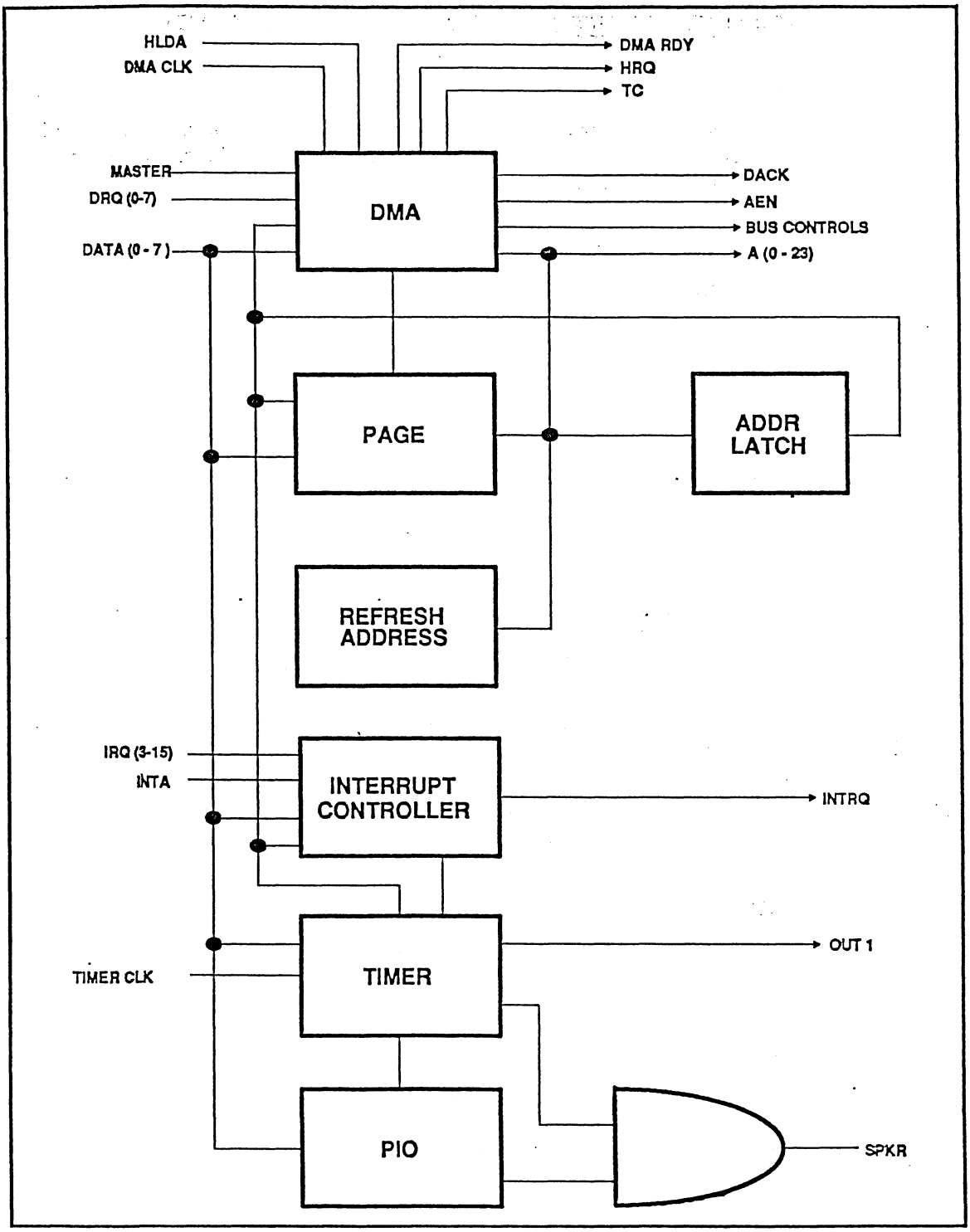

Figure 4.1 FE3010B FUNCTIONAL BLOCK DIAGRAM

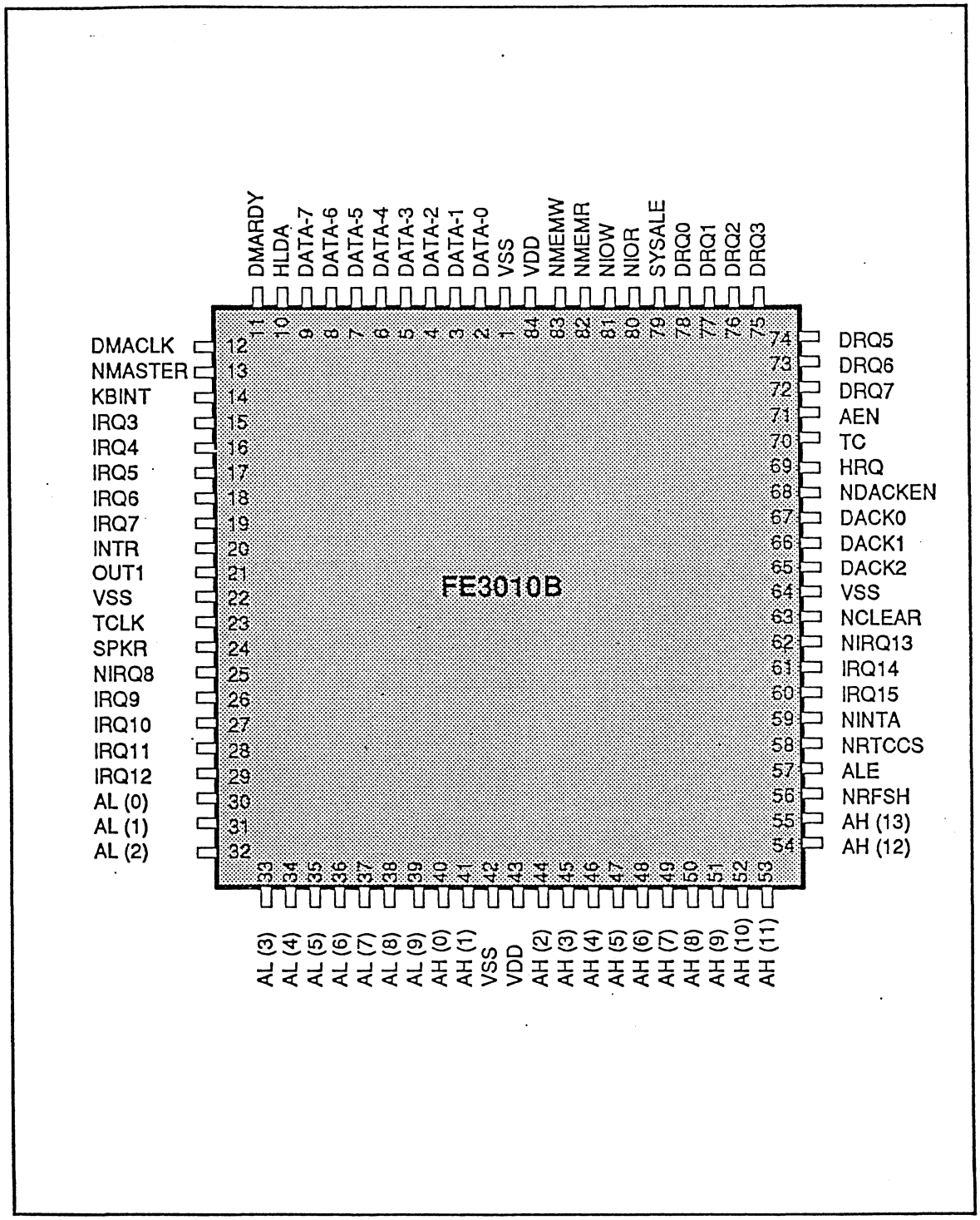

Figure 4.2 FE3010B PIN LOCATIONS

PIN	TYPE	SYMBOL	FUNCTION
1		Vss	GROUND
2	I/O	DATA(0)	DATA BIT 0
3	I/O	DATA(1)	DATA BIT 1
4	I/O	DATA(2)	DATA BIT 2
5	I/O	DATA(3)	DATA BIT 3
6	I/O	DATA(4)	DATA BIT 4
7	I/O	DATA(5)	DATA BIT 5
8	I/O	DATA(6)	DATA BIT 6
9	I/O	DATA(7)	DATA BIT 7
10	I	HLDA	HOLD ACKNOWLEDGE
			Active high. Acknowledge from the
			CPU (80286) for a request for the
			bus from the DMA controller.
11	I	DMARDY	DMA READY
			Active high
			Signal to indicate that the DMA
			may complete its current cycle.
12	I	DMACLK	DMA CLOCK
			System clock/ DMACLK
			6 MHz / 3 or 6 MHz
			8 MHz / 4 or 8 MHz
			10 MHz / 5 MHz
13	I	NMASTER	BUS MASTER
			Active low
			Signal indicating a master on the
			expansion bus has bus control.
14	I	KBINT	KEYBOARD INTERRUPT
			Active high
15	I	IRQ3	INTERRUPT REQUEST 3
			Active high
16	I	IRQ4	INTERRUPT REQUEST 4
			Active high
17	I	IRQ5	INTERRUPT REQUEST 5
			Active high
18	I	IRQ6	INTERRUPT REQUEST 6
			Active high
19	I	IRQ7	INTERRUPT REQUEST 7
			Active high
20	O	INTR	INTERRUPT REQUEST TO CPU
			(80286)
			Active high
21	O	OUT1	TIMER CHANNEL 1 OUTPUT
22		Vss	GROUND

Table 4.1 PIN ASSIGNMENT INFORMATION

PIN	TYPE	SYMBOL	FUNCTION
23	I	TCLK	TIMER CLOCK
			(1.19 MHz clock for timer)
24	O	SPKR	SPEAKER DATA
25	I	NIRQ8	INTERRUPT REQUEST 8
			Active low
26	I	IRQ9	INTERRUPT REQUEST 9
			Active high
27	I	IRQ10	INTERRUPT REQUEST 10
			Active high
28	I	IRQ11	INTERRUPT REQUEST 11
			Active high
29	I	IRQ12	INTERRUPT REQUEST 12
			Active high
30-39	I/O	AL(0-9)	ADDRESS BIT 0-9

NOTE

All addresses going in the FE3010B during CPU cycles are latched with ALE except for A0. This allows compatibility for 16-bit writes to the FE3010B, although 8-bit accesses are preferred. A0 is latched in the FE3000A, so no external latch on A0 is necessary if the FE3000A is used with the FE3010B.

40	O	AH(0)	ADDRESS BIT 10
41	O	AH(1)	ADDRESS BIT 11
42		V_{SS}	GROUND
43		V_{DD}	+5 VOLTS SUPPLY
44	O	AH(2)	ADDRESS BIT 12
45	O	AH(3)	ADDRESS BIT 13
46	O	AH(4)	ADDRESS BIT 14
47	O	AH(5)	ADDRESS BIT 15
48	O	AH(6)	ADDRESS BIT 16
49	O	AH(7)	ADDRESS BIT 17
50	O	AH(8)	ADDRESS BIT 18
51	O	AH(9)	ADDRESS BIT 19
52	O	AH(10)	ADDRESS BIT 20
53	O	AH(11)	ADDRESS BIT 21
54	O	AH(12)	ADDRESS BIT 22

Table 4.1 PIN ASSIGNMENT INFORMATION (CONTINUED)

PIN	TYPE	SYMBOL	FUNCTION
55	O	AH(13)	ADDRESS BIT 23
56	I	NRFSH	REFRESH ADDRESS
			Active low
			Signal to enable the refresh address
			to the address bus during a RAM
			refresh cycle.
57	I	ALE	ADDRESS LATCH ENABLE
			Active high
58	O	NRTCCS	REAL TIME CLOCK
59	I	NINTA	INTERRUPT ACKNOWLEDGE
			FROM CPU (80286)
			Active low
			Interrupt acknowledge to the
			interrupt controllers
60	I	IRQ15	INTERRUPT REQUEST 15
			Active high
61	I	IRQ14	INTERRUPT REQUEST 14
			Active high
62	I	NIRQ13	INTERRUPT REQUEST 13
			Active low
			Error interrupt from (80287)
63	I	NCLEAR	SYSTEM CLEAR
			Active low
64		Vss	GROUND
65	O	DACK2	DMA ACKNOWLEDGE BIT 2
DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	illegal
1	0	1	5
1	1	0	6
1	1	1	7
66	O	DACK1	DMA ACKNOWLEDGE BIT 1
67	O	DACK2	DMA ACKNOWLEDGE BIT 0
68	O	NDACKEN	DMA ACKNOWLEDGE ENABLE
			Active low
			Signal to enable DACK0, DACK1,
			and DACK2 decode.

Table 4.1 PIN ASSIGNMENT INFORMATION (CONTINUED)

PIN	TYPE	SYMBOL	FUNCTION
69	O	HRQ	DMA REQUEST TO CPU (80286)
			Active high
70	O	TC	DMA END OF OPERATION
			Active high
			Signal to indicate the DMA
			controller has finished its cycle.
71	O	AEN	DMA AEN
			Active high
			Signal to indicate that the current
			bus is a DMA cycle.
72	I	DRQ7	CHANNEL 7 DMA REQUEST
			Active high
73	I	DRQ6	CHANNEL 6 DMA REQUEST
			Active high
74	I	DRQ5	CHANNEL 5 DMA REQUEST
			Active high
75	I	DRQ3	CHANNEL 3 DMA REQUEST
			Active high
76	I	DRQ2	CHANNEL 2 DMA REQUEST
			Active high
77	I	DRQ1	CHANNEL 1 DMA REQUEST
			Active high
78	I	DRQ0	CHANNEL 0 DMA REQUEST
			Active high
79	O	SYSALE	SYSTEM ALE
			Active high
			Signal to latch the address
			in the address latch.
80	I/O	NIOR	I/O READ COMMAND
			Active low
81	I/O	NIOW	I/O WRITE COMMAND
			Active low
		NOTE	
		Data must be valid before NIOW to the FE3010B goes low because the leading edge of NIOW is used to clock some registers in the FE3010B. This setup time (data valid to NIOW active low) is specified at 0 ns minimum, although 10 ns is recommended to compensate for any external variation.	
82	O	NMEMR	MEMORY READ COMMAND
			Active low
83	O	NMEMW	MEMORY WRITE COMMAND
			Active low
84		V_{DD}	+5 VOLTS SUPPLY

Table 4.1 PIN ASSIGNMENT INFORMATION (CONTINUED)

4.1 FE3010B 8237

4.1.1 DMA Controllers

The FE3010B contains two 8237 equivalent DMA Controllers. DMA controller #1 is in the I/O address space from 000 to 00F and is used for 8 bit transfers. DMA controller #2 is in the I/O space from 0C0 to 0DE and is used for 16 bit transfers. Channel 0 of DMA controller #2 is used to cascade DMA controller #1.

AT Bus DMA Channel	DMA Controller	Transfer Type
0	#1 Channel 0	8 bit
1	#1 Channel 1	8 bit
2	#1 Channel 2	8 bit
3	#1 Channel 3	8 bit
4	#2 Channel 0	Cascade DMA Cont. #1
5	#2 Channel 1	16 bit
6	#2 Channel 2	6 bit
7	#2 Channel 3	16 bit

4.1.2 Transfer Modes

Each DMA channel may be programmed in Single Transfer Mode, Block Transfer Mode, Demand Transfer Mode, or Cascade Mode.

Single Transfer Mode

In single transfer mode the channel will make one transfer for each request. The word count will be decremented, and the address will be incremented or decremented at the end of each transfer. When the word count goes from 0000 to FFFF, a terminal count (TC) will be generated. To start a transfer the DRQ should be held active high until a DACK is received. If the DRQ is held active through the cycle, only one transfer will take place. The DRQ must go low and then high to start another transfer. The bus will be released between transfers.

Block Mode Transfer

A transfer is started in block mode by a DRQ and continues until a TC is reached. The DRQ should be held active until DACK becomes active. Block mode should be used with caution since refresh will be locked out. The address and word count behave as in single mode.

Demand Mode

In demand mode a transfer will continue to take place until DRQ is inactive or a TC is reached. If the DRQ is dropped, the bus will be released. If DRQ is activated again, the transfer will resume. The address and word count behave as in single mode.

Cascade Mode

Cascade mode is used to cascade DMA controller #2 to DMA controller #1, and for bus master transfers. A channel in cascade mode will get the bus when a DRQ is active, but the word count and address are ignored. The channel will hold the bus until DRQ is inactive. The IOR, IOW, MEMR, and MEMW signals must be generated by the bus master device. The addresses from the FE3010B are floated when the MASTER signal becomes active.

4.1.3 Transfer Types

There are three types of transfers - read, write, and verify.

Read

A read transfers data from memory to an I/O device.

Write

A write transfers data from and I/O device to memory.

Verify

A verify transfer is a pseudo transfer that does not generate IOR, IOW, MEMR, or MEMW signals.

Autoinitialize

A channel may be programmed to autoinitialize for any transfer type. In this mode when a TC is reached the channel is loaded with the original word count and address, and is ready to start another transfer.

Priority

Each DMA controller has two types of priority fixed and rotating. For fixed priority, channel 0 has the highest priority and channel 3 has the lowest. In rotating priority, the last channel to be serviced has the lowest priority. The DMA controller #2 has priority over the DMA controller #1.

Extended Write

In normal timing the MEMR or IOR pulse is two clock cycles and the MEMW or IOW is one clock cycle. If extended write is selected, the MEMW or IOW will be the same as the MEMR or IOR.

Base and Current Address Registers

Each channel has a 16 bit base and current address register. The current address register is loaded from the base register when the base register is loaded or when on an autoinitilize mode. The current address register is incremented or decremented during a transfer.

Addresses are driven to the bus while NRFSH is low, indicating a refresh cycle. Only address bits A23-A16 (from the page register) and bits A8-A0 (from the refresh counter) are meaningful during refresh. The address counter gets incremented on the rising edge of NRFSH.

Base and Current Word Count

Each channel has a 16 bit base and current word count register. The current word count register is loaded from the base register when the base register is loaded or when on an autoinitilize mode. The current word count is decremented during a transfer.

COMMAND REGISTER Write
This register is cleared by a reset or Master Clear command.

0-1	Unused
2	Controller Disable
3	Must be 0 for extended write, other: no effect
4	Rotating Priority
5	Extended Write
6-7	Unused

STATUS REGISTER Read
Bits 0-3 are cleared by a reset, a Master Clear command or a status read.

0	Channel 0 has Reached TC
1	Channel 1 has Reached TC
2	Channel 2 has Reached TC
3	Channel 3 has Reached TC
4	Channel 0 DRQ Active
5	Channel 1 DRQ Active
6	Channel 2 DRQ Active
7	Channel 3 DRQ Active

REQUEST REGISTER Write
Each channel may be started by a software request. These request are not affected by the mask register. It is cleared by a reset or a Master Clear command.

0-1	Channel Number >	00	Channel 0
2	Request	01	Channel 1
3-7	Unused	10	Channel 2
		11	Channel 3

MASK REGISTER Write
Each channel has a mask bit associated with it. If it is set the channel is disabled. The bits may be set or cleared by software or set by a TC if the channel is not in autoinitilize mode. All the bits are set by a reset or a Master Clear Function.

Single Mask	
0-1	Channel Select
2	Set/Clear Mask (0 = clear, 1 = Set)
3-7	Unused
Clear Mask	
0-7	Unused
Mask All	
0	Channel 0 Mask
1	Channel 1 Mask
2	Channel 2 Mask
3	Channel 3 Mask
4-7	Unused

MODE REGISTER Write

0-1	Channel Select >	00 Channel 0
		01 Channel 1
		10 Channel 2
		11 Channel 3
2-3	Transfer Type	00 Verify
		01 Write
		10 Read
		11 Unused
4	Autoinitialize	
5	Address Decrement	
6-7	Mode	00 Demand
		01 Single
		10 Block
		11 Cascade

CLEAR POINTER Write

Each DMA controller has a pointer flip flop that indicates which half of the word count or address is being accessed. Each time a word count or address is written or read, the pointer is toggled. When the flip flop is cleared bits 0-7 are accessed and when it is set bit 8-15 are accessed. The pointer may be cleared by writing to the Clear Pointer. Any data is ignored.

MASTER CLEAR Write

A write to the Master Clear will:

1. Clear the Command Register
2. Clear the Status Register
3. Clear the Request Register
4. Set the Mask Register
5. Clear the Pointer Flip Flop

Any data will be ignored.

I/O Address	Read/Write	DMA Controller	Function
000	Read/Write	1	Channel 0 Address
001	Read/Write	1	Channel 0 Word Count
002	Read/Write	1	Channel 1 Address
003	Read/Write	1	Channel 1 Word Count
004	Read/Write	1	Channel 2 Address
005	Read/Write	1	Channel 2 Word Count
006	Read/Write	1	Channel 3 Address
007	Read/Write	1	Channel 3 Word Count
008	Read	1	Status
008	Write	1	Command Register
009	Write	1	Request Register
00A	Write	1	Single Mask
00B	Write	1	Mode Register
00C	Write	1	Clear Pointer
00D	Write	1	Master Clear
00E	Write	1	Clear Mask
00F	Write	1	Mask All
0C0	Read/Write	2	Channel 0 Address
0C2	Read/Write	2	Channel 0 Word Count
0C4	Read/Write	2	Channel 1 Address
0C6	Read/Write	2	Channel 1 Word Count
0C8	Read/Write	2	Channel 2 Address
0CA	Read/Write	2	Channel 2 Word Count
0CC	Read/Write	2	Channel 3 Address
0CE	Read/Write	2	Channel 3 Word Count
0D0	Read	2	Status
0D0	Write	2	Command Register
0D2	Write	2	Request Register
0D4	Write	2	Single Mask
0D6	Write	2	Mode Register
0D8	Write	2	Clear Pointer
0DA	Write	2	Master Clear
0DC	Write	2	Clear Mask
0DE	Write	2	Mask All

4.2 Differences with the 8237 Device

The FE3010B implementation has two differences with the Intel 8237. The DMA addresses in the 8237 is valid during the entire DMA cycle, while the FE3010B multiplexes the address and transfer count on the address bus. Therefore, addresses A16-A0 from the FE3010B need to be latched with SYSALE coming out from the FE3010B. In the FE3400B chip set, these latches are provided in the FE3020.

The second difference is that in the cascade mode, the 8237 does not enable the address outputs, while the FE3010B does. Since the only way to use the cascade mode on an AT system is for BUS Master operation, this is not a problem, since the FE3010B disables its address outputs when the MASTER signal becomes active.

4.3 FE3010B 8259 Interrupt Controllers

The FE3010B contains two 8259 equivalent interrupt controllers. Interrupt controller #1 is in the I/O space 020 to 021 and interrupt controller #2 is in the I/O space from 0A0 to 0A1. Interrupt 2 of interrupt controller #1 is used to cascade interrupt controller #2.

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3-7	#1 Level 3 - 7	AT Bus
8	#2 Level 0	Real Time Clock
9-12	#2 Level 1-4	AT Bus
13	#2 Level 5	Co-Processor
14-15	#2 Level 6-7	AT Bus

4.3 1 Interrupt Sequence

1. An interrupt arrives from a peripheral device, the interrupt may be programmed to be level or edge sensitive. In the level mode the interrupt will keep occuring as long as the interrupt is kept high. In the edge mode it must go low and high for each interrupt. The interrupt will set the appropriate bit in the Interrupt Request Register (IRR).

2. If the interrupt has not been masked off it is passed to the priority circuit. There are three types of priority.

a) Fixed

In fixed priority, interrupt 0 has the highest priority and interrupt 7 has the lowest.

b) Automatic Rotation

In automatic rotation the last interrupt serviced has the lowest priority.

c) Specific Rotation

In this mode the lowest priority interrupt can be set by software. The next interrupt will have the highest priority. For example if interrupt 4 is set to the lowest level, the priority will be 5, 6, 7, 0, 1, 2, 3, and 4.

3. The interrupt controller sends a IRQ to the CPU.

4. The CPU responds with a INTA cycle that freezes priority.

5. The CPU sends another INTA that causes the interrupt controller to send a vector to the CPU and set the appropriate bit in the Interrupt Service Register (ISR) and clear the corresponding bit in the IRR if it is in the edge triggered mode. As long as the bit in the ISR is set, all interrupts at the same level or lower will be inhibited unless programmed for special mask mode.

6. An EOI is issued to end the interrupt. This clears the appropriate bit in the Interrupt Service Register. For the slave adapter (interrupt controller #2) two EOI's must be issued. There are three types of EOI's.

a) Specific

An EOI is issued by software for a specific interrupt.

b) Non-Specific

A non-specific EOI is issued by software. The hardware will generate a EOI for the highest level active interrupt.

c) Automatic

An automatic EOI is a non-specific EOI that is caused by the second INTA.

The interrupt controllers may also be operated in a polled mode. In this mode the CPU is set to disable the interrupt input. Instead software must issue a poll command. This takes the place of an INTA, and the software can then read the Interrupt Level to determine the interrupt to be serviced.

When cascading is used and the slave has issued an interrupt, other interrupts from the slave are locked out. If it is desired to preserve priority in the slave (i.e. allow higher interrupts to occur when a lower interrupt is being serviced) Special Fully Nested Mode should be programmed in the master. After a non- specific EOI has been sent to the slave, the ISR should be checked to see if any other interrupts are active. If there are no interrupts active a non-specific EOI should be sent to the master.

4.3.2 Set-Up

The interrupt controllers are setup by a writing a series of initilization command words (ICW). The sequence is started by writing ICW1 with data bit 4 = 1. ICW 2 is then written followed by ICW3 and ICW4 if they are needed.

ICW1 Write	
0	ICW4 Needed
1	Not Cascade Mode
2	Unused
3	Level Triggered
4	1
5-7	Unused
ICW2 Write	
0-2	Unused
3-7	Interrupt Vector
ICW3 Write (Interrupt Controller #1 only)	
0-1	0
2	Interrupt 2 has slave
3-7	0
ICW3 Write (Interrupt Controller # 2 only)	
0-2	Slave I/D
3-7	0
ICW4	
0	1
1	Auto EOI
2-3	0
4	Special Fully Nested Mode
5-7	0

4.3.3 Operation

Once the interrupt controllers are set-up, they may be programmed by Operation Control Words (OCW).

OCW1	
0	Interrupt 0 Mask
1	Interrupt 1 Mask
2	Interrupt 2 Mask
3	Interrupt 3 Mask
4	Interrupt 4 Mask
5	Interrupt 5 Mask
6	Interrupt 6 Mask
7	Interrupt 7 Mask
OCW2	
0-2	Interrupt Level
3-4	0
5-7	001 Non-specific EOI
	011 Specific EOI
	111 Rotate on Specific EOI
	101 Rotate on Non-Specific EOI
	100 Select Rotate on Automatic EOI
	000 Clear Rotate On Automatic EOI
	110 Set Priority
	010 Unused

OCW3

Bits 0, 1, and 2 of OCW3 determine what the next read of the interrupt controller will yield.

0-1	00 Unused
	01 Unused
	10 Select Read IRR
	11 Select Read ISR
2	Poll Command
3	1
4	0
5-6	00 Unused
	01 Unused
	10 Reset Special Mask Mode
	11 Set Special Mask Mode
7	0

Interrupt Controller	Address	Function	Read/Write
1	020	ICW1	Write
1	021	ICW2	Write
1	021	ICW3	Write
1	021	ICW4	Write
1	021	OCW1	Write
1	020	OCW2	Write
1	020	OCW3	Write
1	020	IRR	Read
1	020	ISR	Read
1	021	Mask	Read
1	020, 021	Interrupt Level	Read
2	0A0	ICW1	Write
2	0A1	ICW2	Write
2	0A1	ICW3	Write
2	0A1	ICW4	Write
2	0A1	OCW1	Write
2	0A0	OCW2	Write
2	0A0	OCW3	Write
2	0A0	IRR	Read
2	0A0	ISR	Read
2	0A1	Mask	Read
2	0A0, 0A1	Interrupt Level	Read

4.4 FE3010B 8254 TIMER

The FE3010B contains a 8254 equivalent timer that contains three independent counters. All the timers run off a 1.19 Mhz clock. The GATE0 and GATE1 signals are tied high. The GATE2 signal is tied to Register 61, bit 0. The counters decrement when counting. The largest possible count is 0.

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

Each counter may be programmed for different counting modes and the count may be read back. To initilize a counter the Control Word must be written followed by one or two bytes of count if needed. Each counter may be programmed to count in BCD or binary.

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

CONTROL WORD (format 1)		
0	BCD	
1-3	Mode >	000 Mode 0
		001 Mode 1
		X10 Mode 2
		X11 Mode 3
		100 Mode 4
		101 Mode 5
4-5	Function >	00 Counter Latch Command
		01 Read/Write Low Byte
		10 Read/Write High Byte
		11 Read/Write Low Byte then High Byte
6-7	Counter	00 Counter 0
		01 Counter 1
		10 Counter 2
CONTROL WORD (format 2)		
0	0	
1	Select Counter 0	
2	Select Counter 1	
3	Select Counter 2	
4	-Latch Status	
5	-Latch Count	
6-7	1	

4.4.1 Set-Up

Each counter may be set in one of 5 modes by writing a command word (format 1). The command word must specify the counter and the number of count bytes to be written. A new count may be written at any time.

1. Mode 0 Interrupt on Terminal Count

The counter starts when the count is loaded. When count = 0 the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting.

OUT will go low when the counter starts. It will go high when the count = 0, and stay high until a new count or mode is written.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

2. Mode 1 Hardware Retriggerable One Shot

The counter starts when GATE goes from low to high. When count = 0 the counter will continue counting from FFFF in binary mode or 9999 in BCD mode.

Any time GATE goes from low to high the counter will be reloaded with the original count and the counter started.

OUT will go low when GATE goes from low to high. It will go high when count = 0.
If a new count is written while the counter is counting, it will be loaded the next time GATE goes from low to high.

3. Mode 2 Rate Generator

The counter starts when the count is loaded. When count = 0 the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high the counter is reloaded.

OUT will initially be high. When count = 1 OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded the next time count = 0 or when GATE goes from low to high.

4. Mode 3 Square Wave Generator

The counter starts when the count is loaded. When count = 0 the counter is reloaded and the counter started again. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high the counter is reloaded.

When the counter starts OUT will be high. When the count is half done, OUT will go low. If GATE goes low then OUT will go high.

If a new count is written while the counter is counting, it will be loaded the next time count = 0 or when GATE goes from low to high.

5. Mode 4 Software Triggered Strobe

The counter starts when the count is loaded. When count = 0 the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. OUT will initially be high. When count = 0 OUT will go low for one clock.

If a new count is written while the counter is counting, it will be loaded on the next clock pulse.

6. Mode 5 Hardware Triggered Strobe

The counter starts when the count is loaded. When count = 0 the counter will continue counting from FFFF in binary mode or 9999 in BCD mode. GATE = 1 enables counting. GATE = 0 disables counting. If GATE goes from low to high the counter is reloaded. OUT will be high when the counter starts. When count = 0, OUT will go low for one clock. If a new count is written while

the counter is counting, it will be loaded the next time count = 0 or when GATE goes from low to high.

4.4.2 Reading the Counter

There are three ways of reading the counters.

1. The count is read directly. This mode can cause false readings due to fact that the counter may be changing while it is read.

2. The count may be read via a Counter Latch Command. (See COMMAND WORD format 1). This command latches the count so it may be read without changing.

3. The count may be read via a Read Back Command. (See COMMAND WORD format 2). This command is the equivalent of multiple Counter Latch Commands.

4.4.3 Reading Status

The status of a counter may be read by issuing a Read Back Command with data bit 4 = 0. (See COMMAND WORD format 2). Bits 0-5 are the same as the command word for the counter. Bit 6 tells if the last count that was written has been loaded into the counter. Bit 7 is the reflects the state of the OUT pin.

Status Word	
0	BCD
1-3	Mode
4-5	Function
6	-New Count Written
7	Out Status

4.4.4 Switching Data

In the FE3010B implementation of the timer, if the timer clock is significantly slower than the CPU execution, there is a slight chance that switching data can get latched on a counter latch command. For an AT system with a 1.19Mhz timer clock and 16Mhz or slower bus speed, there is no chance of latching invalid data.

4.4.5 Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers, and refresh cycles. One port ofthe RAM is a read only port for DMA or refresh cycles, and the other is a read/write port for the 80286 CPU.

4.4.6 Refresh Address

This block contains a 9-bit counter that is used for the address during a refresh.

4.5 FE3010B Decode

Address	Decodes	Hex
9 8 7 6 5 4 3 2 1 0		
0 0 0 0 0 X X X X X	DMA Controller 1 (Ch 0-3)	000-01F
0 0 0 0 1 X X X X X	Interrupt Controller Master	020-03F
0 0 0 1 0 X X X X X	Timer	040-05F
0 0 0 1 1 0 X X X 1	PortB (PI0)	060-06F(odd)
0 0 0 1 1 1 X X X 1	Real Time Clock (NRTCCS)	070-07F(odd)
0 0 1 0 0 X X X X X	Page Register	080-09F
0 0 1 0 1 X X X X X	Interrupt Controller Slave	0A0-0BF
0 0 1 1 0 X X X X X	DMA Controller 2 (Ch 4-7)	0C0-0DF

4.5.1 Page Register Decodes

Address	Decode
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6
008A	DMA Channel 7
008F	Refresh

Note: Page register data appears on address bits A23-A16 during refresh and 8 bit DMA cycles. For 16 bit DMA cycles (channels 5- 7), the LSB of the page register does not appear, instead the 16 bit DMA address is shifted up one bit and A0 is floated in the FE3010B to be driven by external logic.

4.5.2 PIO

This block contains the control port to control the speaker and timer channel. It also contains circuitry to detect if refresh is running. This condition may be read back as bit 4. Bits 2 and 3 are read/write, but they do not perform any function. They are used for software compatibility with the IBM PC AT.

Port B (PIO) is an eight bit control and status register on the AT. Bits 0 through 5 are defined in the FE3010B, while bits 6 and 7 are generated in the FE3030. During a read of Port B (address 0061), the FE3010B drives data bits 0-5 and tri-states bits 6 and 7. The FE3030, if used, will drive bits 6 and 7 indicating the parity error and channel check status. Bits 0 through 5 are described below.

Bit	Function
5	OUT2 from timer channel 2 (read only)
4	Toggles on each refresh (read only)
3	Enable parity check (active low)
2	Enable channel check (active low)
1	Enable speaker (active high)
0	Gate for timer channel 2

Bits 3 and 2 perform no function on the FE3010B, they are duplicated here to provide the read/write capability, but the actual enable functions are performed in the FE3030.

4.6 Absolute Maximum Ratings *

T_A=+25 °C	
Power supply voltage, V_{DD} @ V_{SS}=0	3.0 V to 7.0 V
Power dissipation, PDMAX @V_{DD}=5.25V	200mW
Current, I_{DD} @V_{DD}=5.25V	38mA
Input voltage,VI	0.0V to V_{DD} 0.3V
Output voltage,VO	0.0V to V_{DD} 0.3V
Operating temperature, TOPT	0° C to 70° C
Storage temperature, TSTG	-40° C to 125° C

* Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.7 Capacitance

(TA=+25° C, V_{DD} = 0V)

Parameter	Symbol	Max Limits	Test Condition
Input capacitance	C_I	10 pF	fc=1MHz unmeasured pins returned to 0V
I/O capacitance	C_{IO}	15 pF	

4.8 DC Characteristics

TA = 0° C to 70° C, V_{DD} = 5V +/- 5%

[ALE, DMACLK, DMARDY, DRQ0, DRQ1, DRQ2, DRQ3, DRQ5, DRQ6, DRQ7, HLDA, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, KBINT, NCLEAR, NINTA, NIRQ13, NMASTER, NRFSH, TLCK, NIRQ8]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	Vss	0.8	V	V_{DD} = 5V +/- 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V +/- 5%
Input low current	I_{IL}	-10.0	-300.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		40.0	uA	V_{IN} = V_{DD}

[A(0), A(1), A(2), A(3), A(4), A(5), A(6), A(7), A(8), A(9), DATA(0), DATA(1), DATA(2), DATA(3), DATA(4), DATA(5), DATA(6), DATA(7), NIOR, NIOW]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	Vss	0.8	V	V_{DD} = 5V +/- 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V +/- 5%
Input low current	I_{IL}		-10.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		10.0	uA	V_{IN} = V_{DD}
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0mA
Output current	IOZ	-10.0	10.00	uA	0V < V_{OUT} < V_{DD}

[AEN, DACK0, DACK1, DACK2, HRQ, INTR, NDACKEN, NRTCCS, OUT1, SPKR, SYSALE]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -2.0 mA

[A(10), A(11), A(12), A(13), A(14), A(15), A(16), A(17), A(18), A(19), A(20), A(21), A(22), A(23), NMEMR, NMEMW]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0 mA
Output current	IOZ	-10.0	10.00	uA	$0V<V_{OUT}<V_{DD}$

4.9 AC Characteristics

TA = O°C to +70°C, V_{DD} = +5V =/-5% load capacitance = 85 pF, operating at 8 MHz.

Symbol	Parameter	Min	Max	Unit
t1	DRQ high setup time to DMACLK high	3	-7	ns
t2	HRQ active high delay from DMACLK rising edge	10	49	ns
t3	DMACLK high setup time delay from HLDA rising edge	-2	4	ns
t4	AEN active high delay from DMACLK falling edge	14	69	ns
t5	AEN inactive low delay from DMACLK rising edge	15	74	ns
t6	SYSALE active high delay from DMACLK rising edge	10	54	ns
t7	SYSALE inactive low delay from DMACLK rising edge	14	69	ns
t8	NIOR and NMEMR active low delay from DMACLK rising edge	12	60	ns
t9	NIOW and NMEMW active low delay from DMACLK rising edge	12	60	ns
t10	NIOR and NMEMR inactive high delay from DMACLK rising edge	11	52	ns
t11	NIOW and NMEMW inactive high delay from DMACLK rising edge	11	52	ns
t12	NDACKEN active low delay from DMACLK falling edge	13	63	ns
t13	NDACKEN inactive high delay from DMACLK falling edge	10	49	ns
t14	TC active high delay from DMACLK falling edge	11	58	ns
t15	TC inactive low delay from DMACLK falling edge	13	68	ns
t16	DMARDY high setup time delay to DMACLK rising edge	-13	2	ns
t17	ADDR active delay from AEN rising edge	2	18	ns
t18	ADDR valid delay from AEN rising edge	70	109	ns
t19	ADDR float delay from AEN falling edge	1	9	ns
t20	DATA valid delay from NIOR falling edge	14	68	ns
t21	DATA float delay from NIOR rising edge	11	51	ns
t22	ADDR valid setup time to SYSALE inactive low	71	111	ns
t23	SYSALE inactive low to ADDR valid hold time	121	124	ns
t24	ADDR valid delay from NRFSH falling edge	15	78	ns
t25	ADDR float delay from NRFSH rising edge	10	60	ns
t26	SYSALE active high from delay NFRSH falling edge	6	29	ns
t27	SYSALE inactive low delay from NRFSH rising edge	8	40	ns

Symbol	Parameter	Min	Max	Unit
t28	SYSALE active high delay from ALE rising edge	5	31	ns
t29	SYSALE inactive low delay from ALE falling edge	9	46	ns
t30	INTR (master) active high delay from IRQ rising edge	11	105	ns
t31	INTR (slave) active high from ALE rising edge	27	136	ns
t32	DATA valid delay from NINTA falling edge	17	84	ns
t33	DATA float delay from NINTA rising edge	9	45	ns
t34	NRTCCS active low delay from ALE rising edge	13	66	ns
t35	NRTCSS inactive high delay from ALE rising edge	9	46	ns
t36	OUT1 active high delay from TCLK falling edge	7	53	ns
t37	OUT1 inactive low delay from TCLK falling edge	10	63	ns
t38	DATA invalid time delay from DATA to NIOW inactive high	9	28	ns
t39	DATA set-up time to NIOW active low	0		ns

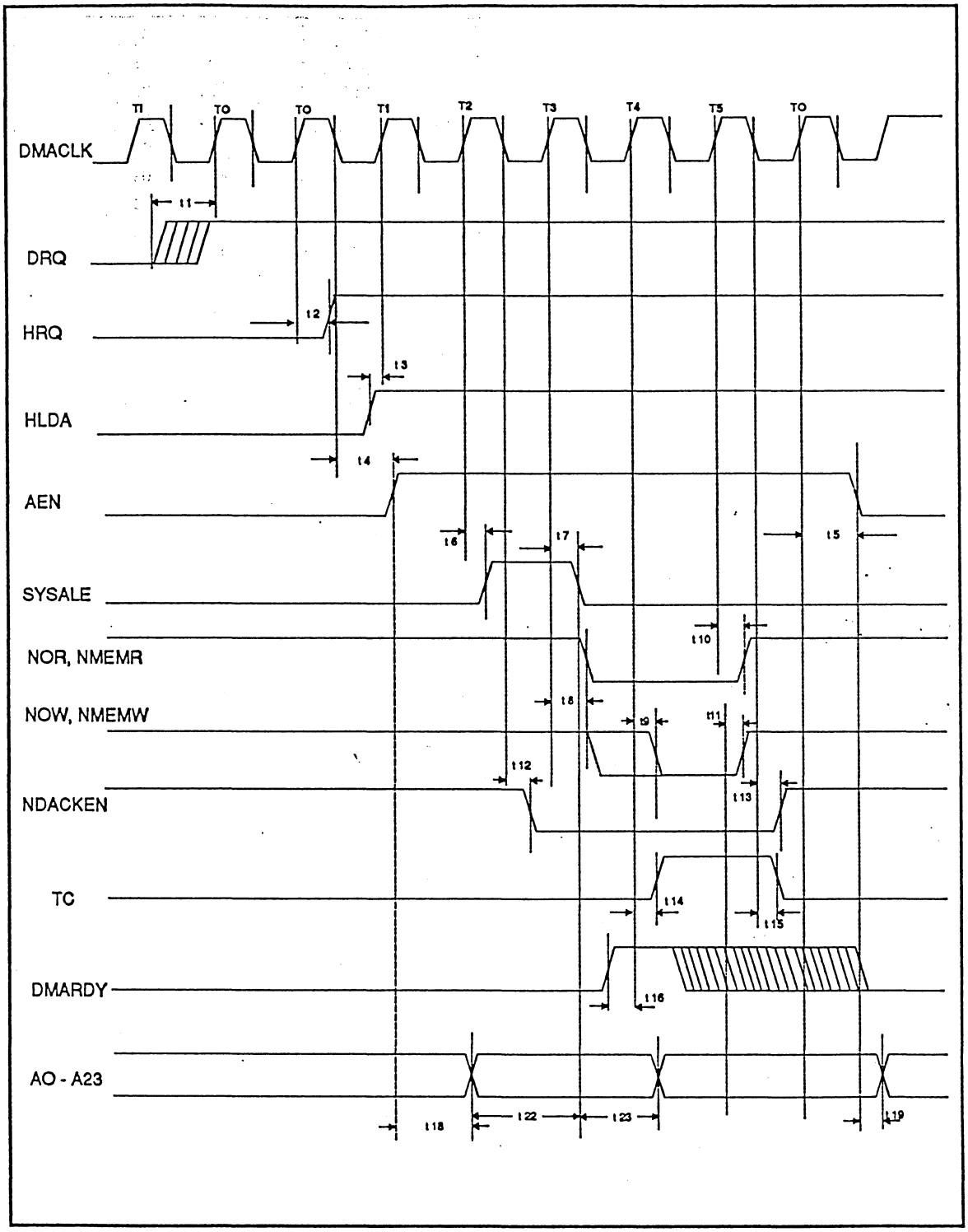

Figure 4.3 DMA CYCLE

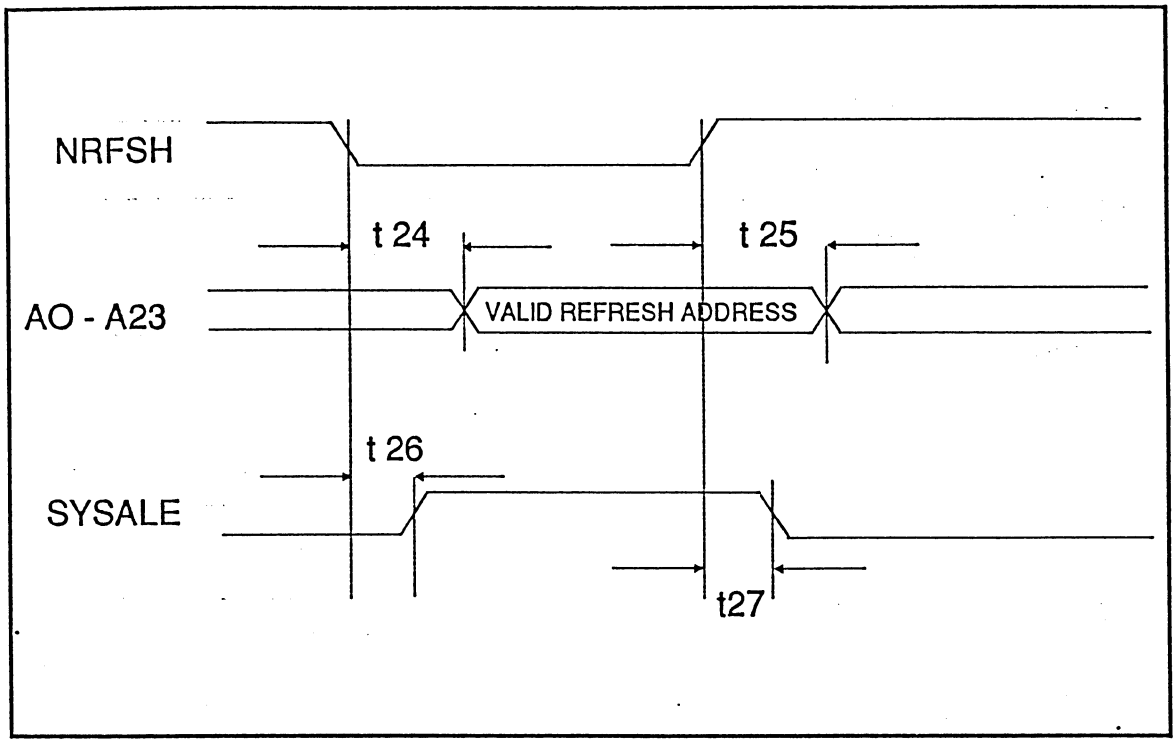

Figure 4.4 REFRESH CYCLE

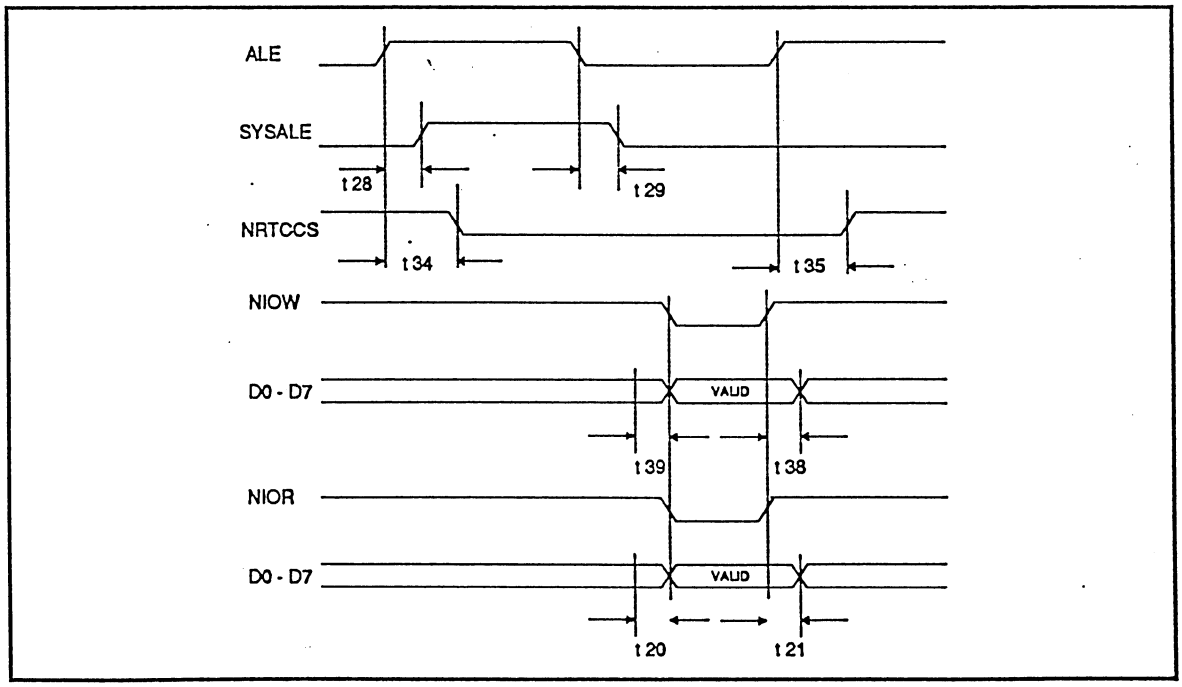

Figure 4.5 CPU CYCLE

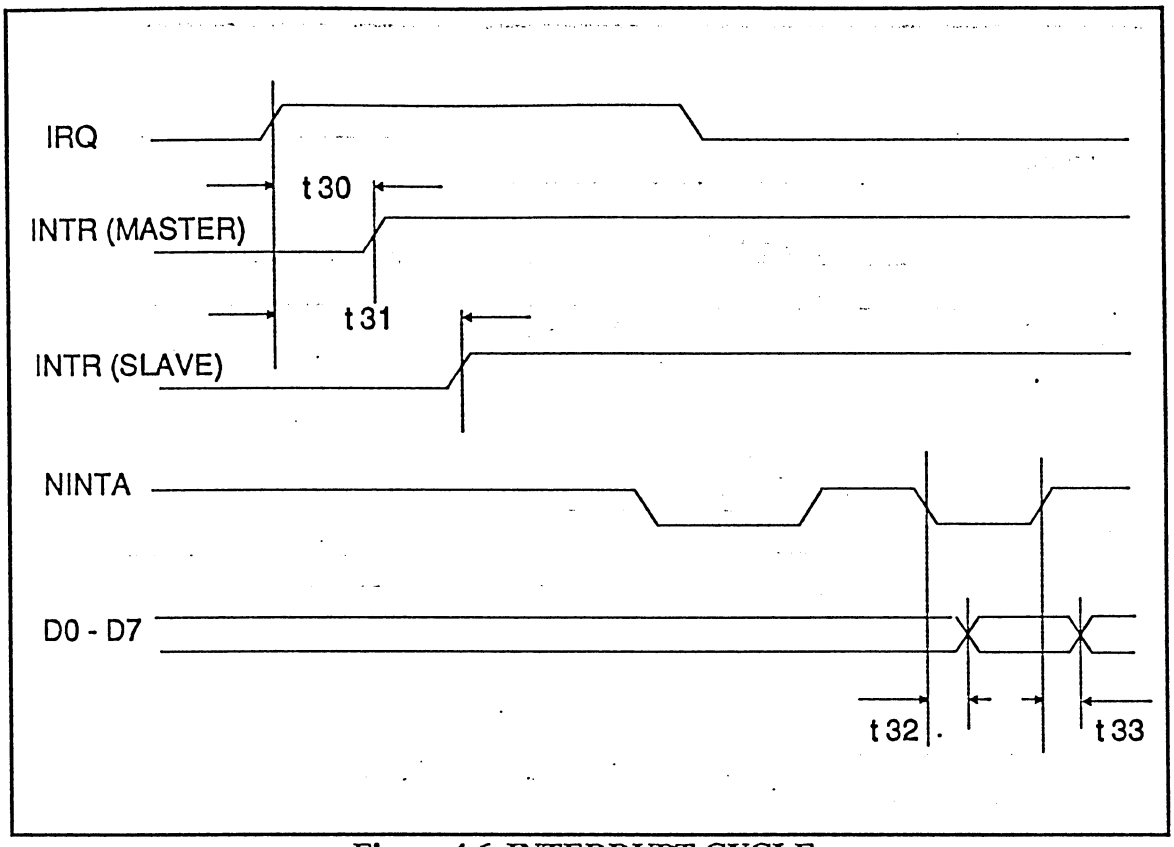

Figure 4.6 INTERRUPT CYCLE

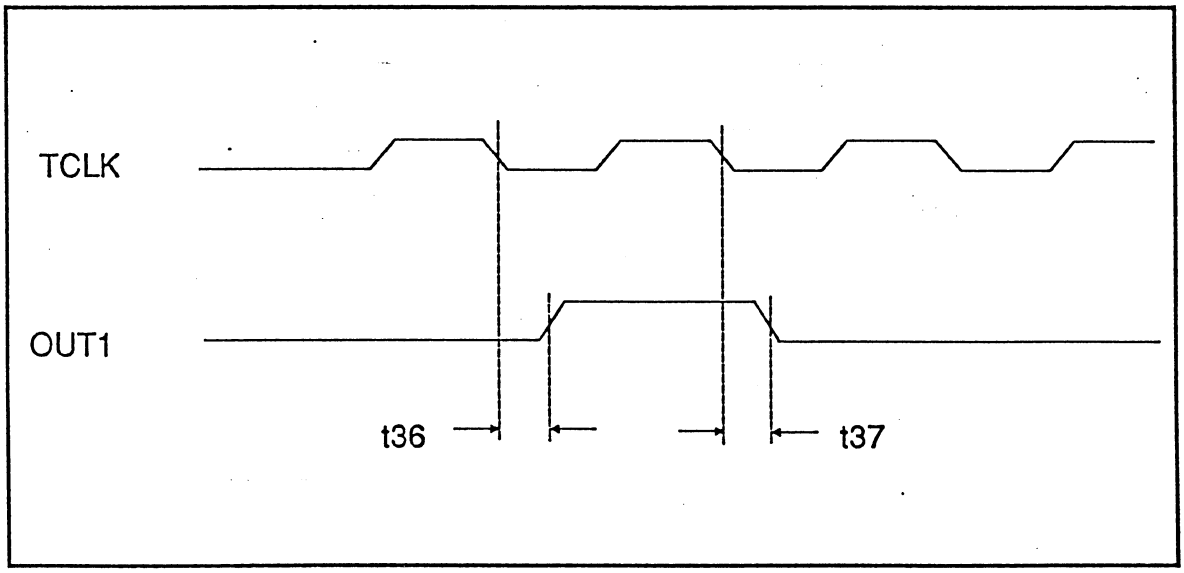

Figure 4.7 TIMER CYCLE

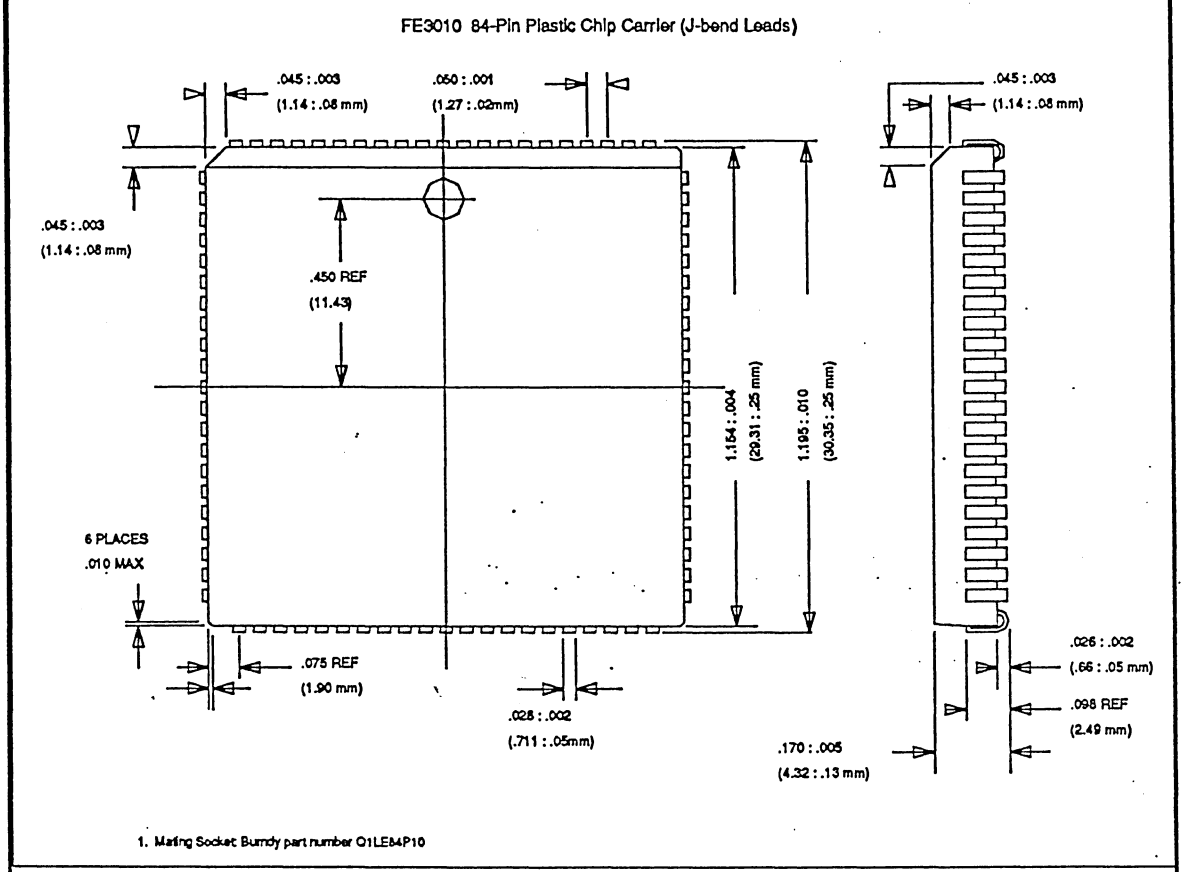

Figure 4.8 FE3010B 84-PIN DIMENSIONS

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FE3021 ADDRESS BUFFER AND MEMORY CONTROLLER

5.0 Introduction

The FE3021 device is designed to reduce chip count, increase flexibility, and provide improved operating speed and functionality when used with the FE3001, FE3010, and FE3031 devices to implement a low cost, high performance AT compatible computer.

Chip count is reduced by integrating the memory controller, AT bus address buffers, and I/O Manager functions into one chip.

The memory controller is a high performance design, with programmable modes of operation. It controls page mode DRAM or static column DRAM.

Up to 4 banks of DRAM may be controlled. The DRAM bank locations are programmable on 128K byte boundaries. One memory bank allows split addressing, so that one portion may be placed in conventional memory with the remainder in extended memory, with an additional mode to allow copying BIOS code from ROM to RAM for faster execution.

The major features of the FE3021 device include the following:

- Page mode DRAM access with interleaved memory banks
- Controls up to 4 banks (up to 8 MBytes) of memory
- On- chip RAS and CAS drivers for DRAM chips
- On- chip DRAM address multiplexer
- LIM standard EMS expanded memory hardware (supports EMS 4.0 multi-tasking)
- On- chip address and control signal buffers for directly driving AT bus
- Zero wait state access at 16 MHz using 100 ns DRAM with page mode access
- Generates chip selects for floppy controller, 8042, 80287, and NMI
- Generates programmable chip selects for four additional devices
- Maps main and EGA BIOS into one physical PROM
- "Hot" reset generation for quick 80286 switch from protected to real mode
- Fast Alternate Gate A20 generation
- 132 pin JEDEC plastic flat package

A major function of the FE3021 is to generate chip select decodes for peripheral chips on the system board, for instance, the floppy controller, hard disk controller, serial, and parallel port chips. The floppy and hard disk chip selects may be disabled or may be enabled for either the primary or secondary address decode, as defined by IBM. Four programmable chip selects are available, for supporting serial, parallel, mouse, or other types of ports. Refer to Figure 5.1 for Pin assignment information and locations.

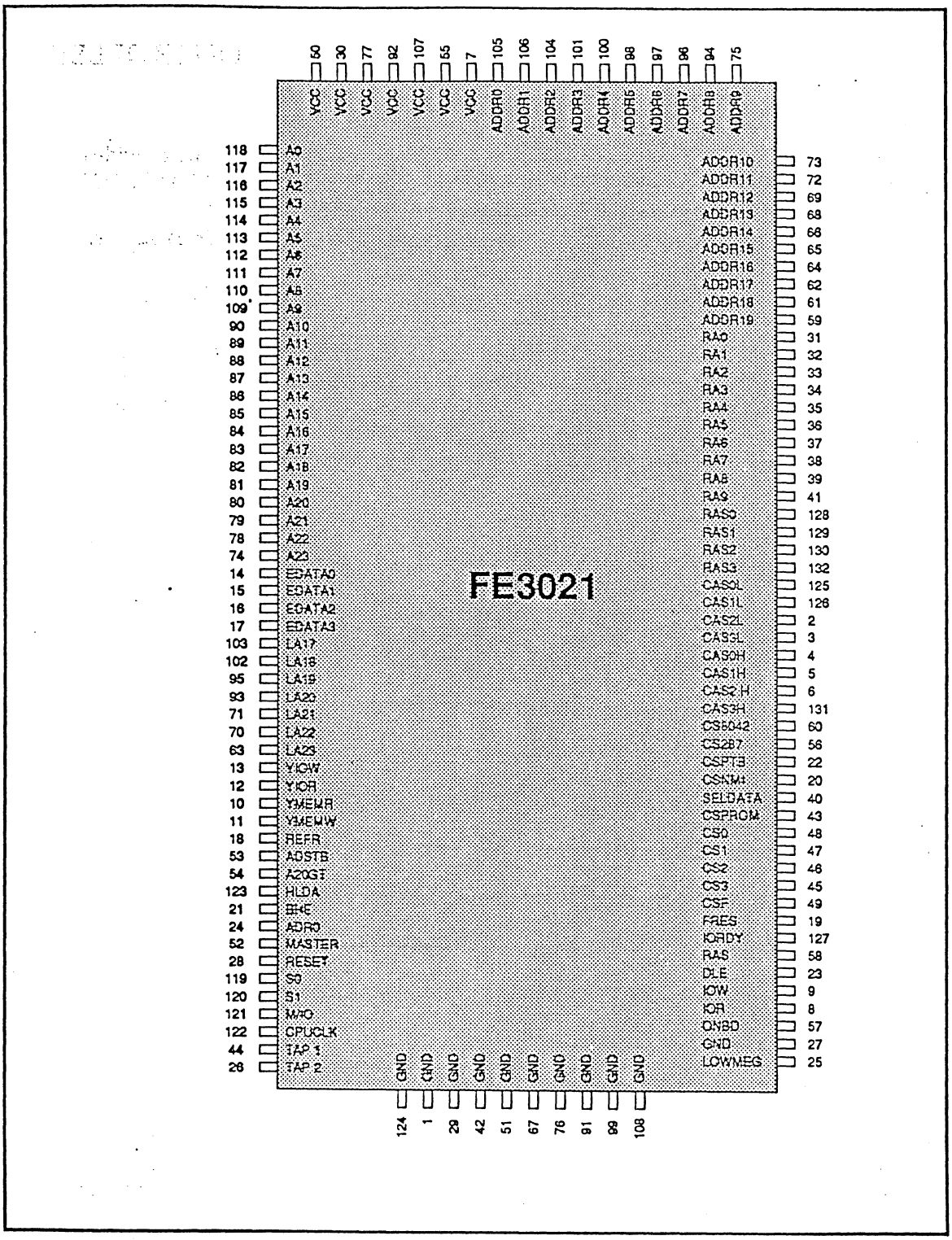


Figure 5.1 FE3021 PIN ASSIGNMENT INFORMATION

To reduce chip count and improve performance, particularly when an EGA graphics controller is placed on the system board, separate blocks of ROM may be mapped into a single physical ROM. For instance, the EGA BIOS and standard BIOS may be placed into the same pair of ROM chips or into a single 8 bit wide ROM. Besides reducing chip count, EGA operating speed will be improved, since EGA BIOS will be accessed 16 bits at a time. To improve BIOS performance, ROM code may be copied into excess RAM, and the BIOS ROM mapped out and replaced by RAM 16K bytes at a time. (Excess RAM is the 384K left over after the lower 640K out of a 1 MB RAM is used.)

5.1 80286 Interface

This interface port connects with the 80286 address lines and the 80286 bus status lines. By connecting directly to the 80286 and by duplicating a portion of the 82288 bus controller logic, early determination of memory or I/O accesses may be made, as well as whether the access will be 8 bits or 16 bits.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
74	A23	I/O	80286 ADDRESS LINE
78	A22	I/O	" "
79	A21	I/O	" "
80	A20	I/O	" "
81	A19	I/O	" "
82	A18	I/O	" "
83	A17	I/O	" "
84	A16	I/O	" "
85	A15	I/O	" "
86	A14	I/O	" "
87	A13	I/O	" "
88	A12	I/O	" "
89	A11	I/O	" "
90	A10	I/O	" "
109	A9	I/O	" "
110	A8	I/O	" "
111	A7	I/O	" "
112	A6	I/O	" "
113	A5	I/O	" "
114	A4	I/O	" "
115	A3	I/O	" "
116	A2	I/O	" "
117	A1	I/O	" "
118	A0	I/O	" "
119	S0-	I	80286 STATUS LINE
120	S1-	I	80286 STATUS LINE
121	M/IO-	I	80286 STATUS LINE
122	CPUCLK	I	80286 CLOCK
123	HLDA	I	80286 HOLD ACKNOWLEDGE LINE

Table 5.1 80286 INTERFACE PIN FUNCTIONS

5.2 Data Bus Interface and Bus Control

The data bus port is 4 bits wide, which should connect to the EDATA local data bus, and is used to access the I/O Manager control logic. The upper 4 bits should be ignored when reading the control registers.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
17	EDATA3	I/O	CONTROL REGISTER DATA LINE
16	EDATA2	I/O	" "
15	EDATA1	I/O	" "
14	EDATA0	I/O	CONTROL REGISTER DATA LINE

5.3 I/O Chip Selects

This logic section generates chip selects for standard system board functions such as the 8042 keyboard controller, 80287 math coprocessor, floppy controller, and hard disk controller. It also generates chip selects for up to 4 additional I/O ports which may have programmable addresses and wait state characteristics.

PIN NUMBER	PIN NAME	I/O	FUNCTION
48	CS0-	O	PROGRAMMABLE CHIP SELECT 0
47	CS1-	O	PROGRAMMABLE CHIP SELECT 1
46	CS2-	O	PROGRAMMABLE CHIP SELECT 2 OR R. T. CLOCK CHIP SELECT
45	CS3-	O	PROGRAMMABLE CHIP SELECT 3 OR H. D. CONT. CHIPSELECT
49	CSF	O	FLOPPY DISK CONTROLLER CHIP SELECT OR OPERATION OR CONFIG. REGISTER SELECT
60	CS8042-	O	8042 KEYBOARD CONT. SELECT
56	CS287-	O	80287 COPROCESSOR SELECT
20	CSNMI-	O	NMI LOGIC
22	CSPTB-	O	ENABLE MEMORY PARITY AND I/O CHECK.

5.4 I/O Control

This logic section contains control logic for the I/O bus.

The IORDY signal will go low when generating wait states. For 12 Mhz systems, this signal may be tied directly to the bus signal IOCHRDY. For 16 MHz or 20 Mhz systems, this signal should instead be "AND"ed with the IOCHRDY bus signal through a 74F08, and the combined signal sent to the FE3001. The IORDY pin will normally be at a high impedance state. When generating wait states, it will go low. When going from a low to a high state, the IORDY pin will be actively driven high for one processor clock time, then the output will tri-state. An external pullup resistor should be used to keep the IORDY signal high when the IORDY pin is at a high impedance state. The state of IORDY- is sampled at the rising edge of RESET-; if IORDY- is low at this time, the FE3021 will fetch data and instructions from the BIOS ROM 8 bits at a time, otherwise a 16 bit wide ROM is assumed.

The IOR-, IOW-, MEMW-, and MEMR- lines which directly drive the bus are active only when devices on the expansion bus are actually being accessed. This is done so that the slow devices on the expansion bus, designed for 8 MHz system operation, will not be spuriously selected when the current bus cycle is a 16 MHz or 20 MHz access. When on-board 16-bit devices are being accessed, the address setup and hold times as well as the data setup and hold times will be reduced, since accesses can be made at the full processor rate of 16 or 20 MHz.

PIN NUMBER	PIN NAME	I/O	FUNCTION
127	IORDY	O	READY LINE, OPEN DRAIN. DIRECTLY CONNECTED TO IOCHRDY BUS LINE.
40	SELDAT-	O	DIRECTION OF DATA TRANCEIVER - DATA TO EDATA BUS
8	IOR-	I/O	SYSTEM I/O READ COMMAND SIGNAL, DRIVES EXPANSION BUS. AN INPUT IN MASTER MODE.
9	IOW-	I/O	SYSTEM I/O WRITE COMMAND SIGNAL, DRIVES EXPANSION BUS. AN INPUT IN MASTER MODE.
10	YMEMR-	I	UNGATED SYSTEM MEMORY READ COMMAND SIGNAL FROM FE3001
11	YMEMW-	I	UNGATED SYSTEM MEMORY WRITE COMMAND SIGNAL FROM FE3001
53	ADSTB	I	ADDRESS STROBE FROM FE3001
12	YIOR-	I/0	UNGATED I/O READ STROBE FROM FE3001, AN OUTPUT IN MASTER MODE.
13	YIOW-	I/O	UNGATED I/O WRITE STROBE FROM FE3001, AND OUTPUT IN MASTER MODE.

Table 5.2 I/O CONTROL PIN FUNCTIONS

The following table lists the data work size, I/O addresses, and chip selects generated for each variable port type.

The PORT 0, PORT 1, PORT 2, and PORT 3 addresses are fully programmable, with the choice of either using nine I/O addresses for decode, or masking the A8 address bit (for instance, for decoding dual serial ports). The LSB (A0) address is always ignored. The lower 2, 3, or 4 bits of the address may also be ignored so that 2, 4, 8, or 16 bytes may be allocated for the port.

All FE3021 control registers, except those used for EMS page mapping, are accessed by first writing eight times to address FFF00 (in an area allocated for ROM BIOS). Any memory access outside of the ROM BIOS address space, either data access or instruction fetch, will abort the unlocking process. Once unlocked, memory accesses outside of the ROM BIOS area may be made without affecting the unlocked state. When unlocked, the address space from FFF01 to FFFFE becomes register controls for the FE3021 device. The controls are locked again by reading location

FFFFF. This access method guarantees that all control register changes will be made through the BIOS.

A Version Number register provides information on the version of the FE3021 chip. It also contains a bit which toggles between '0' and '1' which provides indication that the register set has been unlocked.

VERSION NUMBER

	7	6	5	4	3	2	1	0
FFF01	X	X	X	X	VER			T

T : toggles between 0 and 1 with every read access of the Version Number register.

V : 000 when T=0 for initial version
111 when T=1 for initial version

System board devices may be located on the EDATA bus rather than on the I/O expansion slot DATA bus. The SELDAT- signal which controls the DATA to EDATA bus direction is affected by the two port location registers. This option is available for peripheral devices which cannot directly drive the high current I/O slot DATA bus. Note, however, that DMA transfers cannot be made to devices on the EDATA bus.

The SELDAT- signal is active (low) when IOR- is active and address bits A8 and A9 are low, or the PORTS LOCATION register indicates that an addressed port is on the EDATA bus. The SELDAT- signal is also low when MEMR- is active and the 8-bit BIOS is being accessed.

PORTS LOCATION REGISTER

	7	6	5	4	3	2	1	0
FFF06	X	X	X	X	A	B	C	D

A = 0	PORT 0 ON DATA BUS
A = 1	PORT 0 ON EDATA BUS
B = 0	PORT 1 ON DATA BUS
B = 1	PORT 1 ON EDATA BUS
C = 0	PORT 2 ON DATA BUS
C = 1	PORT 2 ON EDATA BUS
D = 0	PORT 3 ON DATA BUS
D = 1	PORT 3 ON EDATA BUS

THE PORT LOCATION REGISTER IS CLEARED BY A MASTER RESET.

PORT 3 CONTROL REGISTER

	7	6	5	4	3	2	1	0
FFF08	X	X	X	X	WS		O	OB

WS	HIGH SPEED WAIT STATES
00	1
01	2
10	3
11	4

0B	CS3 - WAIT STATES
0	DEFAULT (SLOW)
1	HIGH SPEED HARD DISK CONTROLLER

THE PORT 3 CONTROL REGISTER IS CLEARED BY A MASTER RESET.

ENABLE PORTS REGISTER

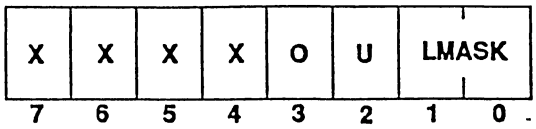
	7	6	5	4	3	2	1	0
FFF10	X	X	X	X	EN3	EN2	EN1	EN0

THE ENABLE PORTS REGISTER IS CLEARED BY A MASTER RESET

The PORT 0, PORT 1, PORT 2, and PORT 3 chip selects are enabled with the Enable Ports register. If the Enable bit is 0, then the port chip select bit will always be at an inactive (high) state. All four ports are disabled after master reset.

For ports 0, 1, and 2, the access will have the default wait states: 1 wait state for 16 bit accesses and 4 wait states for 8 bit accesses, with the wait states timed from the System Clock. The selected chip must generate IOCS16- if it is a 16 bit peripheral.

For port 3, the access will normally have the default wait states but may also be programmed to have high speed wait state timing for an on-board 16 bit hard disk controller capable of high speed access. If the OB field is '1', the WS field will set the number of high speed wait states, timed from the CPU Clock, when the disk controller data port is accessed. The other disk controller ports will always be accessed at low speed.



LMASK	ADDRESS BITS COMPARED
00	A9 A8 A7 A6 A5 A4 A3 A2 A1 X
01	A9 A8 A7 A6 A5 A4 A3 A2 X X
10	A9 A8 A7 A6 A5 A4 A3 X X X
11	A9 A8 A7 A6 A5 A4 X X X X

U = 0 : INCLUDE A8 IN ADDRESS COMPARISON

LMASK	ADDRESS BITS COMPARED
00	A9 X A7 A6 A5 A4 A3 A2 A1 X
01	A9 X A7 A6 A5 A4 A3 A2 X X
10	A9 X A7 A6 A5 A4 A3 X X X
11	A9 X A7 A6 A5 A4 X X X X

U = 1 : IGNORE A8 IN ADDRESS COMPARISON

THE PORT ADDRESS MASK REGISTER IS CLEARED BY A MASTER RESET.

PORT	PORT CONTROL REGISTER ADDRESS
0	FFF09
1	FFF11
2	FFF19
3	FFF21

PORT ADDR - LOWER MSB

X	X	X	X	X	X	A9	A8
7	6	5	4	3	2	1	0

PORT ADDR - UPPER LSB

X	X	X	X	A7	A6	A5	A4
7	6	5	4	3	2	1	0

PORT ADDR - LOWER LSB

X	X	X	X	A3	A2	A1	0
7	6	5	4	3	2	1	0

PORT	PORT I/O ADDRESS REGISTERS		
	A9-A8	A7-A4	A3-A0
0	FFF0A	FFF0B	FFF0C
1	FFF12	FFF13	FFF14
2	FFF1A	FFF1B	FFF1C
3	FFF22	FFF23	FFF24

The PORT I/O ADDRESS registers for all four ports are set to all zeros by a master reset.

The following table lists the I/O addresses and chip selects generated for each fixed port type. The number of wait states for the fixed ports is set by the External I/O Wait State Control register. The chip selects are not gated with IOR- or IOW-. The CSNMI- signal is decoded for both even and odd addresses, so that access may be made to the FE3001 control register at address 073. When writing to I/O port 070, the IOW- output to the expansion bus will not be asserted.

The floppy controller operations register select, configuration register select, and floppy disk controller chip select may be generated from the CSF and CS3-pins, (when CS3- has been defined to be the hard disk chip select. The operations register is being accessed when CSF is active (high), CSHD- is inactive (high), and A1 is high. The configuration register is being accessed when both CSF and CSHD- are active. The floppy chip select is active when CSF is high, CS3- is high, and A2 is high.

PORT	BIT SIZE	I/O ADDRESS	ACTIVE PIN	FUNCTION
FLOPPY	8	3F2 372	CSF	FDC OPERATION SELECT. 3F2 IS PRIMARY ADDRESS, 372 IS SECONDARY
	8	3F4-3F5 374-375	CSF	3F4-3F5 ARE PRIMARY ADDRESSES, 374-375 ARE SECONDARY.
	8	3F6 376	CS3-*	HARD DISK CONTROLLER CHIP SELECT. 3F6 IS PRIMARY ADDRESS, 376 IS SECONDARY.
	8	3F7 377	CSF CS3-*	CS3- AND CSF PINS WILL BE ASSERTED. 3F7 IS PRIMARY ADDRESS, 377 IS SECONDARY.
80287	8	0E0-0FF	CS287-	80287 CHIP SELECT.
8042	8	060-06E (EVEN)	CS8042-	8042 CHIP SELECT.
NMI LOGIC	8	070-07F	CSNMI-	REAL TIME CLOCK AND NMI LOGIC SELECT
PARITY CHECK	8	061-06F (ODD)	CSPTB-	PARITY CHECK SELECT AND PORT 1 CLOCK. EXTERNAL LOGIC MUST SEPARATE THE SIGNALS.
HARD DISK	16	1F0 170	CS3-*	HDC CHIP SELECT - DATA PORT ACCESS. 1F0 IS PRIMARY ADDRESS, 170 IS SECONDARY
	8	1F1-1F7 171-177	CS3-	HDC CHIP SELECT - TASK FILE. 1F1-1F7 ARE PRIMARY ADDRESSES, 171-177 ARE SECONDARY.

Table 5.3 I/O ADDRESSES/CHIP SELECTS FOR FIXED PORTS

*WHEN CS3- PIN IS PROGRAMMED AS HDC CHIP SELECT.

PRIMARY / SECONDARY PORT FUNCTION SELECT

	X	X	X	X	DH	DF	H	F
FFF49	7	6	5	4	3	2	1	0

DH=0: CS3- pin will respond to address programmed by FFF22-FFF24
DH=1: CS3- pin will respond to hard disk addresses
DF=0: Enable CSF output
DF=1: Disable CSF output (output always high)
H=0: Primary hard disk port Address
H=1: Secondary hard disk port Address
F=0: Primary floppy disk port Address
F=1: Secondary floppy disk port Address

DH, DF, H, and F are cleared to '0' by master reset

5.5 Memory Control

Four RAS pins are available for controlling up to four 16 bit wide banks of system board RAM. Eight CAS pins control the low and high bytes of each bank. During a refresh cycle, all RAS signals will be active (ignoring the RAM configuration register FFF57) and CAS signals will stay inactive.

The RAS and CAS lines drive the DRAM array directly.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
128	RAS0-	O	RAS SIGNAL FOR DRAM MEMORY BANK 0
129	RAS1-	O	RAS SIGNAL FOR DRAM MEMORY BANK 1
130	RAS2-	O	RAS SIGNAL FOR DRAM MEMORY BANK 2
132	RAS3-	O	RAS SIGNAL FOR DRAM MEMORY BANK 3
125	CASL0-	O	CAS SIGNAL FOR DRAM MEMORY BANK 0, LOW BYTE
126	CASL1-	O	CAS SIGNAL FOR DRAM MEMORY BANK 1, LOW BYTE
2	CASL2-	O	CAS SIGNAL FOR DRAM MEMORY BANK 2, LOW BYTE
3	CASL3-	O	CAS SIGNAL FOR DRAM MEMORY BANK 3, LOW BYTE
4	CASH0-	O	CAS SIGNAL FOR DRAM MEMORY BANK 0, HIGH BYTE
5	CASH1-	O	CAS SIGNAL FOR DRAM MEMORY BANK 1, HIGH BYTE
6	CASH2-	O	CAS SIGNAL FOR DRAM MEMORY BANK 2, HIGH BYTE
131	CASH3-	O	CAS SIGNAL FOR DRAM MEMORY BANK 3, HIGH BYTE
18	REFR-	I	MEMORY REFRESH SIGNAL
43	CSPROM-	O	BIOS PROM SELECT
26	TAP2-	I	SECOND TAP OUTPUT OF RAS DELAY LINE
44	TAP1-	I	FIRST TAP OUTPUT OF RAS DELAY LINE
58	RAS-	O	TO RAS DELAY LINE INPUT

Table 5.4 MEMORY CONTROL PIN INFORMATION

5.6 Memory Address Multiplexer

The memory address multiplexer generates the row and column addresses for the DRAM. The memory address multiplexer outputs should be buffered by external drivers when driving the memory array.

PIN NUMBER	MNEMONIC	I/O	FUNCTION
31	RA0	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 0 (LSB)
32	RA1	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 1
33	RA2	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 2
34	RA3	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 3
35	RA4	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 4
36	RA5	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 5
37	RA6	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 6
38	RA7	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 7
39	RA8	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 8
41	RA9	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 9 (MSB)

Table 5.5 MEMORY ADDRESS MULTIPLEXER OUTPUTS

64K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
MEMORY MODE		MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
INDEPENDENT	RAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
INDEPENDENT	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A9
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20	A18)	A16	A15	A14	A13	A12	A11	A18	A17
PAGE MODE	CAS	(A10	A9)	A8	A7	A6	A5	A4	A3	A2	A1

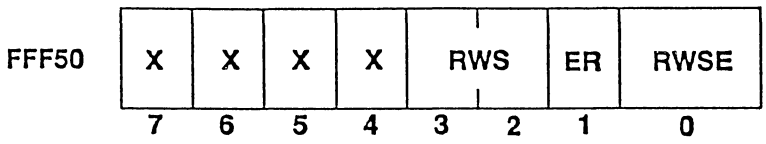
256K DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
INDEPENDENT	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A10	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	(A20)	A18	A16	A15	A14	A13	A12	A20	A19	A17
PAGE MODE	CAS	(A10)	A9	A8	A7	A6	A5	A4	A3	A2	A1

1 MBIT DRAM ADDRESS MULTIPLEXER CONFIGURATION											
INDEPENDENT	RAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
NON PAGE MODE	CAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
INDEPENDENT	RAS	A20	A18	A16	A15	A14	A13	A12	A11	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A12	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
4 WAY INTLV	RAS	A20	A18	A16	A15	A14	A13	A22	A21	A19	A17
PAGE MODE	CAS	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

REFRESH ADDRESS - ALL DRAM SIZES										
	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Table 5.6 ADDRESS MULTIPLEXER CONFIGURATIONS

SYSTEM BOARD ROM WAIT STATE
CONTROL REGISTER



RWS	HIGH SPEED WAIT STATE
00 *	1
01	2
10	3
11	4

RWSE=1: ENABLES RWS, OTHERWISE ON-BOARD ROM AND RAM WAIT STATES WILL BE SET BY FE3001.

ER = 1: EARLY EPROM/SYSTEM ADDRESS WILL BE GENERATED.

THIS REGISTER IS CLEARED TO ZERO BY MASTER RESET.

The RWSE bit is used to select between default wait states or programmble wait states for on-board RAM and ROM. The FE3001 wait state generator will generate 1 wait state for 16 bit devices and 4 wait states for 8 bit devices. If the RWSE bit is '0', then the FE3001 will generate the wait states. If the RWSE bit is '1', then the FE3021 will generate a programmable number of wait states, set by the RWS field. The on-board ROM and RAM wait states are generated using the high speed processor clock.

The ER bit will cause the EPROM or system address to be output to the expansion bus one high speed clock faster than normal. This will give more address setup time for the EPROM, which may allow the use of slower and less expensive EPROM. However, the expansion bus address hold time for the previous cycle will be reduced by the same amount. At 16 MHz, with early EPROM addressing enabled, the bus address hold time will be about 30 ns (one high speed clock).

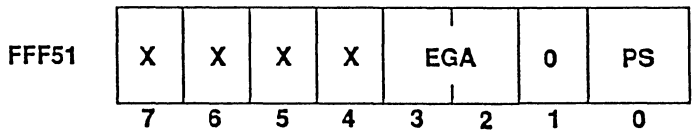
The system BIOS address space is from F0000 to FFFFF. If the EGA BIOS is to be mapped, then the BIOS ROM chip select is also active when the region from C0000 to C3FFF is addressed. The address output onto the expansion bus will be automatically translated. The BIOS PROM size and number of wait states will then apply to both regions F0000-FFFFF and C0000-C3FFF.

The BIOS EPROM size may either be 8 bits or 16 bits. The EPROM size is determined at reset time, and is signaled by the IORDY line. If the IORDY line is high at the trailing edge of master reset, then the EPROM size is set to 16 bits. If the IORDY line is low at the trailing edge of master reset, then the EPROM size is set to 8 bits.

The CSPROM- signal is only active when MEMR- is active.

MEMORY ADDRESS RANGE FOR ACTIVE CSPROM-	FUNCTION
0F0000-0FFFFF FF0000-FFFFFF	BIOS SIZE = 64K (DEFAULT).
0E0000-0FFFFF FE0000-FFFFFF	BIOS SIZE = 128K.
0C0000-0C3FFF	16K EGA BIOS MAPPING ENABLED. ADDRESSES TRANSLATED TO 0F8000-0FBFFF
0C0000-0C7FFF	32K EGA BIOS MAPPING ENABLED. ADDRESSES TRANSLATED TO 0F8000-0FFFFF

EPROM / RAM MAP CONTROL REGISTER



EGA = 00: No EGA mapping.
01: 16K EGA map. C0000 - C3FFF mapped to F8000 - FBFFF
10: 32K EGA map. C0000 - C7FFF mapped to F8000 - FFFFF

PS = 0: PROM chip select will be active when address is 0F0000-0FFFFF or FF0000-FFFFFF, for 64K of BIOS.
Default case after master reset.
1: PROM chip select will be active when address is 0E0000-0FFFFF or FE0000-FFFFFF, for 128K of BIOS.

A single contiguous block of memory may be write protected, so that when BIOS ROM is copied into RAM, the RAM copy will not be inadvertently altered.

Master reset clears the upper address boundary registers and presets the lower address boundary registers, which disables write protection. Write protection is enabled on the address range where the RAM address is less than or equal to the upper address boundary as well as greater than or equal to the lower address boundary. Write protection is programmable on 64K boundaries, and the write protection boundaries must be equal to or above 80000H and equal to or below FFFFFH. Write protection will not affect EMS writing even if the EMS window address range is covered by write protection boundaries. This allows protection of BIOS code copied into RAM without affecting operation of EMS.

Write protection is accomplished by not asserting CAS when MEMW is active.

RAM WRITE PROTECT
UPPER ADDRESS BOUNDARY

	7	6	5	4	3	2	1	0
FFF53	X	X	X	X	'1'	A18	A17	A16

THIS REGISTER IS CLEARED BY MASTER RESET

RAM WRITE PROTECT
LOWER ADDRESS BOUNDARY

	7	6	5	4	3	2	1	0
FFF55	X	X	X	X	'1'	A18	A17	A16

THIS REGISTER IS PRESET TO ALL '1' BY MASTER RESET

Three of the memory banks , may be programmed to various sizes, on 128K boundaries. The fourth memory bank's starting address location is fixed at 100000(hex).

A pair of window registers determines the address range for each memory bank. This allows banks 0, 1 , or 2 to be positioned at varying points and in different order than the bank number. If one bank of memory is defective, it can be disabled and the other banks can be programmed to replace it.

Bank 0 has three pairs of window registers to allow split addressing, so that the bank can be configured around the 640K-1024K area reserved for video and BIOS. A hardware address translator is used to move the top split. One additional split addressing mode allows copying user and video BIOS into RAM for faster execution. n this mode, the hardware address translator is turned off. A typical configuaration when using this mode is where there are two banks of 256K DRAM. The bottom split would be used for conventional memory from 8000 to 9FFFF. The top split could be used for extended memory or could be used to copy main BIOS from ROM to RAM in the address range E0000 or F0000 to FFFFF. A middle split is available for copying user and video BIOS from ROM to RAM. This middle split has boundaries programmable between C0000 to DFFFF in 16K address increments.

In non-interleaved mode, bank 3's position is fixed. The lower boundary starts at 100000(hex). The upper boundary is at 11FFFF(hex) for 64K DRAM, at 17FFFF(hex) for 256K-DRAM, and at 2FFFFF(hex). In interleaved mode, bank 3's position is set by bank 0 (for 4 way interleave) or by bank 2 (for 2 way interleave).

BANK 0 - LOWER SPLIT

UPPER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF57	X	X	X	X	A19	A18	A17	'0'

UPPER BOUNDARY MUST BE 0FXXXX OR BELOW

LOWER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF59	X	X	X	X	A19	0	0	0

LOWER BOUNDARY MUST BE 00XXXX OR 08XXXX

UPPER ADDRESS BOUNDARY = 09XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = 08XXXX (HEX) BY MASTER RESET

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF5B	X	X	X	X	A19	A18	A17	'0'

LOWER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF5D	X	X	X	X	A19	A18	A17	'0'

BANK 0 - UPPER SPLIT

UPPER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF5A	X	X	X	X	A23	A22	A21	A20

LOWER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF5C	X	X	X	X	A23	A22	A21	A20

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(UPPER SPLIT DISABLED)

BANK 0 - MIDDLE SPLIT

UPPER ADDRESS BOUNDARY - LSD

FFF5F	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - LSD

FFF61	X	X	X	X	A15	A14	'0'	'0'
	7	6	5	4	3	2	1	0

BANK 0 - MIDDLE SPLIT

UPPER ADDRESS BOUNDARY - MSD

FFF5E	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF60	X	X	X	X	'1'	'1'	'0'	A16
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET
LOWER ADDRESS BOUNDARY = FFXXXX (HEX) BY MASTER RESET
(UPPER SPLIT DISABLED)

BANK 1

UPPER ADDRESS BOUNDARY - LSD

FFF63	X	X	X	X	A19	A18	A17	'0'
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - LSD

FFF65	X	X	X	X	A19	A18	A17	'0'
	7	6	5	4	3	2	1	0

BANK 1

UPPER ADDRESS BOUNDARY - MSD

FFF62	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - MSD

FFF64	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

UPPER ADDRESS BOUNDARY = 07XXXX (HEX) BY MASTER RESET
LOWER ADDRESS BOUNDARY = 00XXXX (HEX) BY MASTER RESET

BANK 2

UPPER ADDRESS BOUNDARY - LSD

FFF67	X	X	X	X	A19	A18	A17	'0'
	7	6	5	4	3	2	1	0

LOWER ADDRESS BOUNDARY - LSD

FFF69	X	X	X	X	A19	A18	A17	'0'
	7	6	5	4	3	2	1	0

BANK 2

UPPER ADDRESS BOUNDARY - MSD

FFF66	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE CLEARED BY MASTER RESET

LOWER ADDRESS BOUNDARY - MSD

FFF68	X	X	X	X	A23	A22	A21	A20
	7	6	5	4	3	2	1	0

THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

(BANK 2 DISABLED BY MASTER RESET)

BANK 3.

UPPER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF6B	X	X	X	X	A19	A18	A17	'0'

LOWER ADDRESS BOUNDARY - LSD

	7	6	5	4	3	2	1	0
FFF6D	X	X	X	X	A19	A18	A17	'0'

BANK 3

UPPER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF6A	X	X	X	X	A23	A22	A21	A20

THESE REGISTERS ARE CLEARED BY MASTER RESET

LOWER ADDRESS BOUNDARY - MSD

	7	6	5	4	3	2	1	0
FFF6C	X	X	X	X	A23	A22	A21	A20

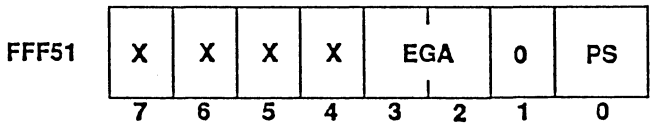
THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET
(BANK 3 DISABLED BY MASTER RESET)

When bank 3 is used, registers FFF6A-FFF6D must be programmed as follows:

All DRAM sizes:	FFF6C=0001	FFF6D=0000
For 64K DRAM:	FFF6A=0001	FFF6B=0001
For 256K DRAM:	FFF6A=0001	FFF6B=011
For 1MBIT DRAM:	FFF6A=0010	FFF6B=1111

The RAM banks may be either independent or two-way or four-way page interleaved. DRAM banks which are interleaved must be the same DRAM size.

Bank 0 may be split into three different areas. The S bit is set to '0' when there is either one or two splits and the middle split is not used. This would usually be the case where bank 0 is composed of 256K or 1 Mbit DRAM, and the upper portion of bank 0 is used for extended or expanded memory, and the lower portion is used to backfill conventional memory. The S bit is set to '1' when there are three splits and the middle split is used to replace user ROM. In this case, the address span of the lower boundary of the lowest used split to the upper boundary of the highest used split must not exceed the DRAM size. For instance, if bank 0 is composed of 256K DRAM and the lower split is not used, and the middle split has user ROM at C0000-C3FFF copied into it, then the upper split may be programmed for extended memory from 100000 to 120000.



CFG	FUNCTION
000*	ALL BANKS ARE INDEPENDENT
011	BANK 2 PAIRED WH BANK 3, BANKS 0 AND 1 ARE INDEPENDENT
101	BANK 0 PAIRED WITH BANK 1, BANKS 2 AND 3 ARE INDEPENDENT
111	BANK 0 PAIRED WITH BANK 1, BANK 2 PAIRED WITH BANK 3
110	ALL FOUR BANKS ARE INTERLEAVED

S	FUNCTION
0*	BANK 0 SPLIT ADDRESSING AROUND BIOS AREA
1	BANK 0 SPLIT ADDRESSING INCLUDES BIOS AREA

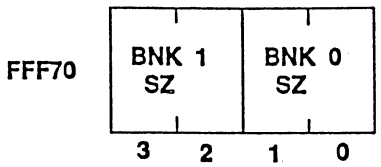
*: DEFAULT AFTER MASTER RESET

The following table illustrates memory system characteristics with various configurations of memory and processor speed, both for page mode and non-page mode DRAM access. For a page mode hit, the read and write accesses may have different performance. For a page mode miss or the first access to a page, the read and write accesses have the same performance. In a page mode miss, RAS- starts out low and must be brought high for a RAS precharge time before the memory can be accessed.

RAM MODE	CPU FREQ	"WAIT STATES" HIT READ/WRITE	MISS R/W	DRAM SPEED	TYPICAL DRAM
	20 MHz	1/1	NA	70 NS	NMB AAA2801
	16 MHz	1/1	NA	100 NS	FUJ 81C258-10
INDEPENDENT	16 MHz	1/1	NA	80 NS	NMB AAA2801
(NON PAGE	12.5 MHz	0/1	NA	80 NS	NMB AAA2801
MODE)	12.5 MHz	1/1	NA	120 NS	FUJ MB81256-12
	10 MHz	0/1	NA	100 NS	TBD
	10 MHz	1/1	NA	150 NS	FUJ MB81256-15
	8 MHz	0/0	NA	120 NS	TBD
PAGE MODE	16 MHz	0/1	2	100 NS	FUJ MB81256-10
FAST PG MODE	16 MHz	0/1	2	100 NS	FUJ 81C258-10
					MIT M5M4C1000-10
STATIC					
COLUMN	20 MHz	0/1	2	70 NS	NMB AAA2801-70

Table 5.7 MEMORY SYSTEM CHARACTERISTICS

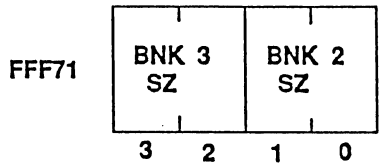
RAM SIZE CONFIGURATION REGISTER - BANK 1 AND 0



SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

BANK 0 SETS THE RAM SIZE FOR BANK 0
BANK 1 PAIRING OR FOR FOUR WAY INTLV.

RAM SIZE CONFIGURATION REGISTER - BANK 3 AND 2



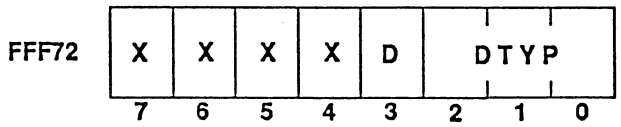
SZ = 00 *: 256K
01 : 1M
10 : RESERVED
11 : 64K

BANK 2 SETS THE RAM SIZE FOR BANK 2
BANK 3 PAIRING

The DRAM timing is set by an external delay line for DMA or master mode transfers. The RAS leading edge becomes active from the active level of the MEMR- or MEMW- signals.

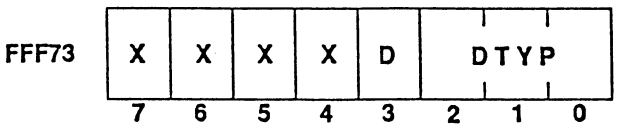
The DRAM timing modes are programmed by writing into register FFF72. The DRAM timing mode is actually switched during a processor hold state caused by a refresh, DMA, or bus master cycle. The Present DRAM Timing Mode register contains the current timing mode. Registers FFF72 and FFF73 will thus disagree until after a processor hold state occurs; typically, a refresh cycle will occur in 10 to 15 microseconds.

DRAM TIMING MODE



DRAM TIMING MODE WILL GO INTO EFFECT AFTER
REFRESH, DMA, OR OTHER HOLD CYCLE

PRESENT DRAM TIMING MODE



READ-ONLY

DTYP	DRAM MODE	
000*	NON-PAGE	(MODE 0)
001	ZERO WAIT STATE READ, ONE WAIT STATE WRITE	(MODE 1)
010	FAST PAGE MODE DRAM AT 20 MHZ CPU RATE	(MODE 2)
011	STANDARD PAGE MODE FOR 8-16 MHZ CPU RATE	(MODE 3)
100	NON-PAGE FOR STANDARD DRAM AT 8-12 MHZ CPU RATE, RAS PULSE WIDTH IS 3 CPU CLOCKS	(MODE 4)
101	NON-PAGE FOR STANDARD DRAM AT 8-12 MHZ CPU RATE, RAS PULSE WIDTH IS 2 CPU CLOCKS	(MODE 5)

*: DEFAULT AFTER MASTER RESET

D=0: NORMAL OPERATION (DEFAULT)

1: RESERVED FOR DIAGNOSTICS;
DISABLES DRAM PAGE MODE HIT/MISS LOGIC.

Refer to Section 2 for the timing relationships of the various memory modes.

5.7 EMS Memory

RAM memory above 640K may be used for expanded memory. EMS memory may be as small as 128K bytes or as large as 7168K bytes. The EMS memory is accessed by two sets of EMS Page Registers, which reside in user I/O space. Each set of EMS Page Registers points to 36 blocks of memory, each block 16K bytes in size, which make up the EMS Page Frame. Four of the blocks are located above 640K, with the other 32 blocks located between 128K and 640K.

Each EMS Page Register is associated with one page of the EMS Page Frame, and consists of an enable bit and a 10 bit page number. When enabled, a 24 bit real address is formed by taking the 10 bit page number and appending the 14 bit address referencing the byte or word in the EMS page. The 24 bit address is then used to access the DRAM memory controlled by the FE3021.

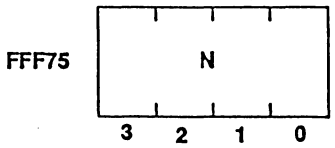
The FE3021 "page hit" circuitry is used for EMS, even if non-page mode is in effect. This will allow EMS access without additional wait states if accesses are made to the same 256 byte page. This is true even for zero wait state page mode operation at 16 MHz or zero wait state non-page mode operation at 12 MHz.

The EMS hardware must first be configured by programming the EMS control registers located in the FFF00-FFFFF register space, which is unlocked by writing to memory location FFF00 eight times. The I/O port locations of the EMS Page Registers are in user I/O space and are their locations are selected with EMS Configuration Registers FFF75 and FFF78.

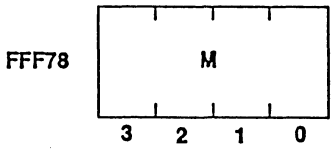
EMS Configuration Register FFF79 is used to completely enable or disable EMS, as well as to switch between the two sets of EMS Page registers.

EMS DMA Control Register FFF7A is used to control the selected EMS map register set during DMA or aster transfers. This allows DMA transfers to be made to particular EMS task, whether or not it is the currently selected task.

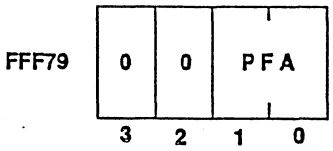
EMS CONFIGURATION REGISTER N



EMS CONFIGURATION REGISTER M

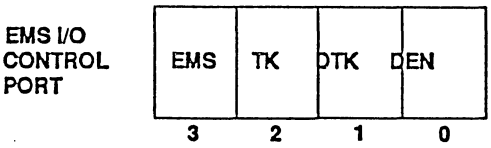


EMS CONFIGURATION REGISTER



PFA = 00 : EMS PAGE FRAME C4000-D3FFF
PFA = 01 : EMS PAGE FRAME C8000-D7FFF
PFA = 10 : EMS PAGE FRAME CC000-DBFFF
PFA = 11 : EMS PAGE FRAME D0000-DFFFF

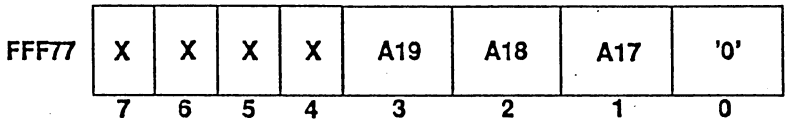
EMS CONTROL REGISTER



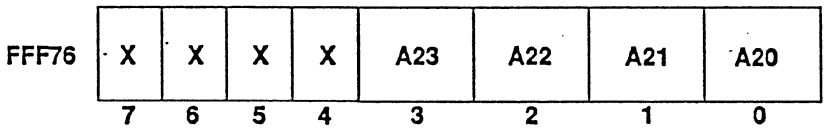
DEN=0 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "TK" BIT
DEN=1 : DMA TRANSFERS MADE TO MAP REGISTER SET SPECIFIED BY "DTK" BIT

On-board memory may be allocated either to extended or to EMS memory in 128K byte blocks. EMS memory is allocated from the top of on-board memory down to the desired limit.

EMS LOWER ADDRESS BOUNDRY - LSD

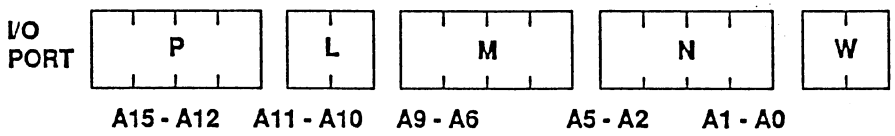


EMS LOWER ADDRESS BOUNDRY - MSD



THESE REGISTERS ARE PRESET TO ALL '1' BY MASTER RESET

EMS PAGE REGISTER ADDRESS FORMAT



P	W	EMS PAGE			
		PFA=00	PFA=01	PFA=10	PFA=11
0000	11	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF	DC000-DFFFF
0000	10	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF	D8000-DBFFF
0000	01	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF	D4000-D7FFF
0000	00	C4000-C7FFF	C8000-CBFFF	CC000-CFFFF	D0000-D3FFF
1001	11	9C000-9FFFF	624K TO 640K.		
1001	10	98000-9BFFF	608K TO 624K.		
1001	01	94000-97FFF	592K TO 608K.		
1001	00	90000-93FFF	576K TO 592K.		
1000	11	8C000-8FFFF	560K TO 576K.		
1000	10	88000-8BFFF	544K TO 560K		
1000	01	84000-87FFF	528K TO 544K.		
1000	00	80000-83FFF	512K TO 528K.		
0111	11	7C000-7FFFF	496K TO 512K.		
0111	10	78000-7BFFF	480K TO 496K.		
0111	01	74000-77FFF	464K TO 480K.		
0111	00	70000-73FFF	448K TO 464K.		
0110	11	6C000-6FFFF	432K TO 448K.		
0110	10	68000-6BFFF	416K TO 432K.		
0110	01	64000-67FFF	400K TO 416K.		
0110	00	60000-63FFF	384K TO 400K.		
0101	11	5C000-5FFFF	368K TO 384K		
0101	10	58000-5BFFF	352K TO 368K.		
0101	01	54000-57FFF	336K TO 352K.		
0101	00	50000-53FFF	320K TO 336K.		
0100	11	4C000-4FFFF	304K TO 320K.		
0100	10	48000-4BFFF	288K TO 304K.		
0100	01	44000-47FFF	272K TO 288K.		
0100	00	40000-43FFF	256K TO 272K.		
0011	11	3C000-3FFFF	240K TO 256K.		
0011	10	38000-3BFFF	224K TO 240K.		
0100	01	34000-37FFF	208K TO 224K.		
0011	00	30000-33FFF	192K TO 208K.		
0010	11	2C000-2FFFF	176K TO 192K.		
0010	10	28000-2BFFF	160K TO 176K.		
0010	01	24000-27FFF	144K TO 160K		
0010	00	20000-23FFF	128K TO 144K.		

Table 5.8 EMS PAGE REGISTER INFORMATION

5.8 Test Mode

All output pins will become tristated if YMEMR- and YMEMW- are active simultaneously while MR- is active. The outputs will remain tristated if MR- is brought inactive while YMEMR- and YMEMW- are both active. The outputs will become active drivers again when MR- is brought low without both YMEMR- and YMEMW- active. This "all output tristate" mode allows an in-circuit board tester to drive the FE3021 output pins.

5.9 FE3021 Pinout

The FE3021 is packaged in a 132-pin plastic flat pack. The pins are grouped below by function, and pin numbers are given for each type of package.

The output signal drive capability listed in the charts below are sizes for the actual I/O drivers and are sized for AC drive only. Refer to the DC Characteristics section for the DC output drive specifications.

80286 INTERFACE		
A23	77	7 MA I/O
A22	78	7 MA I/O
A21	79	7 MA I/O
A20	80	7 MA I/O
A19	81	7 MA I/O
A18	82	7 MA I/O
A17	83	7 MA I/O
A16	84	7 MA I/O
A15	85	7 MA I/O
A14	86	7 MA I/O
A13	87	7 MA I/O
A12	88	7 MA I/O
A11	89	7 MA I/O
A10	90	7 MA I/O
A9	109	7 MA I/O
A8	110	7 MA I/O
A7	111	7 MA I/O
A6	112	7 MA I/O
A5	113	7 MA I/O
A4	114	7 MA I/O
A3	115	7 MA I/O
A2	116	7 MA I/O
A1	117	7 MA I/O
A0	118	7 MA I/O
S0-	119	TTL INPUT
S1-	120	TTL INPUT
M/IO	121	TTL INPUT
CPUCLK	122	TTL INPUT
HLDA	123	TTL INPUT
IORDY	124	12 MA O.C.

DATA BUS		
EDATA3	17	4 MA I/O
EDATA2	16	4 MA I/O
EDATA1	15	4 MA I/O
EDATA0	14	4 MA I/O
CHIP SELECTS AND CONTROL		
CS0-	48	4 MA OUT
CS1-	47	4 MA OUT
CS2-	46	4 MA OUT
CS3-	45	4 MA OUT
CSF	49	4 MA OUT
CS8042-	55	4 MA OUT
CS287-	56	4 MA OUT
CSNMI-	20	4 MA OUT
CSPTB-	22	4 MA OUT
ADSTB-	53	TTL INPUT
SELDAT-	50	4 MA OUT
YMEMR-	10	TTL INPUT
YMEMW	11	TTL INPUT
YIOR-	12	4 MA I/O
YIOW-	13	4 MA I/O
IOR-	8	12 MA I/O
IOW-	9	12 MA I/O
MEMORY ADDRESS MUX		
RA9	41	4 MA OUT
RA8	39	4 MA OUT
RA7	38	4 MA OUT
RA6	37	4 MA OUT
RA5	36	4 MA OUT
RA4	35	4 MA OUT
RA3	34	4 MA OUT
RA2	33	4 MA OUT
RA1	32	4 MA OUT
RA0	30	4 MA OUT
RAS-	51	4 MA OUT
TAP1-	44	TTL IN
TAP2-	26	TTL IN

AT BUS		
LA23	63	12 MA I/O
LA22	70	12 MA I/O
LA21	71	12 MA I/O
LA20	93	12 MA I/O
LA19	95	12 MA I/O
LA18	102	12 MA I/O
LA17	103	12 MA I/O
ADDR19	59	12 MA OUT
ADDR18	61	12 MA OUT
ADDR17	62	12 MA OUT
ADDR16	64	12 MA I/O
ADDR15	65	12 MA I/O
ADDR14	66	12 MA I/O
ADDR13	68	12 MA I/O
ADDR12	69	12 MA I/O
ADDR11	72	12 MA I/O
ADDR10	73	12 MA I/O
ADDR9	75	12 MA I/O
ADDR8	92	12 MA I/O
ADDR7	96	12 MA I/O
ADDR6	97	12 MA I/O
ADDR5	98	12 MA I/O
ADDR4	100	12 MA I/O
ADDR3	101	12 MA I/O
ADDR2	104	12 MA I/O
ADDR1	106	12 MA I/O
ADDR0	107	12 MA I/O
GROUND	POWER	
1	31	
29	40	
42	60	
58	74	
67	94	
76	105	
91	131	
99		
108		
127		

MEMORY CONTROL		
RAS0-	128	12 MA OUT
RAS1-	129	12 MA OUT
RAS2-	130	12 MA OUT
RAS3-	132	12 MA OUT
CASOL-	125	12 MA OUT
CAS1L-	126	12 MA OUT
CAS2L	2	12 MA OUT
CAS3L	3	12 MA OUT
CASOH-	4	12 MA OUT
CAS1H-	5	12 MA OUT
CAS2H-	6	12 MA OUT
CAS3H-	7	12 MA OUT
REFR-	18	TTL INPUT
CSPROM-	43	4 MA OUT
ONBD-	57	4 MA OUT
MASTER-	52	TTL INPUT
BHE	21	TTL INPUT
DBLE-	23	4 MA OUT
ADRO	24	TTL INPUT
LOMEG-	25	4 MA OUT
RESET-	28	TTL INPUT
A20GT	54	TTL INPUT
FRES-	19	4 MA OUT

5.10 DC Operating Characteristics

T_a = 0° to 70° C Vcc = 5 V =/- .25 V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
IIL	INPUT LEAKAGE		+/-10	UA	VIN=.4 TO VCC
IOZ	TRISTATE AND OPEN DRAIN OUTPUT LEAKAGE		+/-10	UA	VOUT=.4 TO VCC
VIH	INPUT HIGH VOLTAGE	2.0		V	
VIL	INPUT LOWVOLTAGE		.8	V	
ICC	SUPPLY CURRENT		50	mA	ALL OUTPUTS OPEN, INPUTS AT 2.0V, CLKOUT=SYSCLK= 16 MHZ

FOR OUTPUTS YIOR-, YIOW-, RA9-RA0, ONBD-, LOMEG-, A23-A0, CSF, CS0-, CS1-, CS2-, CS3-, CS8042-, CS287-, CSNMI-, CSPTB-, RAS0-, RAS1-, RAS2-, RAS3-, CAS0L-, CAS1L-, CAS2L-, CAS3L-, CAS0H-, CAS1H-, CAS2H-, CAS3H-, CSPROM-, SELDAT-, AND EDATA3-EDATA0

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IOUT=-1 mA
VOL	OUTPUT LOW VOLTAGE		.4	V	IOUT=1 mA

FOR OUTPUTS ADDR19-ADDR0, LA23-LA17, IOR-, IOW-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOH	OUTPUT HIGH VOLTAGE	2.4		V	IOUT=-12 mA
VOL	OUTPUT LOW VOLTAGE		.4	V	IOUT=12 mA

FOR TRI-STATE OUTPUT - IORDY

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VOL	OUTPUT LOW VOLTAGE		.4	V	IOUT=12 mA

5.11 AC Timing Characteristics

load capacitance = 50 pF for outputs: CSF, CS0-, CS1-, CS2-, CS3-, CS8042-, CS287-, CSNMI-, CSPTB-, SELDAT-, RA0-RA9, ONBD-, LOMEG-

load capacitance = 100 pF for output: IORDY, A19-A0, EDATA3-EDATA0

load capacitance = 200 pF for outputs: RAS0-, RAS1-, RAS2-, RAS3-, CAS0L-, CAS1L-, CAS2L-, CAS3L-, CAS0H-, CAS1H-, CAS2H-, CAS3H-, LA17, ADDR19-ADDR0, IOR-, IOW-

5.12 Clock Timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
T1	CPUCLK CYCLE	25		NS
T2	CPUCLK HIGH PULSE WIDTH	11		NS
T3	CPUCLK LOW PULSE WIDTH	11		NS
T6	S0-,S1- SETUP TO CPUCLK	3		NS
T7	S0-,S0- HOLD FROM CPUCLK		10	NS
T8	MIO SETUP TO CPUCLK	10		NS
T9	MIO HOLD FROM CPUCLK		10	NS

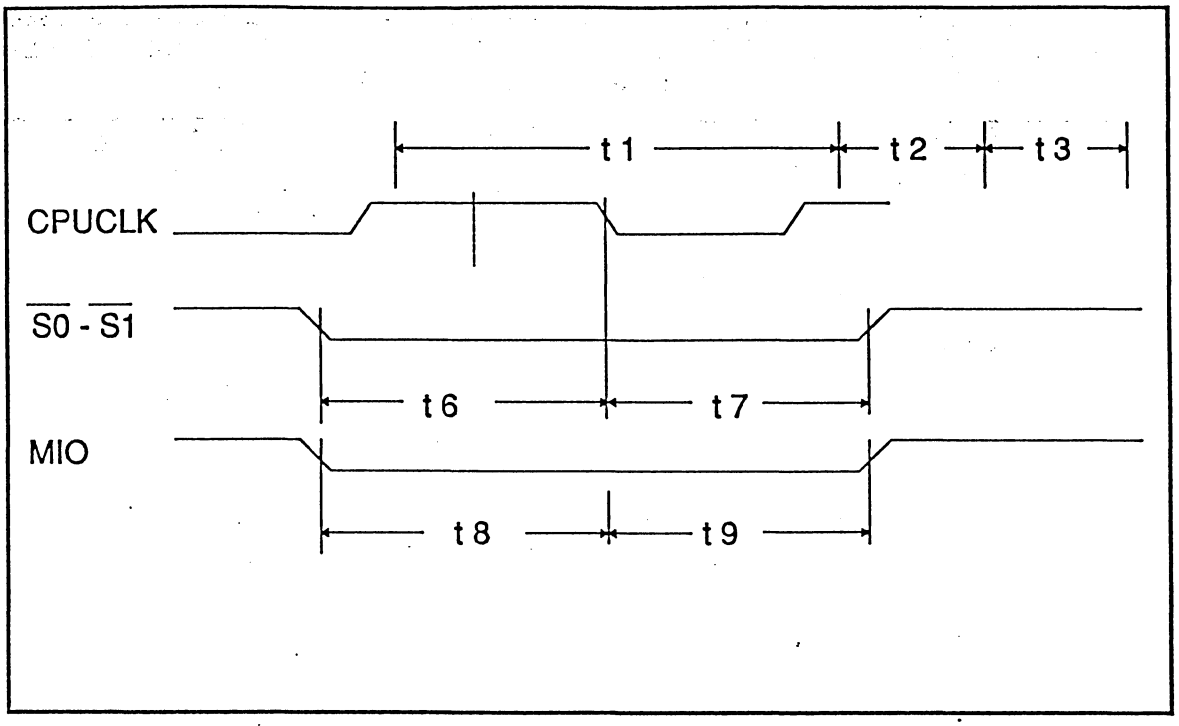


Figure 5.2 CLOCK TIMING

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS
T11	ADSTB PULSE WIDTH	32		NS
T12	ADDRESS SETUP TO ADSTB	30		NS
T13	ADDRESS HOLD FROM ADSTB END	10		NS
T14A	ADSTB TO OUTPUTS ZWS-, ONBD-, CSPROM-, RAS0-, RAS1-, RAS2-, RAS3-, CASOL-, TO CAS3L, CASOH- TO CAS3H		35	NS
T14B	ADSTB TO OUTPUTS CS0-, CSPTB-, CS2-, CS3-, CSF, CS287-, CSNMI-, CS1-, CS8042-		45	NS
T15	IORDY FROM ADSTB		35	NS
T16	IORDY FROM CPUCLK		35	NS

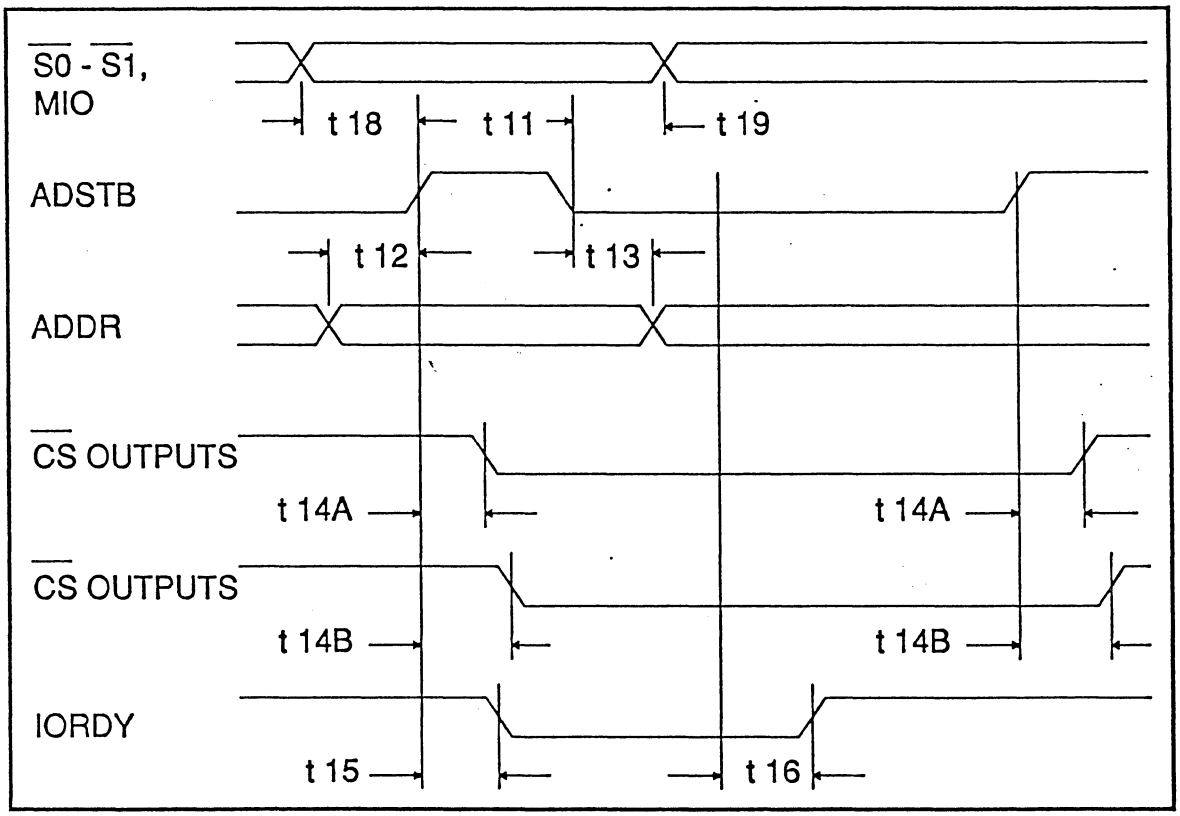


Figure 5.3 CLOCK TIMING

5.13 Register Read and Write Timing

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
T20	DATA VALID FROM RE- START	120		NS	REGISTERS UNLOCKED
T21	DATA HOLD FROM RE- END	0	30	NS	REGISTERS UNLOCKED
T24	DATA SETUP TO MEMW- OR IOW- END	120		NS	REGISTERS UNLOCKED
T25	DATA HOLD FROM MEMW- OR IOW- END		12	NS	REGISTERS UNLOCKED
T26	IOR- TO SELDAT-		35	NS	

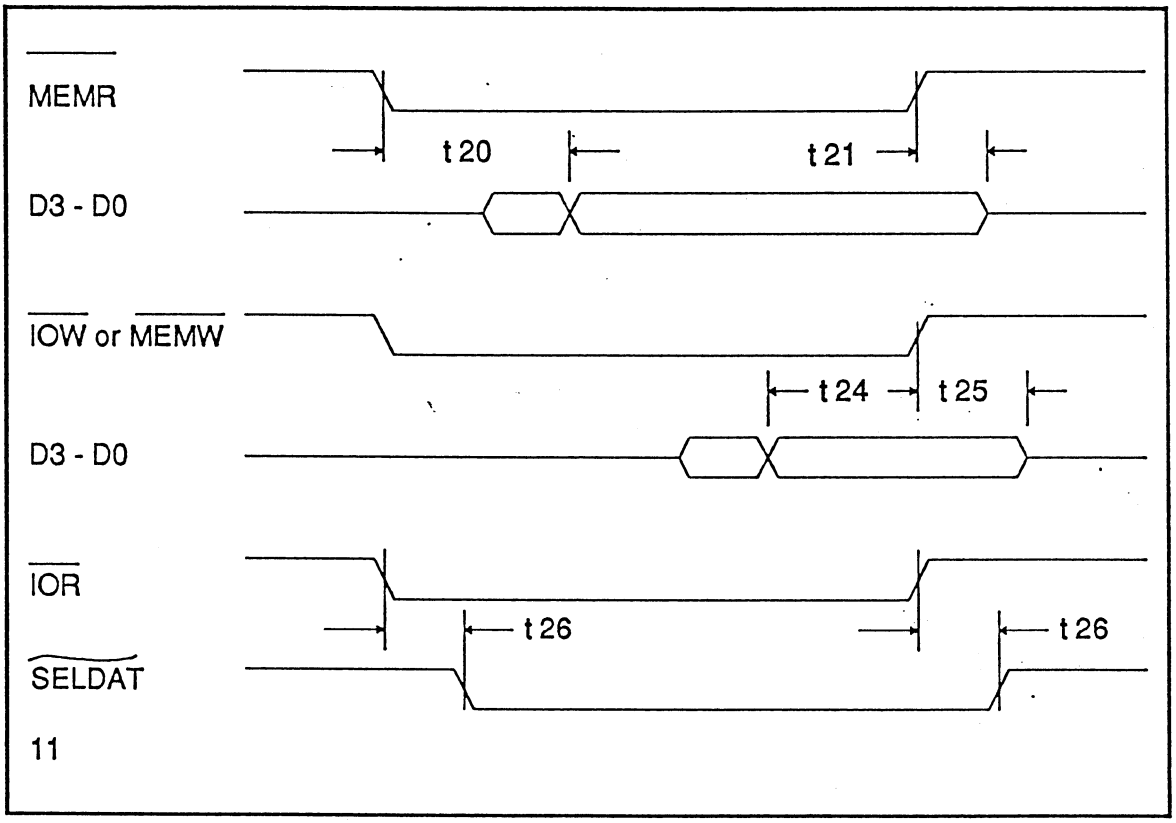


Figure 5.4 REGISTER R/W TIMING DIAGRAM

FE3031 AT DATA BUFFER

6.0 Introduction

This section describes the pinouts, signals, timing and electrical specifications of the FE3031 AT Data Buffer IC. The FE3031 contains all of the data buffers necessary to implement an AT compatible computer. It is part of the FE3600 AT Core Logic chip set for 16MHz 80286 based AT computers. A block diagram of the FE3031 is shown in Figure 6.1.

6.1 Features

- 100 Pin PLCC
- PC/AT Data Bus Buffers
- Peripheral Data Bus Buffer
- Memory Data Bus Buffers
- Parity Generator/Checker
- 1.25 Micron CMOS Technology

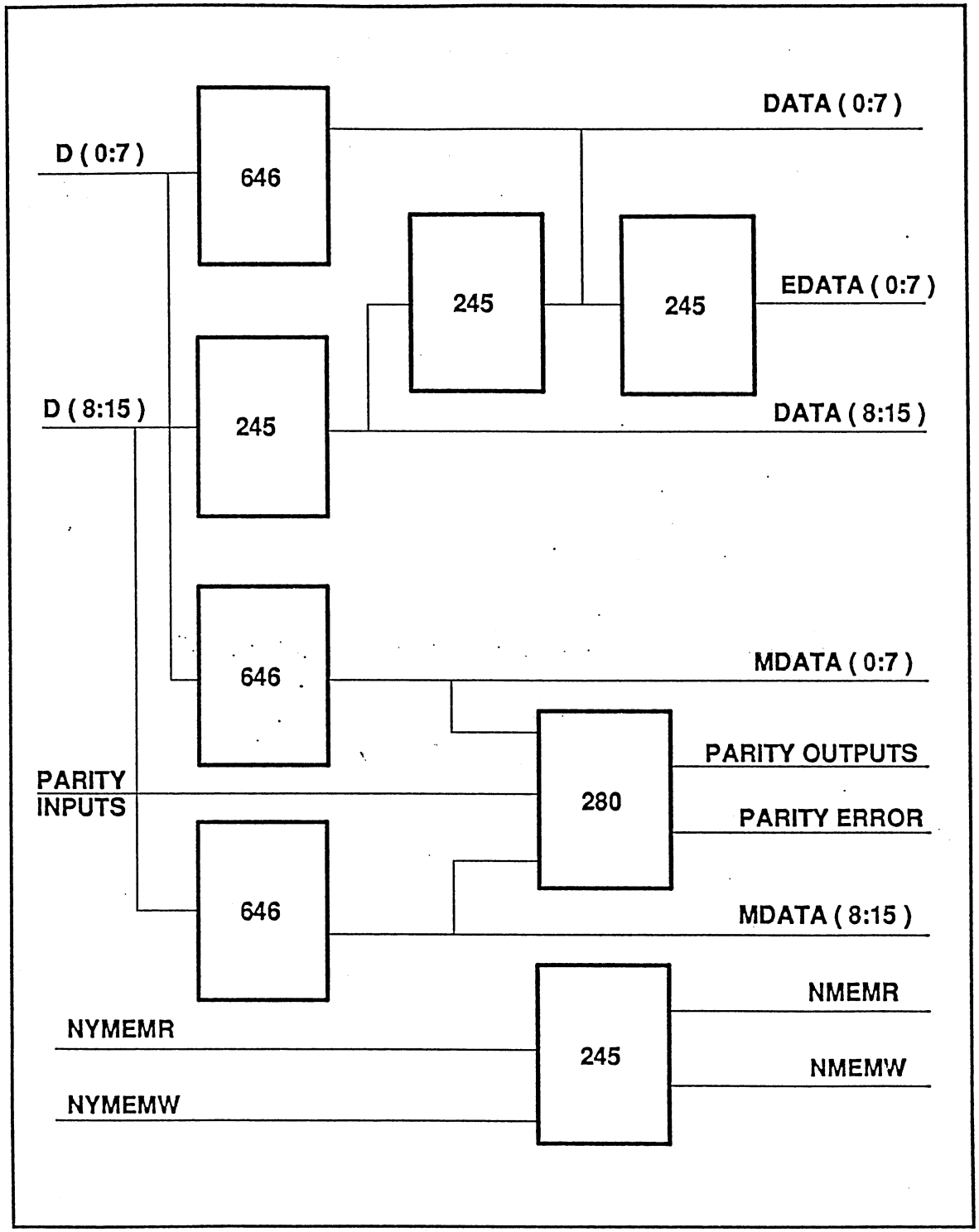


Figure 6.1 FE3031 FUNCTIONAL BLOCK DIAGRAM

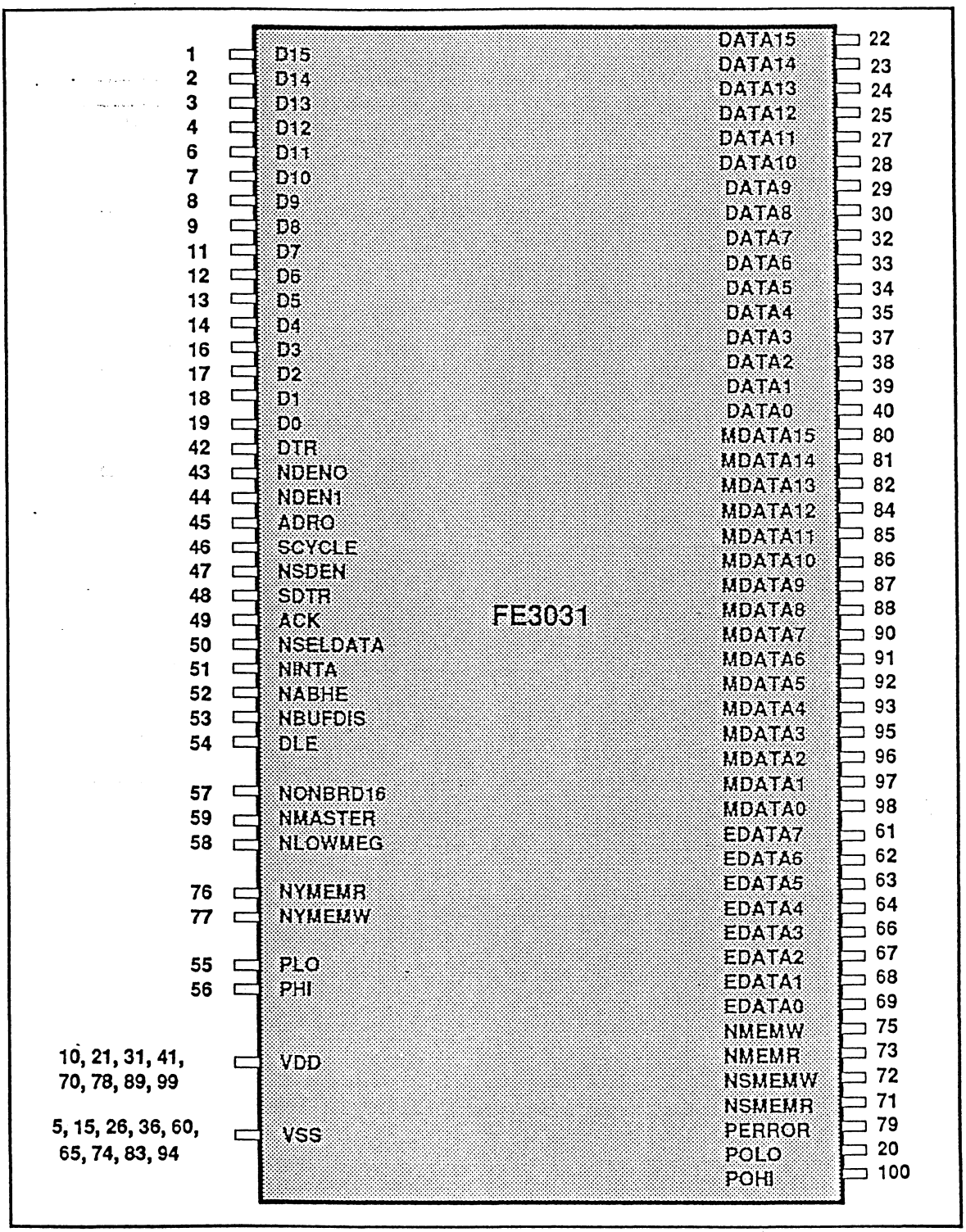


Figure 6.2 FE3031 PIN ASSIGNMENTS AND LOCATIONS

6.2 Signal Descriptions

PIN#	SIGNAL	TYPE	DESCRIPTION
1-4 6-9 11-14 16-19	D(0:15)	I/O	80286 Local Data Bus
5,15 26,36 60,65 74,83 94	VSS		Ground
10,21 31,41 70,78 89,99	VDD VDD VDD VDD		+5V VDD
20	POLO	O	Low byte parity bit to the DRAMs
22-25 27-30 32-35 37-40	DATA (0:15)	I/O	PC/AT Data Bus
42	DTR	I	Data direction for DATA buffers
43	NDEN0	I	Low byte data enable to DATA buffers
44	NDEN1	I	High byte data enable to DATA buffers
45	ADR0	I	Address bit 0 for MDATA buffers and byte swap
46	SCYCLE	I	Latch low byte during byte swap read
47	NSDEN	I	Byte swap data buffer enable
48	SDTR	I	Byte swap data direction to swap buffer
49	ACK	I	DMA Acknowledge signal to the PC/AT bus
50	NSELDATA	I	EDATA bus enable
51	NINTA	I	Interrupt acknowledge
52	NABHE	I	High byte enable for MDATA bus
53	NBUFDIS	I	Disable Buffers when low
54	NDLE	I	Latch MDATA bus during a read
55	PLO	I	Low byte parity bit from DRAMs
56	PHI	I	High byte parity bit from DRAMs
57	NONBRD16	I	NONBRD indicates a local DRAM operation

Table 6.1 FE3031 SIGNAL DESCRIPTIONS

PIN	SIGNAL	TYPE	DESCRIPTION
58	NLOWMEG	I	NLOWMEG indicates access of low MB of memory
59	NMASTER	I	Master on PC bus has control of the bus
61-64 66-69	EDATA (0:7)	I/O	Peripheral Data Bus for FE3001, FE3010, RTC and Keyboard controller
71	NSMEMR	O	Low 1 MB Memory Read to PC bus
72	NSMEMW	O	Low 1 MB Memory Write to PC bus
73	NMEMR	I/O	Memory read to/from AT bus
75	NMEMW	I/O	Memory read to/from AT bus
76	NYMEMR	I/O	Memory read to/from FE3001
77	NYMEMW	I/O	Memory write to/from FE3001
79	PERROR	O	RAM parity error
80-82 84-88 90-93 95-98	MDATA (0:15)	I/O	Memory Data bus
100	POHI	O	High byte parity bit to the DRAMs

Table 6.1 FE3031 SIGNAL DESCRIPTIONS (CONT.)

6.3 Absolute Maximum Ratings

Ambient Temperature (operating) =	0° to + 70°C
Storage Temperature =	-40° to +125°C
Voltage on any pin to ground =	+7 V
Power Dissipation =	400 mW

6.4 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IL}	Input LOW Voltage		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V	
I_{OL}	LOW V Output Current[1]		4	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[1]		-4	mA	V_{OH} = 2.4 V
I_{OL}	LOW V Output Current[2]		18	mA	V_{OL} = 0.4 V
I_{OH}	HIGH V Output Current[2]		-18	mA	V_{OH} = 2.4 V
V_{DD}	Supply Voltage (Any V_{DD})	4.75	5.25	V	

Notes:

1. Output currents are for D(0:15), EDATA(0:7), NYMEMR, NYMEMW, PERROR
2. Output currents are for DATA(0:15), MDATA(0:15), NMEMR, NMEMW, NSMEMR, NSMEMW, POLO, PHI

6.5. AC Characteristics

SIGNAL PATH		PROP DLY (MAX)1	UNIT
D(0:7) from	DATA (0:7)	22	ns
	MDATA (0:7)	20	ns
	ADR0	30	ns
	NBUFDIS	30	ns
	NONBRD16	30	ns
	NYMEMR	30	ns
	NDEN0	30	ns
	DATA (8:15)	40	ns
	EDATA (0:7)	40	ns
D(8:15) from	DATA (8:15)	22	ns
	MDATA (8:15)	20	ns
	NABHE	30	ns
	NBUFDIS	30	ns
	NONBRD16	30	ns
	NYMEMR	30	ns
	NDEN1	30	ns
	DATA (0:7)	40	ns
	EDATA (0:7)	40	ns
DATA (0:7) from	D(0:7)	22	ns
	D(8:15)	40	ns
	DATA(8:15)	22	ns
	EDATA(0:7)	22	ns
	NSDEN	30	ns
	NDEN0	30	ns
	NINTA	30	ns
	NSELDATA	30	ns
DATA (8:15) from	D (8:15)	22	ns
	DATA (0:7)	22	ns
	NDEN1	30	ns
EDATA (0:7) from	DATA(0:7)	36	ns
	D(0:7)	36	ns
	D (8:15)	36	ns
	NINTA	40	ns
	NSELDATA	40	ns
DATA(8:15) from	D(8:15)	22	ns
	D(8:15)	36	ns
	NINTA	40	ns
	NSELDATA	40	ns
NYMEMW from	NMEMW	33	ns
	NMASTER	40	ns
NYMEMR from	NMEMR	33	ns
	NMASTER	40	ns

Table 6.2 AC CHARACTERISTICS

SIGNAL PATH	PROP DLY (MAX) 1	UNIT
NMEMW from NYMEMW	20	ns
NMASTER	30	ns
NONBRD16	30	ns
NMEMR from NYMEMW	20	ns
NMASTER	30	ns
NONBRD16	30	ns
NSMEMW from NYMEMW	20	ns
NMASTER	30	ns
NONBRD16	30	ns
NSMEMR from NYMEMW	20	ns
NMASTER	30	ns
NONBRD16	30	ns
PERROR from MDATA(0:15)	40	ns
PLO	40	ns
PHI	40	ns
ADR0	40	ns
NABHE	40	ns
POLO from D(0:7)	35	ns
POHI from D(8:15)	35	ns

Table 6.2 AC CHARACTERISTICS (CONT.)

Notes: 1. Prop delays are for 75pf load. Add 8nS for 200pf load.

6.6 PC/AT Data Bus Cycles

This description of the data bus cycles of the FE3600 PC/AT expansion bus includes CPU, DMA, and MASTER cycles. The data portion of the PC/AT expansion bus is a 16 bit wide bus divided into two bytes. In general, the low byte (DATA[0:7]) is accessed during cycles in which the address is even. The high byte (DATA[8:15]) is accessed when the address is odd. During 16 bit operations, both low and high bytes are accessed. There are several combinations of byte wide, word wide, even and odd addressing. Each of these combinations present a unique pattern of bus buffer enables and directions. These data buffer control states are described in this document.

NOTES:

* *Eight bit devices on the PC/AT bus are always on the low byte (DATA[0:7]) of the expansion bus regardless of address. Sixteen bit devices use ADR0 and NEBHE to distinguish between high and low byte transfers.*
* *In previous designs, the data buffers on the PC/AT were inactive during DMA. This was due to the on board DRAM being on the system bus. Now that the DRAM is on the 286 local bus the data buffers must be enabled and directed during DMA operations.*
* *A block diagram of the data bus hardware on the PC/AT board is shown in Figure 6.4. It represents the equivalent 74LSXXX circuitry for the data buffers contained on the board. Signals used in this document are discussed in Table 6.4.*

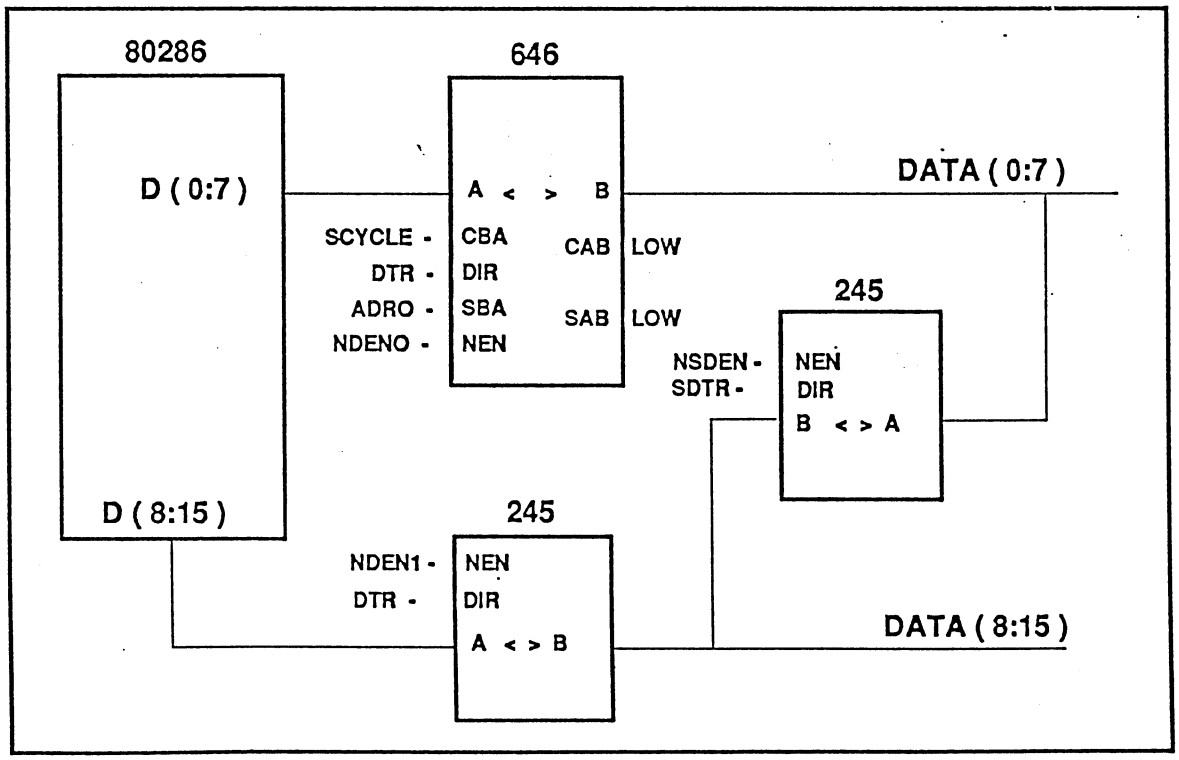


Figure 6.3 PC/AT DATA BUS ARCHITECTURE

'646				
NEN NDEN0	DIR DTR	CBA SCYCLE	SBA ADR0	OPERATION
X	X	^	X	LATCH B DATA
0	0	X	0	A <------B (REAL TIME)
0	0	X	1	A <------B (LATCHED DATA)
0	1	X	X	A ------>B (REAL TIME)
1	X	X	X	BUFFERS DISABLED

'245	
DIR	OPERATION
0	A <---------- B
1	A ----------> B

COMMAND SIGNALS	DEFINITIONS
S0, S1	BUS CYCLE STATUS FROM 286
NMEMR	SYSTEM MEMORY READ
NMEMW	SYSTEM MEMORY WRITE
NIOR	SYSTEM I/O READ
NIOW	SYSTEM I/O WRITE
NNPCS	NUMERIC PROCESSOR CHIP SELECT
A0	ADDRESS BIT 0 FROM 286
NBHE	BUS HIGH ENABLE FROM 286
HLDA	HOLD ACKNOWLEDGE FROM 286
HLDA1	DMA HOLD ACKNOWLEDGE FROM DMA CONTROLLER
NPROMSL	BIOS DECODE FROM MEMORY/IO DECODER
NONBRD	ON BOARD DRAM OR I/O DECODE
NIOCS16	16 BIT I/O DEVICE DECODE FROM EXPANSION BUS
NMEMCS16	16 BIT MEMORY DEVICE DECODE FROM EXPANSION BUS
NMASTER	BUS CONTROL SIGNAL FROM BUS MASTER
CONTROL SIGNALS	**DEFINITIONS**
DTR	DATA TRANSMIT/RECEIVE
NDEN0	LOW BYTE DATA ENABLE
NDEN1	HIGH BYTE DATA ENABLE
NSDEN	BYTE SWAP BUFFER ENABLE
SCYCLE	LOW BYTE DATA LATCH
SDTR	BYTE SWAP BUFFER TRANSMIT/RECEIVE
ADR0	SYSTEM ADDRESS BIT 0

Table 6.3 SIGNAL DEFINITIONS

6.7. CPU Cycles

The following cycles represent data cycles under CPU control for all devices excluding the on board DRAM and the 80287 Math Co-Processor. Since the 80287 and on board DRAM are on the local bus, the data bus drivers for the expansion bus will be disabled. This is accomplished by setting NDEN0, NDEN1 and NSDEN = 1 when NONBRD + /MNIO = 0 or NNPCS = 0. Note that on board I/O is indicated by NONBRD + MNIO = 0. On board I/O devices are on the system bus.

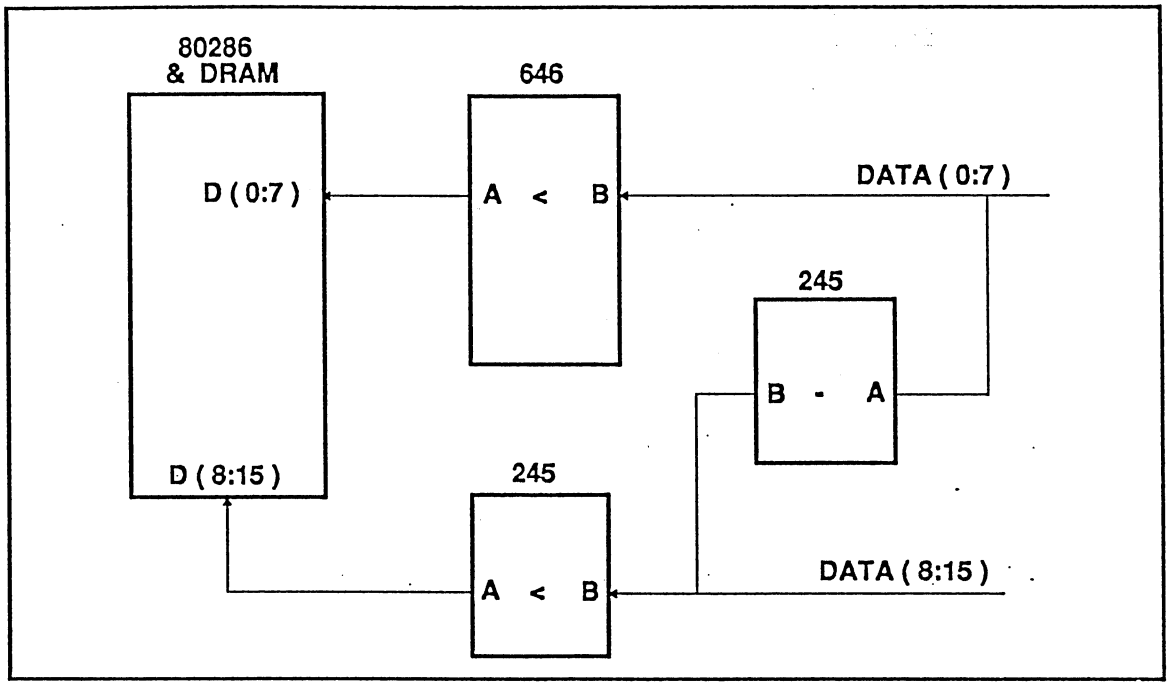
The following cycles are described in this section.

6.7.1 16 bit transfer, read from 16 bit device
6.7.2 16 bit transfer, write to 16 bit device
6.7.3 16 bit transfer, read from 8 bit device
6.7.4 16 bit transfer, write to 8 bit device
6.7.5 8 bit transfer, low byte read from 8 or 16 bit device
6.7.6 8 bit transfer, low byte write to 8 or 16 bit device
6.7.7 8 bit transfer, high byte read from 8 bit device
6.7.8 8 bit transfer, high byte write to 8 bit device
6.7.9 8 bit transfer, high byte read from 16 bit device
6.7.10 8 bit transfer, high byte write to 16 bit device

For all CPU cycles HLDA=0 and NINTA=1. In the following tables, NCS16 indicates that there is a 16 bit device on the expansion bus. The boolean equation for NCS16 is:

NCS16 = NPROMCS * (NIOCS16 + MNIO) * (NMEMCS16 + /MNIO)

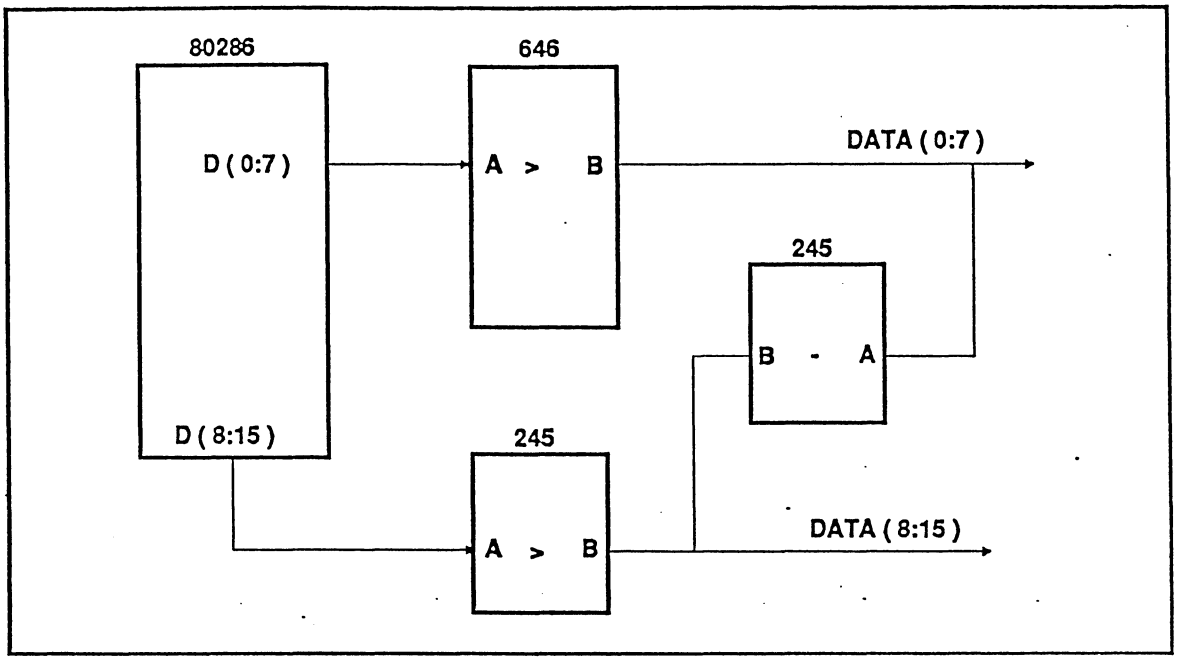
6.7.1 16 bit read from 16 bit device



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
NBHE	0
NCS16	0

CONTROL SIGNALS	STATE
DTR	0
NDENO	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X
ADRO	0

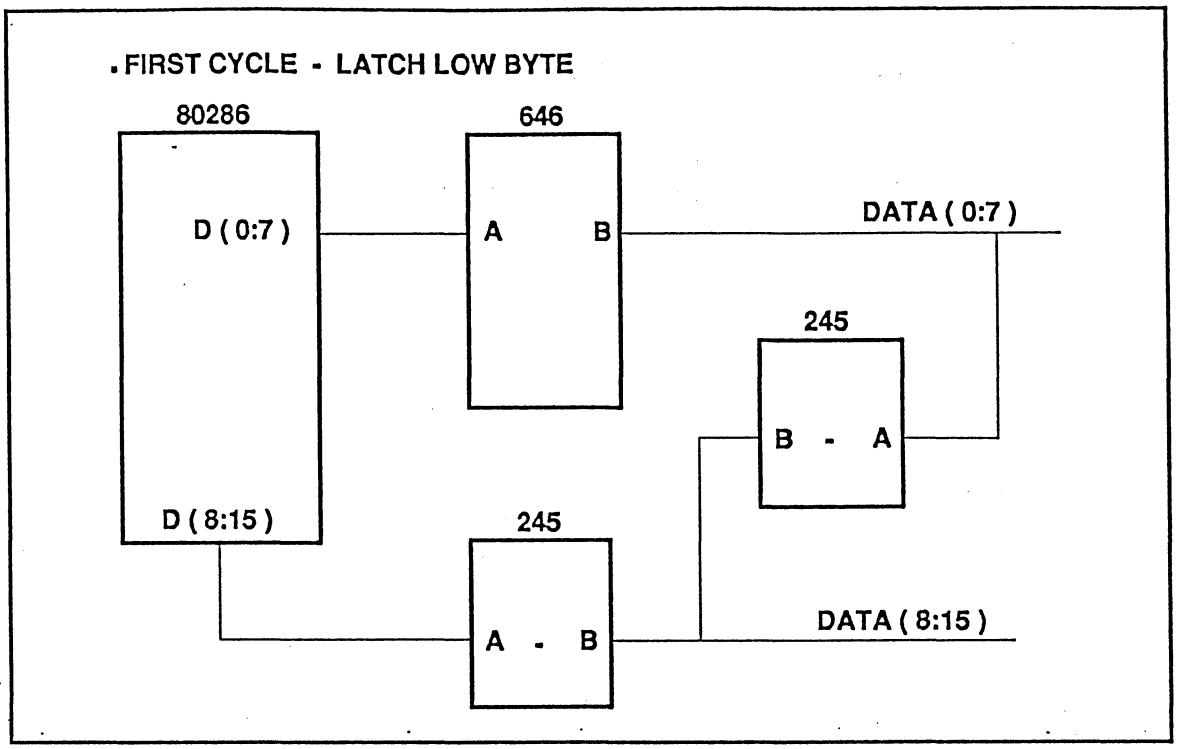
6.7.2 16 bit write to 16 bit device



INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
NBHE	0
NCS16	0

CONTROL SIGNALS	STATE
DTR	1
NDENO	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X
ADRO	0

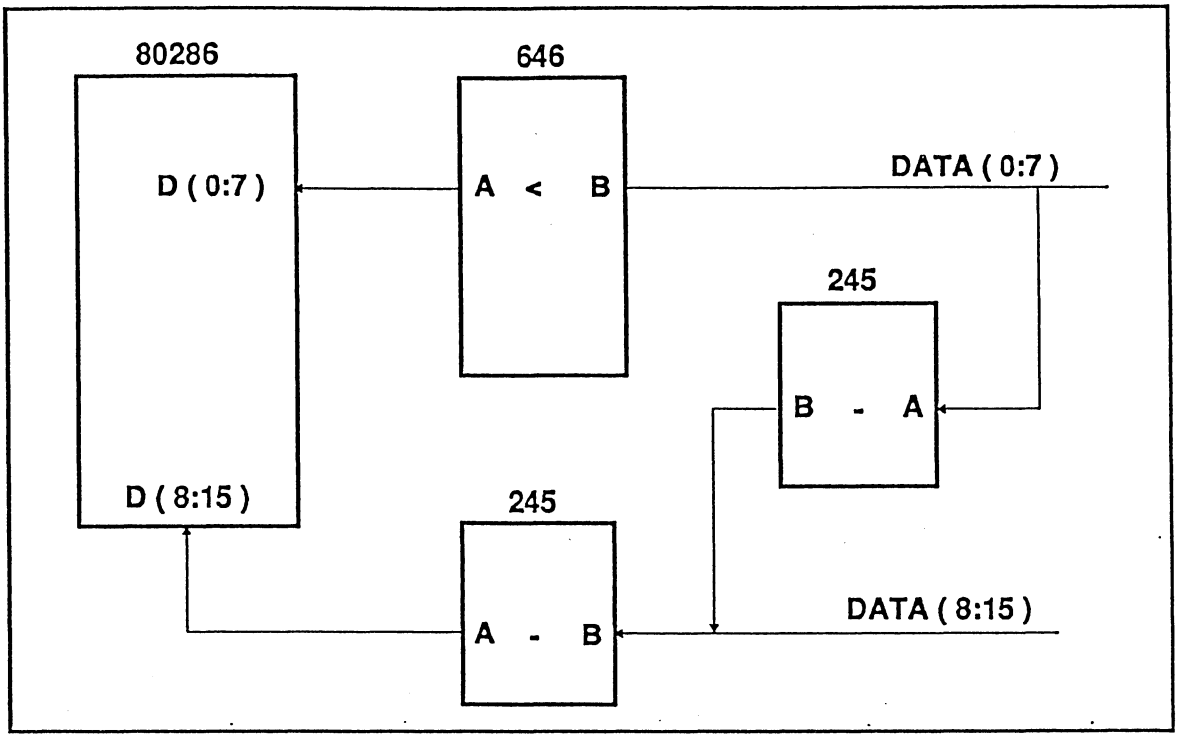
6.7.3 16 bit read from 8 bit device



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
NBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	X
NDEN0	X
NDEN1	X
NSDEN	1
SCYCLE	^
SDTR	X
ADR0	0

* *Second cycle - Enable latched low byte to 286 low byte and enable bus low byte to 286 high byte.*



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
NBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	0
NDEN0	0
NDEN1	0
NSDEN	0
SCYCLE	X*
SDTR	1
ADRO	1

* SCYCLE must not change from low to high during the cycle.

6.7.4 16 bit write to 8 bit device

INPUT SIGNALS	STATE
S1	1
S0	0
A0	0
NBHE	0
NCS16	1

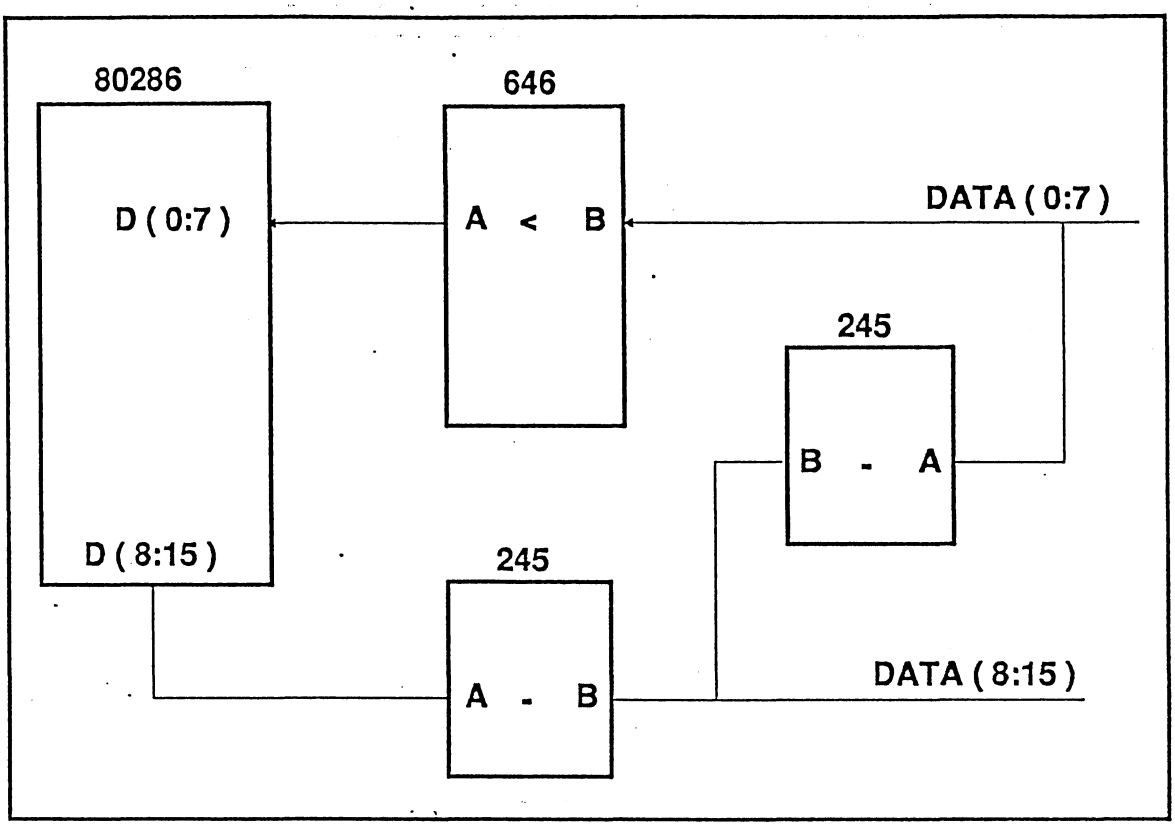
- First cycle

- 8 bit, low byte write to 8 bit device or 16 bit device
- ADR0 is driven low during this cycle
- NEBHE is driven high during this cycle

- Second cycle

- 8 bit, high byte write to 8 bit device
- ADR0 is driven high during this cycle
- NEBHE is driven low during this cycle

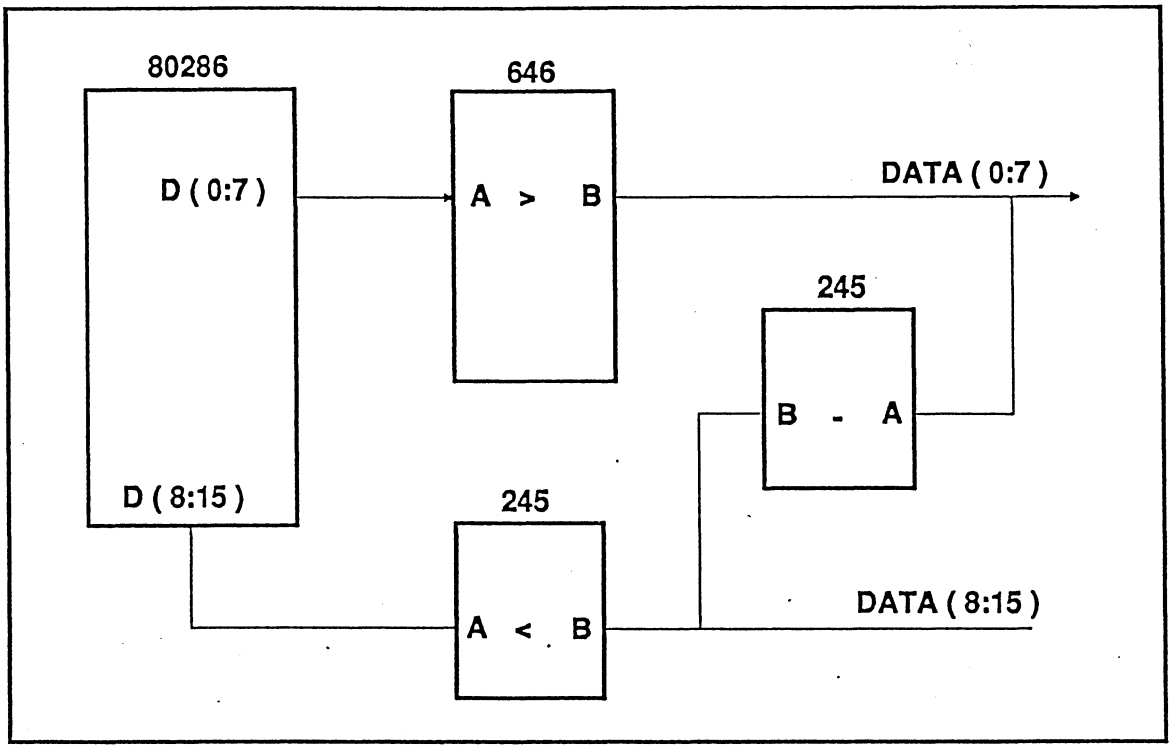
6.7.5 8 bit, low byte read from 8 bit device or 16 bit device



INPUT SIGNALS	STATE
S1	0
S0	1
A0	0
NBHE	1
NCS16	X

CONTROL SIGNALS	STATE
DTR	0
NDEN0	0
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X
ADR0	0

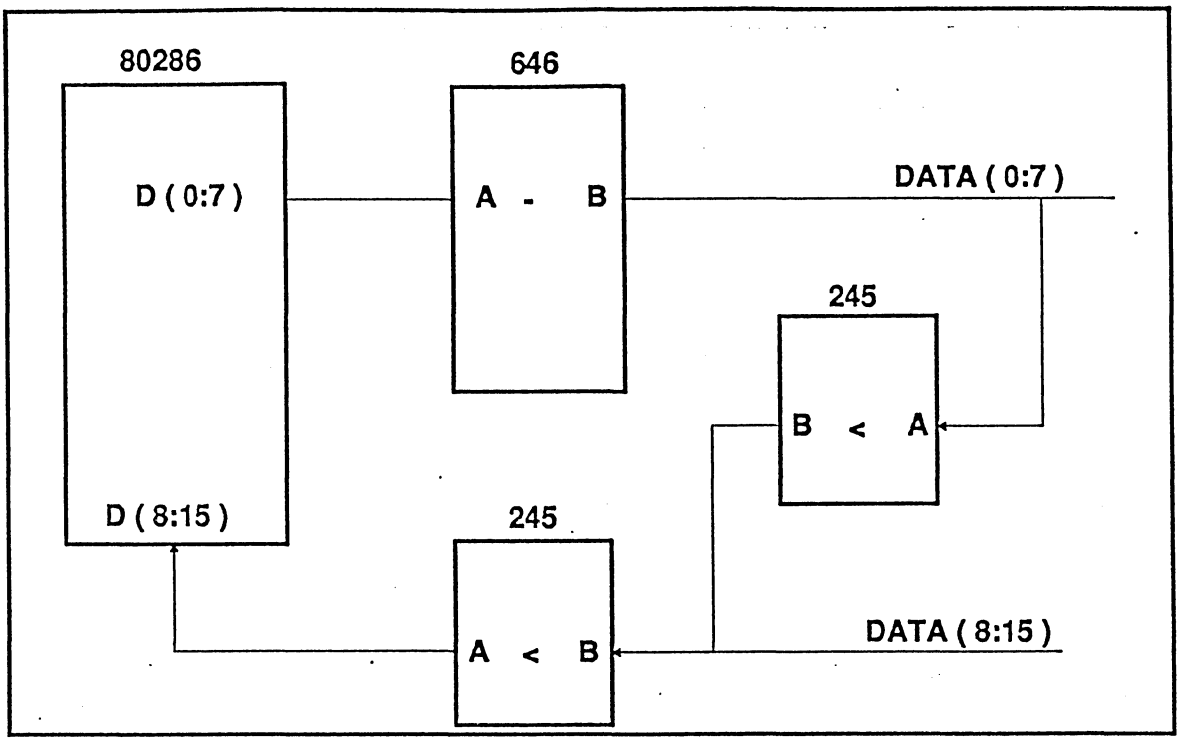
6.7.6 8 bit, low byte write to 8 bit device or 16 bit device



INPUT SIGNALS	STATE
S1	1
A0	0
NBHE	1
NCS16	X

CONTROL SIGNALS	STATE
DTR	1
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X
ADR0	0

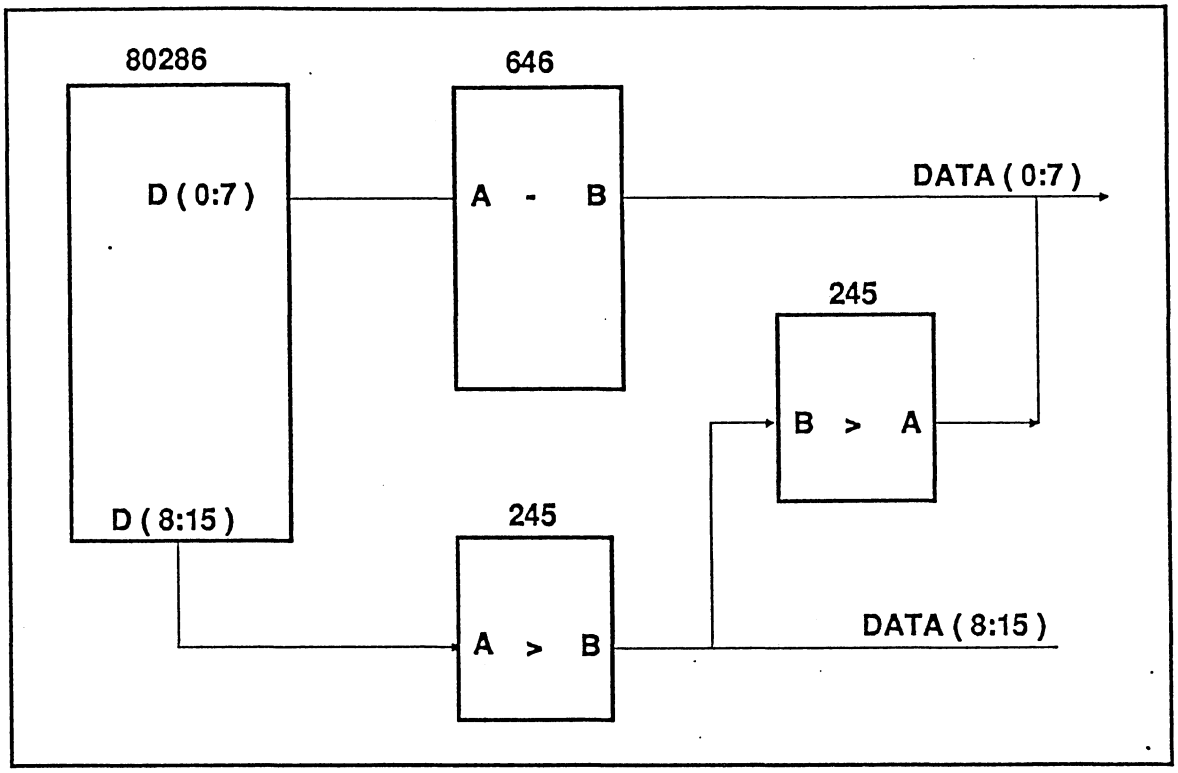
6.7.7 8 bit, high byte read from 8 bit device



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
NBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	0
NDEN0	1
NDEN1	0
NSDEN	0
SCYCLE	X
SDTR	1
ADR0	1

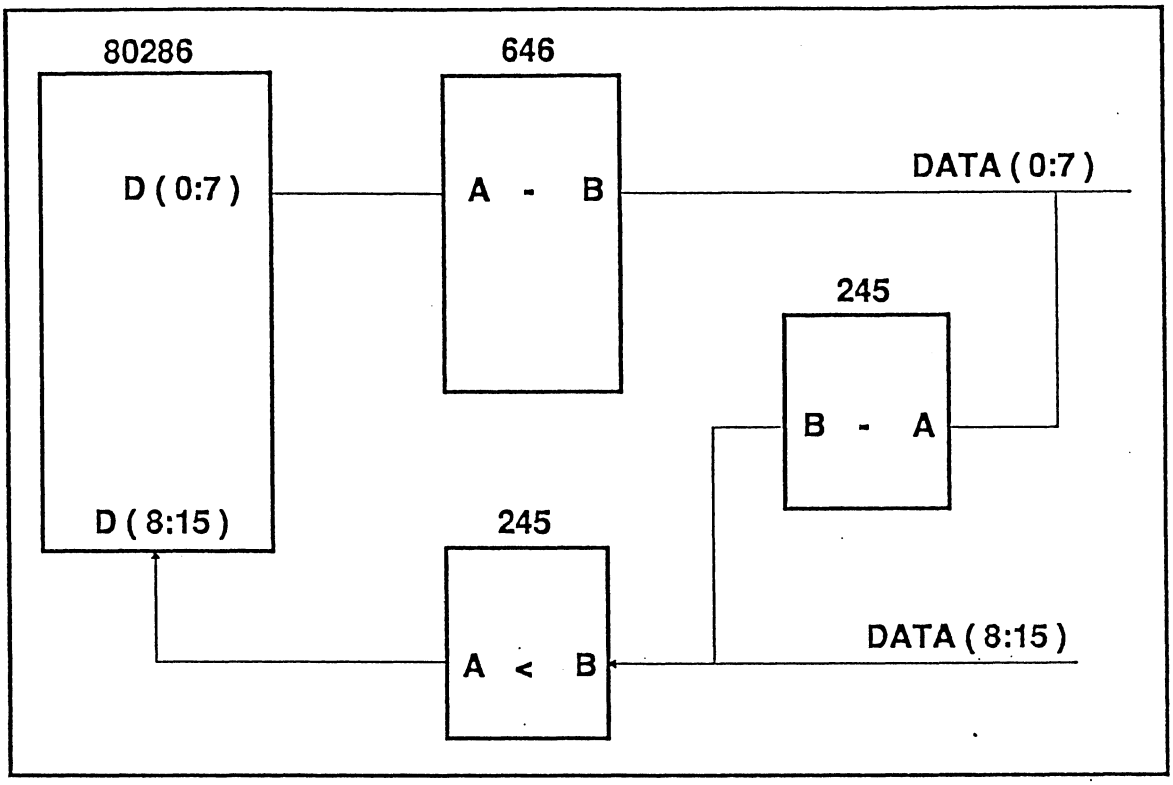
6.7.8 8 bit, high byte write to 8 bit device



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
NBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	1
NDEN0	1
NDEN1	0
NSDEN	0
SCYCLE	X
SDTR	0
ADR0	1

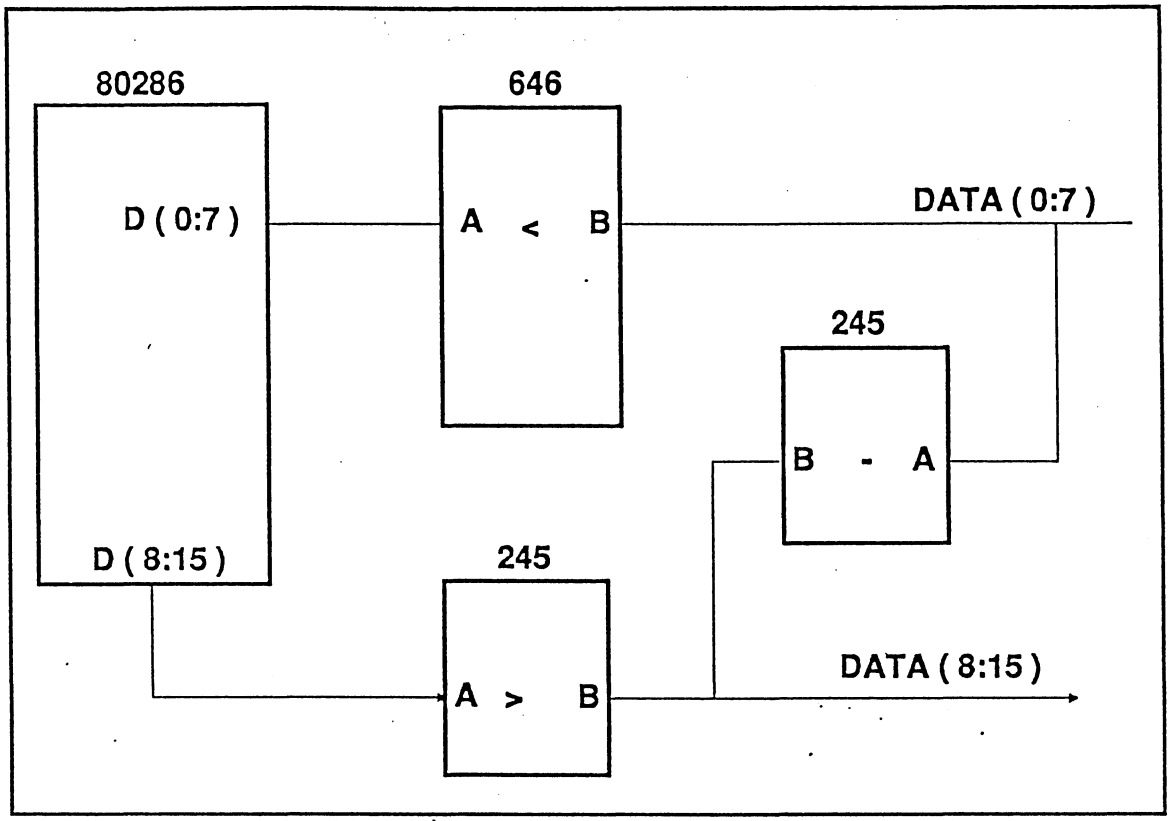
6.7.9 8 bit, high byte read from 16 bit device



INPUT SIGNALS	STATE
S1	0
S0	1
A0	1
NBHE	0
NCS16	0

CONTROL SIGNALS	STATE
DTR	0
NDEN0	1
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X
ADR0	1

6.7.10 8 bit, high byte write to 16 bit device



INPUT SIGNALS	STATE
S1	1
S0	0
A0	1
NBHE	0
NCS16	0

CONTROL SIGNALS	STATE
DTR	1
NDEN0	1
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X
ADR0	1

6.8 DMA Cycles

The following cycles represent data cycles under DMA control for all devices. DMA may be for on board DRAM (NONBRD=0) or system memory (NONBRD=1). Note that NONBRD decode for on board I/O will be disabled during DMA.

The following DMA cycles are described in this section.

- **For on board DRAM (NONBRD = 0)**

6.8.1 8 bit DMA from even memory address to 8 bit I/O device.
6.8.2 8 bit DMA to even memory address from 8 bit I/O device.
6.8.3 8 bit DMA from odd memory address to 8 bit I/O device.
6.8.48 bit DMA to odd memory address from 8 bit I/O device.
6.8.5 16 bit DMA from memory to 16 bit I/O.
6.8.6 16 bit DMA to memory from 16 bit I/O.

- **For system memory (NONBRD = 1)**

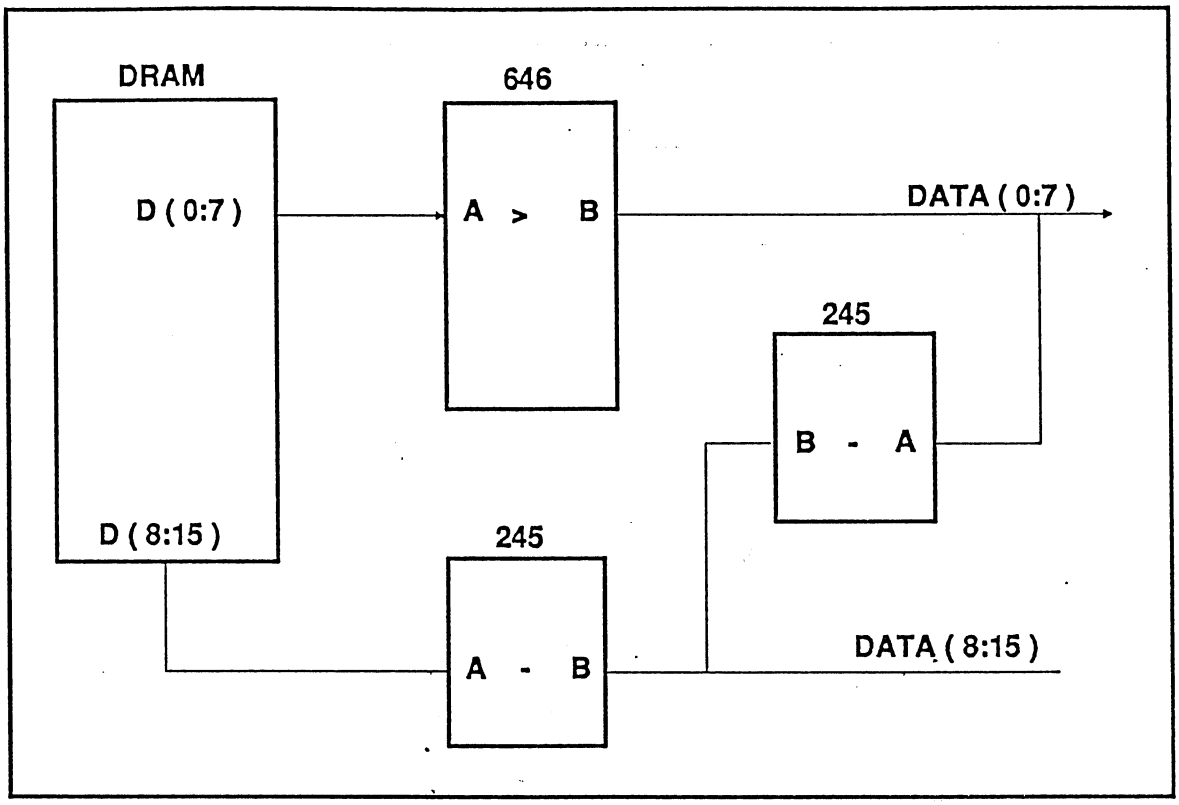
6.8.7 8 bit DMA from 16 bit memory, odd address to 8 bit I/O device.
6.8.8 8 bit DMA to 16 bit memory, odd address from 8 bit I/O device.

- **For all other DMA cycles the data buffers are disabled.**

6.8.9 All other DMA cycles.

For all DMA cycles HLDA=1, HLDA1=1 and NMASTER=1.

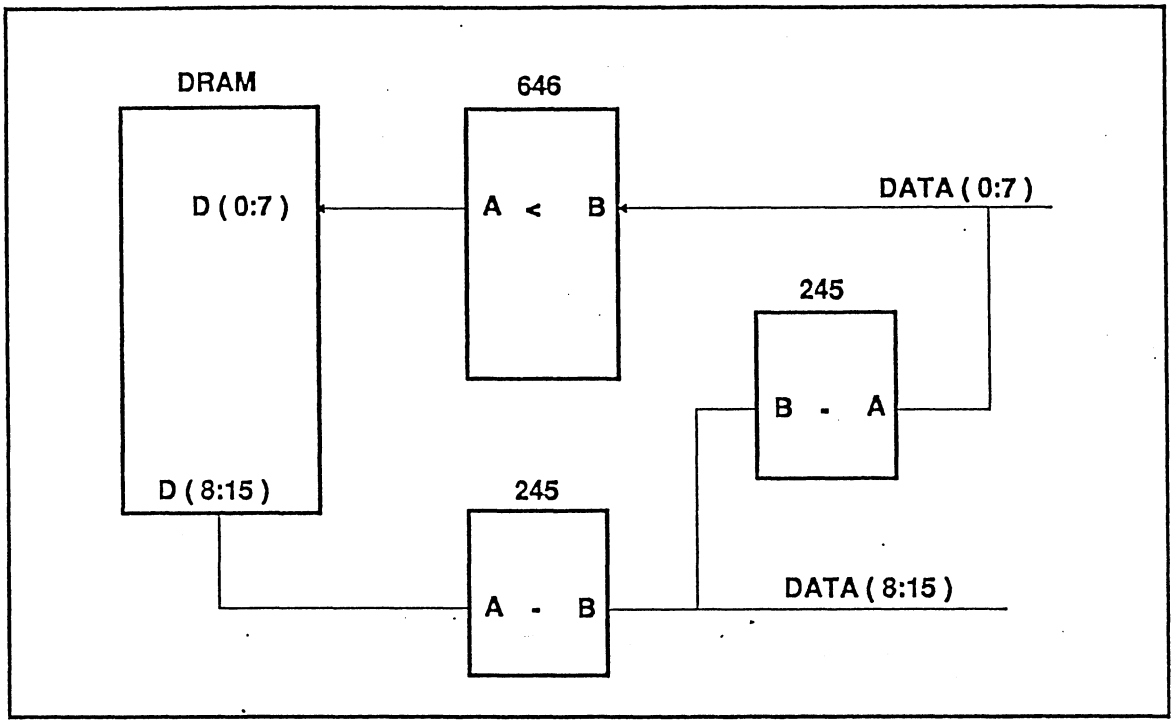
6.8.1 8 bit DMA transfer from even memory address to 8 bit I/O device



INPUT SIGNALS	STATE
NDMAMR	0
NMEMW	1
NIOR	1
NIOW	0
ADR0	0
NEBHE	1

CONTROL SIGNALS	STATE
DTR	1
NDEN0	0
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X

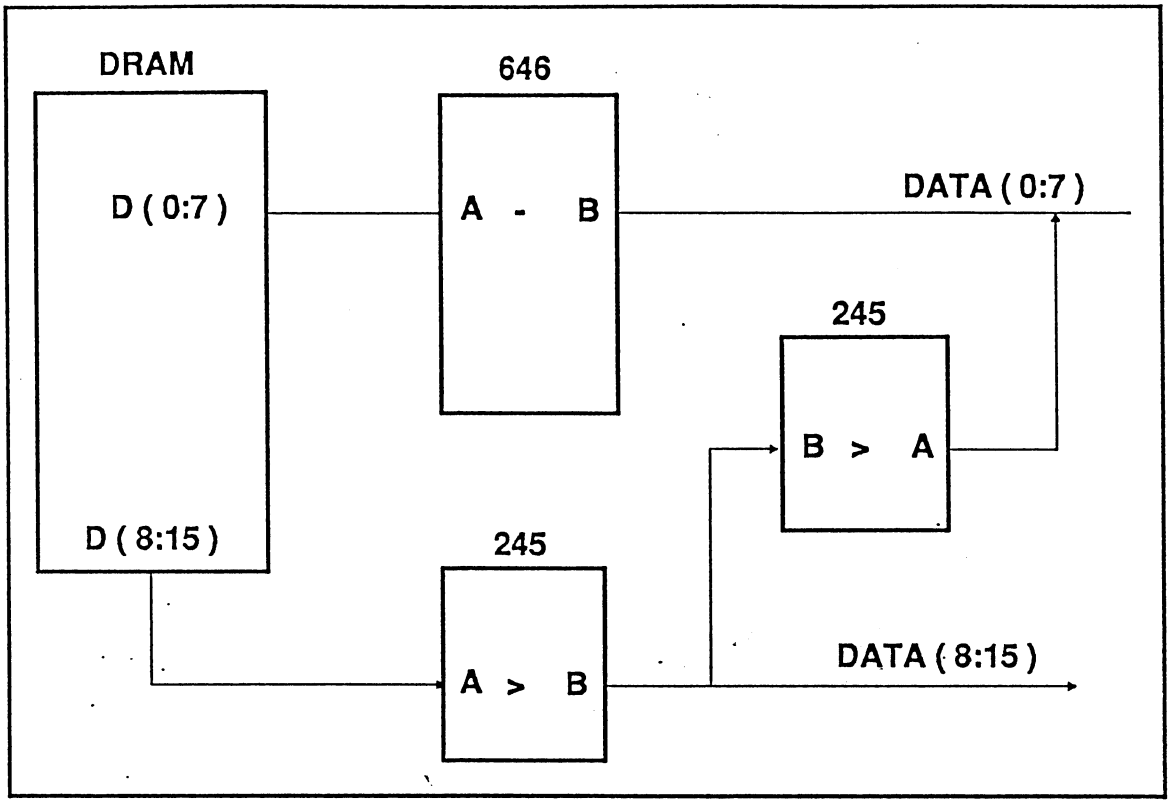
6.8.2 8 bit DMA transfer to even memory address from 8 bit I/O device



INPUT SIGNALS	STATE
NDMAMR	1
NMEMW	0
NIOR	0
NIOW	1
ADR0	0
NEBHE	1

CONTROL SIGNALS	STATE
DTR	0
NDEN0	0
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X

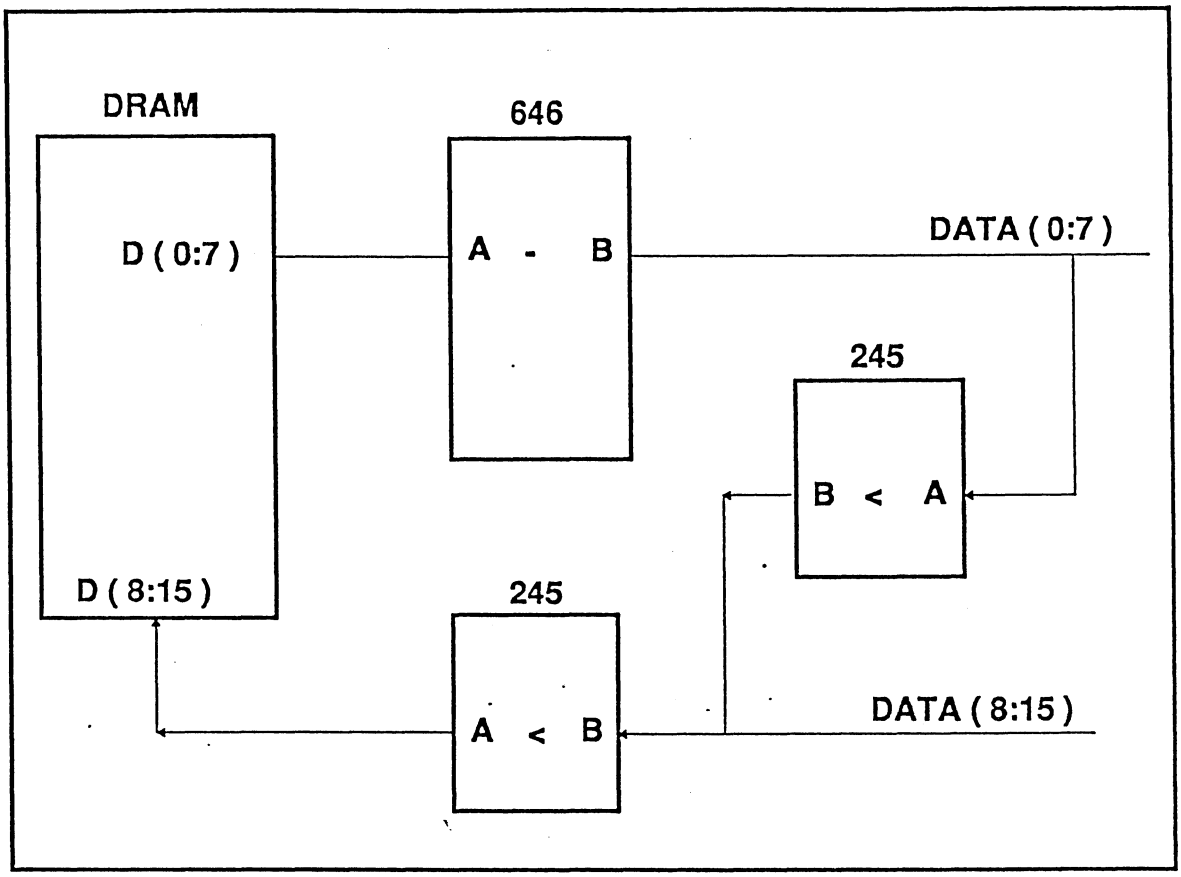
6.8.3 8 bit DMA transfer from odd memory address to 8 bit I/O device



INPUT SIGNALS	STATE
NDMAMR	0
NMEMW	1
NIOR	1
NIOW	0
ADR0	1
NEBHE	0

CONTROL SIGNALS	STATE
DTR	1
NDEN0	1
NDEN1	0
NSDEN	0
SCYCLE	X
SDTR	0

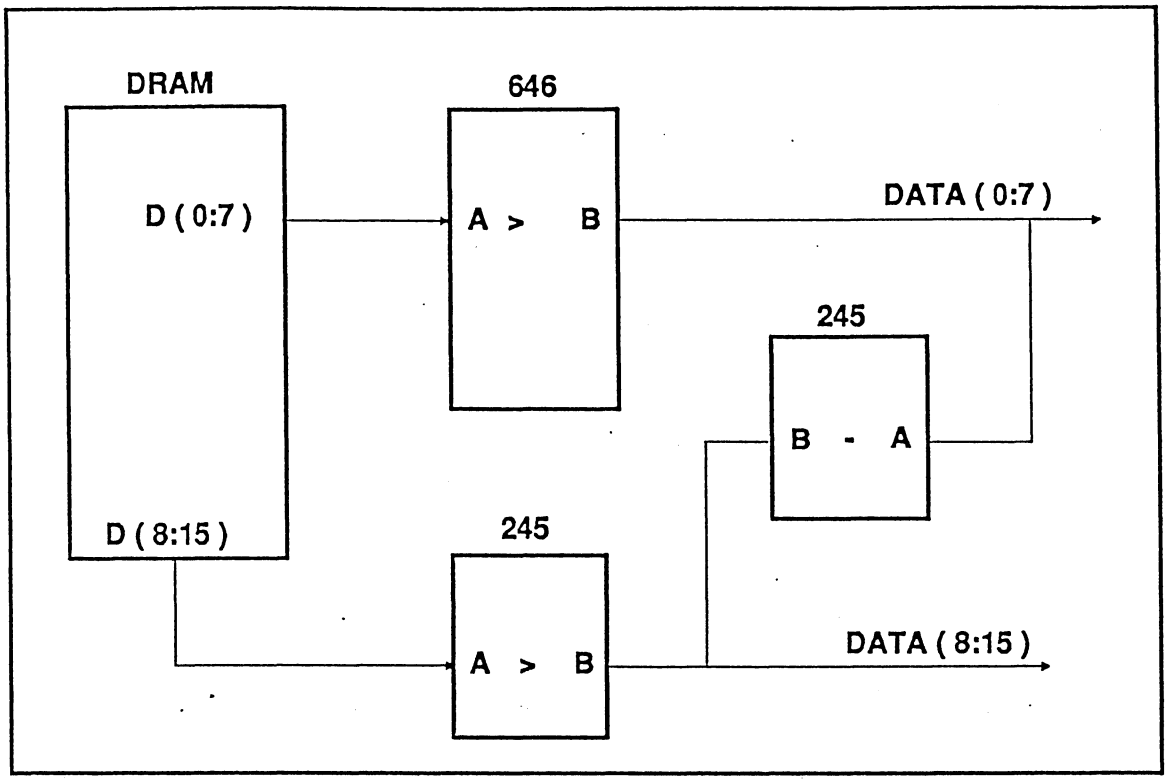
6.8.4 8 bit DMA transfer to odd memory address from 8 bit I/O device



INPUT SIGNALS	STATE
NDMAMR	1
NMEMW	0
NIOR	0
NIOW	1
ADR0	1
NEBHE	0

CONTROL SIGNALS	STATE
DTR	0
NDEN0	1
NDEN1	0
NSDEN	0
SCYCLE	X
SDTR	1

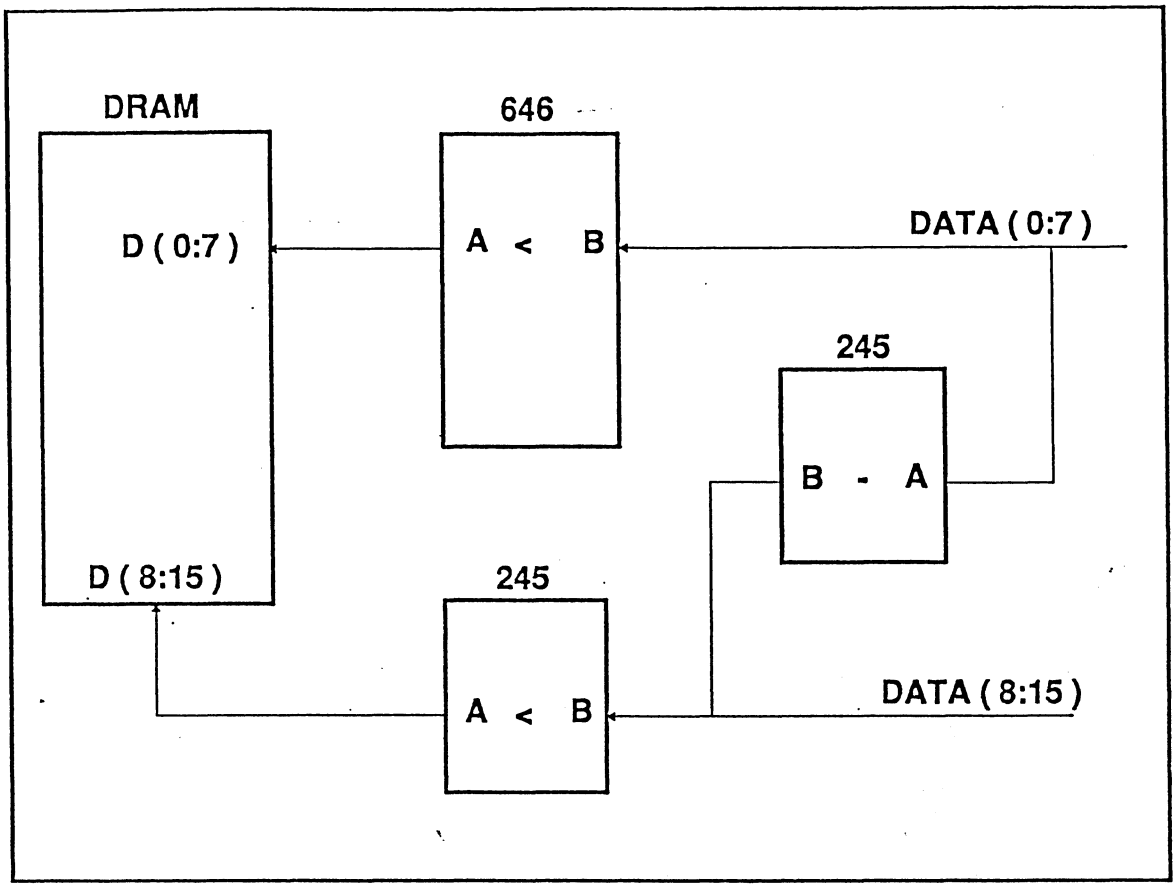
6.8.5 16 bit DMA transfer from memory to 16 bit I/O



INPUT SIGNALS	STATE
NDMAMR	0
NMEMW	1
NIOR	1
NIOW	0
ADR0	0
NEBHE	0

CONTROL SIGNALS	STATE
DTR	1
NDEN0	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

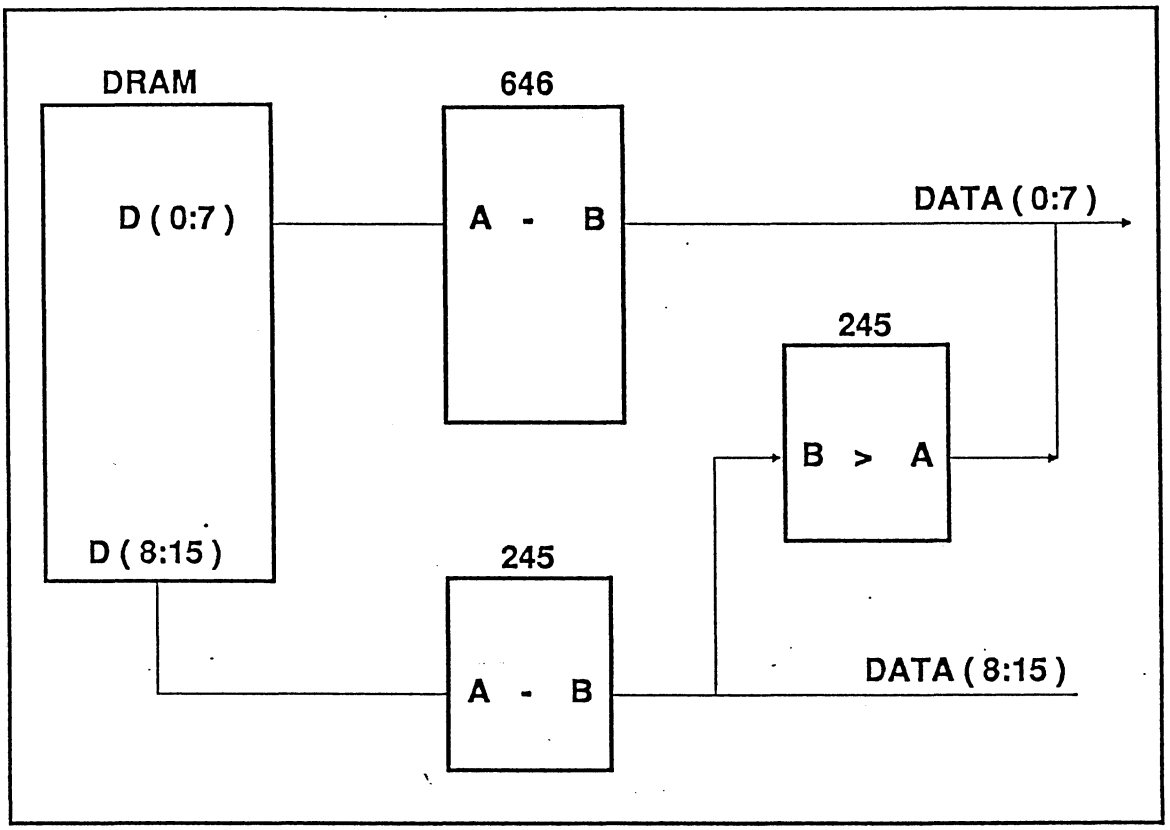
6.8.6 16 bit DMA transfer to memory from 16 bit I/O



INPUT SIGNALS	STATE
NDMAMR	1
NMEMW	0
NIOR	0
NIOW	1
ADR0	0
NEBHE	0

CONTROL SIGNALS	STATE
DTR	0
NDEN0	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

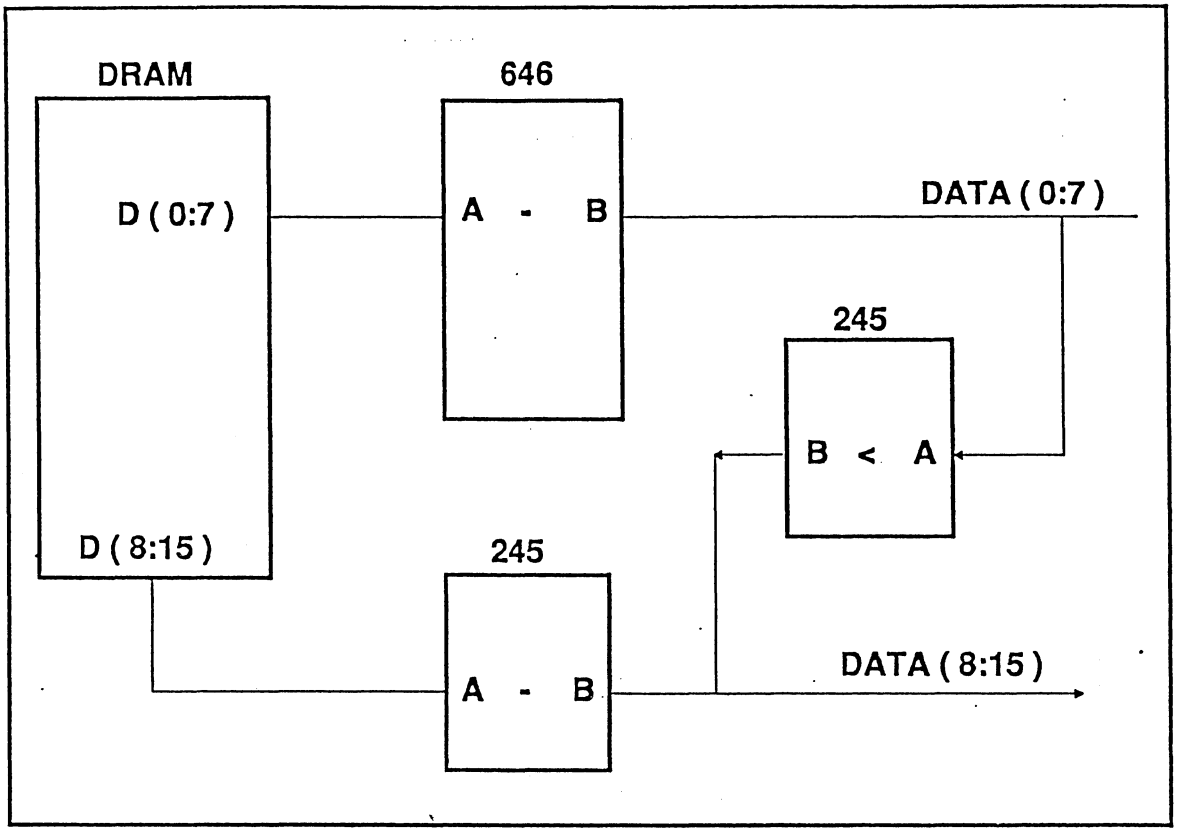
6.8.7 8 bit DMA from 16 bit memory, odd address to 8 bit I/O device.



INPUT SIGNALS	STATE
NDMAMR	0
NMEMW	1
NIOR	1
NIOW	0
ADR0	1
NEBHE	0
NMEMCS16 * NPROMSL	0

CONTROL SIGNALS	STATE
DTR	X
NDEN0	1
NDEN1	1
NSDEN	0
SCYCLE	X
SDTR	0

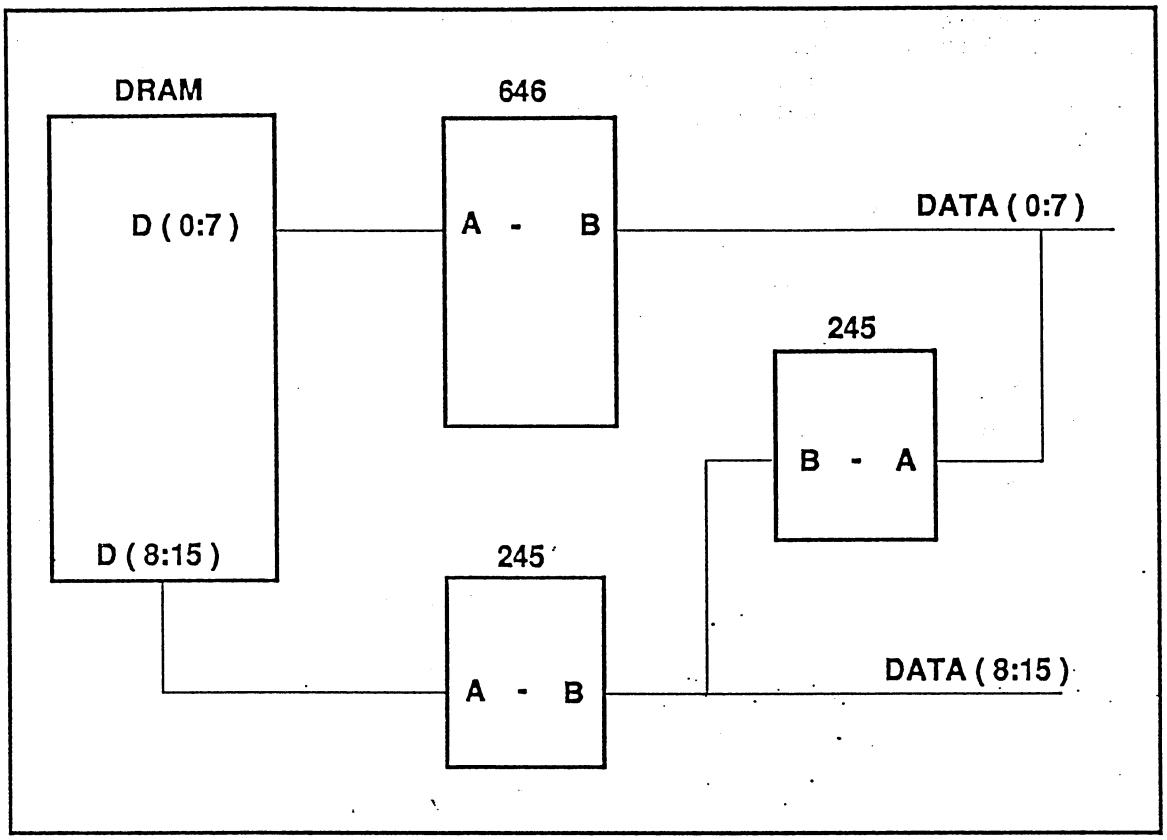
6.8.8 8 bit DMA to 16 bit memory, odd address from 8 bit I/O device



INPUT SIGNALS	STATE
NDMAMR	1
NMEMW	0
NIOR	0
NIOW	1
ADR0	1
NEBHE	0
NMEMCS16 * NPROMSL	0

CONTROL SIGNALS	STATE
DTR	X
NDEN0	1
NDEN1	1
NSDEN	0
SCYCLE	X
SDTR	1

6.8.9 All other DMA cycles (data buffers disabled).



INPUT SIGNALS	STATE
NDMAMR	
NMEMW	
NIOR	
NIOW	
ADR0	
NEBHE	

CONTROL SIGNALS	STATE
DTR	X
NDEN0	1
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X

6.9 Bus Master Cycles

The following cycles represent data cycles under the control of a bus master other than the 80286 or DMA controller. This condition is indicated by hold acknowledge active (HLDA=1) and bus master asserted (NMASTER=0). It is assumed that the bus master is always a 16 bit device. On board DRAM and On board I/O are distinguished by the memory or I/O read/write commands.

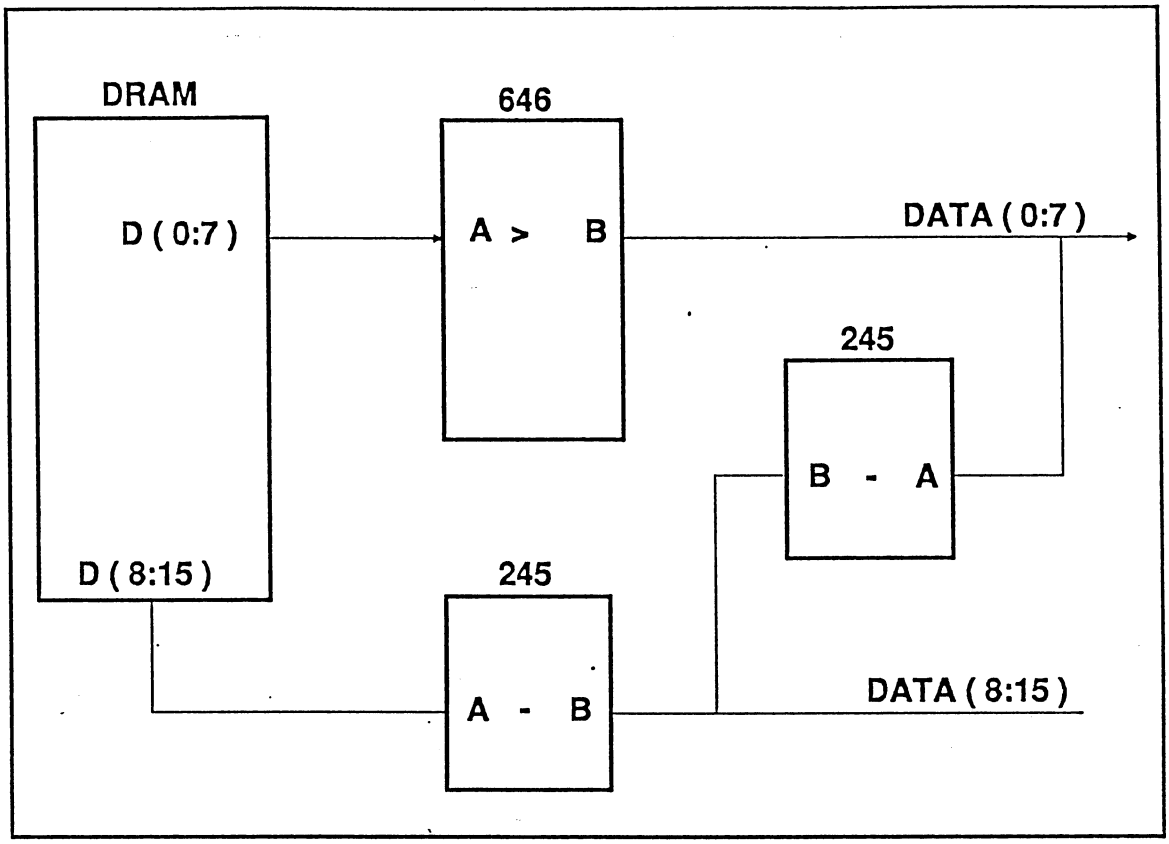
- For on board DRAM

6.9.1 8 bit transfer low byte read from memory
6.9.2 8 bit transfer low byte write to memory
6.9.3 8 bit transfer high byte read from memory
6.9.4 8 bit transfer high byte write to memory
6.9.5 16 bit transfer read from memory
6.9.6 16 bit transfer write to memory

- For system memory and I/O

6.9.7 8 bit transfer high byte read from 8 bit system memory or I/O
6.9.8 8 bit transfer high byte write to 8 bit system memory or I/O

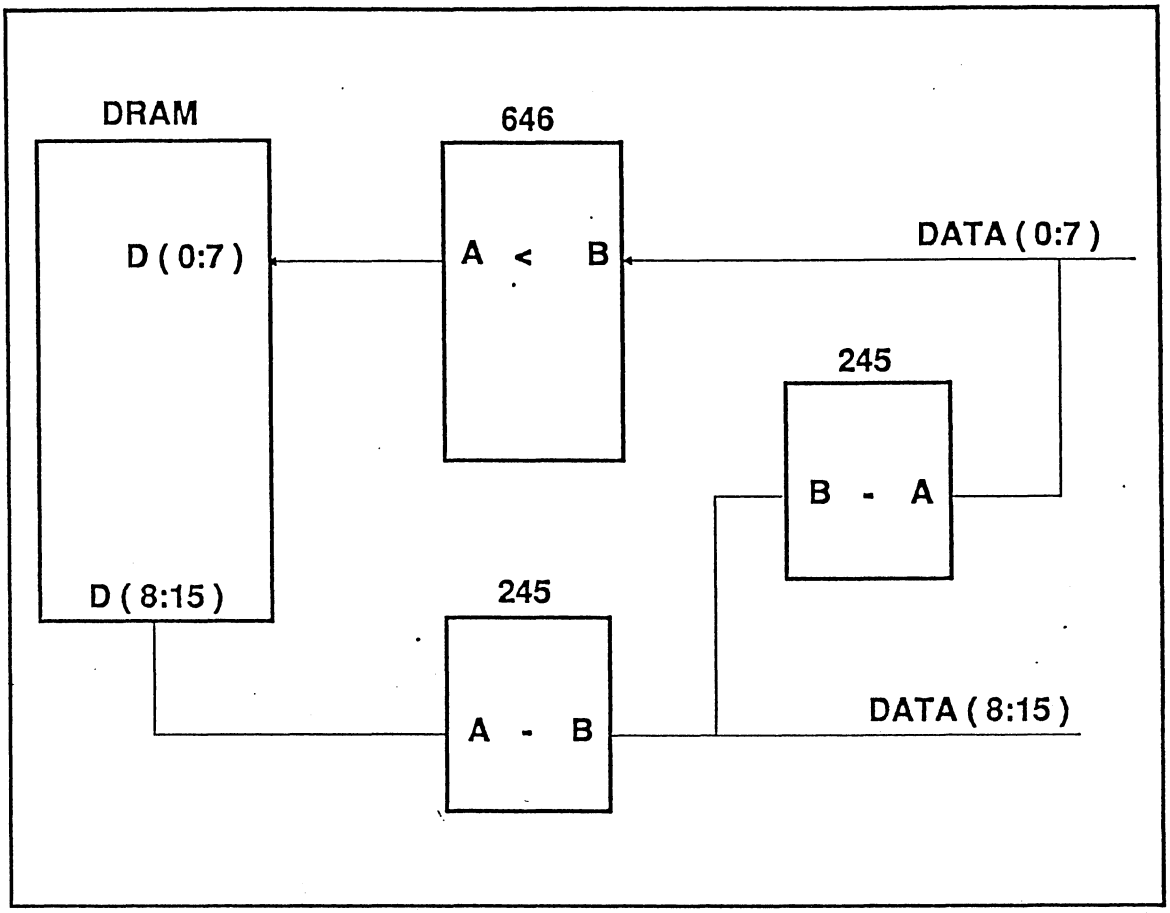
6.9.1 8 bit low byte read from memory



INPUT SIGNALS	STATE
NMEMR	0
NMEMW	1
ADR0	0
NEBHE	1
NCS16	1

CONTROL SIGNALS	STATE
DTR	1
NDEN0	0
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X

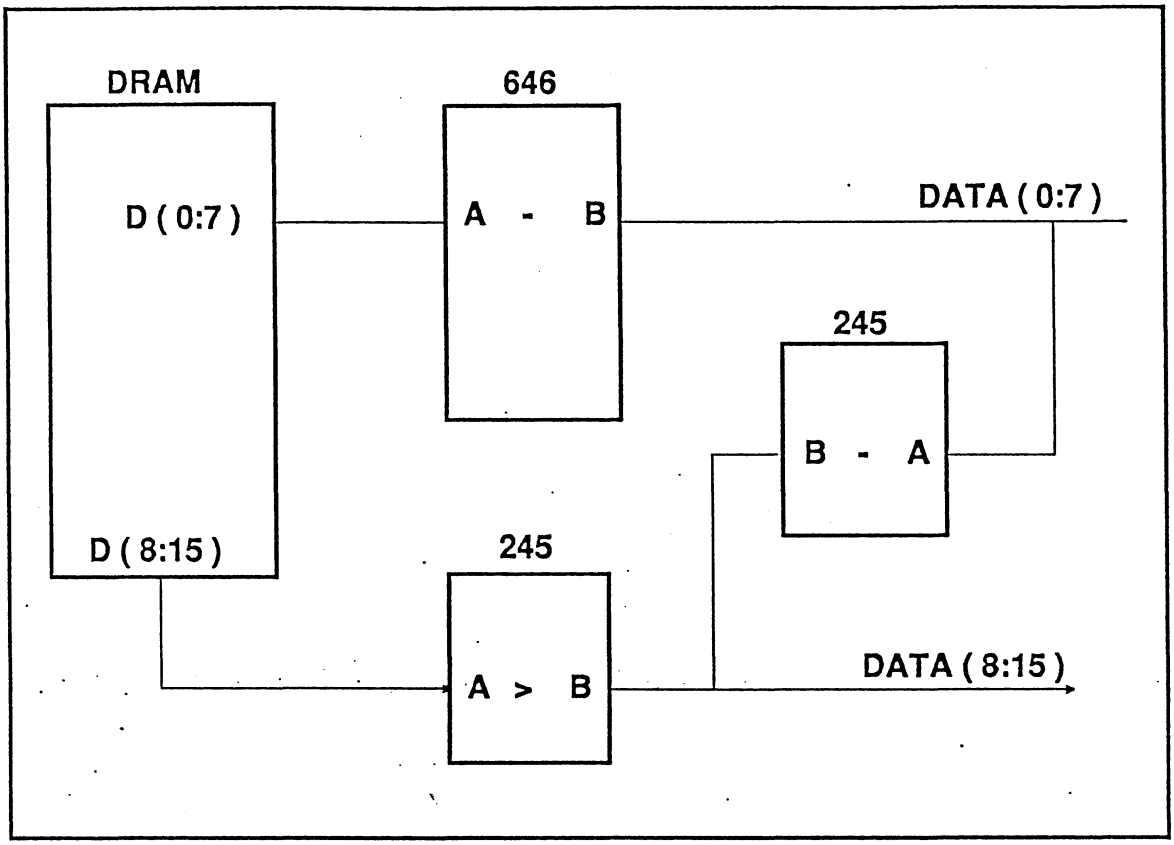
6.9.2 8 bit low byte write to memory



INPUT SIGNALS	STATE
NMEMR	1
NMEMW	0
ADR0	0
NEBHE	1
NCS16	1

CONTROL SIGNALS	STATE
DTR	0
NDENO	0
NDEN1	1
NSDEN	1
SCYCLE	X
SDTR	X

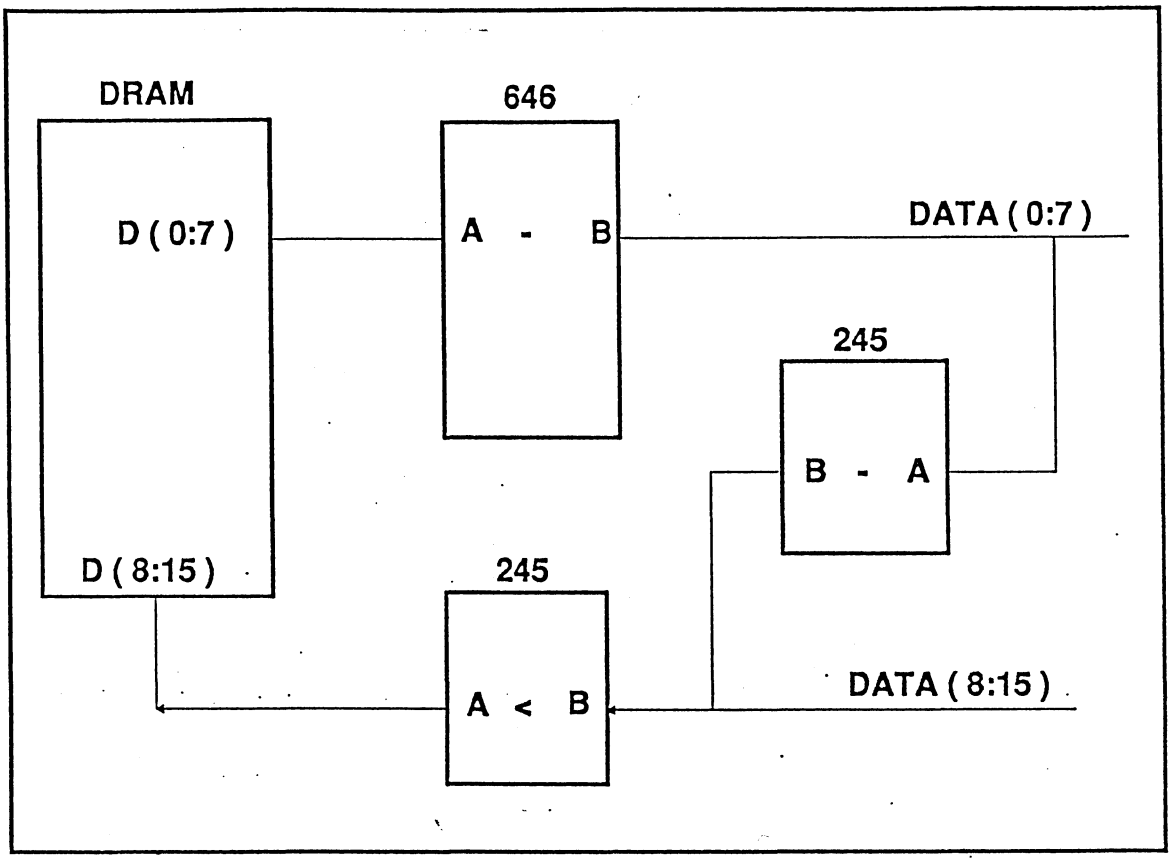
6.9.3 8 bit high byte read from memory



INPUT SIGNALS	STATE
NMEMR	0
NMEMW	1
ADR0	1
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	1
NDEN0	1
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

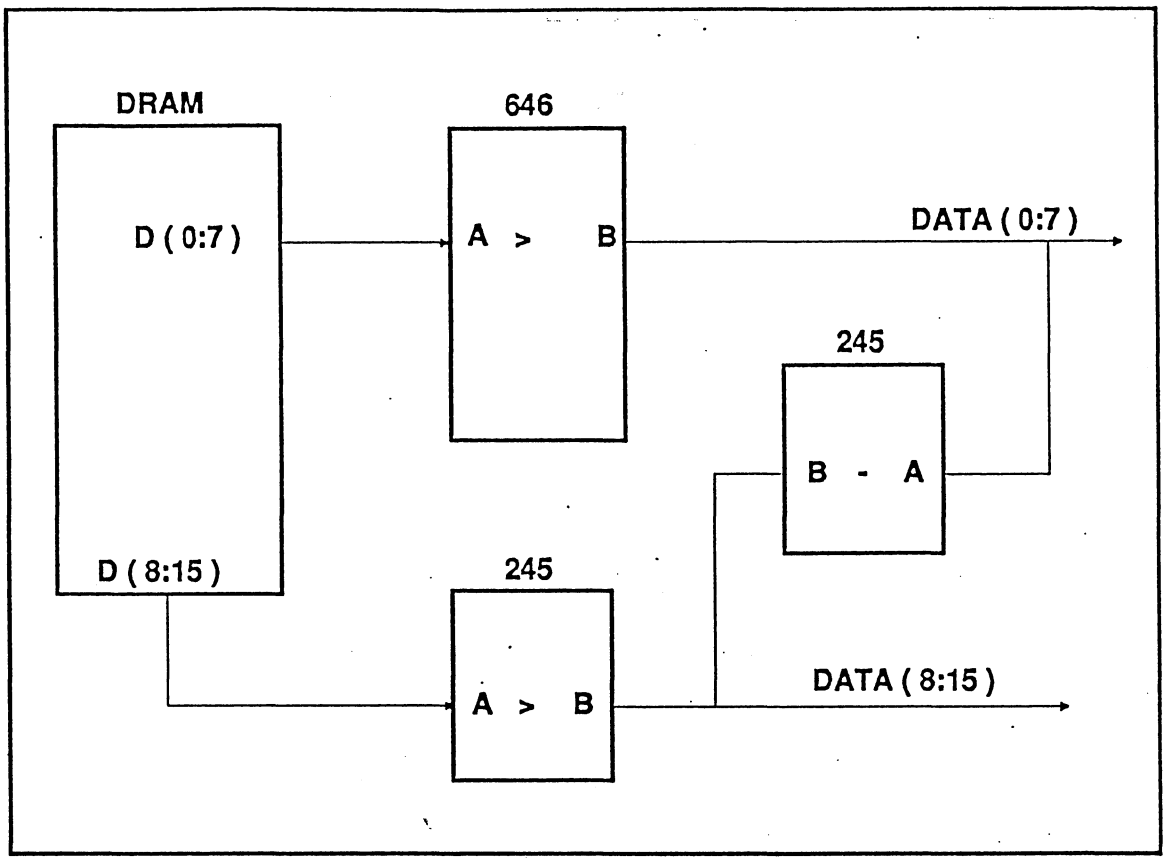
6.9.4 8 bit high byte write to memory



INPUT SIGNALS	STATE
NMEMR	1
NMEMW	0
ADR0	1
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	0
NDEN0	1
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

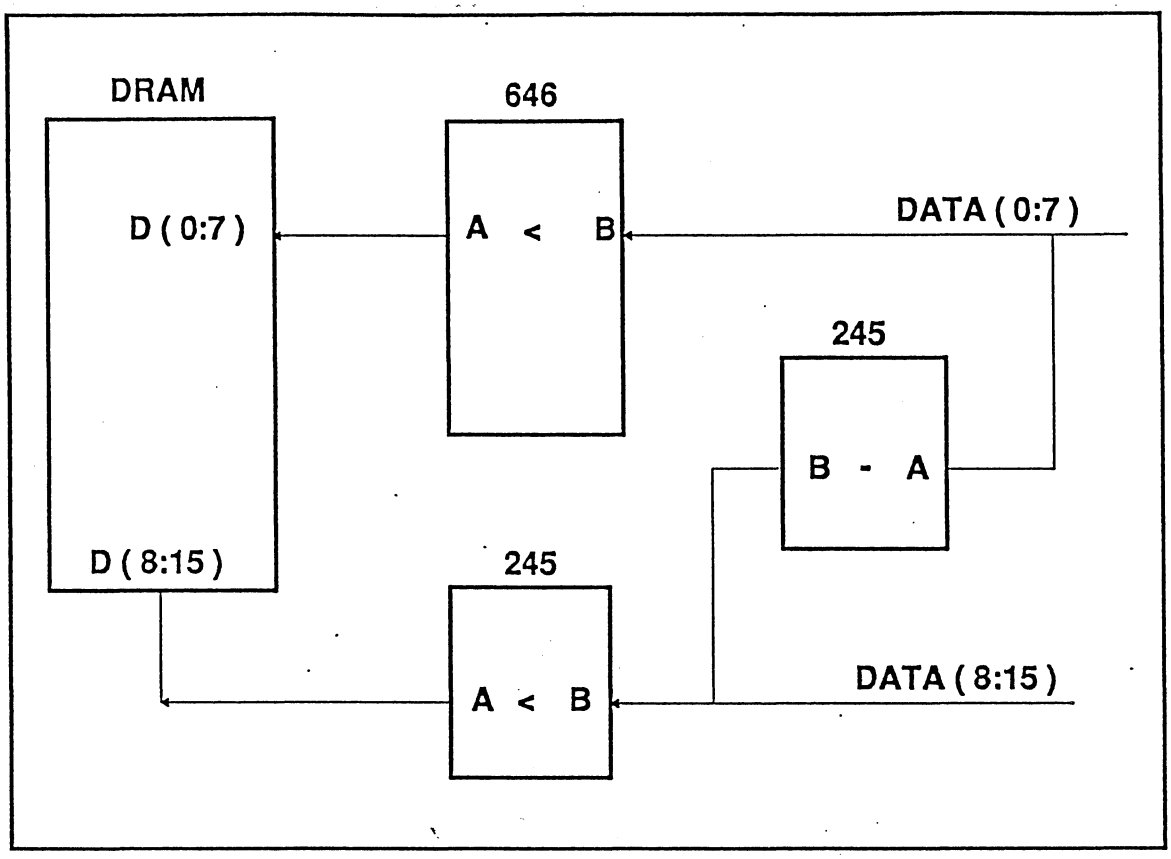
6.9.5 16 bit read from memory



INPUT SIGNALS	STATE
NMEMR	0
NMEMW	1
ADR0	0
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	1
NDEN0	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

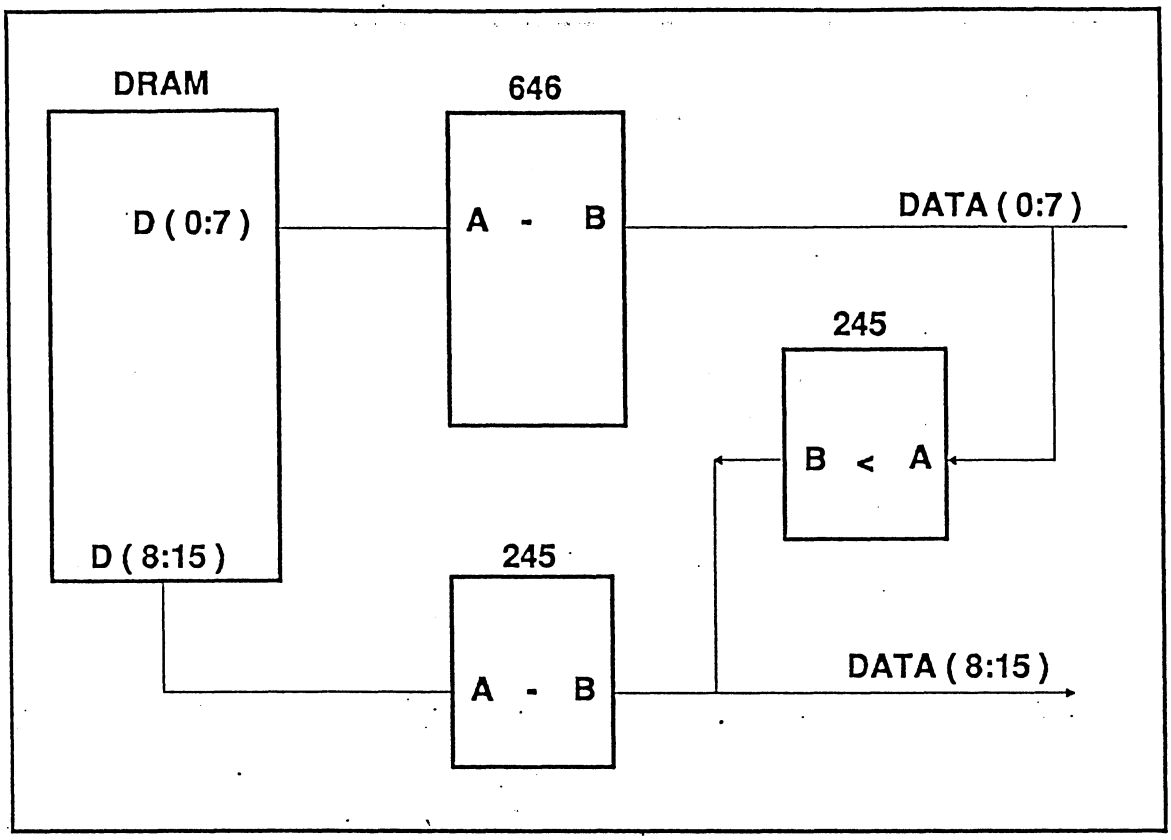
6.9.6 16 bit write to memory



INPUT SIGNALS	STATE
NMEMR	1
NMEMW	0
ADR0	0
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	0
NDEN0	0
NDEN0	0
NDEN1	0
NSDEN	1
SCYCLE	X
SDTR	X

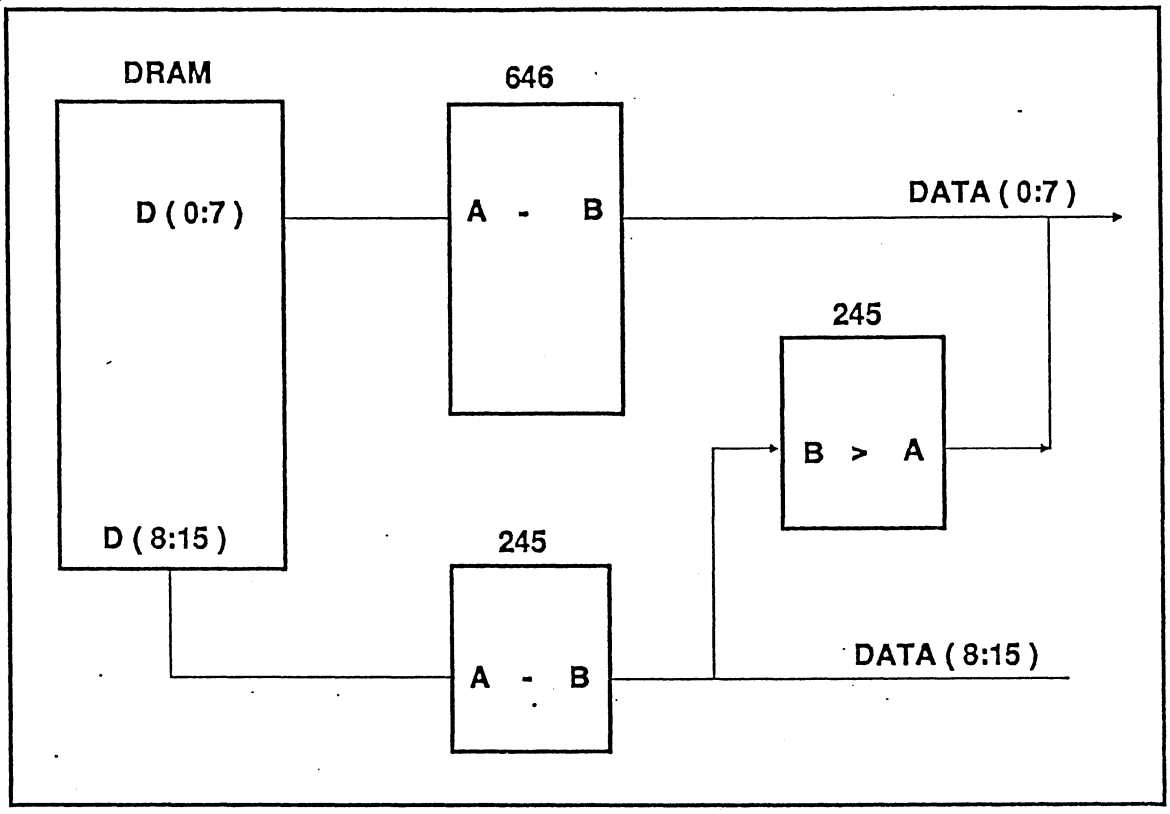
6.9.7 8 bit high byte read from 8 bit device



INPUT SIGNALS	STATE
NMEMR * NIOR	0
NMEMW * NIOW	1
ADR0	1
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	X
NDEN0	1
NDEN1	1
NSDEN	0
SCYCLE	X
SDTR	1

6.9.8 8 bit high byte write to 8 bit device



INPUT SIGNALS	STATE
NMEMR * NIOR	1
NMEMW * NIOW	0
ADR0	1
NEBHE	0
NCS16	1

CONTROL SIGNALS	STATE
DTR	X
NDEN0	1
NDEN1	1
NSDEN	0
SCYCLE	X
SDTR	0

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