Cyrix 6x86™ Processor
Technical Brief

The Cyrix 6x86 processor family offers the highest level of performance available for desktop PCs today.

Architectural Features	Cyrix 6x86™ processor	Pentium® Pro (P6) processor	Pentium® processor
Full x86 Instruction Set Optimization	X		
Superscalar	X	X	X
Superpipelined	X	X	
Register Renaming	X	X	
Data Dependency Removal	X	X	
Multi-Branch Prediction	X	X	
Speculative Execution	X	X	
Out-of-Order Completion	X	X	
80-Bit Floating Point	X	X	X
16-KByte Primary Cache	X	X	X

The 6x86™ processor family offers the highest level of performance available for desktop PCs today. Through the use of innovative, sixth-generation architectural techniques, the 6x86 processors achieve best-in-class performance that surpasses the Pentium® processor in each performance class.

Architectural Overview

The 6x86 processor consists of five major functional blocks — the Integer Unit (IU), Cache Unit (CU), Memory Management Unit (MMU), Floating Point Unit (FPU) and Bus Interface Unit (BIU). Instructions are executed in the X and Y pipelines within the Integer Unit. The superscalar architecture of the IU enables multiple instructions to be processed simultaneously.

The IU and FPU are optimized for maximum instruction throughput by using advanced architectural techniques including register renaming, out-of-order completion, branch prediction and speculative execution. These design innovations eliminate many data dependencies and resource conflicts to achieve high performance when executing existing software programs as well as future applications.

The Cache Unit stores the most recently used data and instructions allowing fast access to the information by the IU and FPU. Physical addresses are calculated by the MMU and passed to the Cache Unit and the BIU. The BIU provides the interface between the external system board and the processor's internal execution units.

Architectural Benefits

The 6x86 processor incorporates sixth-generation architectural innovations to overcome bottlenecks and achieve breakthrough performance. The *superscalar architecture* provides two pipelines to execute multiple instructions in parallel for faster processing and higher performance. *Superpipelining* increases the number of pipeline stages to avoid execution stalls and keep information flowing faster for higher frequency scalability. *Register renaming* provides temporary data storage for instant data availability without waiting for the CPU to access the on-chip cache or main system memory. *Data dependency removal* provides instruction results to both pipelines simultaneously so that neither pipeline is stalled. *Speculative execution* allows the pipelines to continuously execute instructions following a branch operation without stalling the pipelines. *Out-of-order-completion* lets the faster instruction exit the pipeline out of order, saving processing time without disrupting program flow.

Designed for Microsoft® Windows®95

Cyrix® Advancing the Standards

The Cyrix 6x86™ processor.

Cyrix Worldwide Offices

United States
Corporate Office
Richardson, Texas
Tel: (214) 968-8388
Fax: (214) 699-9857

Tech Support and Sales: (800) 462-9749
E-mail: tech_support@cyrix.com
BBS: (214) 968-8610 (up to 28.8K baud)

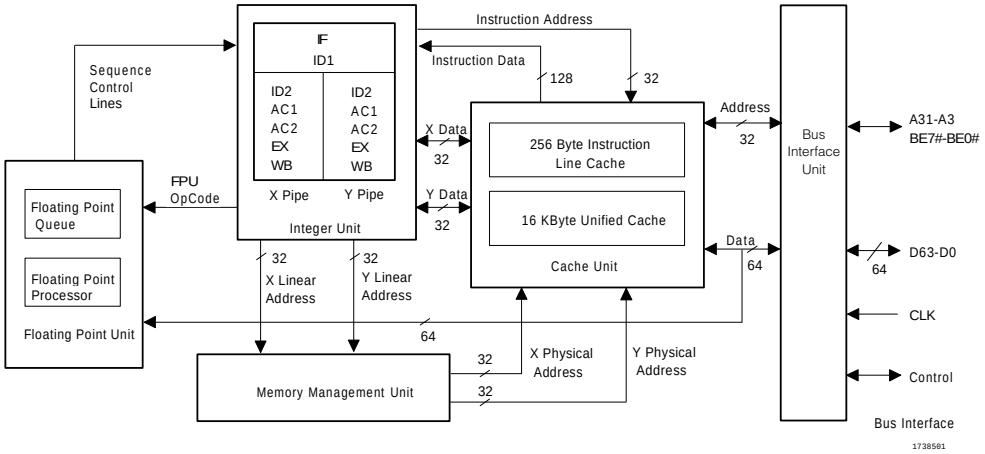
See us on the Internet World Wide Web:
http://www.cyrix.com

Europe
United Kingdom
Cyrix International Ltd.
Tel: (44) 1793-417777
Fax: (44) 1793-417770

Japan
Cyrix K.K.
Tel: (81) 45-471-1661
Fax: (81) 45-471-1666

Taiwan
Cyrix International, Inc.
Tel: (886) 2-718-4118
Fax: (886) 2-719-5255

Hong Kong
Cyrix International, Inc.
Tel: (852) 2485-2285
Fax: (852) 2485-2920



Technical Specifications

L1 Cache	16-KByte; write-back; 4-way associative; unified instruction and data; dual port address
Bus	64-bit external data bus; 32-bit pipelined address bus
Pin/Socket	P54C socket compatible (296-pin PGA)
Compatibility	Fully compatible with x86 operating systems and software including Windows® 95, Windows,® Windows® NT, OS/2,® DOS, Solaris and UNIX®
Floating Point Unit	80-bit with 64-bit interface; parallel execution; uses x87 instruction set; IEEE-754 compatible
Voltage	3.3-volt core with 5-volt I/O protection
Power Management	System Management Mode (SMM); hardware suspend; FPU auto-idle
Multiprocessing	Supports SLiC/MP™ and OpenPIC™ interrupt architectures
Burst Order	1-plus-4 or linear burst

Processor Part No.	**Performance Rating***	**Bus/Clock Speed**
6x86-P200+GP	P200+	75/150 MHz
6x86-P166+GP	P166+	66/133 MHz
6x86-P150+GP	P150+	60/120 MHz
6x86-P133+GP	P133+	55/110 MHz
6x86-P120+GP	P120+	50/100 MHz

*Call Cyrix Technical Support to get the Cyrix P-Rating white paper, Part No. 94279-00.

Cyrix Corporation
P.O. Box 850118
Richardson, TX 75085-0118
Tel: (214) 968-8388
Fax: (214) 699-9857