CHIPS AND TECHNOLOGIES, INC.
3050 ZANKER ROAD, SAN JOSE, CA 95134
408-434-0600

PRELIMINARY

82C5058
REFERENCE MANUAL

NOVEMBER 1989
CPI062/11-89
REV B
STK# 10062-001

CHIPS 82C5058
Single Chip SCSI
Controller Solution
Reference Manual
Revision B

Revision History

Revision	Change Activity	Date	Approved
A	First Release	2/24/89	BJM/JGC
B	Second Release	10/12/89	BJM/JGC

PREFACE

AUDIENCE

This manual is intended for firmware design engineers who are interested in programming or supporting the CHIPS 82C5058 Single Chip SCSI Controller Solution; however, such topics as pin descriptions that would be of interest to hardware design engineers are also addressed.

SCOPE

This manual contains the information a firmware design engineer needs to program this chip to implement the CHIPS 82C5058 on a disk drive controller. **It is assumed the reader already has a working knowledge of disk drive controllers.**

CONTENTS

The information in this manual is divided into four chapters, four appendixes, an index, and a glossary.

- Chapter 1 provides an overview of the CHIPS 82C5058 Single Chip SCSI Controller Solution.
- Chapter 2 which is intended for hardware design engineers describes the 82C5058 hardware specifications. It supplies physical and functional pin specifications, signal descriptions, electrical specifications, and packaging specifications.
- Chapter 3 which is directed at firmware engineers describes the operational modes of the 82C5058 registers.
- Chapter 4 which is intended for firmware engineers provides a detailed description of the commands and operation of the 82C5058.
- Appendix A contains the track format options for MFM, RLL2,7, and ESDI soft and hard sectored track formats.
- Appendix B contains a diagram and an example of a table setup to initialize the Format Parameter Register File.
- Appendix C provides the DRAM from SRAM pin conversion.

- Appendix D contains schematics for a typical controller configuration with the 82C5058 and 256K x 9 DRAM, 64K x 9 DRAM, or 64K x 8 SRAM configuration options.
- Appendix E contains the crystal circuit application notes.
- The glossary provides a list of abbreviations, and definitions of the key terms used throughout this manual.

RELATED PUBLICATIONS

- *CHIPS 5055B Memory Controller & Programmable Data Sequencer Reference Manual.* (Document Number: 3001469, Revision C, September 30, 1988).
- *CHIPS 5080C SCSI Multifunctional Device Reference Manual* (Document Number: 3001237, Revision A, September, 1985).
- *American National Standard for Information Systems - Small Computer System Interface (SCSI).* (X3.131-1986.).
- *ESDI Specification, ANSI Working Document.*
- *Seagate STXXX Micro Winchester OEM Manual.*

NOTATIONAL CONVENTIONS

The following conventions are used throughout this manual:

UPPERCASE	is used to indicate names of commands and signals.
-	a minus sign prefix to a signal name indicates an active low polarity.
+	a plus sign prefix to a signal name indicates an active high polarity.

Table of Contents

CHAPTER 1. AN OVERVIEW OF THE 5058

CHAPTER 2. 5058 HARDWARE SPECIFICATIONS

CHAPTER 3. THE REGISTERS

Chapter 4. 5058 OPERATION

FIGURES

TABLES

An Overview Of The 82C5058 1

INTRODUCTION

The CHIPS 82C5058 Single Chip SCSI Controller Solution is a CMOS LSI Applications Specific Integrated Circuit (ASIC) designed to be the primary component in a high-performance intelligent SCSI Winchester disk controller system. It provides three essential functions in a disk controller system: It manages the flow of data for a serial peripheral, it controls access to the external RAM buffer memory that is required for such transfers and it allows a microprocessor to have full control of the SCSI bus. The 82C5058 is designed to be used with a microprocessor having either a Z8- or 8051-type bus structure.

The 82C5058 consists of three functional sections:

1. A DMA controller.
2. A data sequencer.
3. A SCSI interface controller.

The CHIPS 82C5058 incorporates a dual-bus architecture, providing separate ports for microprocessor and memory buffer operations. With the goal of achieving the highest possible performance, this dual-bus structure is used so that disk data transfers can occur simultaneously with microprocessor operations.

In the DMA controller, Channel 0 is used for moving blocks of data between the data sequencer and the external buffer, while Channel 1 is used for moving blocks of data between the SCSI host interface and the buffer. (When the data sequencer is not using Channel 0, this channel can also be used to allow the microprocessor to access the RAM buffer.) DMA controller operation is programmed by writing the DMA Controller Registers, while operation may be monitored by reading the DMA Controller Registers.

The programmable data sequencer provides format control, error detection, and serial/parallel (SERDES) conversion functions normally associated with disk controllers. It is designed to be used with NRZ (Non-Return to Zero) interfaces such as those used in the ESDI (Enhanced Small Device Interface) or any of the CHIPS family of encode/decode VCO devices. Flexible operation of the sequencer is made possible by Write Registers that program its operation, while Read Registers allow the firmware to monitor operation. In addition, complete flexibility in disk formatting is permitted by a 64-byte on device format RAM, which is accessed through three of the Data Sequencer Write Registers (WR25, WR30 & WR31).

In addition to an external RAM buffer, a byte-oriented microprocessor such as the Z8 or 8051, with its associated memory, the CHIPS 82C5058 may be connected with the CHIPS 5070 Encode/Decode/PLL for MFM encoding/ decoding up to 5 Mbits/sec or the CHIPS 5027 Encode/Decode/PLL for RLL 2,7 encoding/decoding up to 10 Mbits/sec thus providing a total solution for an embedded SCSI interfacing disk drive.

ARCHITECTURAL OVERVIEW

The following is a brief description of the major circuit blocks of the CHIPS 82C5058 (See Figure 1-1).

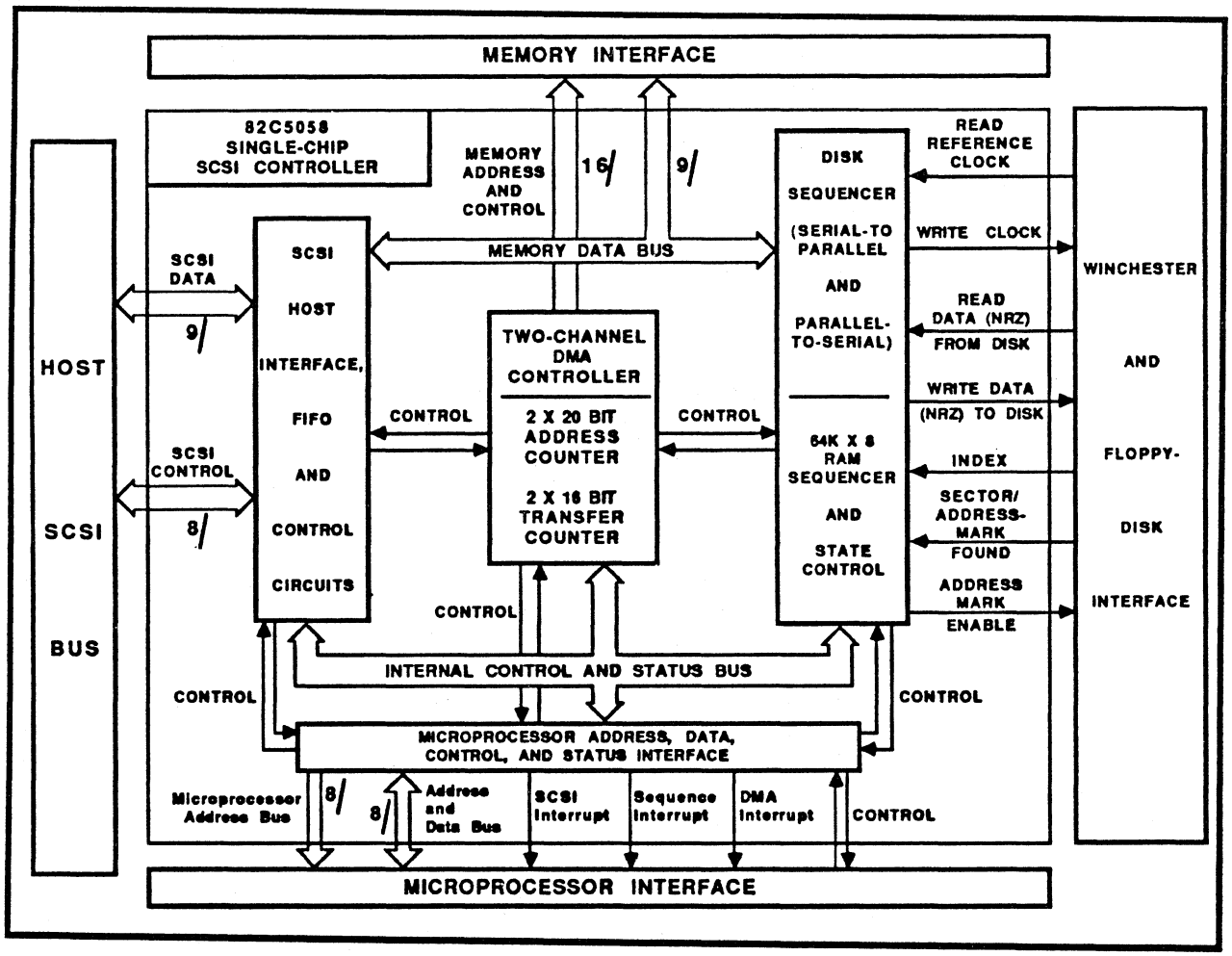


Figure 1-1. Functional Block Diagram

The first five blocks constitute the DMA section of the device:

1. **Parallel DMA Interface.** This is the parallel data interface. All parallel data transfers from either the sequencer, the buffer, or the microprocessor are transferred through this block.

2. **Counters.** This block consists of two address up-counters and two transfer down-counters. Each are 16 bits allowing $65{,}536_{10}$ maximum. There is one address counter and one transfer counter for each of the two channels, providing independent channel control and **concurrent operation**. Both channels share a common memory, the buffer RAM.

3. **Address Multiplexer.** As a function of DMA priority and resolution (see next block), this block puts the address for Channel 0 or Channel 1 onto the external memory address pins (MEM A0-14). Channel 0 is the highest priority channel; Channel 1 is the lowest. Priority is only important when there is a conflict; that is, if there is a collision, Channel 0 wins. When the 82C5058 is configured with a dynamic RAM (DRAM) buffer, refresh is the lowest priority.

4. **Priority Resolver/Channel Control.** This block, through the microprocessor and the micro control and decode logic (see below), determines which channel is enabled and the polarity of the control lines to the host buffer interface.

The following block is shared by the DMA controller and the data sequencer functions.

5. **Micro Control and Decode.** This block does all register address decoding. It decodes the microprocessor addresses (AD0-7), providing the required control to the address counters and the transfer counters. This block also contains registers that provide information for the priority resolver/channel control block. These are the Channel 0 and Channel 1 Control Registers (WR08 and WR09) and the Memory Cycle Timing Register (WR10). Thus this block serves both the DMA controller and the data sequencer functions.

The following describes the data sequencer portion of the circuitry.

6. **Format RAM.** The format RAM is a 64 X 8 bit RAM that allows for 16 pairs of 8-bit bytes to be used as count and value numbers associated with format states. This allows for 16 format states having associated count and value numbers. A state corresponds to a type of field encountered on a disk. Depending upon the type of field on the disk, a value may or may not be used, for example a sync field would have a value associated with it but a CRC/ECC field would not. A count is always used, since it is the number of byte times that the sequencer remains in its current state (i.e., loops back on itself).

Refer to Appendix A for track format examples and descriptions.

7. **Sequencer.** This block is fed by the format RAM. The sequencer addresses the format RAM and gets back a count. The sequencer loads an internal counter with this number and begins to count down. This number programs the device to be in a given field for a certain amount of time, or for a certain number of bytes. There are sixteen different states with each state representing a specific field in the overall disk format.

Refer to Appendix B, Table B-1 and Figure B-1 for an example of ST506/412 soft sector format.

8. **State Decode Control and Generation.** The sequencer block feeds the state decode control and generation block, which in turn feeds nearly all other blocks in the data sequencer portion of the 82C5058. Control signals are derived from the sequencer state and the current field count.

9. **CRC/ECC Generator.** In read mode, NRZ data comes into this block and, based on state and timing from the state control generation logic, the data is checked for the proper CRC or ECC bits. The data is then fed to the serial/parallel converter (SERDES) block.

In write mode, NRZ data arrives from the serial/parallel converter (SERDES) block and CRC or ECC bits are generated according to user-programmable registers (WR11 and Bit 6 of WR28). In addition, the signal WRT CLK (write clock) is generated and output. For the various CRC/ECC polynomials that can be used, see the "CRC/ECC" section that follows.

10. **Serial/Parallel Converter (SERDES).** In the read direction, this block converts serial data to parallel; in the write direction, converts parallel data to serial. NRZ DATA IN is synchronized to RD REFCLK and NRZ DATA OUT is synchronized to WRTCLK.

11. **ID Compare Error.** This block compares, on a real-time, byte-by-byte basis, data being read from the sector ID of a disk to the ID Registers programmed (WR20-23) by the user. The output of this block goes to the state decode control and generation block, which has the power to stop processing, retries, etc.

12. **AD I/O Buffer.** This is an I/O buffer. Internal to the 82C5058 is a bidirectional data bus, and this block buffers data between the internal bus and the microprocessor.

From the microprocessor AD0-7 interface bus (multiplexed low order address and data), (data) or address/data come into an internal buffer and this block drives the internal data bus, D0-7. D0-7 also goes to the micro control and decode block, which picks off the address at ALE (8051 mode) or -AS (Z8 mode) time and feeds them back out on the microprocessor address bus, MICRO A0-7. This is basically a convenience for other devices in the system.

Note: The AD0-7 bus, via the internal bus, D0-7, supplies the address and transfer counters with their initial values. The two address counter pairs are WR0 and WR1 for Channel 0, and WR4 and WR5 for Channel 1; the two transfer counters are effectively WR2 and WR3 for Channel 0, and WR6 and WR7 for Channel 2. While AD0-7 provides the initial values, the micro control and decode block decodes the addresses from AD0-7 and generates the appropriate controls.

Inside the 82C5058, the AD I/O buffer drives that portion of the device that is microprocessor controlled.

INTERFACES

There are four interfaces on the CHIPS 82C5058:

1. The SCSI host interface consists of an 8-bit data bus with parity (HOST_D(0-7) & P), and all the control signals each with 48 ma. open drain drivers and Schmidt trigger receivers.

2. The memory interface consists of an 8-bit data bus with parity (MEM D(0-7) & P), an address bus, along with the memory control signals. Note that the address bus is 15 bits (MEMA0-14), addressing up to 32K bytes. Using two chip selects, 64K bytes may be addressed in SRAM mode, and 1 megabyte may be addressed in DRAM mode.

Refer to Appendix C for DRAM addressing.

3. The microprocessor interface consists of an 8-bit multiplexed address/data bus (AD0-7), an 8-bit demultiplexed address bus (A_0-7, latched off of AD0-7 at ALE or -AS time, depending on CONFIG), and various microprocessor bus control signals.

4. The drive interface contains the serial data lines to and from the disk (or the Encoder/Decoder, PLL circuitry) and various control signals required for reading and writing a disk.

REGISTERS

There are four groups of registers in the 82C5058. One group is used for controlling and monitoring DMA controller operation. This group consists of Write Registers WR00-15 and Read Registers RR00-15. Another group is used for controlling and monitoring data sequencer operation. These are Write Registers WR16-34, and Read Registers RR16-31. All of these registers can be directly written or read.

Still another group is used for controlling and monitoring SCSI interface operation. These are Write Registers WR64-73, and Read Registers RR64-71. All of these registers can be directly written or read.

The final group is available for formatting of the disk. This group is indirectly accessed by WR30 (value register) and WR31 (count register) and WR25. The format RAM is viewed as sixteen register pairs containing information that determines the overall format of the disk. This information is written by indexing via WR25 and writing the **value** of the field into WR30 and the **count** (the number of times the value is repeated in the stream) in WR31.

A summary of the registers available in the 82C5058 is provided in Chapter 3, Tables 3-1, 3-2, and 3-3.

CRC/ECC

The CRC/ECC block generates and checks the CRC or ECC bytes that are appended to the sector ID and data fields. WR11 and WR28 determine the selection of the **computer generated polynomial.** Bits 1 and 2 of WR11 determine the selection of the polynomial for the data fields:

16-bit CRC: (X16)+(X12)+(X15)+1 (Floppy Compatible CRC)
32-bit ECC: (X32)+(X24)+(X18)+(X15)+(X14)+(X11)+(X8)+(X7)+1
48-bit ECC: Proprietary. *
56-bit ECC: Proprietary. *

If Bit 6 of WR28 is cleared (0), then the ID field will use the same polynomial as selected for the data field above. If Bit 6 is set (1), then the ID field will use the 16-bit CRC polynomial--regardless of the selection of the polynomial for the data field. This allows for great flexibility in the choice of error detection schemes. The actual correction is achieved by the microprocessor use of the syndrome returned from the device upon receipt of an error. Sector size, and the level of code optimization have an impact upon both detection and correction capability.

* Contact CHIPS for Sublicense of the polynomials.

FEATURES

Memory Controller Features:

- High-performance dual-bus architecture
- Two independent DMA channels
- 10 megabyte device bandwidth at 40 Mhz clock
- 20-bit address and 16 bit transfer count registers for each channel
- Holding registers for address counts for non-contiguous memory transfers.
- Independent mask for channel-end interrupt
- Bus access resolved on channel priority basis
- Logic to demultiplex the microprocessor Address/Data and drive the low order microprocessor address lines
- Programmable interrupt polarity
- Programmable auto-count reinitialization
- Programmable memory access cycle timing (2 to 5 clock cycles)
- Buffer memory address for 64K SRAM (2 memory chip enables for 32Kx8 SRAM)
- DRAM support for up to 1 megabyte
- Data memory parity generate and check option
- Channel 1 optional level request (for synchronous transfer)

SCSI Interface Controller Features:

- Includes internal single ended drivers and receivers
- Support for external differential drivers and receivers for target mode only
- Asynchronous DMA transfer rate to greater than 3 Mbytes/second
- Synchronous transfer rate to 8 Mbytes/second for target mode only
- 8 byte FIFO for synchronous transfer to offset of 7
- Direct microprocessor control of all SCSI control signals
- Full through parity from host data bus to memory data bus
- Programmable arbitration delay for different crystals
- Flexible interrupt capability

Programmable Data Sequencer Features:

- High-level instruction set including:
  - Read/Write
  - Individual sector formatting
  - Track formatting
  - Read ID
  - Read/Write long
  - Read syndrome
  - Verify (with data in buffer)
  - Check data ECC
  - Check track format
- Supports up to 20 MHz serial bit rate (NRZ)
- Programmable disk format:
  - Programmable sector size up to 65,536 bytes/sector
  - Programmable ID data and size
  - Programmable gap sizes and fill characters
  - User-definable Header Flag Byte or Nibble
  - Selectable 32, 48, or 56 bit ECC polynomial and ID CRC or ECC or flexible disk compatible ID and data field CRC
- Hard or soft sector modes
- NRZ serial disk interface
- Direct interface to ESDI-type drives, both hard and soft sectored
- Multi-sector transfer capability with automatic sector increment
- Programmable automatic ID retries
- Low power consumption (CMOS)
- Logic to transfer data between the micro bus and buffer memory
- ESDI ID Sync Timeout programmable
- ESDI Write Gate to AM ENABLE programmable
- Format Track with data from buffer
- Programmable Write Gate disable for embedded servo

82C5058 Hardware Specifications 2

This chapter is directed at hardware engineers intending to design the CHIPS 82C5058 Single Chip SCSI Controller Solution into their disk drive controller systems. Physical and functional pin specifications, signal descriptions, timing specifications, and electrical specifications are provided.

PHYSICAL SPECIFICATIONS

The CHIPS 82C5058 device is available in an 100-pin QFP package. Package specifications and pin-out diagrams are provided for this package.

100-pin QFP Package

Refer to Figure 2-1 for physical pin out of the 100-pin QFP package. Table 2-1 provides a pin list for the 100-pin QFP package. Note an active low polarity is indicated by a minus sign (-) prefix; a plus sign (+) prefix indicates high polarity. For information on this package's pin functions, refer to the section "Signal Descriptions" and Table 2-1 later in this chapter.

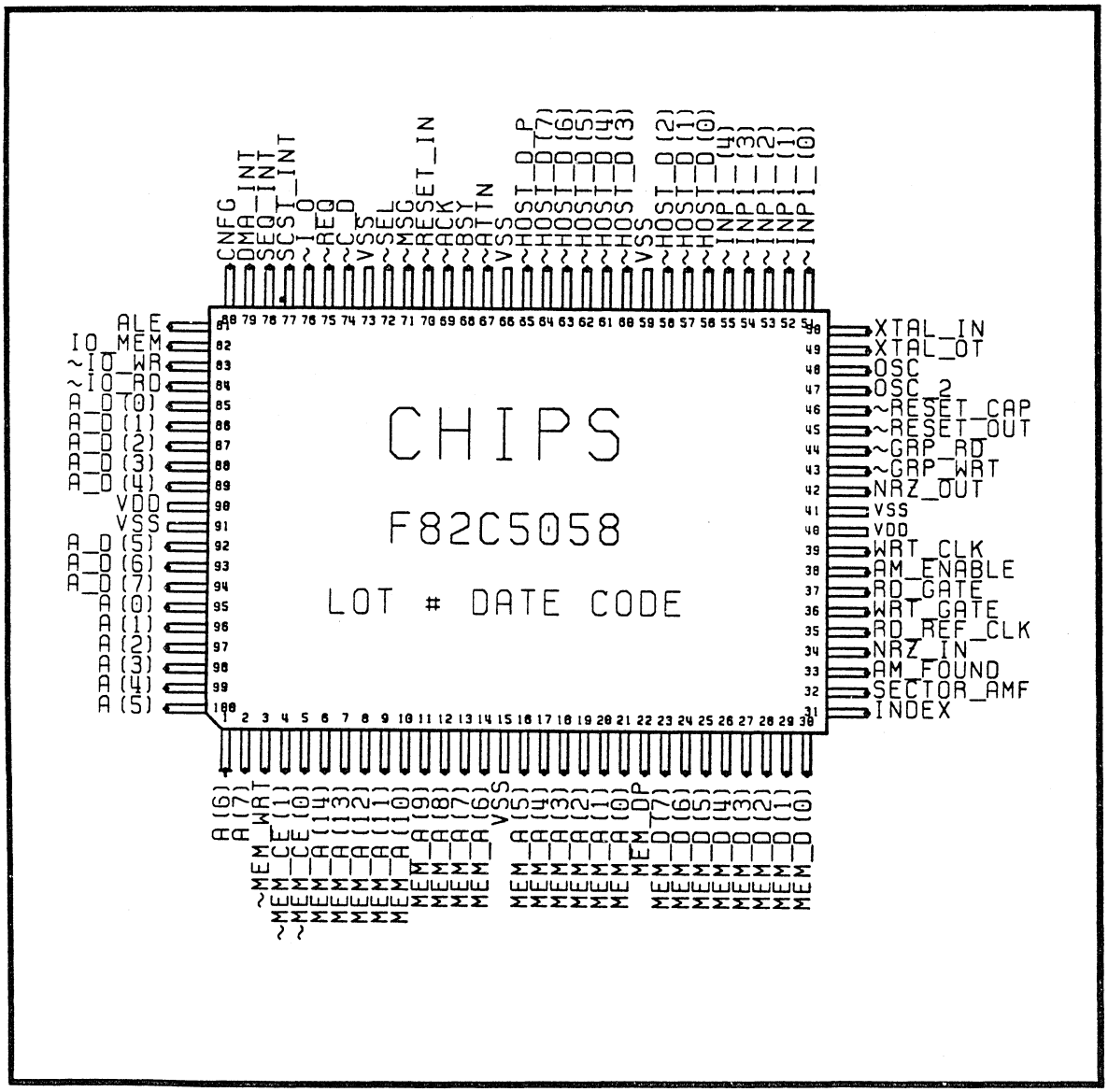


Figure 2-1. Physical Pin out of the 100-pin QFP Package

Table 2-1. A Pin List of the 100-pin QFP Package

Pin Number	Pin Name	I/O	Pin Number	Pin Name	I/O
1	A_(6)	O	51	-INP1_(0)	I/O
2	A_(7)	O	52	-INP1_(1)	I/O
3	-MEM_WRT	O	53	-INP1_(2)	I/O
4	-MEM_CE(1)	O	54	-INP1_(3)	I
5	-MEM_CE(0)	O	55	-INP1_(4)	I
6	MEM_A(14)	O	56	-HOST_D(0)	I/O
7	MEM_A(13)	O	57	-HOST_D(1)	I/O
8	MEM_A(12)	O	58	-HOST_D(2)	I/O
9	MEM_A(11)	O	59	VSS	
10	MEM_A(10)	O	60	-HOST_D(3)	I/O
11	MEM_A(9)	O	61	-HOST_D(4)	I/O
12	MEM_A(8)	O	62	-HOST_D(5)	I/O
13	MEM_A(7)	O	63	-HOST_D(6)	I/O
14	MEM_A(6)	O	64	-HOST_D(7)	I/O
15	VSS		65	-HOST_DP	I/O
16	MEM_A(5)	O	66	VSS	
17	MEM_A(4)	O	67	-ATN	I/O
18	MEM_A(3)	O	68	-BSY	I/O
19	MEM_A(2)	O	69	-ACK	I/O
20	MEM_A(1)	O	70	-RESET_IN	I/O
21	MEM_A(0)	O	71	-MSG	I/O
22	MEM_DP	I/O	72	-SEL	I/O
23	MEM_D(7)	I/O	73	VSS	
24	MEM_D(6)	I/O	74	-C/D	I/O
25	MEM_D(5)	I/O	75	-REQ	I/O
26	MEM_D(4)	I/O	76	-I/O	I/O
27	MEM_D(3)	I/O	77	INT_SCSI	O
28	MEM_D(2)	I/O	78	INT_SEQ	O
29	MEM_D(1)	I/O	79	INT_DMA	O
30	MEM_D(0)	I/O	80	CNFG	I
31	INDEX	I	81	ALE/-AS	I
32	SECTOR_AMF	I	82	IO_MEM/_DM	I
33	AM_FOUND	I	83	-IOWR/R-W	I
34	NRZ_IN	I	84	-IORD/-DS	I
35	RD_REF_CLK	I	85	A/D_(0)	I/O
36	WRT_GATE	O	86	A/D_(1)	I/O
37	RD_GATE	O	87	A/D_(2)	I/O
38	AM_ENABLE	O	88	A/D_(3)	I/O
39	WRT_CLK	O	89	A/D_(4)	I/O
40	VDD		90	VDD	
41	VSS		91	VSS	
42	NRZ_OUT	O	92	A/D_(5)	I/O
43	-GRP_WRT	O	93	A/D_(6)	I/O
44	-GRP_RD	O	94	A/D_(7)	I/O
45	-RESET_OUT	O	95	A_(0)	O
46	-RESET_CAP	I/O	96	A_(1)	O
47	OSC_2	O	97	A_(2)	O
48	OSC	O	98	A_(3)	O
49	XTALOT	O	99	A_(4)	O
50	XTALIN	I	100	A_(5)	O

100-pin QFP Package Specifications

Figure 2-2 provides a diagram of the package specifications for the 100-pin QFP package.

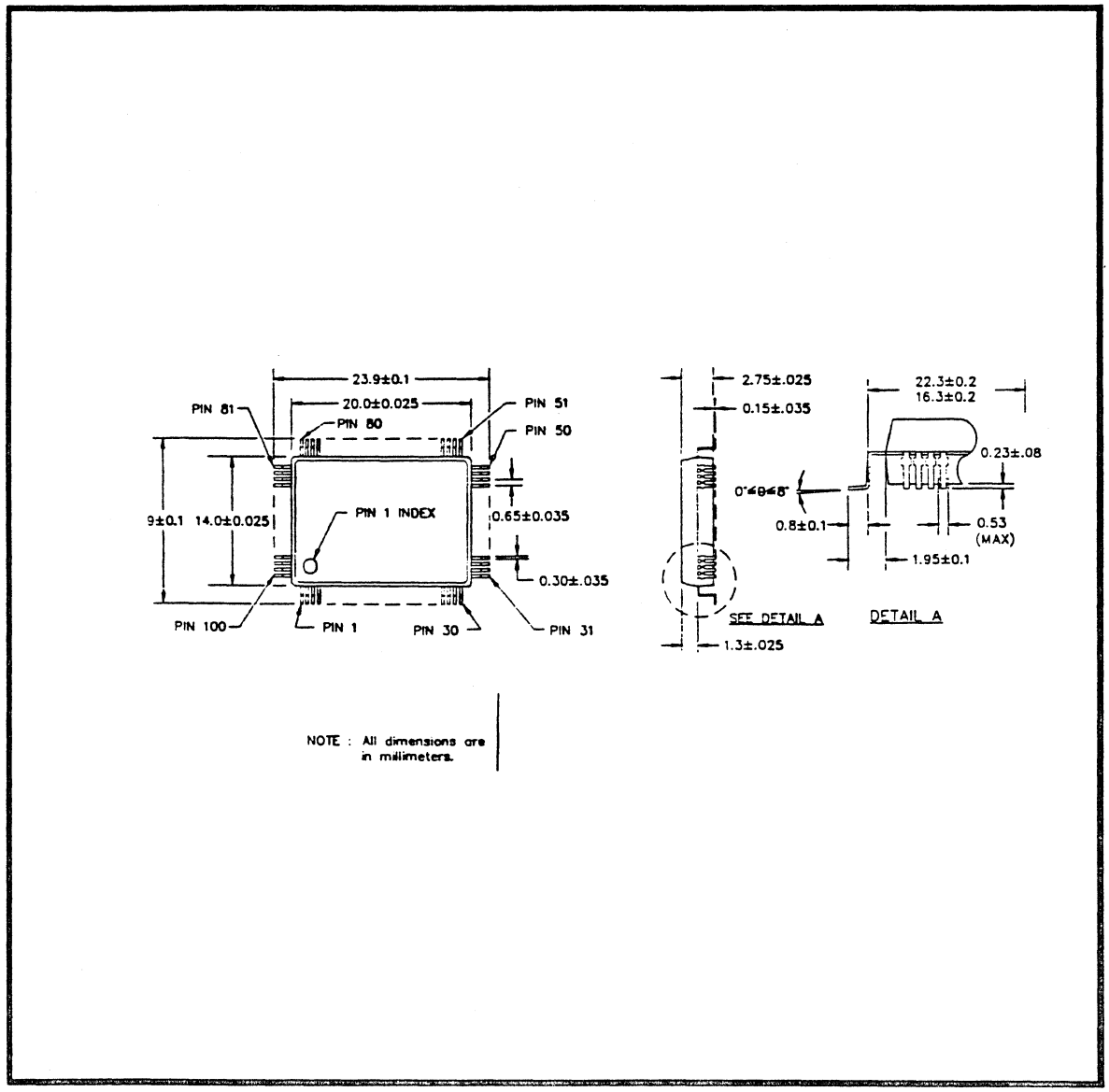


Figure 2-2. Diagram of the 100-pin QFP Package Specification

A TYPICAL SYSTEM

Figure 2-3 shows a typical system configuration using the CHIPS 82C5058 Single Chip SCSI Controller Solution with a RAM buffer, a data separator, and a microcomputer with an associated ROM and RAM.

See Appendix D for schematics of a typical system configuration using the CHIPS 82C5058 with 3 separate RAM buffer configuration options.

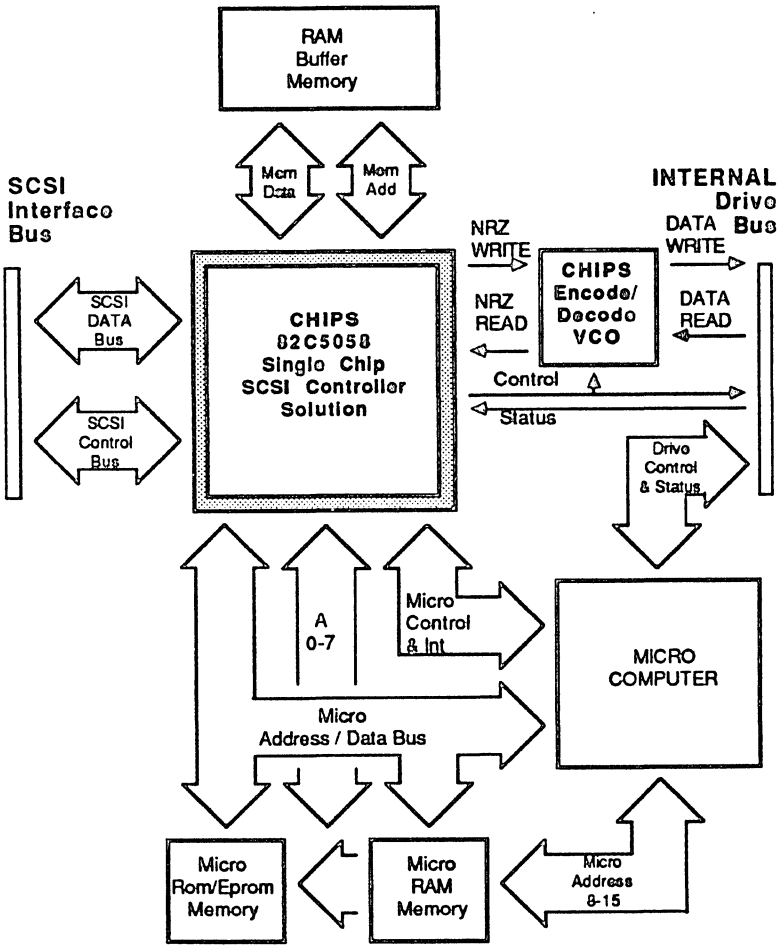


Figure 2-3. A Typical System Configuration Using the CHIPS 82C5058

SIGNAL DESCRIPTIONS

Table 2-1 is a list of the signals in alphabetical order. Note that in all the tables an active low state is indicated by a negative sign (-) prefix. When the pin(s) can be configured for more that one function, such as ALE_-AS, the other functions are listed as a subset.

Input/Output Signals

Table 2-2 lists the 82C5058 input/output signals and their functions.

Table 2-2 Input/Output Signals

Signal Symbol	Signal Name	I/O	Pin Number	Function
A_(0:7)	Micro Address (Active High)	O	95-100 1-2	This 8-bit address bus is the address demultiplexed from the microprocessor's address/data bus (AD0-7). In 8051 mode, the address is latched on the falling edge of ALE; in Z8 mode, it is latched on the rising edge of -AS. This bus may be used to access the microprocessor's external memory and peripheral chips.
-ACK	Acknowledge (Active Low)	I/O	69	This driver/receiver I/O line is asserted by the initiator and is a response to the target assertion of -REQ used to handshake all Data, Commands, Status and Messages between the initiator and target. The Driver Enable Bit must be set along with the Initiator Bit to allow this device to assert this signal. If in I/O mode, the microcomputer has direct control and access to this signal by WR41h and RR41h or indirect control of this signal by WR47h and RR47h. (If in DMA mode and Channel Control Register is configured in SCSI protocol mode, an internal state machine controls transfers.)
AD(0-7)	Address/Data (Active High) (Tri state)	I/O	85-89 92-94	This is the multiplexed 8-bit address/data bus from the microprocessor. In 8051 mode (CONFIG grounded), addresses are latched into the Address Register on the falling edge of ALE in Z8 mode (CONFIG left open), addresses are latched on the rising edge of -AS. See the signal ALE/-AS below.) If the address is within the range of the internal chip select (AD7=0), data is either written to or read from the Memory Controller/Data Sequencer Registers, depending on: in 8051 mode, whether -IOWR or -IORD is active; in Z8 mode, assuming -DS is low, whether R/-W is low or high.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
ALE_-AS				
ALE	Address Latch Enable (8051 mode) (Active High)	I	81	In 8051 mode, the falling edge of ALE is used to latch the address portion of AD(0-7) on the microprocessor bus into the (Active High) internal address buffer.
-AS	Address Strobe (Z8 mode) (Active Low)			In Z8 mode, the rising edge of -AS is used to latch the address.
AM ENABLE	Address Mark Enable (Active High)	O	38	If ESDI mode is selected, this output is active at state 1 strobe time. This function is used for writing an Address Mark to the disk if the ESDI device is configured in soft sectored mode. If ESDI mode is not selected,AM_ENABLE is active for state strobe 3 and 9, and may be used to enable external encoding of a "illegal pattern" Sync Byte.
AM FOUND	Address Mark (Active High)	I	33	This inupt signal is used by the sequencer during a read operation for byte synchronization. It is an output from the VCO/Encode/Decode device, and is used for MFM or 2,7 RLL byte synchronization. If internal synchronization is configured, this input should be grounded.
-ATTN	Attention (Active Low)	I/O	67	This driver/receiver I/O line allows direct microcomputer control and access of this signal by WR41h and RR41h. This signal is used by the initiator to notify the target of a request for a Message Out phase.
-BSY	Busy (Active Low)	I/O	68	This driver/receiver I/O line is asserted by the target and is a response to the initiator Selection phase. The microcomputer has direct control and access of this signal by WR41h and RR41h during arbitration.
-C/D	Command/Data (Active Low)	I/O	74	This driver/receiver I/O line allows direct microcomputer control and access of this signal by WR41h and RR41h. This signal is used by the target to define a Command phase if Asserted or a Data phase if not asserted. The Driver Enable Bit must be set to allow this device to assert this signal.
CONFIG	Configuration (Active High)	I	80	This internally pulled up input signal is internally pulled up is used to select the microprocessor bus type configuration option for the 82C5058. When CONFIG is grounded, the device is configured for an 8051 type processor. When CONFIG is left open, the device is configured for Z8 type processor.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
-GRPRD	Group Read Strobe (Active Low)	O	44	This signal is strobed whenever the microprocessor reads any of the following registers: RR12 through RR15. It may be used to enable status onto the microprocessor bus (AD0-7). It may also be used as an external peripheral chip select for devices such as the Intel 8255 PIO or 8273 FDC.
-GRPWRT	Group Write (Active Low)	O	43	This signal is strobed whenever the microprocessor accesses any of the following registers: WR12 through WR15 and RR11. It may be used to latch data from the microprocessor data bus (AD0-7) into an external register. It may also be used as an external peripheral chip select as noted under -GRPRD above.
-HOSTD(0:7)	Host Data Bus (Active Low)	I/O	56-58 60-64	This driver/receiver I/O lines are the SCSI host data bus used for all host to/from controller command, status and data transfer.
-HOSTD_P	Host Parity (Active Low)	I/O	65	This driver/receiver I/O line is the SCSI host data bus ODD parity used for all host to/from controller command, status and data transfer. This device always generates ODD parity when transfer is from this device and only checks the ODD parity when transfer is to this device and PARITY is enabled.
INDEX	Index (Programmable)	I	31	This is a Schmidt trigger input signal from the disk that is received once per revolution. The data sequencer uses the asserting edge of the INDEX pulse for synchronization during formatting, and for timing-out commands.
-INP(4:0)	Input Port(4:0) (Active Low)	I/O	51-55	The internally pulled-up Schmidt trigger input lines are used by the microcomputer for default information like the SCSI ID. If Differential Driver mode is configured, these five pins have a totally different meaning. In this mode INP(2:0) are output signals while -INP(4:3) are input signals. The -INP(0) output pin is an active low -ARBITRATE function. This output is asserted low during re-selection and is used to enable the Device ID on the bus. The -INP(1) output pin is an active low -DIF_DIR function that is used to control the external differential drivers and receivers. This signal is asserted low when the direction is to the Host. The -INP(2) output pin is an active low -TAR_EN function.that is used to enable the external target drivers (-REQ, -C/D, -I/O and -MSG). The -INP(3) input pin is an active low -DIF_BSY function. The -INP(4) input pin is an active low -DIF_SEL function.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
INT_SCSI	Interrupt SCSI (Programmable)	O	77	This output, if enabled, is asserted when any enabled interrupting sequence is detected, and is cleared when the microprocessor reads status or the interruption event is disabled or deasserted.
INT MEM Count=0 or	Interrupt, Memory Controller (Programmable)	O	79	Assuming that interrupts are enabled for a channel (Bit 3=1 of WR08 for Channel 0 or WR09 for Channel 1) and that Transfer disables the channel, (Bit 4=0 of WR08 WR09) then the signal INT MEM is asserted when Channel Enable (Bit 0, same register) goes to 0 for that channel (i.e. on the deasserting edge of the Channel Enable signal). INT MEM is deasserted when the microprocessor writes to the Channel Control Register (WR08 or WR09) of the channel that caused the interrupt. The polarity of INT MEM is controlled by Bit 2 of the Memory Cycle Timing Register (WR10).
INT SEQ	Interrupt, Sequencer (Programmable)	O	78	If sequencer interrupts are enabled (Bit 7 of WR29 is set), this output is asserted when the sequencer has completed a command or for any function that causes Busy to transition from Busy to not-Busy. It is deasserted when the microprocessor reads the Sequencer Status Register (RR16).
IO_-MEM_-DM				
IO/-MEM	I/O/-Memory (8051 mode) (I/O Active High)	I	82	In 8051 mode, this line is connected to an 8051 address line to differentiate between an I/O cycle and a memory cycle.
-DM	-Data Memory (Z8 mode) (Active Low)			In Z8 mode, it is an active low chip enable and connected to the Z8 -DM line.
-IORD_-DS				
-IORD	I/O Read (8051 mode) (Active Low)	I	84	In 8051 mode, this input, when low, enables the information from the register selected by the previously latched address onto the microprocessor bus (AD0-7).
-DS	Data Strobe (Z8 mode) (Active Low)			In Z8 mode, this input provides the timing for data movement to or from selected registers and the microprocessor bus (AD0-7).

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
-IOWR_R/-W				
-IOWR	I/O Write (8051 mode) (Active Low)	I	83	In 8051 mode, this input, when low, enables the information from the microprocessor bus (AD0-7) into the register selected by the previously latched address.
R/-W	Read/Write (Z8 mode) (Read Active High) (Write Active Low)			In Z8 mode, assuming -DS is low, this input specifies the direction of the data transfer. When low with -DS low, data is written low from the microprocessor bus (AD0-7) to the sequencer. When high with -DS low, data is read from the selected register to the microprocessor.
-I/O	In/Out (Active Low)	I/O	76	This driver/receiver I/O line allows direct microcomputer control and access of this signal by WR41h and RR41h if in I/O mode or Channel 1 control if DMA mode is configured. This signal is asserted by the target to define a Direction Out phase. The Driver Enable Bit must be set to allow this device to assert this signal.
MEMA(0-14)	Memory Address (Active High)	O	21-16 14-6	The Memory Address Bus is used to output the contents of the Memory Address Register of the selected channel to the external RAM buffer. The 82C5058 can address a 32K SRAM buffer. If the 82C5058 is configured for two chip selects, then MEMA0 is converted to MEMA15 (output pin), and MEMA0 is internally used to select between the two chip selects (2x32K SRAMs), -MEMCE0 and -MEMCE1. In SRAM mode this allows addressing up to 64K bytes. For various DRAM configurations (64K x 8, 64K x 16, 256K x 8, 256K x 16, and 1M x 8), refer to Appendix C.
-MEMCE0	Memory Chip Enable Zero (Active Low)	O	5	This output is an active low chip enable for the external RAM buffer memory addressed by MEMA0-14. When this output and -MEMWRT are asserted, data is written to the selected address in the RAM buffer memory. When this output is asserted and -MEMWRT is deasserted, data is read from the RAM buffer memory. When two chip selects are enabled, this output is asserted when MEMA0 is low or Channel 1 is in word mode, while a memory cycle is in process.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
-MEMCE1	Memory Chip Enable One (Active Low)	O	4	This output is an active low chip enable for the external buffer memory addressed by MEMA0-14 when two chip selects are enabled. When this output and -MEMWRT are asserted, data is written to the selected address in the buffer memory. When this output is asserted and -MEMWRT is deasserted, data is read from the buffer memory. This output is asserted when MEMA0 is high or Channel 1 is in word mode, while memory cycle is in process.
MEMD(0-7)	Memory Data (Active High) (Tri-state)	I/O	30-23	This is an 8-bit bidirectional bus used to transfer data to and from the RAM buffer. The MEMD0-7 are driven when ACK0 is low, and data is transferred from the 82C5058 to the buffer memory.
MEMDP	Memory Data Parity Bit (Active High) (Tri-state)	I/O	22	This bit is the bidirectional odd parity for the memory data bus. **Odd** parity is always generated by this device to write in external buffer memory but is only checked if programmed for memory parity.
-MEMWRT	Memory Write (Active Low)	O	3	This output is an active low write enable for the external RAM buffer.
-MSG	Message (Active Low)	I/O	71	This driver/receiver I/O line allows direct microcomputer control and access of this signal by WR41h and RR41h. This signal is used by the target to define a Message phase if Asserted or a Data phase if not asserted. The Driver Enable Bit must be set to allow this device to assert this signal.
NRZ IN	NRZ Data In (Non-Return to Zero) (Active High)	I	34	This serial data input line is the NRZ read data from the drive or data separator/PLL: CHIPS 5070 MFM Encode/Decode/VCO. CHIPS 5027 2,7RLL Encode/Decode/VCO. ESDI-type disk drive.
NRZ OUT	NRZ Data Out (Non-Return to Zero) (Active High)	O	42	When WRTGATE is active, this line outputs serial NRZ write data from the sequencer. All data are output to: CHIPS 5070 MFM Encode/Decode/VCO or 5027 2,7 R.LL Encode/Decode/VCO or ESDI-type disk drive.
OSC	Oscillator (Active High)	O	48	This is a TLL clock at the XTAL (crystal) frequency.
OSC_2	Oscillator/2 (Active High)	O	47	This is a TLL clock at one-half the XTAL (crystal) frequency.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
RDGATE	Read Gate (Active High)	O	37	This signal is asserted during a sequencer read operation; it indicates that the drive or data separator should present read data on the NRZ IN line. When in external Sync mode (Bit 4 of WR29 is set), the data separator must provide AM FOUND.
RD_REF_CLK	Read/Reference (Active High)	I	35	This signal has two functions: When WRTGATE is true, this signal is used as a write (reference) clock to generate the write data at the NRZOUT pin. When RDGATE is true, a read clock, locked to the read data on the NRZIN line, must be supplied. **Note: A clock must always be present on this pin.**
-REQ	Request (Active Low)	I/O	75	This driver/receiver I/O line is asserted by the target and is used to handshake all Data, Commands, Status and Messages between the initiator and target. If in I/O mode, the microcomputer has direct control and access of this signal by WR41h and RR41h or indirect control of this signal by WR47h and RR47h. If in DMA mode and Channel 1 control register is configured in SCSI protocol mode, an internal state machine controls transfers. The Driver Enable Bit must be set to allow this device to assert this signal.
-RESET	Reset (Active Low)	I/O	70	When asserted, if not disabled the sequencer goes Not-Busy (Bit 0 of RR16 is cleared), the Read Gate (RD GATE) and the Write Gate (WR GATE) signals are deasserted, and the drive Data Over/Under Run and micro memory Over/Under Run Bits of the sequencer Extended Status Register (Bits 0 and 1 or RR17) are set=0. It also clears the SCSI interface to a Bus Free state.
-RESET CAP	Reset Capacitor (Active Low)	I/O	46	This input/output pin is to be connected to an external capacitor to provide a power-up reset signal of an externally controllable pulse width. The capacitor is discharged by either a power-on condition or a -RST in asserted low. The -RESET_OUT time is determined by the RC time constant of an internal 100k ohm resister and the external capacitor. When the charge reaches a threshold of 3 volts, the -RESET_OUT signal is deasserted. If an external open collector reset signal is applied to this pin, this device will react as if a power-on condition has occurred.

Table 2-2 Input/Output Signals (continued)

Signal Symbol	Signal Name	I/O	Pin Number	Function
RESET_OUT	Reset Out (Active Low)	O	45	This output signal (if enabled) is asserted on power-on or when the SCSI bus reset (-RESET) is asserted, or the-RESET_CAP pin is externally asserted. It remains asserted until the RC time constant of the -RESET-_CAP pin reaches the 3.0 volt threshold.
SECTOR/AMF	Sector/Address Mark Found (Programmable)	I	32	This Schmidt trigger input can be used for either the Sector line from a hard sectored disk drive or the Address Mark Found line from a soft-sectored ESDI drive
-SEL	Select (Active Low)	I/O	72	This driver/receiver I/O line is asserted by the initiator and is used during a Selection phase. The microcomputer has direct control and access of this signal by WR41h and RR41h This signal is also asserted during a START ARBITRATION command.
WRTCLK	Write Clock (Active High)	O	39	This output is a clock at the RD_REF_CLK frequency. The high to low edge of this clock is used to clock the NRZOUT write data signal.
WRTGATE	Write Gate (Active High)	O	36	This signal is asserted during a sequencer write operation; it indicates that data on the NRZOUT line should be written on the disk.
XTALIN, XTALOT	Crystal 0-1 (Active High)	I O	50,49	The XTAL lines may be connected to an external crystal oscillator, or if an external clock source is available, a clock input may be connected to the XTALIN input with XTALOT left open. In either case OSC,and OSC_2, are derived from the XTALIN frequency. Note that if an external crystal source is used, it must be a fundamental parallel resonant type in the range of 1 MHz to 24MHz, or a third overtone to 40 MHz. Also, an external resistor must be connected across the crystal with a capacitor to ground from both sides. **Note: See Appendix E, the applications section for critical circuit description, layout and crystal selection.**
VDD	Vdd +5		40,90	
VSS	Vss Ground		15,41,59 66,73,91	

ELECTRICAL SPECIFICATIONS

The CHIPS 82C5058 is manufactured using a proven low-power CMOS technology process. It operates from a single +5 volt supply. Refer to the following sections and tables for information on absolute ratings, standard test conditions, D.C. characteristics, A.C. parameters and timings.

D.C. SPECIFICATIONS

1. Absolute Maximum Ratings:

The absolute maximum ratings are as follows:

- A power supply voltage of -0.3 to 7.0 VDC.
- An ambient operating temperature of 0 to 70.0 degrees C.
- A storage temperature of -65.0 to +150.0 degrees C.

Caution: Stresses greater than those indicated may cause permanent damage to the device. Operation of the device at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

2. Standard Test Conditions:

The characteristics listed below are the test conditions, unless otherwise noted, for the "D.C. Characteristics" that follow. Note that voltages are referenced to GND and that positive current flows into the reference pin. The standard conditions are as follows:

- Vdd = 5.0 VDC $\pm$ 0.25 VDC
- GND = 0 VDC
- 0 degrees C< TA< 70 degrees C

3. D.C. Characteristics:

Table 2-3. D.C. Characteristics

PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
Voh-Output High Voltage	Vdd = min	2.4		Volts	Ioh=Iohmax*
Vol-Output Low Voltage	Vdd = min	0.4		Volts	Iol=Iolmax*
Vol-Output Low Voltage	Vdd = min	0.5		Volts	Iol=Iolmax* 48 ma. Driver
Vih-Input High Voltage		2.2		Volts	
Vil-Input Low Voltage			0.8	Volts	
Ii Input Current	Vdd = max		±10.0	uA	
Oiz			±10.0	uA	
Icc-Read Cycle 20 MHz, 40 MHz Clock	Vdd = max		100	mA	Ta = 70 deg. C

Note: See Table 2-4 for Signal Drive Strengths.

4. Output Driver Characteristics

Output signals have one of three types of drive strengths:
Type 2: Iolmax = 2.0 mA, Iohmax = -2.0 mA
Type 4: Iolmax = 4.0 mA, Iohmax = -4.0 mA
Type 8: Iolmax = 8.0 mA, Iohmax = -8.0 mA
Type 48: Iolmax = 48.0 mA

Table 2-5 below indicates the drive strength for each output driver signal.

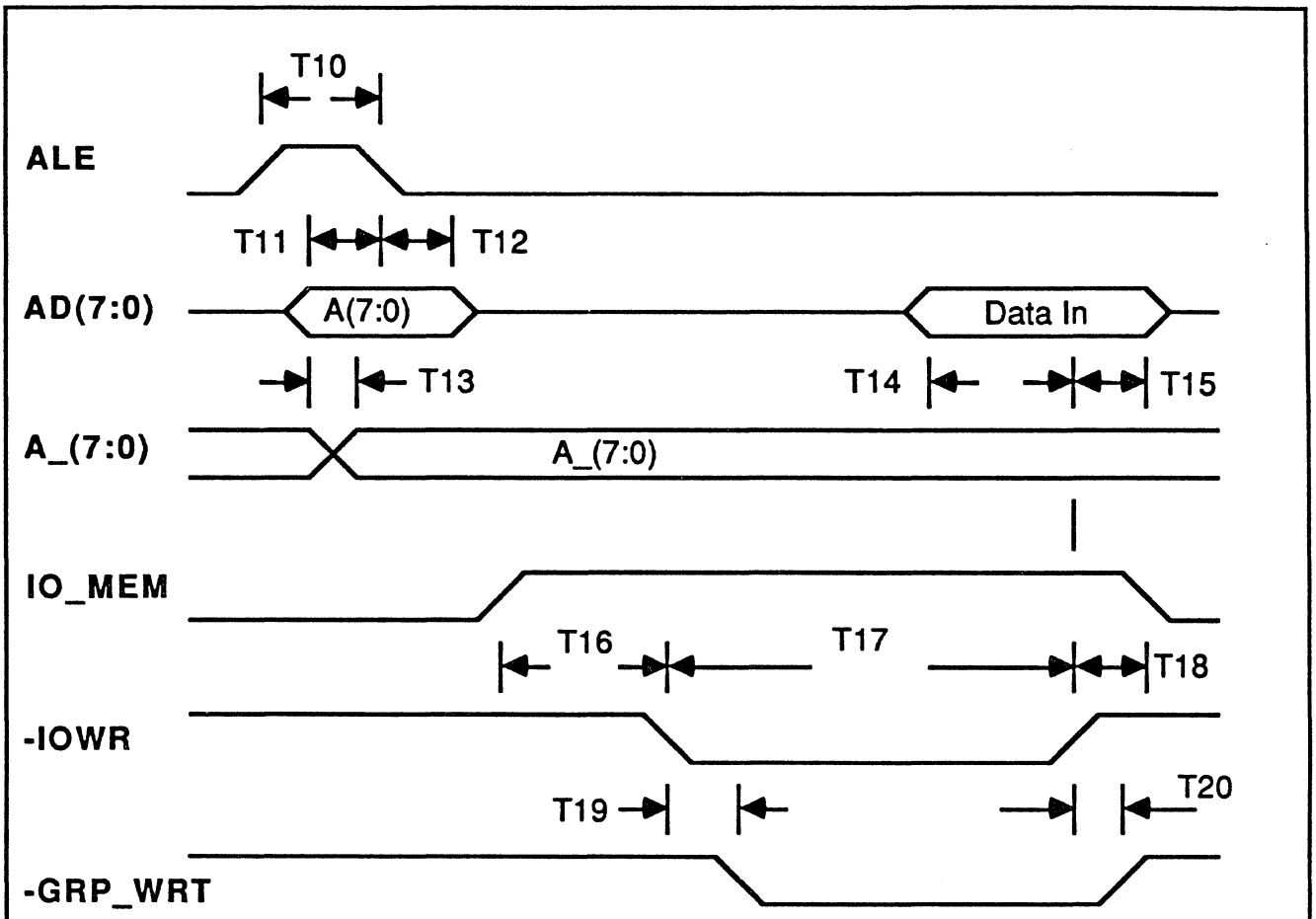
Table 2-4. Output Driver Signal Strength

Signal	Driver Type
A_(7:0)	2 MA
-ATN	48 MA
-ACK	48 MA
A/D(7:0)	2 MA
AM_ENABLE	2 MA
-BSY	48 MA
-C/D	48 MA
-GRP_RD	2 MA
-GRP_WT	2 MA
-HOST_D(7:0)&P	48 MA
INT_MEM	2 MA
INT_SEQ	2 MA
INT_SCSI	2 MA
-INP1(2:0)	2 MA
-I/O	48 MA
MEMA_(0-14)	2 MA
-MEMCE_(0-1)	2 MA
-MEMD0-7&P	2 MA
-MEMWRT	2 MA
-MSG	48 MA
NRZ_OUT	2 MA
OSC	2 MA
OSC_2	8 MA
-RESET_IN	48 MA
-RESET_OUT	2 MA
-RESET_CAP	8 MA
-REQ	48 MA
RD_GATE	2 MA
-SEL	48 MA
WRT_CLK	2 MA
WRT_GATE	2 MA

5. A.C. SPECIFICATIONS

The relevant timing diagrams and A.C. characteristics for interfacing the 82C5058 are provided in the following timing specification sections. These specifications are valid over the standard test conditions. All output timing assumes a capacitive load of 30 pf.

Microprocessor WRITE Internal Register Operation 8051 mode

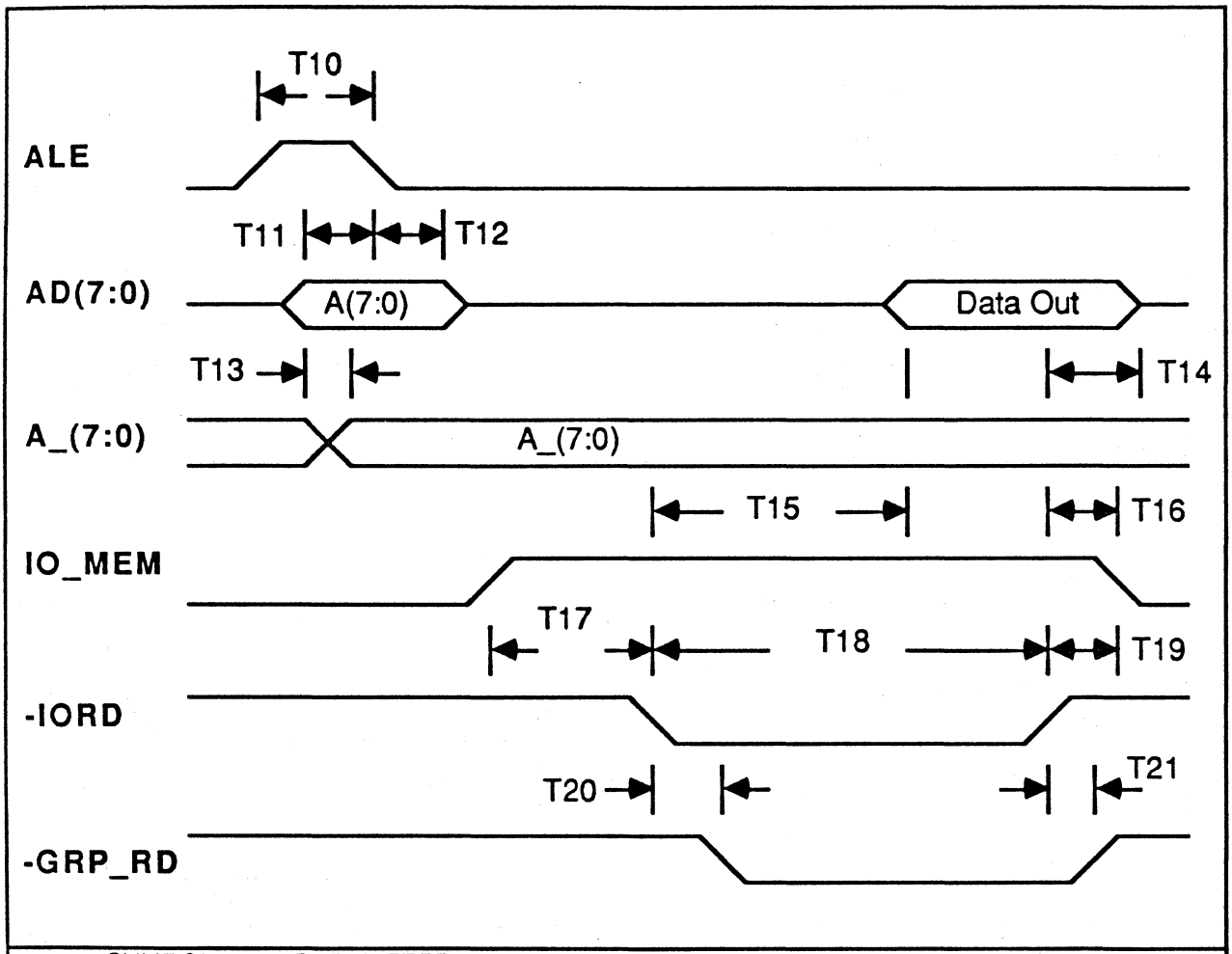


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	ALE pulse width	25		ns
T11	Address setup to ALE low	10		ns
T12	Address hold to ALE low	10		ns
T13	AD_(0-7) delay to MICRO_A(0-7)		25	ns
T14	Data setup to -IOWR high	15		ns
T15	Data hold to -IOWR high	15		ns
T16	IO_MEM setup to -IOWR low	15		ns
T17	-IOWR pulse width	50		ns
T18	-IO_MEM hold to -IOWR high	15		ns
T19	-GRPWRT low delay from -IOWR low		25	ns
T20	-GRPWRT high delay from -IOWR high		25	ns

Notes: 1. -GRPWRT is only asserted for address range 0Ch to 0Fh.

Figure 2-4. Microprocessor WRITE Internal Register Operation

Microprocessor READ Internal Register Operation 8051 mode

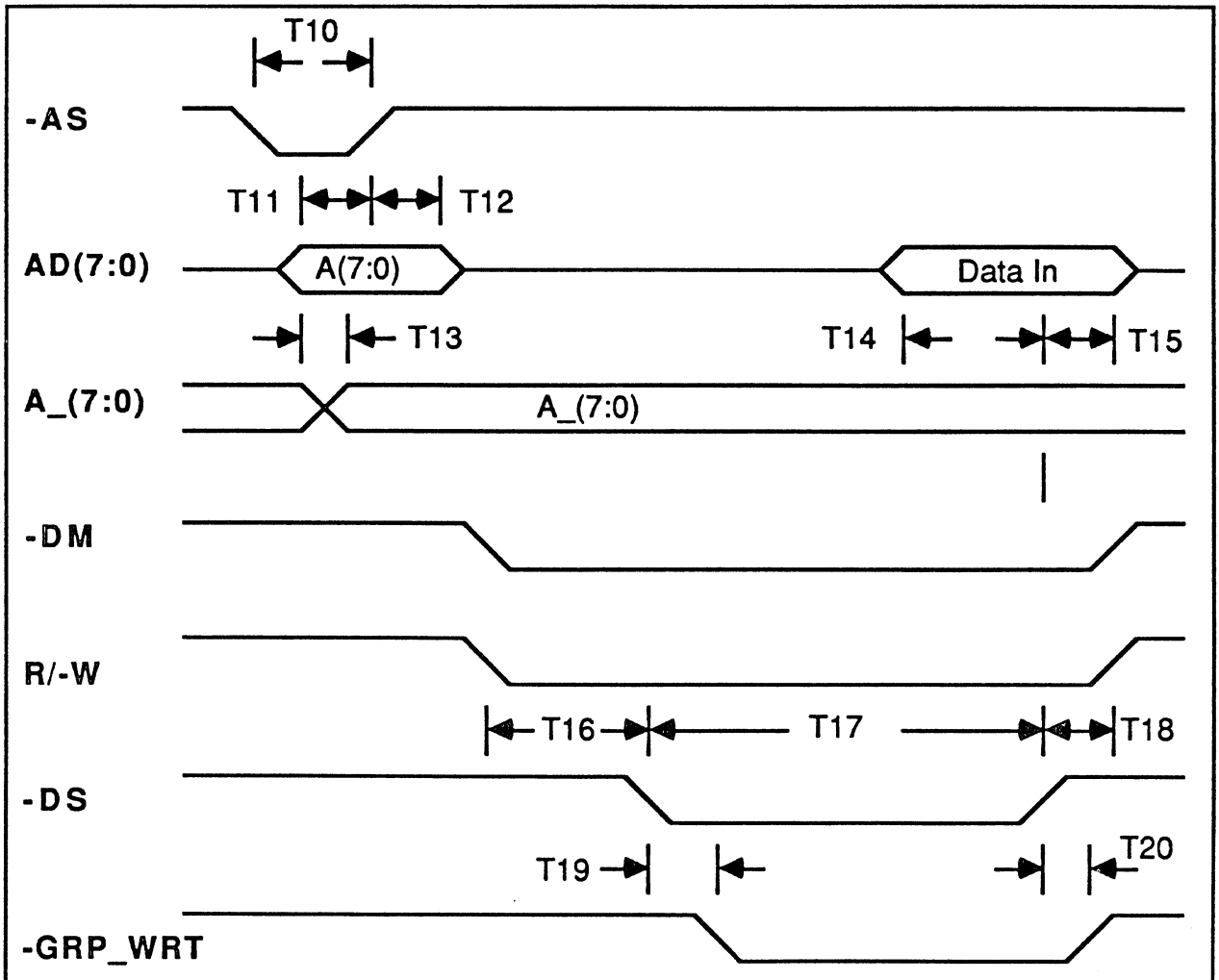


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	ALE pulse width	25		ns
T11	Address setup to ALE low	10		ns
T12	Address hold to ALE low	10		ns
T13	AD_(0-7) delay to MICRO_A(0-7)		25	ns
T14	-IORD high to data hi-z		25	ns
T15	-IORD low to data valid		40	ns
T16	-IORD high to data invalid	0		ns
T17	IO_MEM setup to -IORD low	15		ns
T18	-IORD pulse width	50		ns
T19	IO_MEM hold to -IORD high	15		ns
T20	-GRPRD low delay from -IORD low		25	ns
T21	-GRPRD high delay from -IORD high		25	ns

Notes: 1. -GRPRD is only asserted for address range 0Ch to 0Fh.

Figure 2-5. Microprocessor READ Internal Register Operation

Microprocessor WRITE Internal Register Operation Z8 mode

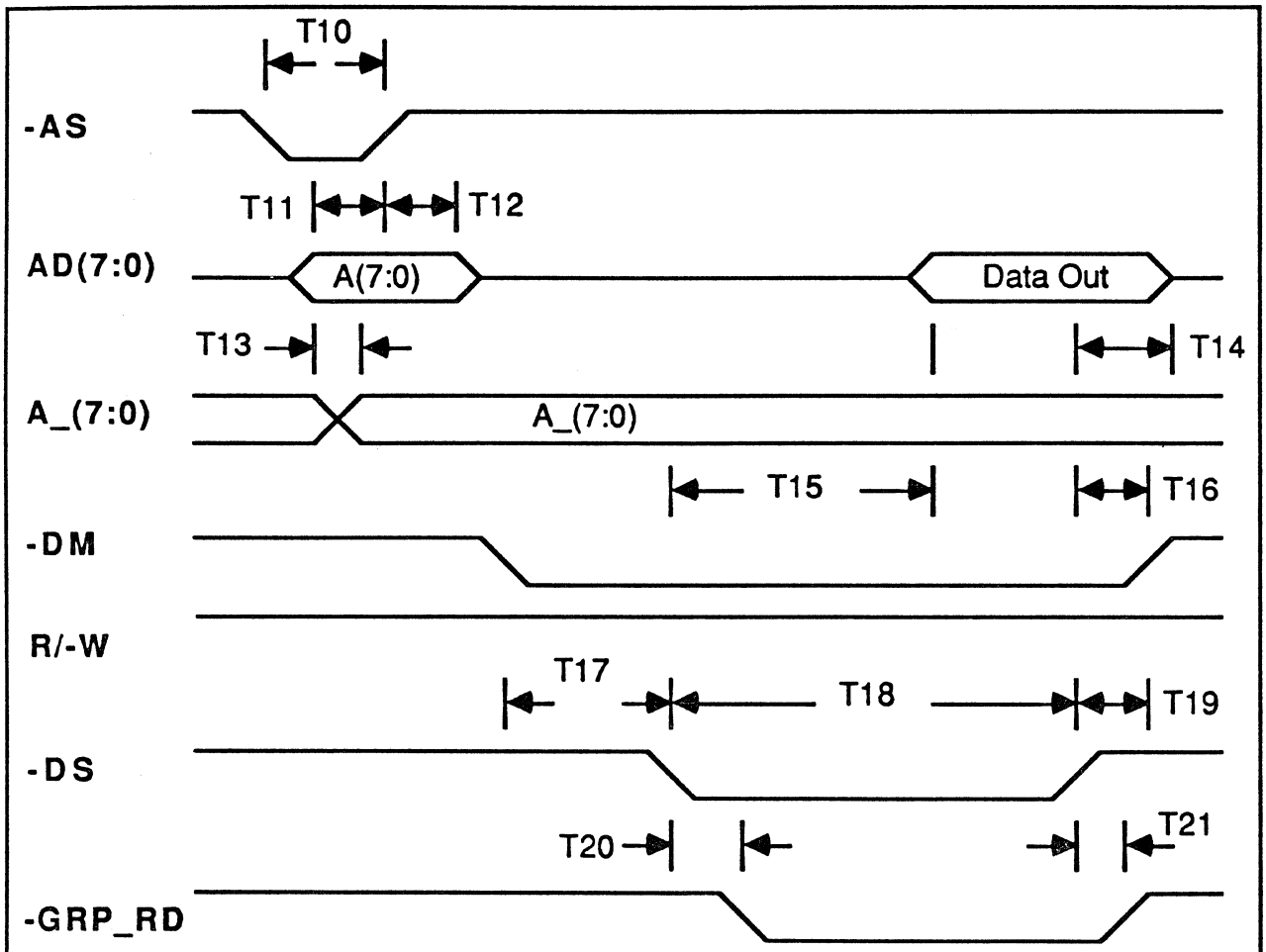


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-AS pulse width	25		ns
T11	Address setup to -AS high	10		ns
T12	Address hold to -AS high	10		ns
T13	AD_(0-7) delay to MICRO_A(0-7)		25	ns
T14	Data setup to -DS high	15		ns
T15	Data hold to -DS high	15		ns
T16	-DM & R/-W setup to -DS low	15		ns
T17	-DS pulse width	50		ns
T18	-DM & R/-W hold to -DS high	15		ns
T19	-GRPWRT low delay from-DS low		25	ns
T20	-GRPWRT high delay from -DS high		25	ns

Notes: 1. -GRPWRT is only asserted for address range 0Ch to 0Fh.

Figure 2-6. Microprocessor WRITE Internal Register Operation

Microprocessor READ Internal Register Operation Z8 mode

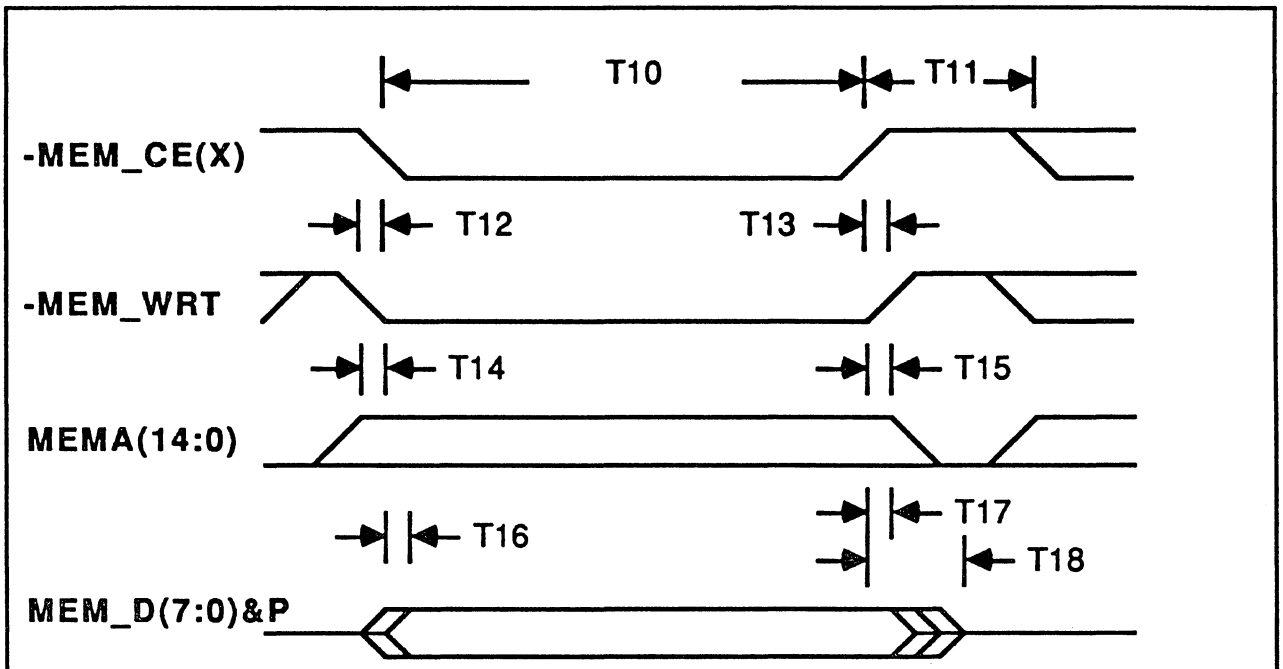


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-AS pulse width	25		ns
T11	Address setup to -AS high	10		ns
T12	Address hold to -AS high	10		ns
T13	AD_(0-7) delay to MICRO_A(0-7)		25	ns
T14	-DS high to data hi-z		25	ns
T15	-DS low to data valid		40	ns
T16	-DS high to data invalid	0		ns
T17	-DM & R-/W setup to -DS low	15		ns
T18	-DS pulse width	50		ns
T19	-DM & R/-W hold to -DS high	15		ns
T20	-GRPRD low delay from -DS low		25	ns
T21	-GRPRD high delay from -DS high		25	ns

Notes: 1. -GRPRD is only asserted for address range 0Ch to 0Fh.

Figure 2-7 Microprocessor READ Internal Register Operation

DMA Buffer WRITE Operation (Static Ram)

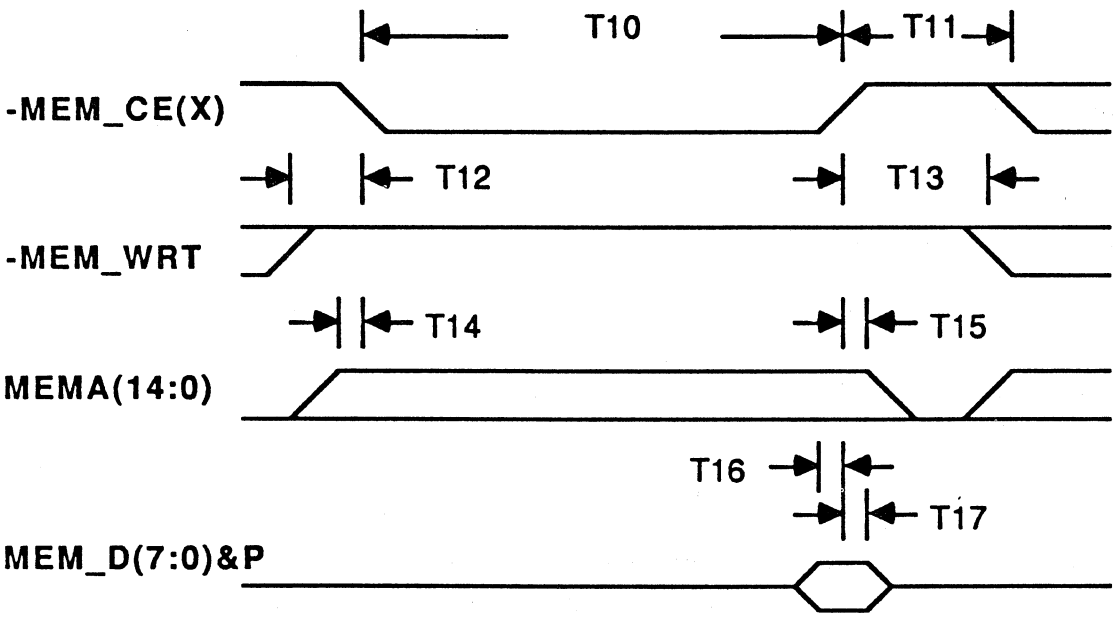


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-MEM_CE (0-1) low pulse width	n CP - 5		ns
T11	-MEM_CE (0-1) high pulse width	1 CP - 5		ns
T12	-MEM_WRT setup from -MEM_CE (0-1) low	2		ns
T13	-MEM_WRT hold from -MEM_CE (0-1) high	5		ns
T14	MEMA (0-14) setup from -MEM_CE (0-1) low	2		ns
T15	MEMA (0-14) hold from -MEM_CE (0-1) high	5		ns
T16	MEM_D (0:7) & P valid from -MEM_CE (0-1) low		0	ns
T17	MEM_D (0:7) & P invalid from -MEM_CE (0-1) high	5		ns
T18	MEM_D (0:7) & P tri-state from -MEM_CE (0-1) high		15	ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0-7) and MEM_D-P driven by this device.

Figure 2-8. DMA Buffer WRITE Operation SRAM

DMA Buffer READ Operation (Static RAM)

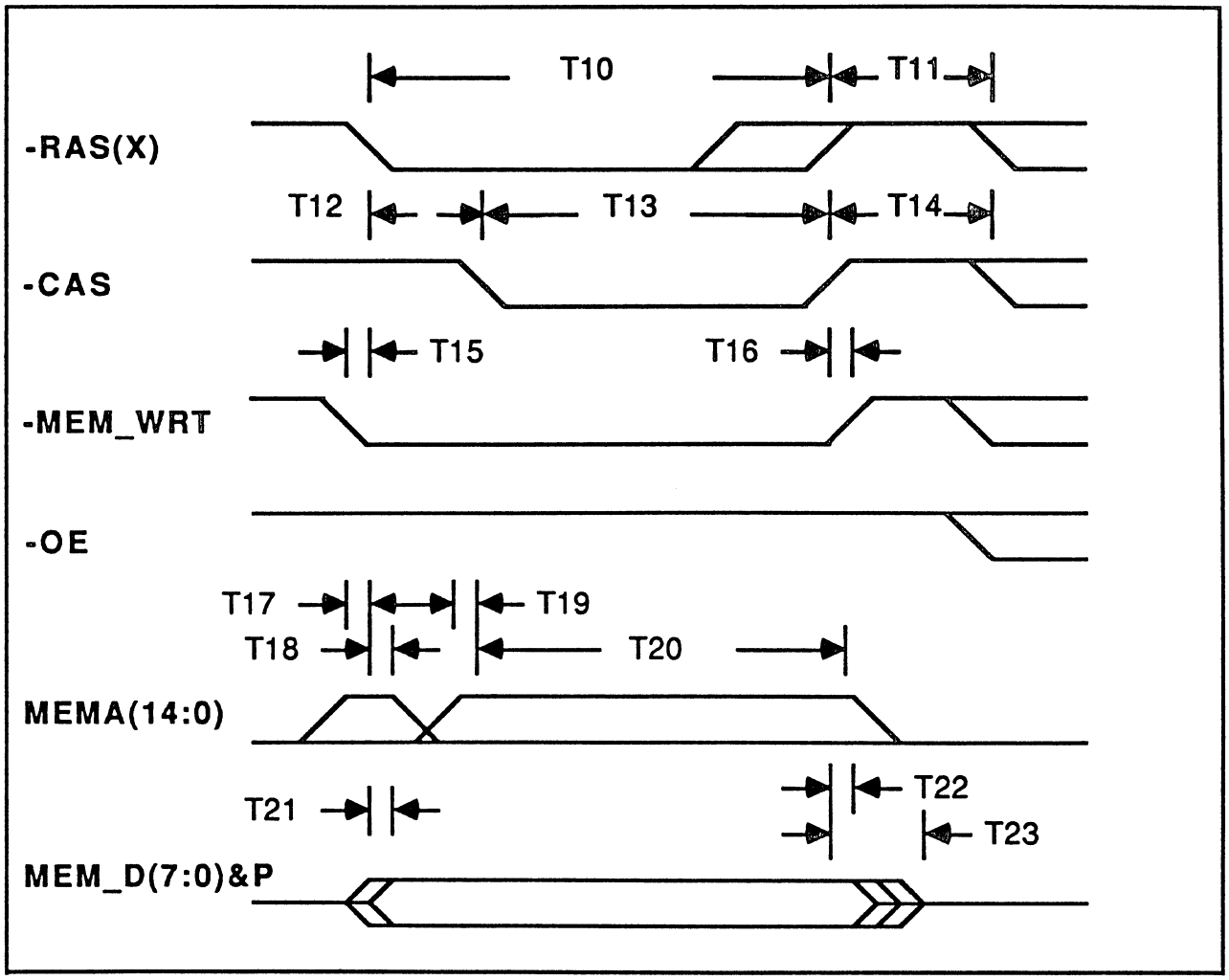


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-MEM_CE (0-1) low pulse width	n CP - 5		ns
T11	-MEM_CE (0-1) high pulse width	1 CP - 5		ns
T12	-MEM_WRT setup before -MEM_CE (0-1) low	5		ns
T13	-MEM_WRT hold after-MEM_CE (0-1) high	5		ns
T14	MEMA (0-14) setup from -MEM_CE (0-1) low	2		ns
T15	MEMA (0-14) hold from -MEM_CE (0-1) high	5		ns
T16	MEM_D (0:7) & P setup from -MEM_CE (0-1) high	5		ns
T17	MEM_D (0:7) & P hold from -MEM_CE (0-1) high	0		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0:7) driven by MEMORY device.
4. MEM_D-P driven by MEMORY device if PARITY ENABLED.

Figure 2-9. DMA Buffer READ Operation SRAM

DMA Buffer WRITE Operation (DYNAMIC Ram)

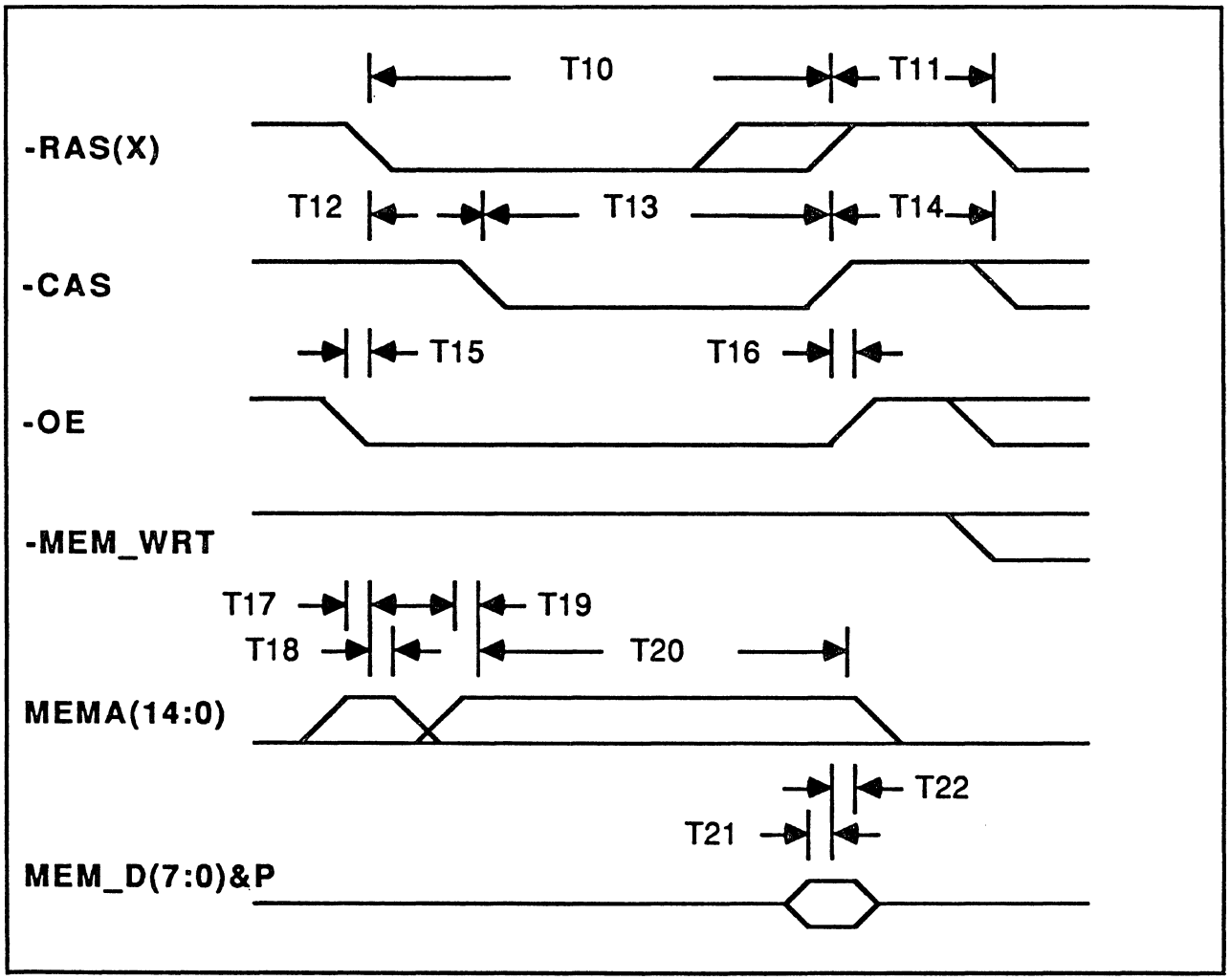


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-RAS (0-1) low pulse width	n CP - 5		ns
T11	-RAS (0-1) high pulse width	2 CP - 5		ns
T12	-RAS (0-1) low to -CAS low	1 CP - 5		ns
T13	-CAS low pulse width	n-1 CP - 5		ns
T14	-CAS) high pulse width	2 CP - 5		ns
T15	-MEM_WRT setup from -RAS (0-1) low	2		ns
T16	-MEM_WRT hold from -RAS (0-1) high	5		ns
T17	MEMA (0-9) setup from -RAS (0-1) low	2		ns
T18	MEMA (0-9) hold from -RAS (0-1) high	1 CP - 5		ns
T19	MEMA (10-19) setup from -CAS low	5		ns
T20	MEMA (10-19) hold from -CAS high	n-1 CP		ns
T21	MEM_D (0:7) & P valid from -RAS (0-1) low		0	ns
T22	MEM_D (0:7) & P invalid from -CAS (0-1) high	5		ns
T23	MEM_D (0:7) & P tri-state from -CAS (0-1) high		15	ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0-7) and MEM_D-P driven by this device.
4. -RAS(0-1) low programmable as n CP or n-1 CP.
5. If -RAS(0-1) low programmed as n-1 CP, -RAS high = 3 CP.

Figure 2-10. DMA Buffer WRITE Operation DRAM

DMA Buffer READ Operation (DYNAMIC RAM)

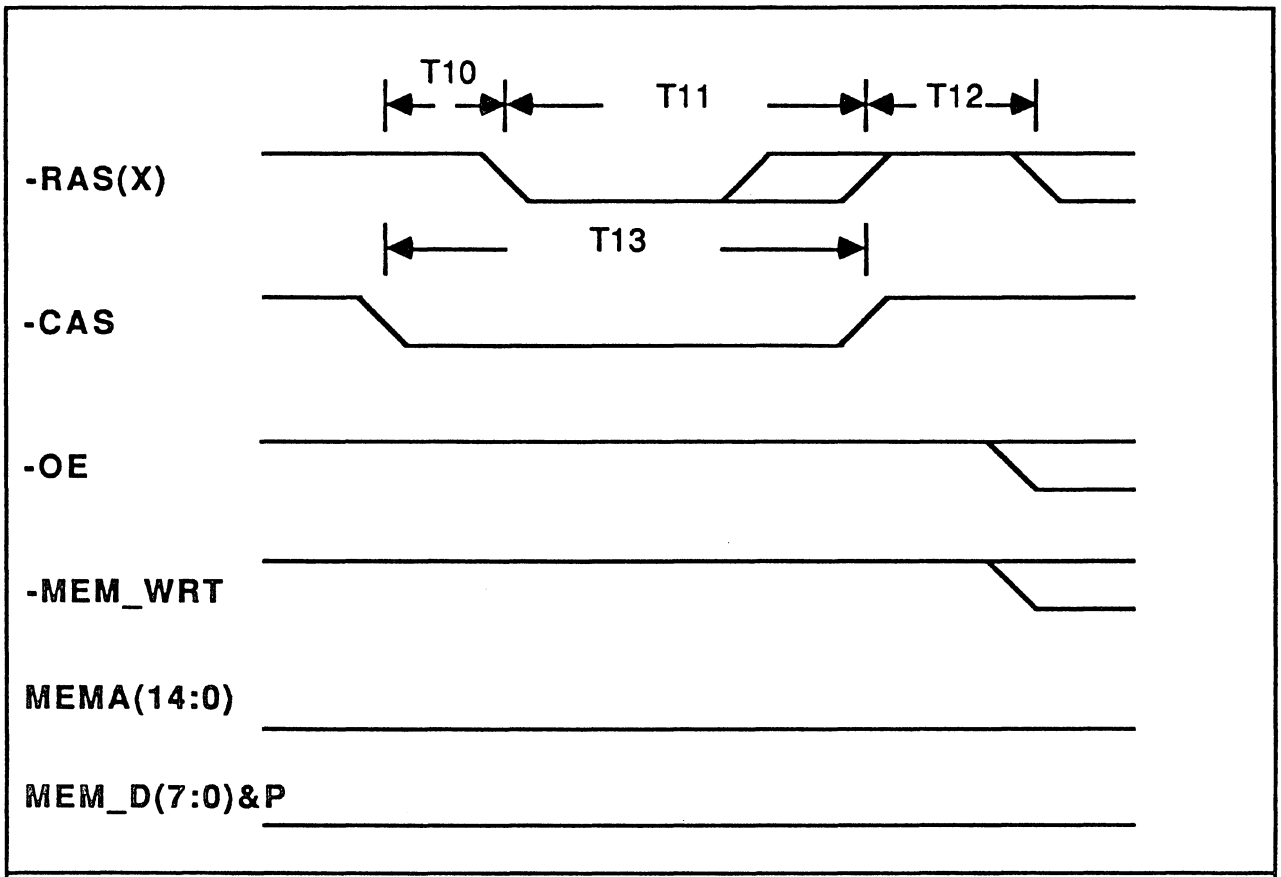


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-RAS (0-1) low pulse width	n CP - 5		ns
T11	-RAS (0-1) high pulse width	2 CP - 5		ns
T12	-RAS (0-1) low to -CAS low	1 CP - 5		ns
T13	-CAS low pulse width	n-1 CP - 5		ns
T14	-CAS) high pulse width	2 CP - 5		ns
T15	-OE setup from -RAS (0-1) low	2		ns
T16	-OE hold from -CAS high	5		ns
T17	MEMA (0-9) setup from -RAS (0-1) low	2		ns
T18	MEMA (0-9) hold from -RAS (0-1) high	1 CP - 5		ns
T19	MEMA (10-19) setup from -CAS low	5		ns
T20	MEMA (10-19) hold from -CAS high	n-1 CP		ns
T21	MEM_D (0:7) & P setup from -CAS high	5		ns
T22	MEM_D (0:7) & P hold from -CAS high	0		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. MEM_D (0-7) and MEM_D-P driven by the DRAM.
4. -RAS(0-1) low programmable as n CP or n-1 CP.
5. If -RAS(0-1) low programmed as n-1 CP, -RAS high = 3 CP.

Figure 2-11. DMA Buffer READ Operation DRAM

DMA Buffer REFRESH Operation (DYNAMIC RAM)

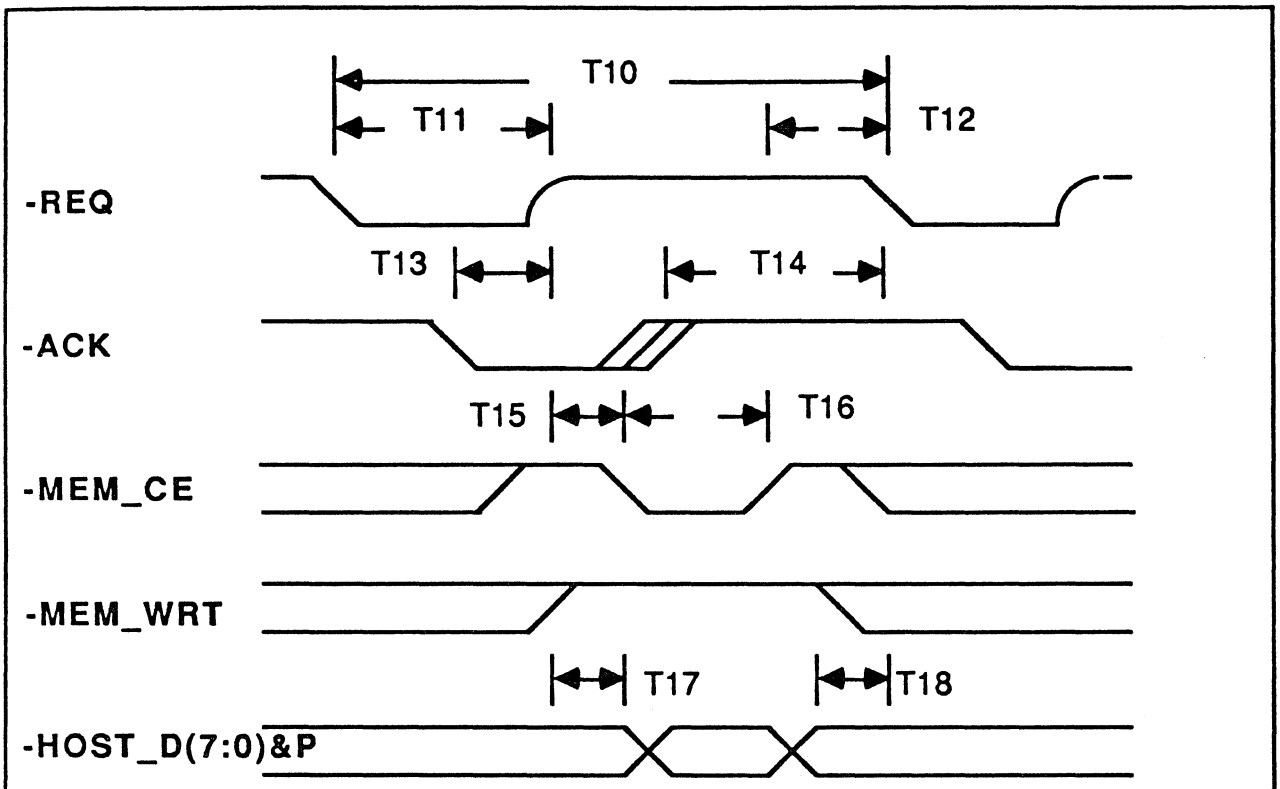


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-CAS low to -RAS(0-1) low	10		ns
T11	-RAS (0-1) low pulse width	n CP - 5		ns
T12	-RAS (0-1) high pulse width	2 CP - 5		ns
T13	-CAS low pulse width	n CP - 5		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. -RAS(0-1) low programmable as n CP or n-1 CP.
4. If -RAS(0-1) low programmed as n-1 CP, -RAS high = 3 CP.

Figure 2-12. DMA Buffer REFRESH Operation DRAM

SCSI Asynchronous DMA Data Transfer (Buffer to Host)

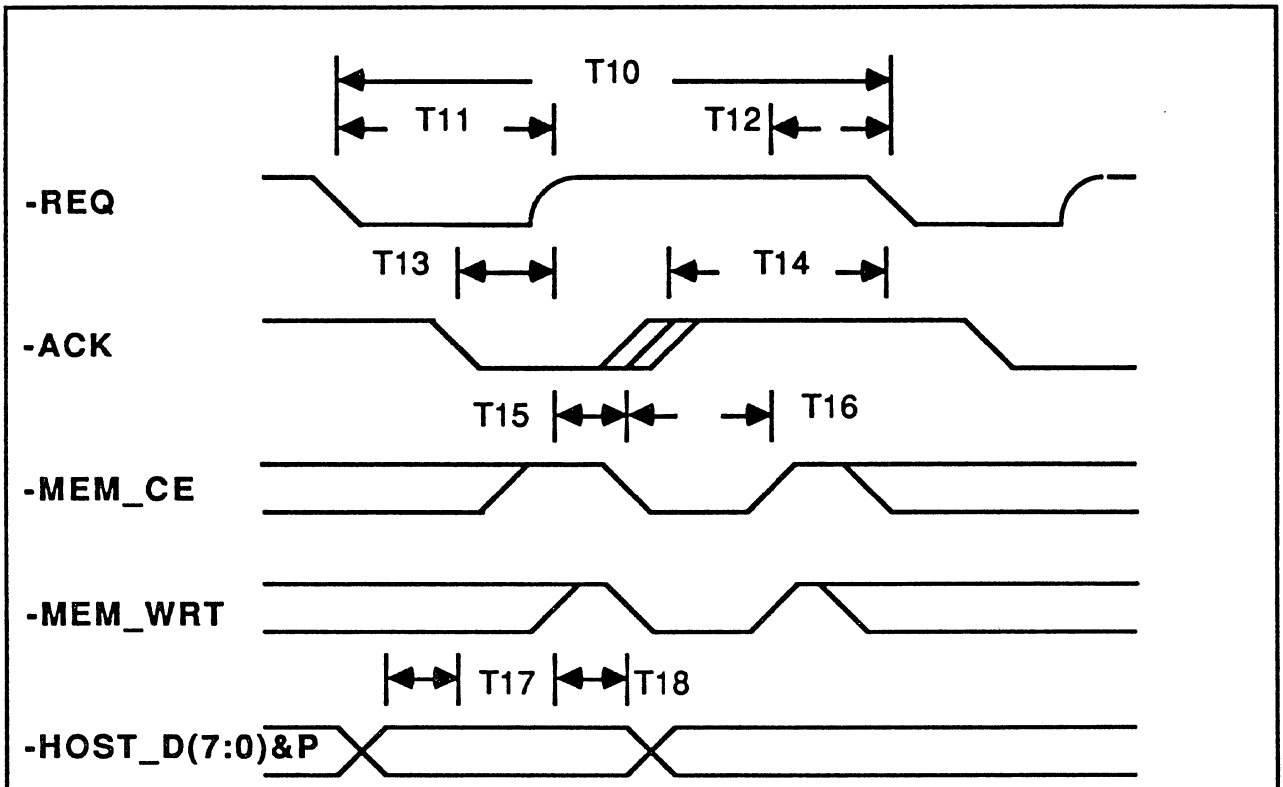


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-REQ low to -REQ low	8 CP		ns
T11	-REQ low pulse width	1 CP		ns
T12	-MEM_CE (0-1) high to -REQ low	2 CP		ns
T13	-ACK low to -REQ high	1 CP		ns
T14	-ACK high to -REQ low	2 CP		ns
T15	-REQ high to -MEM_CE (0-1) low	2 CP		ns
T16	-MEM_CE(1:0) low pulse width	n CP - 5		ns
T17	-HOST_D(7:0)&Parity hold after -REQ high	2 CP		ns
T18	-HOST_D(7:0)&Parity setup before -REQ low	2 CP		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. -REQ rise time is a function of an external pull-up.
4. -HOST_D(7:0) and Parity driven by this device.

Figure 2-13. SCSI Asynchronous DMA Data Transfer (Buffer to Host)

SCSI Asynchronous DMA Data Transfer (Host to Buffer)

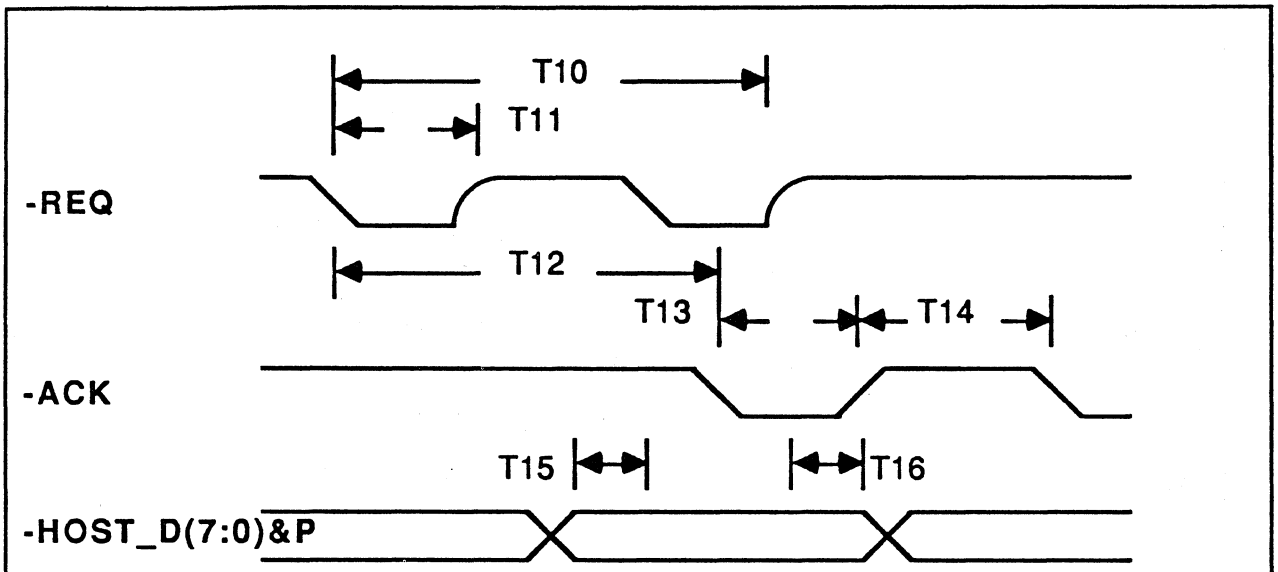


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-REQ low to -REQ low	8 CP		ns
T11	-REQ low pulse width	1 CP		ns
T12	-MEM_CE (0-1) high to -REQ low	2 CP		ns
T13	-ACK low to -REQ high	1 CP		ns
T14	-ACK high to -REQ low	2 CP		ns
T15	-REQ high to -MEM_CE (0-1) low	2 CP		ns
T16	-MEM_CE(1:0) low pulse width	n CP - 5		ns
T17	-HOST_D(7:0)&Parity setup before -ACK low	10		ns
T18	-HOST_D(7:0)&Parity hold after -REQ high	0		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. -REQ rise time is a function of an external pull-up.
4. -HOST_D(7:0) and Parity driven by the HOST.

Figure 2-14. SCSI Asynchronous DMA Data Transfer (Host to Buffer)

SCSI Synchronous DMA Data Transfer (Buffer to Host)

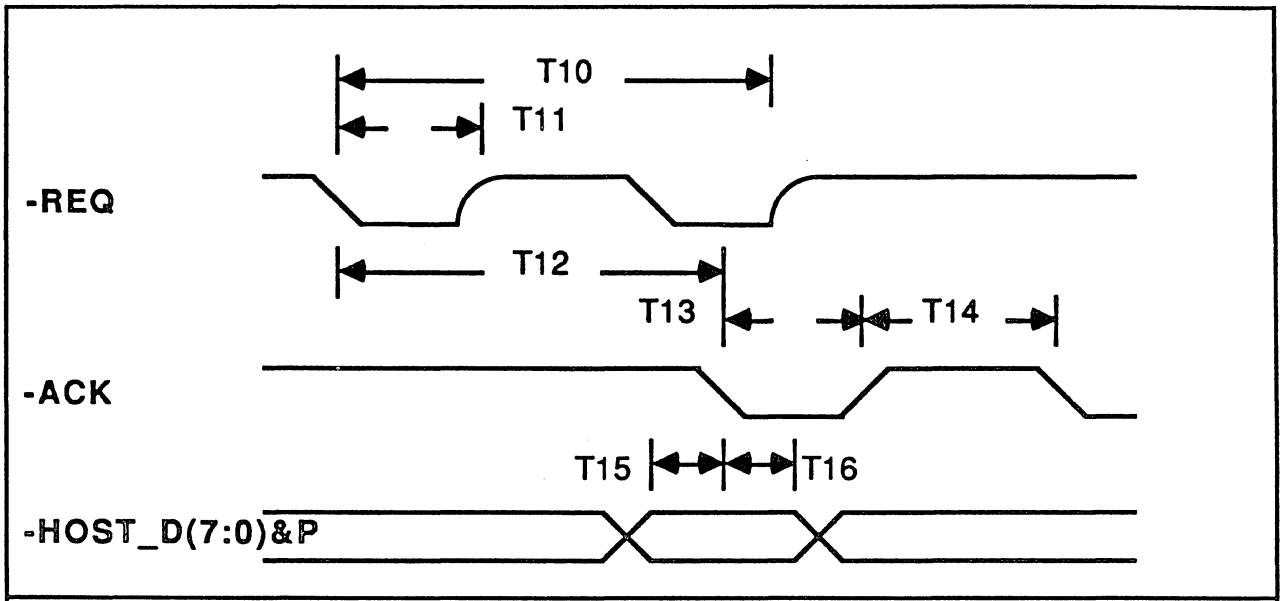


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-REQ low to -REQ low	4 CP		ns
T11	-REQ low pulse width	2 CP	3 CP	ns
T12	-REQ pulses before -ACK pulses	1	7	pulse
T13	-ACK low pulse width	2 CP		ns
T14	-ACK high pulse width	2 CP		ns
T15	-HOST_D(7:0)&Parity setup before -REQ low	1 CP		ns
T16	-HOST_D(7:0)&Parity hold after -REQ high	1 CP		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. -REQ rise time is a function of an external pull-up.
4. -HOST_D(7:0) and Parity driven by this device.
5. If REQ to REQ period <4 in WR-73, pulse width = 2 CP.
6. Offset count of REQ pulses before ACK pusle controlled by WR-72.

Figure 2-15. SCSI Synchronous DMA Data Transfer (Buffer to Host)

SCSI Synchronous DMA Data Transfer (Host to Buffer)

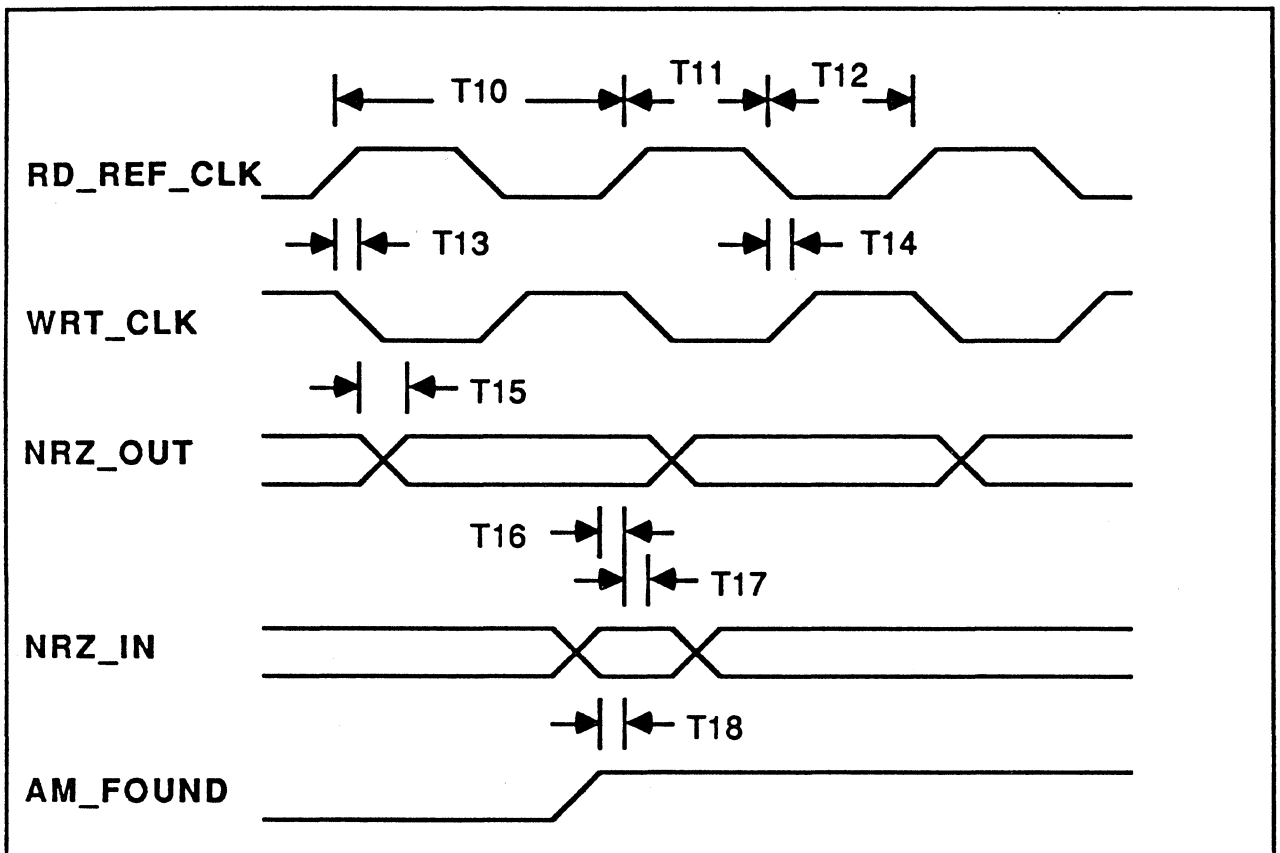


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	-REQ low to -REQ low	4 CP		ns
T11	-REQ low pulse width	2 CP	3 CP	ns
T12	-REQ pulses before -ACK pulses	1	7	pulse
T13	-ACK low pulse width	2 CP		ns
T14	-ACK high pulse width	2 CP		ns
T15	-HOST_D(7:0)&Parity setup before -ACK low	10		ns
T16	-HOST_D(7:0)&Parity hold after -ACK low	1 CP + 10		ns

Notes:
1. CP programmable OSC or OSC_2.
2. n programmable 2 to 5 CP cycles.
3. -REQ rise time is a function of an external pull-up.
4. -HOST_D(7:0) and Parity driven by the HOST
5. If REQ to REQ period <4 in WR-73, pulse width = 2 CP.
6. Offset count of REQ pulses before ACK pusle controlled by WR-72.

Figure 2-16. SCSI Synchronous DMA Data Transfer (Host to Buffer)

Drive Interface Timing Signals

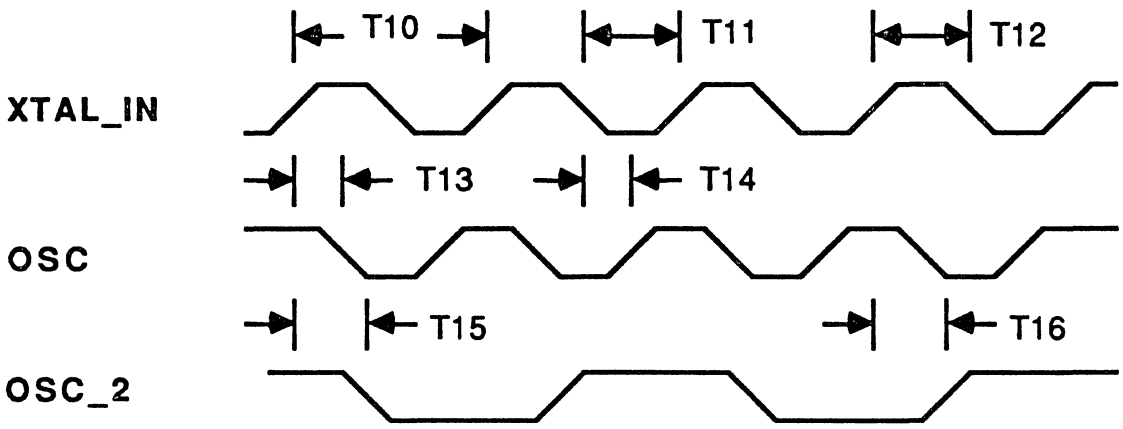


SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	RD_REF_CLK period	50		ns
T11	RD_REF_CLK high	22		ns
T12	RD_REF_CLK low	22		ns
T13	RD_REF_CLK high to WRT_CLK low		16	ns
T14	RD_REF_CLK low to WRT_CLK high		16	ns
T15	WRT_CLK low to NRZ_OUT delay		16	ns
T16	NRZ_IN setup to RD_REF_CLK rising	5		ns
T17	NRZ_IN hold to RD_REF_CLK rising	5		ns
T18	AM_FOUND setup to RD_REF_CLK rising	5		ns

Notes: 1. AM_FOUND only if in external sync mode.

Figure 2-17. DRIVE Interface Timing Signals

CLOCK input and output Timing Signals



SYMBOL	PARAMETER	MIN	MAX	UNIT
T10	XTAL_IN period	25		ns
T11	XTAL_IN low	10		ns
T12	XTAL_IN high	10		ns
T13	XTAL_IN high to OSC low		15	ns
T14	XTAL_IN low to OSC high		15	ns
T15	XTAL_IN high to OSC_2 low		20	ns
T16	XTAL_IN high to OSC_2 high		20	ns

Notes: 1. XTAL_IN driven by TTL clock.

Figure 2-18. CLOCK input and output Timing Signals

ESDI Interface Timing

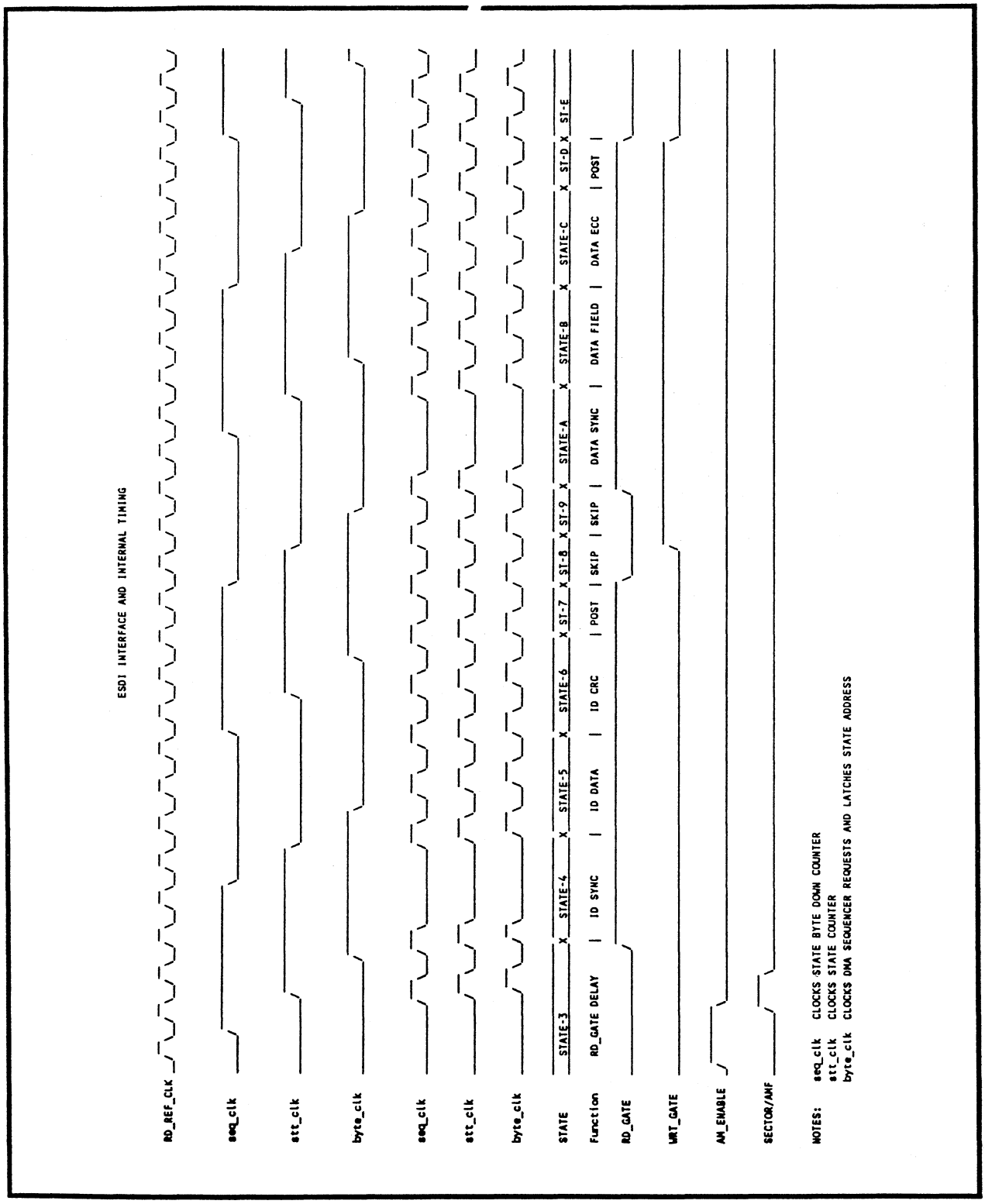


Figure 2-19. ESDI Interface Timing

Command to AM_ENABLE and RD_GATE Timing

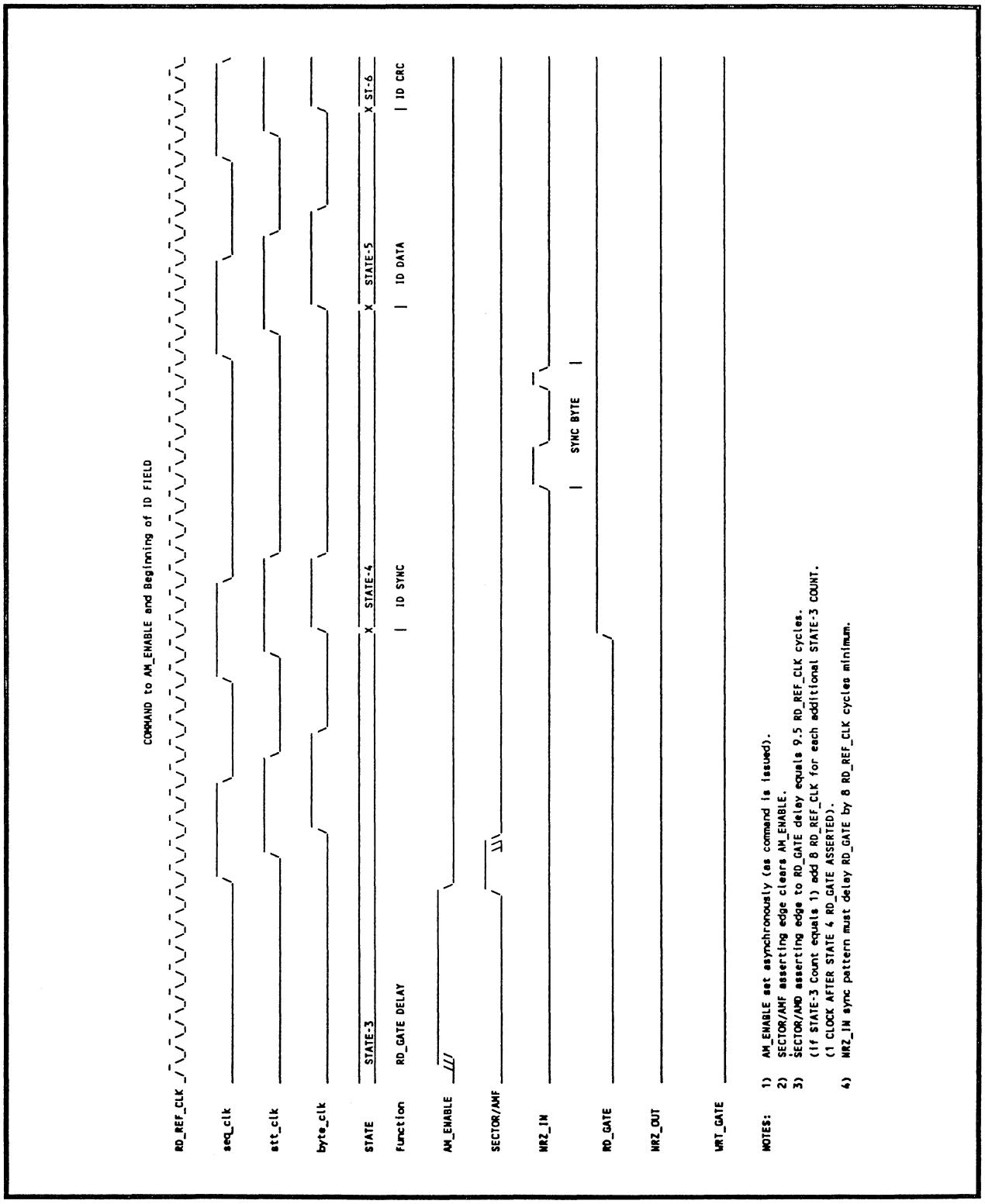


Figure 2-20. Command to AM_ENABLE and RD_GATE Timing

End of ID Field Beginning of DATA Field

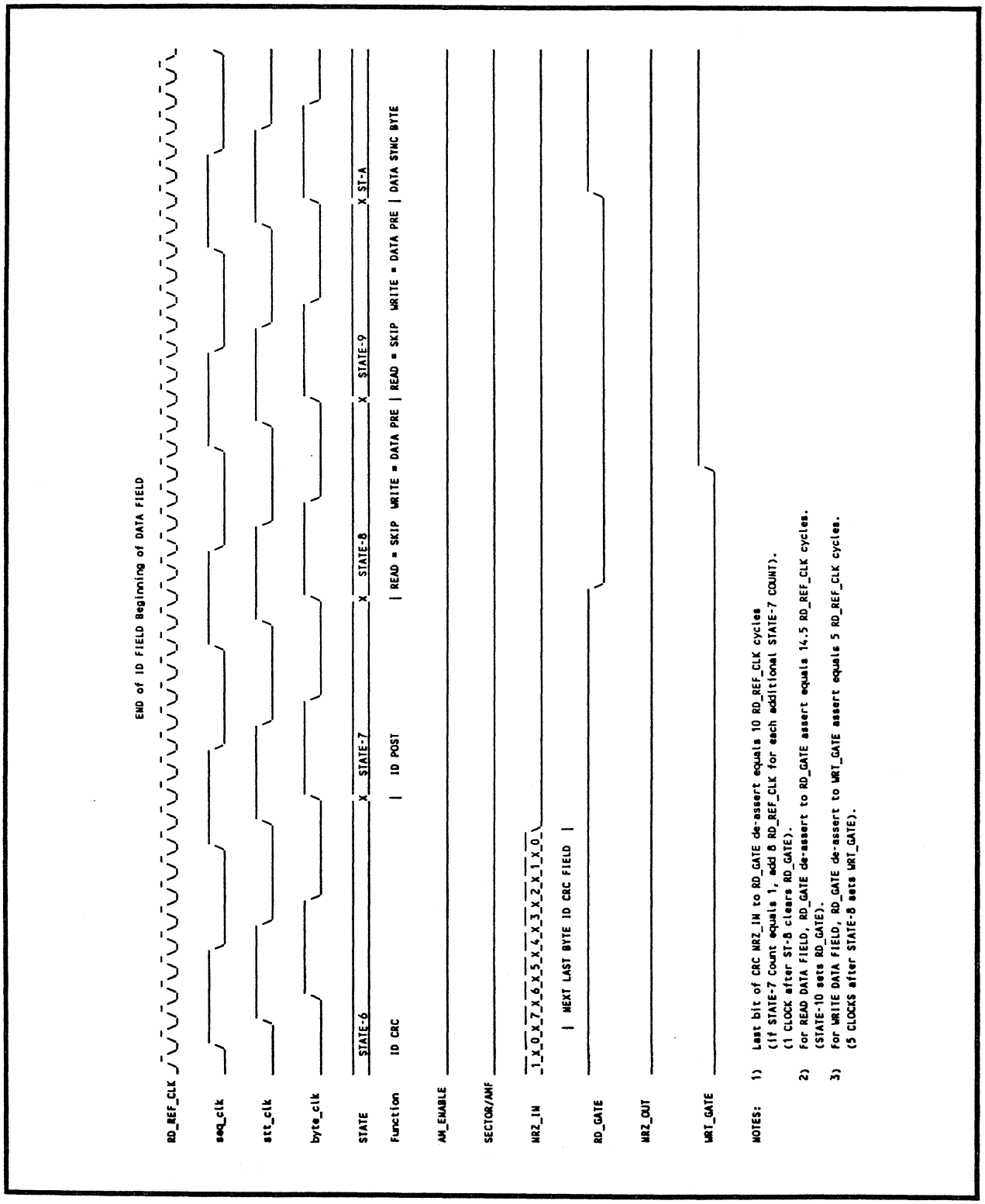


Figure 2-21. End of ID Field Begining of DATA Field

End of DATA Field (Loop State of 0Eh)

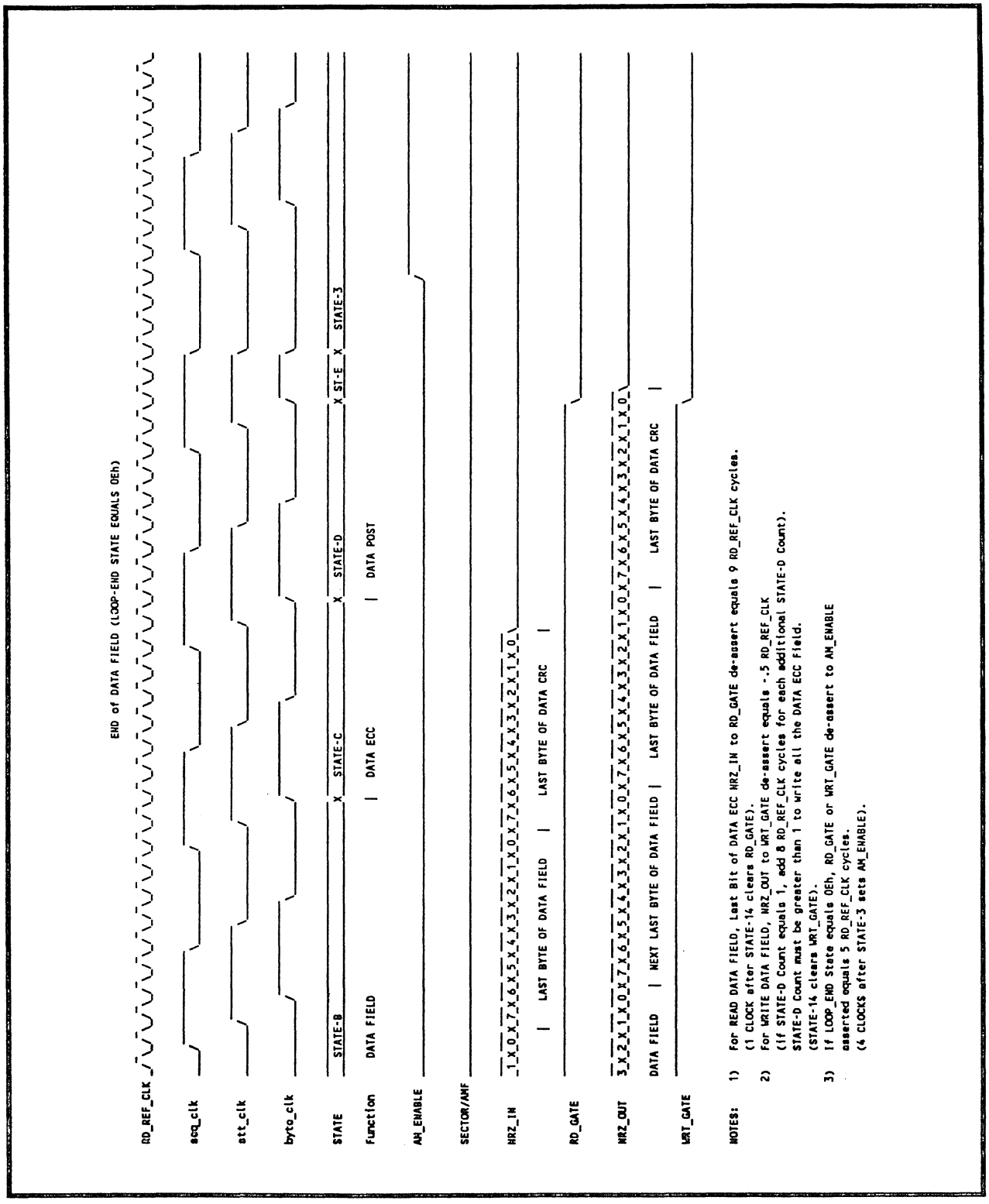


Figure 2-22. End of DATA Field (Loop State of 0Eh)

End of DATA Field (Lood State of 0Fh)

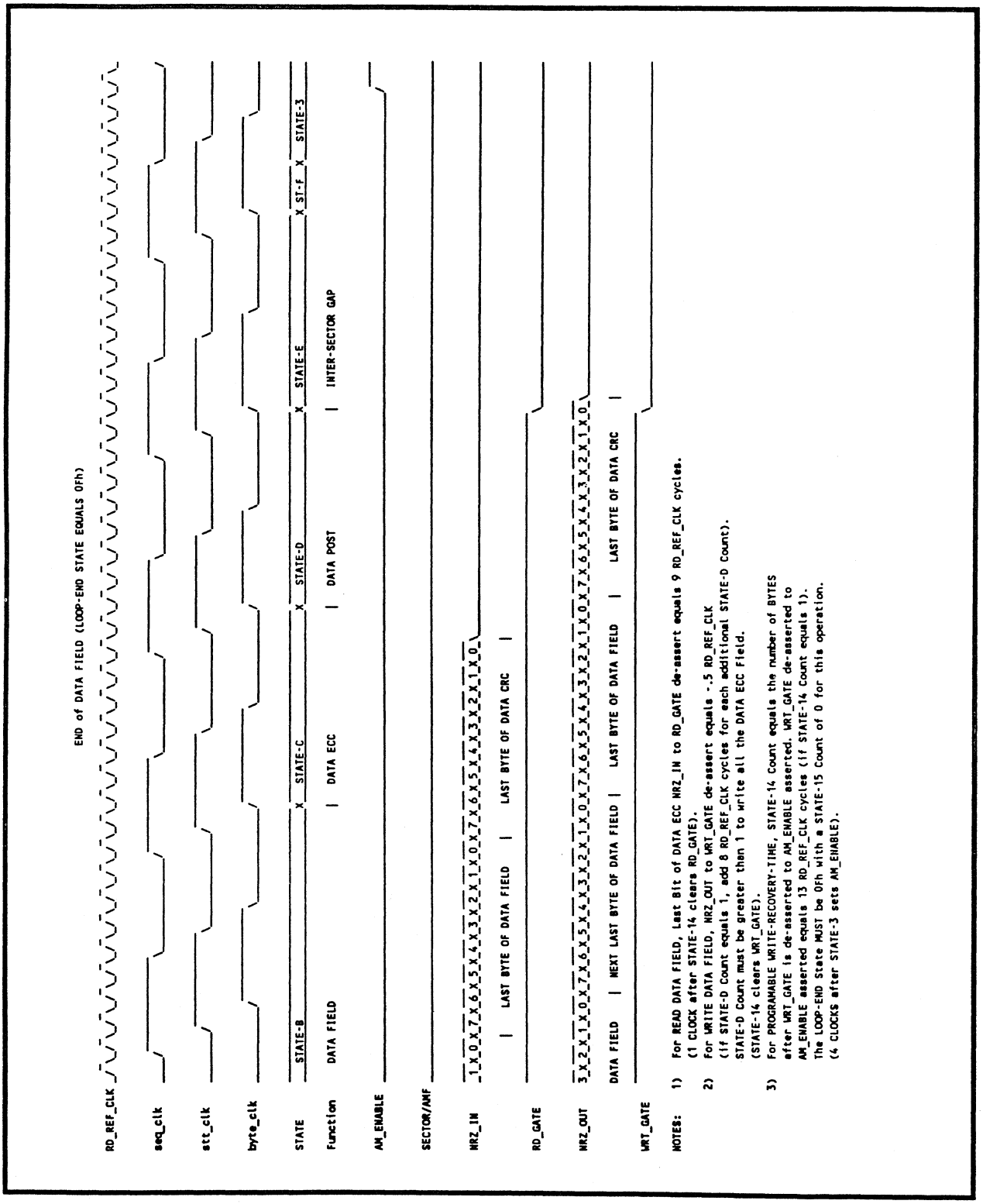


Figure 2-23. End of DATA Field (Loop State of 0Fh)

ESDI Format Track Timing

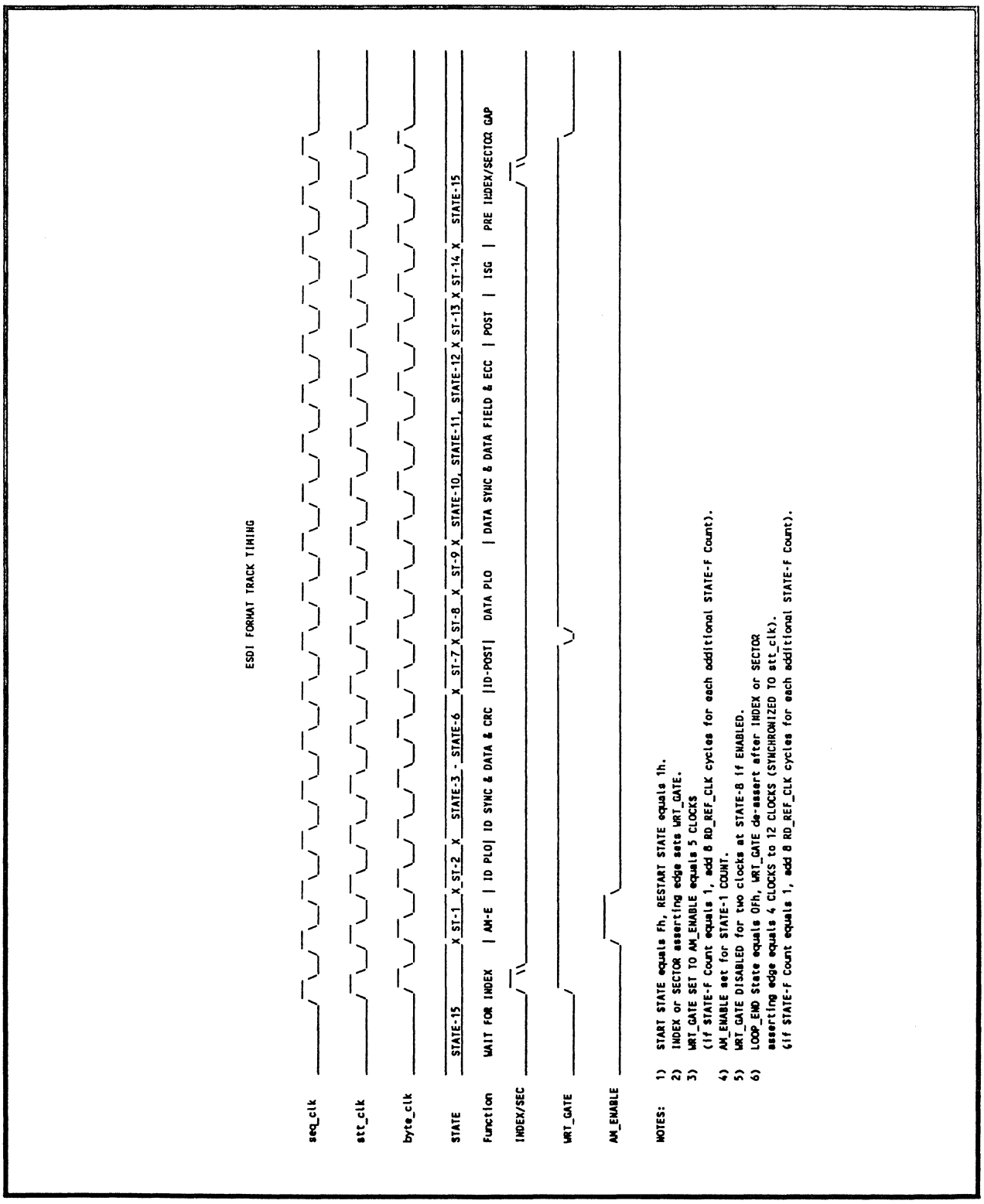


Figure 2-24. ESDI Format Track Timing

82C5058 Registers 3

The CHIPS 82C5058 is designed to offer the system designer greater flexibility by offering a broad range of choices in such matters as operational control, error recovery, timing parameters, physical media organization and format as well as the mode of communication with the SCSI interface. For this purpose, the 82C5058 presents the microprocessor with an easily accessed and programmable interface consisting of a collection of individually addressable byte-wide registers in four groups.

THE FOUR REGISTER GROUPS

The four functional groups of registers are:

- Memory Controller Registers
- Programmable Data Sequencer Registers
- SCSI Interface Registers
- Media Format Registers

The Memory Controller Registers and the Programmable Data Sequencer Registers are directly addressable. The Memory Controller Registers are used to control and monitor data block transfers between the data sequencer and the external RAM buffer and between the external RAM buffer and the SCSI interface. The Programmable Data Sequencer Registers are used to control and monitor the data sequencer (i.e., the data flow between the disk and the 82C5058); several of these registers are also used to indirectly access the media format RAM and hence to configure the disk media. The SCSI Interface Registers are used to configure this device for the proper mode of communication with the host and also perform a one time initialization for speed and device ID.

For the memory controller, there are 16 Write and 16 Read Registers--WR00-15 and RR00-15, respectively. Similarly, for the data sequencer there are 19 Write and 16 Read Registers, WR16-34 and RR16-31, and the SCSI interface has 10 Write and 7 Read Registers, WR64-73 and RR64-71.

The Media Format Registers (indirectly accessed as mentioned above) are a sequence of 16 pairs of byte-wide registers which are set to define the complete bit-sequential organization of each data track on a disk drive. Since disk format is rarely reconfigured after initialization, these registers are accessed indirectly; i.e., via the Programmable Data Sequencer Registers.

ACCESS TO REGISTERS

The registers in the CHIPS 82C5058 are accessed (written or read) in much the same way they are in any microprocessor peripheral component: a particular register is addressed and data is transferred over a byte-wide, bidirectional address/data bus on the microprocessor interface, AD0- 7. Note that the individual control signals and protocol recognized by the 82C5058 will vary according to the microprocessor (Z8 or 8051 type) and strapping the CONFIG (Configuration) control input pin to the 82C5058. In any case, the microprocessor first drives the selected I/O address onto the bus. The address latching signal, ALE (8051 type) or -AS (Z8 type), is then generated by the microprocessor and used by the 82C5058 to internally latch the address for register decoding. Finally, a single byte of data is then transferred over the bus under control of appropriate microprocessor access signals. Detailed timing information for these transfers is described in Chapter 2.

This addressable interface covers an I/O address range of 45 locations for the 82C5058--about one fourth of the typical microprocessor's I/O address space. In order to minimize external hardware requirements, the 82C5058 contains internal address decoding hardware which compares the full 8-bit I/O address as it is presented by the microprocessor and only responds to addresses in the low order 128 locations. Peripheral components connected to the AD0-7 bus are now free to decode higher-order addresses (where the most significant bit is a one) for device or register selection.

WRXX stands for Write Register XX and RRXX stands for Read Register XX, where XX is the decimal equivalent of the 8-bit address placed on AD-07.

I/O read or write operations may be performed by the microprocessor at any time; however, the firmware must take into account that access to some registers may only be appropriate at specific times during command processing.

Table 3-1 lists the Memory Controller Registers. Table 3-2 lists the Data Sequencer Registers. Table 3-3 lists the SCSI Interface Control Registers. Table 3-4 lists Media Format Registers (RAM). (Note that the latter are actually pairs of registers indirectly accessed through the Sequencer Registers.) Following these tables is a complete description of these registers.

Table 3-1. Memory Controller Registers

Control (Write) Registers

Write	Functions
WR00	Channel 0 Address 7-0
WR01	Channel 0 Address 15-8
WR02	Channel 0 Transfer Count 7-0
WR03	Channel 0 Transfer Count 15-8
WR04	Channel 1 Address 7-0
WR05	Channel 1 Address 15-8
WR06	Channel 1 Transfer Count 7-0
WR07	Channel 1 Transfer Count 15-8
WR08	Channel 0 Control
WR09	Channel 1 Control
WR10	Memory Cycle Timing
WR11	CRC/ECC Selection and Control
WR12	Group Write Strobe
WR13	Group Write Strobe
WR14	Group Write Strobe
WR15	Group Write Strobe

Status (Read) Registers

Read	Function
RR00	Channel Status
RR01	Not used
RR02	Channel 0 Transfer Count 7-0
RR03	Channel 0 Transfer Count 15-8
RR04	Not used
RR05	Not used
RR06	Channel 1 Transfer Count 7-0
RR07	Channel 1 Transfer Count 15-8
RR08	Not used
RR09	Not used
RR10	Not used
RR11	Memory to Peripheral Write Strobe
RR12	Group Read Strobe
RR13	Group Read Strobe
RR14	Group Read Strobe
RR15	Group Read Strobe

Table 3-2. Data Sequencer Registers

Control (Write) Registers

Write	Function
WR16	Sequencer Command
WR17	Sequencer Loop Count
WR18	Index Time-Out
WR19	Sub-Block Count
WR20	Cylinder (High Byte)
WR21	Cylinder (Low Byte)
WR22	Head/Flag
WR23	Sector Number
WR24	Micro to Memory
WR25	Sequencer Start/Restart
WR26	Sequencer Loop State and Format RAM Bank Select
WR27	Bit Ring Start Count and Added Control
WR28	ECC Control
WR29	Configuration Control
WR30	Seq Value Register @ Seq Start
WR31	Seq Count Register @ Seq Start
WR32	Optional DMA Control
WR33	DMA Bank Control
WR34	Optional Sequencer Control
WR35	Additional DMA Control
WR36 to	Reserved
WR63	Reserved

Status (Read) Registers

Read	Function
RR16	Sequencer Status
RR17	Extended Sequencer Status
RR18	Retry Count/State Address
RR19	Flag Byte
RR20	Cylinder (High Byte)
RR21	Cylinder (low Byte)
RR22	Head/Flag
RR23	Sector Number
RR24	Memory to Micro
RR25	Sequencer Loop Count
RR26	Test Register
RR27	Force Index Register
RR28	Force Sequencer Reset
RR29	Not used (Reserved)
RR30	Seq Value Register @ Seq Start
RR31	Seq Count Register @ Seq Start
RR32 to	Reserved
RR63	Reserved

Table 3-3. SCSI Interface Registers

Control (Write) Registers

Write	Functions
WR64	SCSI Interrupt Mask
WR65	SCSI Bus Control
WR66	SCSI Interface Command
WR67	Arbitration Timing 1
WR68	Arbitration Timing 2
WR69	SCSI Device ID
WR70	SCSI Data I/O Out (No Handshake)
WR71	SCSI Data I/O Out (With Handshake)
WR72	Synchronous Offset Control
WR73	Synchronous Transfer Period
WR74 to	Reserved
WR127	Reserved

Status (Read) Registers

Read	Function
RR64	SCSI Interrupt Status
RR65	SCSI Bus Status
RR66	SCSI Interface Device Status
RR67	Reserved
RR68	Input Port 1
RR69	SCSI Data I/O In (Direct)
RR70	SCSI Data I/O In (Latched, No Handshake)
RR71	SCSI Data I/O In (Latched, With Handshake)
RR72 to	Reserved
RR127	Reserved

Table 3-4. Media Format Registers (RAM)

Indirectly Addressed

Register Pair	Name
0	ESDI Sector Gap
1	Post-Index Gap
2	ID Preamble
3	ID Sync
4	ID Address Mark
5	ID Header
6	ID CRC/ECC
7	ID Postamble
8	Data Preamble
9	Data Sync
10	Data Address Mark
11	Data Field
12	Data CRC/ECC
13	Data Postamble
14	Inter-Sector Gap
15	Pre-Index/Sector Gap

REGISTER DESCRIPTIONS

1. MEMORY CONTROLLER REGISTERS

1.1 Write Registers

Write Register 00 and Write Register 04--Memory Addresses 7 through 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Memory Address Register (7-0) specifies the least significant byte of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). **This address is automatically incremented after each byte of data is transferred.** WR00 is for Channel 0; WR04 is for Channel 1.

Write Register 01 and Write Register 05--Memory Address 15 through 8

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Memory Address Register (15-8) specifies the most significant eight bits of the starting address in the buffer RAM of the memory block where data is available (for read), or where data is to be stored (for write). **This address is automatically incremented by the overflow of the Memory Address 7-0 Register (7-0).** WR01 is for Channel 0; WR05 is for Channel 1.

Write Register 02 and Write Register 06--Transfer Count 7 through 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

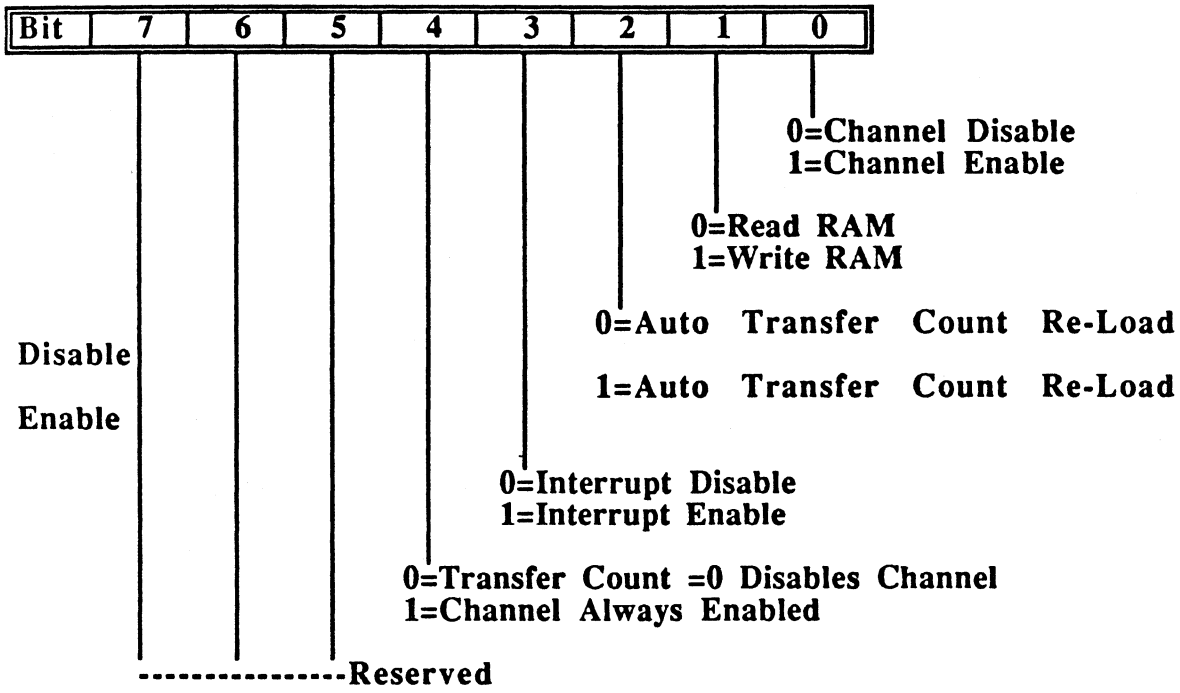
The Transfer Count 7-0 register specifies the least significant byte of the number of transfers to be performed. **The transfer count is automatically decremented after each transfer.** WR02 is for Channel 0; WR06 is for Channel 1. (N-1)

Write Register 03 and Write Register 07--Transfer Count 15 through 8

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

The Transfer Count Bits 15-8 register specifies the most significant eight bits of the number of transfers to be performed. **The transfer count is automatically decremented by the underflow of the corresponding Transfer Count Register (7-0).** WR03 is for Channel 0; WR07 is for Channel 1. **Note: The total 16 bit transfer counter must be loaded with (N-1) of the desired count.**

Write Register 08--Channel 0 Control



BIT 0 = Channel Control

Setting Bit 0=1, enables the channel; setting Bit 0=0 aborts a transfer in progress and disables the channel.

BIT 1 = Channel Read/Write

Bit 1 specifies the direction of the data transfer. When cleared, data is transferred from the RAM buffer memory to the Data Sequencer (or the RR24 in a Memory-to-Micro transfer). When set, data is transferred from the Data Sequencer (or from WR24 in a Micro-to-Memory transfer) to the RAM buffer memory.

BIT 2 = Transfer Count Reload

When Bit 2 set, and a block transfer is complete (Transfer Count = 0) the channel's Transfer Count register is automatically reloaded with its value prior to the transfer. This option allows transfer of a sequence of records without resetting the channel's Transfer Count registers between individual record transfers.

Note: For continuous operation, Bit 0 and Bit 4 must also be set to 1.

BIT 3 = Interrupt Enable/Disable

Bit 3 set enables interrupts (the assertion of INT MEM at the end of a block transfer when Transfer Count = 0); Bit 3 clear disables interrupts.

Note: The deasserting edge of the channel enable signal actually triggers INT MEM. Thus if Bit 4 (see below) is set (the channel is always enabled), then no interrupt will occur--even if Bit 3 is set.

Note: It is recommended not to set Bit 3 for interrupts unless Bit 4 is clear; i.e., the combination, Bit 3 = 1 and Bit 4 = 1, is not logical. When Bit 3 is set (and Bit 4 = 0), the microprocessor would normally respond by reading the Channel Status Register RR00, which tells what channel caused the interrupt, etc.

When Bit 3 is clear, interrupts from the channel are disabled. This option is available because, when only a single channel is being used, the memory interrupt (INT MEM) may not be required. The Sequencer Interrupt (INT SEQ) could be used to tell when a command has been completed.

BIT 4 = Channel Auto Disable

With Bit 4 cleared, the channel is automatically disabled when the Transfer Count reaches 0. To begin another operation on the channel, the Enable Bit (Bit 0) must be set by writing the Control Register.

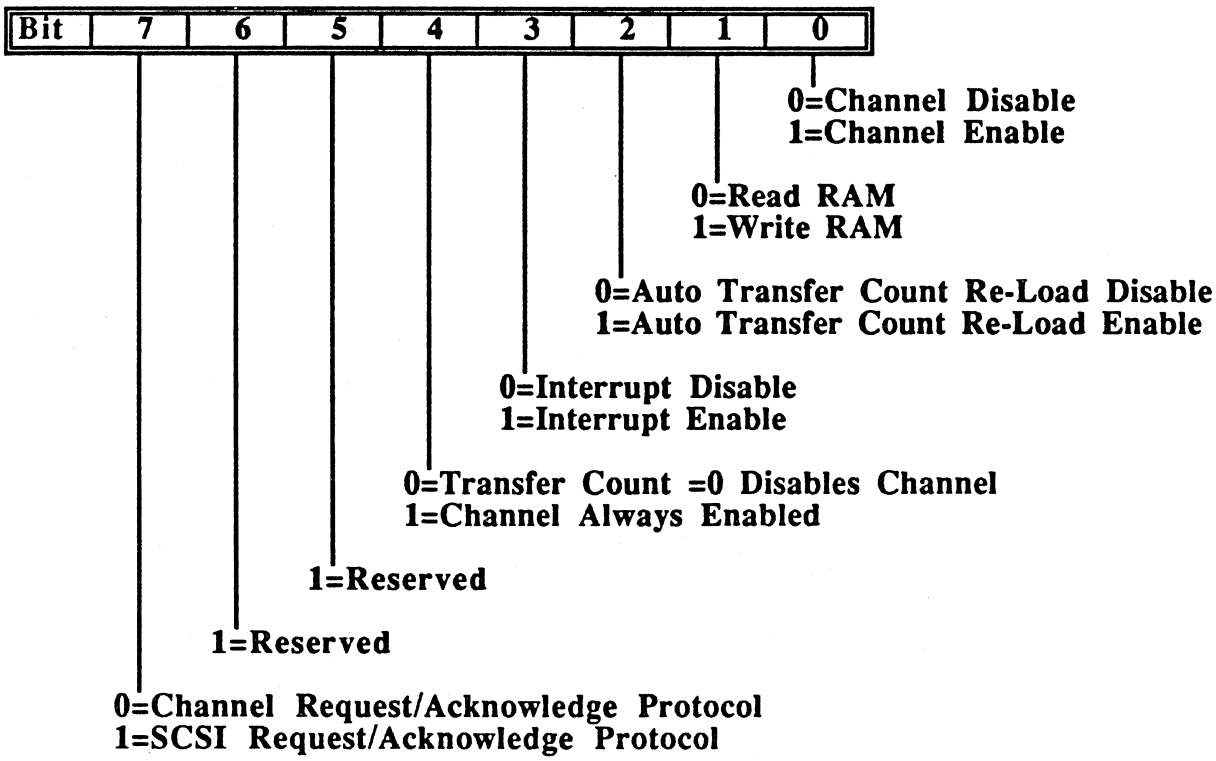
With Bit 4 set, the channel remains enabled after the Byte Count equals 0.

Note: Not all combinations of Bit 4 and Bit 3 are logical. See the note under Bit 3 above.

BITS 5-7 = Reserved

These bits are reserved and must be set to 0.

Write Register 09--Channel 1 Control



BIT 0 = Channel Control

Setting Bit 0=1, enables the channel. Setting Bit 0=0, aborts a transfer in progress and disables the channel.

BIT 1 = Channel Read/Write

Bit 1 specifies the direction of the data transfer. When Bit 1 is set=0, data transfer is from RAM buffer to SCSI interface; when Bit 1 is set=1 data transfer direction is from SCSI interface to the RAM buffer.

BIT 2 = Transfer Count Reload

With Bit 2 set, when a block transfer is complete (Transfer Count = 0) the channel's Transfer Count Register is automatically reloaded with its value prior to the transfer. This option allows the transfer of a sequence of records without resetting the channel's Byte Count Registers between individual record transfers.

Note: For continuous operation, Bit 0 and Bit 4 must also be set.

BIT 3 = Interrupt Enable/Disable

Bit 3 set =1 enables interrupts (the assertion of INT MEM at the end of a block transfer when Transfer Count = 0); Bit 3 set=0 disables interrupts.

Note: The deasserting edge of the channel enable signal actually triggers INT MEM. Thus if Bit 4 (see below) is set (the channel is always enabled), then no interrupt will occur--even if Bit 3 is set.

Note: It is recommended to set Bit 3 for interrupts unless Bit 4 is clear; or, i.e. the combination, Bit 3 = 1 and Bit 4 = 1, is not logical.

When Bit 3 is set (and Bit 4 = 0), the microprocessor would normally respond by reading the Channel Status register RR00, which tells what channel caused the interrupt, etc.

When Bit 3 is set=0, interrupts from the channel are disabled. This option is available because, when only a single channel is being used, the Memory Interrupt (INT MEM) may not be required. The Sequencer Interrupt (INT SEQ) could be used to tell when a command had been completed.

BIT 4 = Channel Auto Disable

With Bit 4 set=0, the channel is automatically disabled when the Transfer Count reaches 0. To begin another operation on the channel, the Enable Bit (Bit 0) must be set by writing the Control Register.

With Bit 4 set=1, the channel remains enabled after the Byte Count equals 0.

Note: Not all combinations of this Bit 4 and Bit 3 are logical. See the note under Bit 3 above.

BITS 5-6 = Reserved

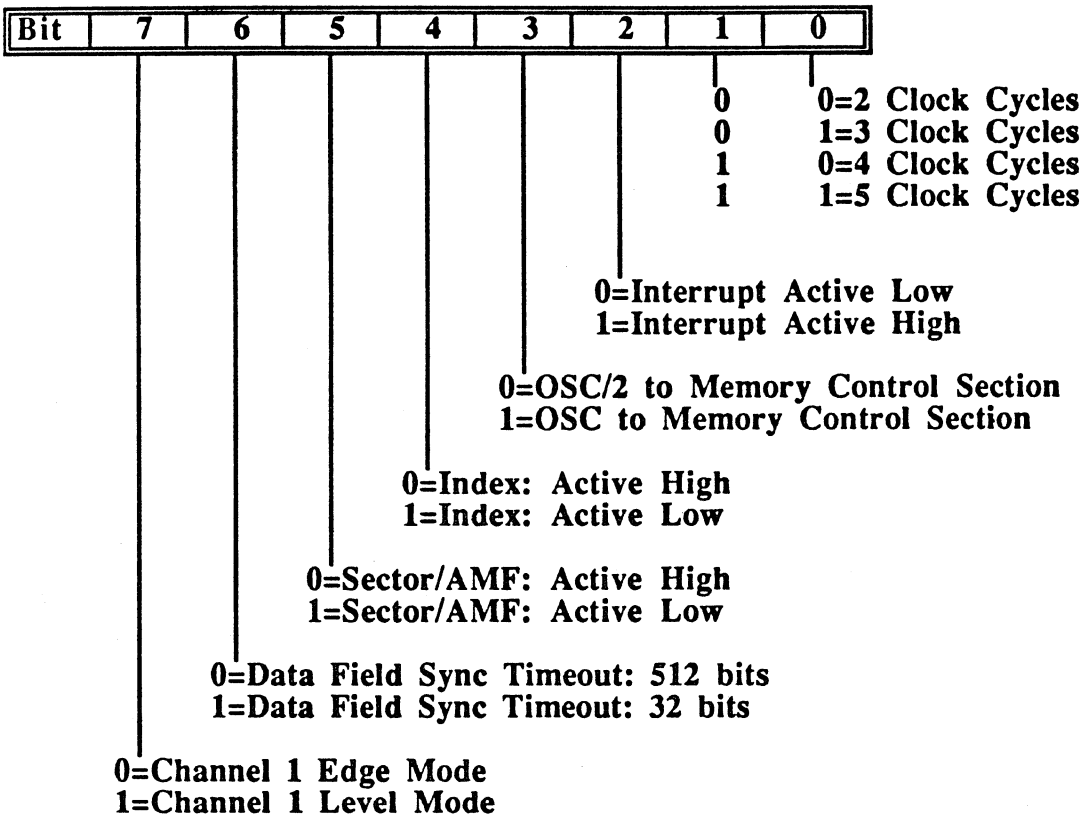
Bits 5 and 6 are reserved and must be set to 0.

BIT 7 = Protocol Select

When Bit 7 is set=0, the channel will use the Channel Request/Acknowledge protocol. The REQ1 pin (input) will function as a host request to the 82C5058, while the ACK1 pin (output) will function as an acknowledge from the 82C5058.

When Bit 7 is set=1, the channel will use the SCSI Request/Acknowledge Handshake protocol. The ACK1 pin on the 82C5058 will function as a request to the host (SCSI Request), while the REQ1 pin will function as the acknowledge (SCSI Acknowledge) from the host.

Write Register 10--Memory Cycle Timing



BITS 0-1 = Memory Cycle

Bits 0 and 1 specify the number of clock cycles to be used in the memory cycle for each transfer. A transfer will be a word transfer (8, 16, or 32 bits as programmed by WR32 Bits 6 and 7). This option is provided to accommodate a range of RAM buffer memory speeds.

Bits	Clock Cycle
00	2
01	3
10	4
11	5

BIT 2 = Interrupt Polarity

Bit 2 specifies the polarity of the memory controller's interrupt line (INT MEM). The polarity (high or low) of INTMEM will follow the state of the bit (i.e. if Set=1, the INTMEM is positive true).

BIT 3 = Memory Clock Select

Bit 3 specifies the clock signal frequency to be used within the memory control section of the device. When Bit 3 is set=1, the clock signal will be at the same frequency as the crystal (XTAL). When Set=0, the clock frequency will be one half the crystal (1/2 XTAL).

BIT 4 = Index Polarity

Bit 4 specifies the polarity of the INDEX input signal. If set=1, then INDEX will be low to high true. If set=0, INDEX will be high to low true.

BIT 5 = Sector/AMF Polarity

Bit 5 specifies the polarity of the SECTOR/AMF input signal. If set = 1, then SECTOR/AMF will be low to high true. If set=0, SECTOR/AMF will be high to low true.

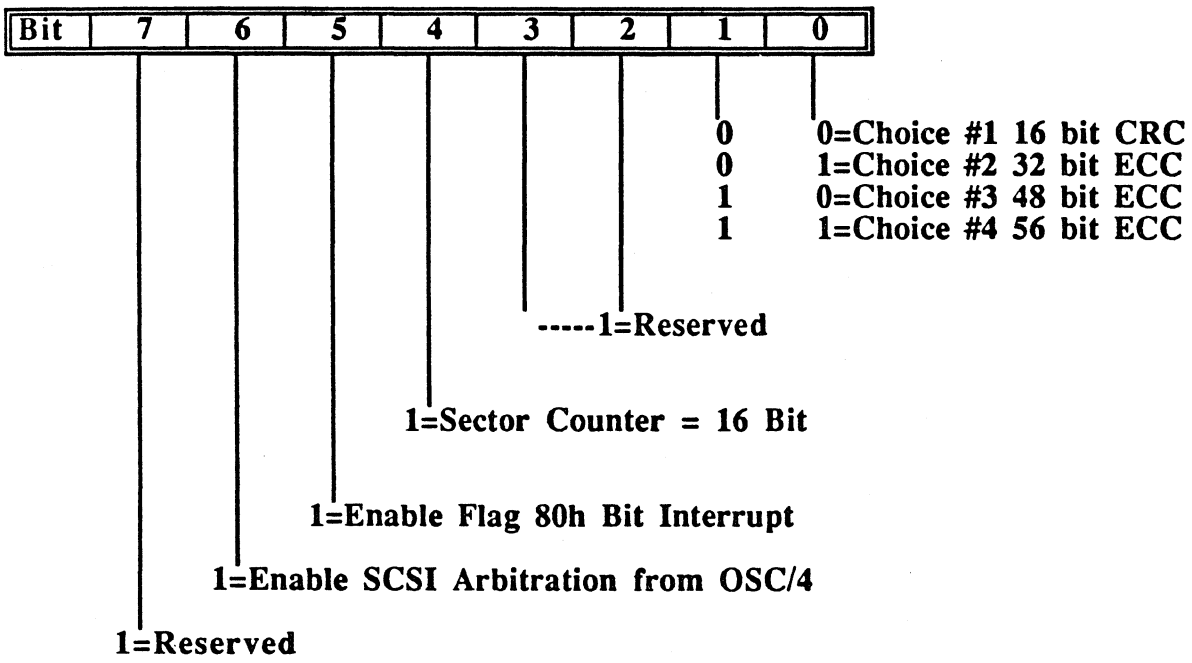
BIT 6 = Data Field Timeout Select

Bit 6 specifies the value of Data Sync Field Timeout (when enabled by Bit 7 or WR28). When Bit 6 is set=0, the timeout value is 512 bits for normal operation; when Bit 6 is set, the timeout is 32 bits for test purposes.

Bit 7 = Channel 1 Mode

Bit 7 specifies the channel 1 mode. When Bit 7 is set=0, REQ (1) is in Edge mode. When Bit 7 is set=1, REQ (1) is in Level mode and as long as REQ (1) is asserted, Channel 1 will continue generating memory cycles and ACK (1) pulses unless a higher priority channel overrides or the channel is disabled.

Write Register 11--CRC/ECC Polynomial Selection and Control



BITS 0-1 = ECC/CRC Select

Bits 0 and 1 select the CRC or ECC polynomial to be used for the data field. If Bit 6 of WR28 is cleared, the same polynomial will also be used for the ID field. If Bit 6 of WR28 is set, however, then the ID field will use the CRC polynomial (first selection listed below) regardless of the selection by Bits 0 and 1 (WR11).

The four possible selections by Bits 0 and 1 are:

Sel. #1: (X16)+(X12)+(X5)+1 (floppy compatible, CRC)
Sel. #2: (X32)+(X24)+(X18)+(X15)+(X14)+(X11)+(X8)+(X7)+1
Sel. #3: Proprietary. *
Sel. #4: Proprietary. *

* Contact SMS for Sublicense.

BITS 2-3 = Reserved

These bits are reserved and must be set to 0.

BIT 4 = Sector Count Select

If Bit 4 is set = 1, the data field length will be equal to the number of a 16 bit counter comprised of the count in State 11, as the low order byte of the counter, and the number loaded into the Sub-block Count WR19, as the high order byte of the counter. This feature is to provide any integer from 1 to 65535 byte per sector. If this bit is set = 0, the data field length will be equal to the product of the Sub-block Count minus 1 times the count in State 11.

BIT 5 = ID Interrupt Control

If Bit 5 is set = 1, this enables a sequencer interrupt that is the result of an ID Head Flag/Flag Byte having the 80h Bit on. If this option is enabled and the most significant flag bit is on, a sequencer interrupt will be generated after the ID has been processed. If other flag bits are on, the sequencer will not abort on flag conditions even if the Ignore ID Flag Bit in the Sequencer Command Register was not set. This sequencer interrupt will be cleared after the microprocessor reads the Extended Status Register RR17.

BIT 6 = SCSI Clock Select

If Bit 6 is set = 1, the timing reference clock for all the SCSI interface arbitration timing is derived from the XTAL_IN divided by four instead of the normal XTAL_IN divided by two. See WR67 and WR68 definition later in this chapter.

BIT 7 = Reserved

This bit are reserved and must be set to 0.

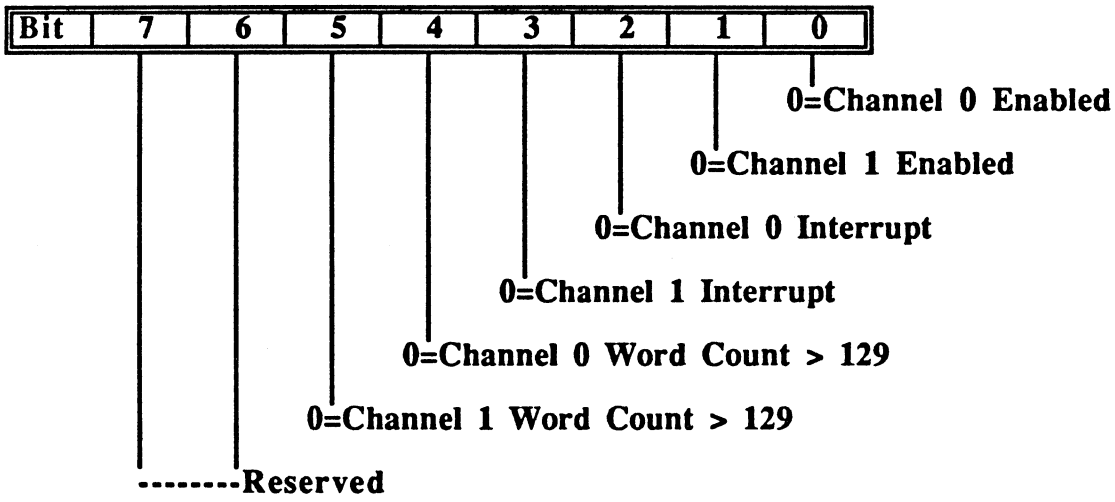
Write Register 12 through Write Register 15--External Group Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

When any of these registers is written, -GRPWRT is asserted. -GRPWRT can be used to strobe information from the microprocessor's data bus (AD0-7) into a peripheral device.

1.2 Read Registers

Read Register 00--Channel Status.



BITS 0-1 = Channel Status

Bits 0 and 1 reflect the status ("0" enabled, "1" disabled) of Memory Controller Channels 0 and 1, respectively.

BITS 2-3 = Channel Interrupt Status

Bits 2 and 3 reflect the interrupt status ("0" = interrupt, "1" = no interrupt) for Channels 0 and 1, respectively.

BITS 4-5 = Transfer Count Status

Bits 4 and 5 are set=0 for each channel when the last 128 transfers are in progress.

BITS 6-7 = Reserved

Bits 6 and 7 are reserved and always 1.

Read Register 02 and Read Register 06--Transfer Count 7 through 0

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

These registers contain the least significant byte (bits 0-7) of the current count in the Transfer Count Register. RR02 is for Channel 0; RR06 is for Channel 1.

Read Register 03 and Read Register 07--Transfer Count 8 through 15

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

These registers contain the most significant byte (bits 8 to 15) of the current count in the Transfer Count Register. RR03 is for Channel 0; RR07 is for Channel 1.

Read Register 11--Memory to Peripheral Write Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

RR11 is used in RAM buffer to peripheral transfers (see RR24 for a complete description of such transfers). When the microprocessor reads RR11, the sequencer generates -GRPWRT for writing data from RR24 into a peripheral device on the microprocessor address/data bus, AD0-7.

Read Register 12 through Read Register 15--External Group Strobe

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

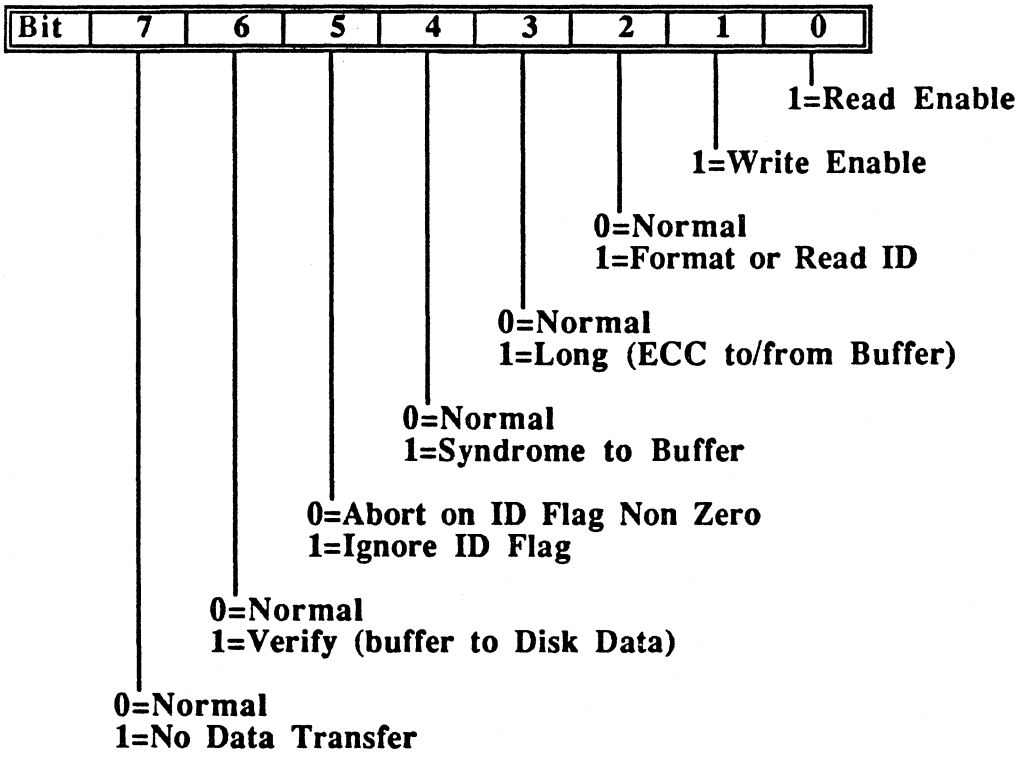
When any of these registers are read, -GRPRD is asserted. -GRPRD may be used to strobe information from a peripheral device onto the microprocessor's data bus.

When the Transfer Enable Bit (Bit 5) in the CRC/ECC Control Register (WR28) is set=1, a read of RR15 will enable data to be latched into the Micro-to-Memory Register (WR24). The rising edge of the strobe (-GRP_RD) will cause a DMA request and transfer the data from WR24 to the buffer.

2. DATA SEQUENCER REGISTERS

2.1 Write Registers

Write Register 16--Sequencer Command



A write to the Command Register initiates a command. The command is defined by the bit combination in this register and other data transfer registers. Valid combinations in this register are listed in Chapter 4 (Operation) in Table 4-1 (Sequencer Command Registers). Furthermore, the effect of each command (valid combination) is also provided there. **Here, only the effect of each bit is described in this section.**

BIT 0 = READ Type Command

When Bit 0 is set=1, the operation is a READ command: data is transferred from the disk to the RAM buffer.

BIT 1 = WRITE Type Command

When Bit 1 is set=1, the operation is a WRITE command: data is transferred from the RAM buffer to the disk.

If Bit 0 is set=1, then Bit 1 must not be set, and vice versa.

The remaining bits (2-7) are command modifiers and, depending on whether an operation is a read or a write, have different meanings.

BIT 2 = FORMAT Option

If Bit 2 is set=1 and the operation is a read (Bit 0 set=1), then only the ID fields will be read (READ ID command).

If Bit 2 is set=1 and the operation is a write (Bit 1 set), then the command is one of the format commands (FORMAT TRACK, FORMAT TRACK LONG, or FORMAT SECTOR).

BIT 3 = LONG Option

If Bit 3 is set=1, then both the data and the CRC/ECC check bits will be written to or read from the RAM buffer. (These are the various LONG operations described in the command set.)

BIT 4 = SYNDROME Option

If Bit 4 is set=1 and the operation is a READ LONG type (Bit 0 is set=1, Bit 3 is set=1), then both the data and the syndrome bytes (the result of the ECC check) are written to the RAM buffer. This applies to READ SYNDROME LONG, READ ID SYNDROME LONG, READ SYNDROME (LONG)-IGNORE FLAG, VERIFY SYNDROME LONG, and the VERIFY SYNDROME LONG-IGNORE FLAG Commands.

BIT 5 = FLAG Option

If Bit 5 is set=0, operation will abort if a flag condition exists.

Note: Flag information is contained in either bits 7-4 of byte 2 (Flag/Head Byte) of the ID Header field, or it is contained in byte 5 of the ID Header field (see WR29, Bit 2). In the former case it is referred to as the Flag Nibble; in the latter case it is referred to as the Flag Byte. When a read or write occurs to a sector that contains non-zero flag information, the Flag Byte/Nibble Bit (Bit 3) of the Extended Status Register (RR17) is set.

When a command is aborted, the processor can read the Status Registers (RR16 and RR17) to determine the cause. Having determined the cause, the microprocessor may choose to read or write the sector anyway, in which case it should set this Bit=1 to ignore the ID Flag and reissue the command.

When Bit 5 is set=1 on a READ or WRITE command, the Flag Byte or Flag Nibble will be ignored.

When Bit 5 is set=1 on a Format command, the command becomes a FORMAT SECTOR command and keys off of the SECTOR line instead of the INDEX line. For this function the sequencer must be in hard sectored mode. **(Note: Bit 5 is dual-function in this regard: In the context of format commands, it has nothing to do with ignoring the ID flag information; it simply toggles between a FORMAT TRACK and a FORMAT SECTOR command.)**

BIT 6 = VERIFY Option

When Bit 6 is set=1 on a read-type command (Bit 0 is set=1), the command becomes a VERIFY command. A VERIFY command is a convenience for checking data written to the disk. The VERIFY command (1) reads data from the disk into the 82C5058; (2) reads data out of the RAM buffer; and (3) performs a byte-by-byte "on the fly" comparison. **Unlike the various read commands, this command does not destroy data in the RAM buffer.**

BIT 7 = NO TRANSFER Option

When Bit 7 is set=1 on a read-type command (Bit 0 is set=1), data is read from the disk but it is not transferred to the RAM buffer. This is for checking purposes: it allows data fields to be read and checked for CRC/ECC errors without transferring the data to the RAM buffer.

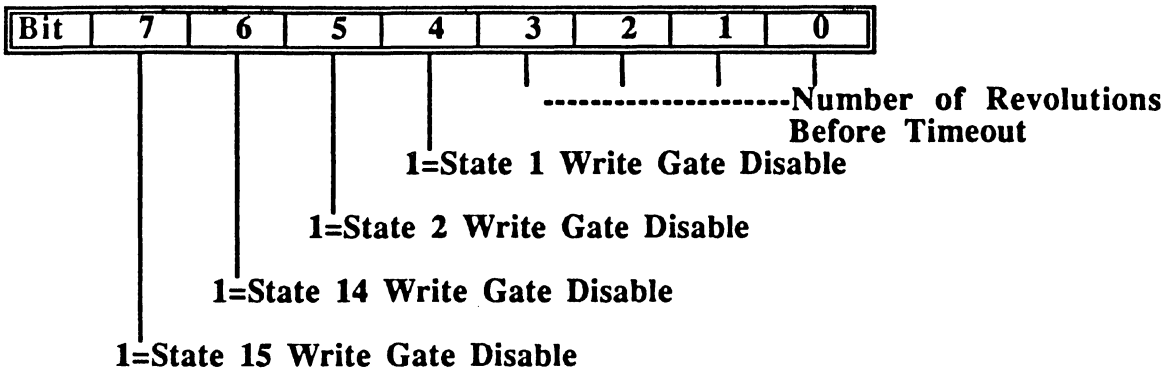
Write Register 17--Sequencer Loop Count

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sectors							

This register specifies the number of sectors to be read or written, or in the case of a FORMAT command, the number of sectors on the track. **(Note: Precisely stated, the value in this register specifies the number of times the loop in the predefined state sequence for the particular command is executed.)** This number is decremented for each sector processed by the command. As a convenience for repeated commands involving the same number of sectors, an internal register stores the initial value of the register and automatically reloads it when a command is complete.

Once a command has been issued, the real time contents of this register can be obtained by reading the Sequencer Loop Count (RR25).

Write Register 18--Index Timeout and Format Write Gate Control



BIT 0-3 = Index Timeout Count

Bits 0-3 of this register specifies the number of disk revolutions, as measured by the number of INDEX pulses, before a command is aborted. **Valid values are X2h through XFh.** This feature allows the sequencer to do automatic retries when it cannot find the ID. The register gets reinitialized after every successful transfer for multi-sector commands. When a command is aborted because Index Timeout is exceeded, the Extended Status Register (Bit 2, RR17) will be set.

A holding register retains the value of this register so that it has to be loaded only when a change is required.

BIT 4-7 = Disable WRT_GATE Option

Bits 4-7 allow disabling of WRT GATE for the specified state (1, 2, 14, or 15, respectively).

Write Register 19--Sub-block Count

Bit	7	6	5	4	3	2	1	0
Byte	Number of Sub-blocks per Sector							

The Sub-block Count is used to determine the number of data bytes per sector (Sector Size).

Sector Size = (Sub-block Count + 1) * Data Field Count

Data Field Count is the count byte from the Format RAM for the Data Field in the Data Segment. Note that Sub-block Count is simply a multiplier that allows the number of bytes for the Data Field to be greater than the maximum count value (256) would allow.

Note: This register should be loaded at initialization and at any time a different Sector Size is used.

Examples:

Sector Size (Bytes)	Sub Block Count	Data Count
128	7h	10h.
256	Fh	10h.
512	1Fh	10h.
1,024	3Fh	10h.
2,048	7Fh	10h.
65,536	FFh	00h
		(00=256)

Write Register 20 through Write Register 23--ID Registers

These four registers are loaded with ID Header information (Cylinder High, Cylinder Low, Head Add, and Sector numbers) to identify a desired sector on a disk. They are then compared to the first four bytes of the ID Header encountered on the disk. Before any command is issued, with the exception of FORMAT and CHECK TRACK FORMAT, these registers should be loaded with the first four bytes of the desired ID Header.

Write Register 20--CYLINDER HIGH (ID BYTE 0)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Write Register 21--CYLINDER LOW (ID BYTE 1)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Write Register 22--Head Number (ID BYTE 2)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh OR X0-XFh							

This byte specifies the value of the third byte of the ID Header.

Note: If the the Head/Flag mode is selected (Bit 2 of WR29 clear), then only the low nibble (bits 3-0) contains Head Number information and only this low nibble is compared. If Flag Byte mode is selected (Bit 2 of WR29 set), then the entire byte contains the head number and is compared.

When Head/Flag mode is selected, valid values are 00h through 0Fh; when Flag Byte mode is selected, valid values are 00h through FFh.

Write Register 23--Sector Number (ID BYTE 3)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register specifies the value of the fourth byte of the ID Header--normally the Sector number to be read or written. It is a counter that is auto-incremented at the end of a valid data field operation. This feature allows sequential operations on one track without having to reload the ID Write Registers.

Write Register 24--Micro/Peripheral to Memory

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to transfer data from the microprocessor, or a peripheral device on the microprocessor bus, to the RAM buffer.

Microprocessor to RAM Buffer Transfers

When the microprocessor writes WR24, the microprocessor data is latched into WR24. The Sequencer then generates a Channel 0 DMA request (REQ0). On the acknowledge from the DMA circuit (ACK0) the data will be transferred from WR24 to the RAM buffer.

Note: Before beginning such a sequence, it is necessary to configure DMA Channel 0 to be in Write mode. Note also that if the DMA does not respond to the Channel 0 request (REQ0), the Micro Memory Over/Under Run Bit in the Extended Status Register (Bit 1 of RR17) will be set along with the Extended

Status Non-Zero Bit in the Sequencer Status Register (Bit 7 or RR16).

Peripheral to RAM Buffer Transfers

The sequencer can also transfer data from a peripheral device that is connected to the microprocessor address/data bus (AD0-7) to the RAM buffer. To transfer data from the peripheral to the RAM buffer, the microprocessor reads RR15.

Note that the transfer Enable Bit in the CRC/ECC Control Register must be set; i.e., Bit 5 of WR28. Also, as noted above, the DMA Channel 0 must be initialized before starting the transfer.

When the microprocessor reads RR15, the sequencer generates the read strobe signal -GRPRD for reading the data from the peripheral so that it can be latched into WR24. On the trailing edge of -GRPRD, a Channel 0 DMA cycle is initiated, using REQ0 and ACK0 to write the contents of WR24 into the RAM buffer.

Write Register 25--Sequencer Start/Restart

Bit	7	6	5	4	3	2	1	0
Byte	Re-Start State 0X-FXh				Start State X0-XFh			

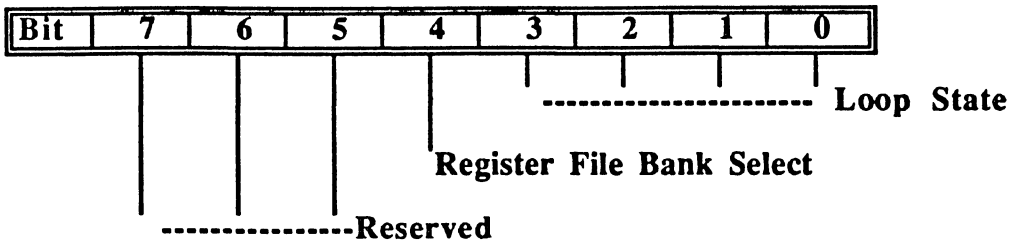
During the executing of a command: Bits 3-0 specify the state number at which the sequencer will begin execution; Bits 7-4 specify the state number from which the sequencer will restart after the Sequencer Loop State (specified by WR26) has been reached.

(Note: The 82C5058 allows sixteen possible states, 0 to 15. A state corresponds to a type of media field. Specifically, a State 0 corresponds to the byte pair (Value, Count) at address 0 in the Format RAM; State 1 corresponds to the byte pair at address 1, and so on. The Value Byte gives the specific value to be encountered in the field; the Count Byte tells the number of times the State loops back on itself (i.e., holds), with the exception of the Data Field, whose total number of bytes is the product of Count and Sub-block Count (a multiplier to allow a greater number of bytes in this field). See Format RAM in the next section for a complete explanation.)

These values depend on the command and the particular disk configuration. Normally, values will be 33h (start and restart on sync field) for all commands except format-type commands, which will use 21h (start with Post-Index Gap Field, restart with ID Preamble).

This register is also used to address the Format RAM. Valid addresses are 00h to 0Fh.

Write Register 26--Sequencer Loop State and Format RAM Select



BITS 0-3 = Loop State

Bits 0-3 of this register determine the state number from which the sequencer jumps back to the Restart State. The value depends on the command and the particular disk configuration, but most commands have a Sequencer Loop State of 0Eh.

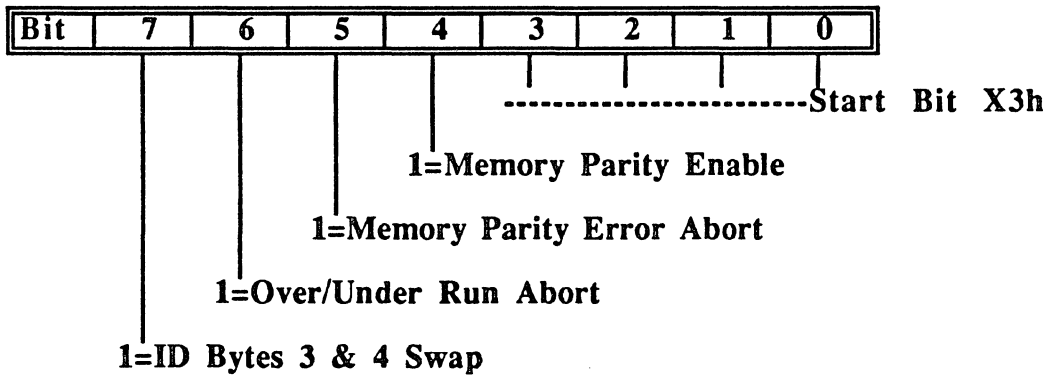
BIT 4 = Bank Select

Bit 4 selects between the two banks of 32 bytes in the Format RAM.

BITS 5-7 = Reserved

These bits are reserved and must be set to 0.

Write Register 27--Bit Ring Start Count and Added Control



BITS 0-3 = Bit Ring Control

Bits 0-3 of this register allow the user to specify the bit-level timing relationship between Sync Detect (AMF in External Sync mode indicates synchronization detection) and Byte Clock (the internal signal that sets the byte boundaries). **This register should be initialized with 03h.**

BIT 4 = Memory Parity Select

Bit 4 controls memory parity checking. If set=1, parity is enabled 0.

Note: If memory parity is enabled, then the functions of Bit 0 and Bit 1 in RR17 (Drive Data Over/Under Run and Micro Mem Over/Under Run) will be OR'd in Bit 0 of RR17, and Bit 1 of RR17 will be used to indicate a parity error.

BIT 5 = Abort On Parity

If Bit 5 is set, a memory parity error will cause an abort, and the Memory Parity Error Bit (Bit 1 of RR17) will be set. (See note above.) If Bit 5 is set=0, a memory parity error will not cause an abort.

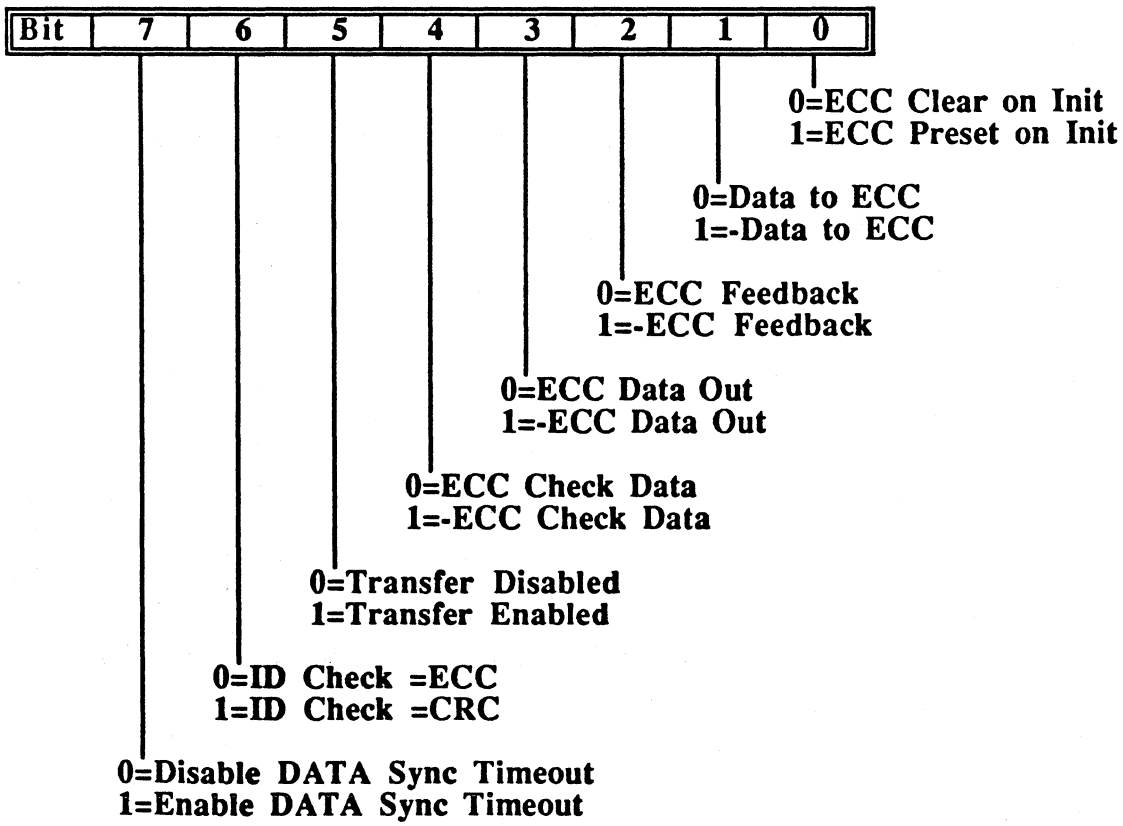
BIT 6 = Abort On Over/Under Run

If Bit 6 is set=1, an Over/Under Run condition will cause an abort.

BIT 7 = Swap ID Bytes

Setting Bit 7=1 swaps the ID Bytes 3 and 4. This is used for floppy disk compatibility.

Write Register 28--CRC/ECC Control



The CRC/ECC Control register allows format and media compatibility with a variety of peripheral devices and error correction schemes.

BIT 0 = ECC Initialization

Bit 0 determines whether or not initialization of the CRC/ECC Shift Register String is cleared (to all 0's) or preset (to all 1's).

BIT 1 = NRZ To ECC Polarity

Bit 1 determines the polarity of the NRZ input data to the CRC/ECC circuitry, and will follow the polarity of this bit. (If Set=1, then ECC= -NRZ, if set =0, ECC= +NRZ.)

BIT 2 = ECC Feedback Polarity

Bit 2 determines the polarity of the CRC/ECC feedback signal, and will follow the polarity of this bit. (If Set=1, then NRZ= +NRZ, if set =0, NRZ= -NRZ.)

BIT 3 = ECC Out Polarity

Bit 3 determines the polarity of the CRC/ECC write data output, and will follow the polarity of this bit. (If Set=1, then -ECC=Data Out, if set =0, ECC=Data Out)

BIT 4 = ECC Check Syndrome Polarity

Bit 4 determines the polarity of the CRC/ECC check signal, and will follow the polarity of this bit. (If Set=1, then -ECC=Check Data, if set =0, ECC=Check Data.)

BIT 5 = Micro-DMA Enable

Bit 5 enables the automatic I/O Read/DMA Write function. In this mode data is transferred from an external peripheral device to the RAM buffer via RR15 (see RR15 for details of such a transfer).

BIT 6 = ID ECC/CRC Select

Bit 6 is used to select what type of error detection is used in the ID field.

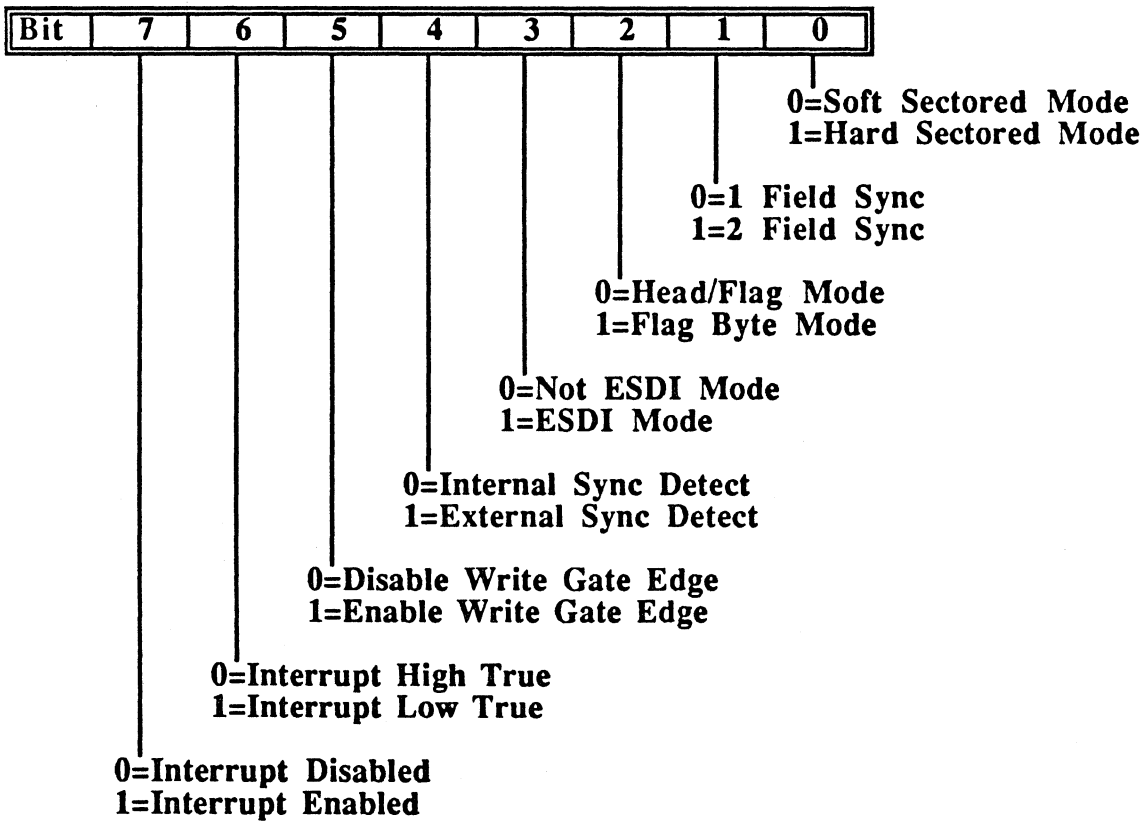
When Bit 6 is set=1, the 16-bit CRC polynomial is used for the ID field: (X16)+(X12)+(X5)+1

When Bit 6 is set=0, the polynomial selected by WR11 will be used for the ID field as well as the data field.

BIT 7 = Data Timeout Select

When Bit 7 is set =1 and the ID Segment has been properly read (ID Match), failure to find the Data Sync field within the period specified by Bit 6 of WR10 (512 bits for normal operation, 32 bits for test purposes) will cause a Data Sync Field Timeout error (Bit 4 of RR17 set).

Write Register 29--Configuration Control



BIT 0 = Hard/Soft Sector Select

Bit 0 selects between hard- and soft-sectored drives. In hard-sectored mode the Sector line is used to re-synchronize the sequencer at State 15 and thereby determine the sector boundaries. If set=0, soft sector mode. If set=1, hard sector mode.

BIT 1 = 1-2 Field Select

Bit 1 selects between "1 Field Sync" (Sync field used, no Address Mark field used) and "2 Field Sync" (both Sync and Address Mark fields used) formats. Setting this Bit=1, selects a 2 field sync format. Setting this Bit=0, selects a 1 field sync format. The "1 Field Sync" is normally used by ESDI drive interfaces; the "2 Field Sync" (Sync byte, Address Mark byte) is used by ST506/412 drive types, including the CHIPS 5070 and 5027 Encode/Decode/PLL ASIC devices.

BIT 2 = Flag Mode Select

Bit 2 selects between two different modes of storing flag information in the ID Header. This information can be used to alert the firmware that a flag condition exists within the sector, thereby stopping a command if the Ignore ID Flag bit (Bit 5 of WR16) is not set.

If Bit 2 is set=0, then the flag information is contained in Bits 4-7 of the 3rd byte (Head/Flag Byte) of the ID Header field. If Bit 2 is set=1 only, the flag information resides in the 5th byte of the ID Header.

Note: Bit 2 also determines which Read Register contains the flag bits that are read from the disk. If Bit 2 is cleared (Head/Flag mode), the Head/Flag Register (RR22) contains the flag information (bits 7-4); if Bit 2 is set (Flag Byte mode), the Flag Byte Register (RR19) contains the flag information.

BIT 3 = ESDI Select

Bit 3 selects between an ESDI and a non-ESDI interface.

If ESDI mode is set=0, the sequencer is in ST506/412 mode, and it asserts RDGATE as soon as any Non-format command is issued. This mode must be used to interface to the CHIPS 5070 MFM and 5027 RLL 2,7 Encode/Decode/PLL ASIC devices.

If Bit 3 is set (1), ESDI mode is configured, and the sequencer assumes the ESDI Search Address/Address Mark Found mode of handshake.

BIT 4 = Internal/External Sync Select

Bit 4 selects between internal synchronization detection (used for ESDI type interfaces) and external synchronization detection (used when the sequencer is configured with the CHIPS 5070 or 5027 Encode/Decode/PLL ASIC device.

If Bit 4 is set=0, the sequencer performs bit-to-byte synchronization (determination of the byte boundary) by comparing (bit to bit) the incoming serial data in the shift register with the Sync Field.

If Bit 4 is set=1, the sequencer uses the AMF line to perform bit-to-byte synchronization.

BIT 5 = Enable WRITE GATE Edge

If bit 5 is set=1 it disables WRTGATE on a FORMAT TRACK command for two bit times after the ID Postamble field--thereby providing an edge of WRTGATE for every PLL Sync Field. **This is required by some ESDI-type drives.**

BIT 6 = Interrupt Polarity

Bit 6 selects between interrupt (INT SEQ) active high or low.

If Bit 6 is set=0 and interrupt enable is set (Bit 7), an interrupt will be generated active high. If Bit 6 is set =1 and interrupt enable is set=1 (Bit 7), an interrupt will be active low.

BIT 7 = Interrupt Enable

Bit 7 set=1 enables interrupts; Bit 7 set=0 disables interrupts. If enabled, an interrupt is generated by any condition that causes the sequencer to change status from Busy to Not Busy. The interrupt is cleared by reading the Status Register, RR16. **(Note: Busy/Not Busy status can be read in Bit 0 of RR16.)**

Write Register 30--Value Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

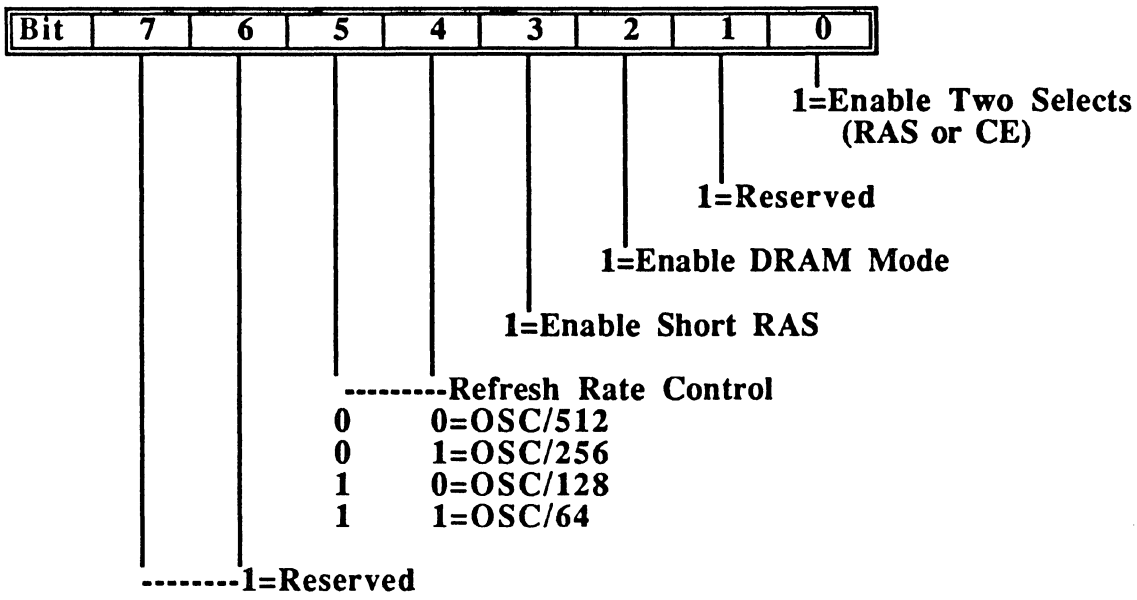
This register is used to write the Value Byte of the Format RAM as indexed by WR25.

Write Register 31--Count Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to write the Count Byte of the Format RAM as indexed by WR25.

Write Register 32--Additional DMA Control



BIT 0 = MEM_CE Control

Setting this bit =1 enables two memory (RAM buffer) chip selects so as to support 64K Byte SRAM (2x(32Kx8): -MEMCE0 and -MEMCE1. (These can function as either Chip Enable (CE), in SRAM mode; or as row a Row Address Strobes (RAS), in DRAM mode.)

Note: When this bit is set=1, MEMA15 is routed onto the MEMA0 pin, while MEMA0 is used internally to determine -MEMCE0 and -MEMCE1. (When MEMA0 is low, -MEMCE0 goes active; when MEMA0 is high, -MEMCE1 goes active.)

BIT 1 = Reserved

This bit is reserved and must be set to 0.

BIT 2 = SRAM/DRAM Control

Bit 2 enables DRAM mode; i.e., multiplexed addresses, RAS, CAS, and -REFSH are generated. If set=1, DRAM mode. If set=0, SRAM mode.

BIT 3 = Enable Short RAS

Bit 3 enables a shorter RAS time; i.e., RAS is one clock less than it would be as configured by WR10, Bits 0 and 1. This is for extended precharge time. If set=1, short RAS, if set=0, normal.

BITS 4-5 = Refresh Rate

These bits set the refresh rate (internal refresh counter) as a function of the oscillator. Bits 5, and 4 value, see table below:

Bit 5	Bit 4	Value
0	0	OSC/512
0	1	OSC/256
1	0	OSC/128
1	1	OSC/64

BITS 6-7 = Reserved

These bits are reserved and must be set to 0.

Write Register 33--DMA Bank Control

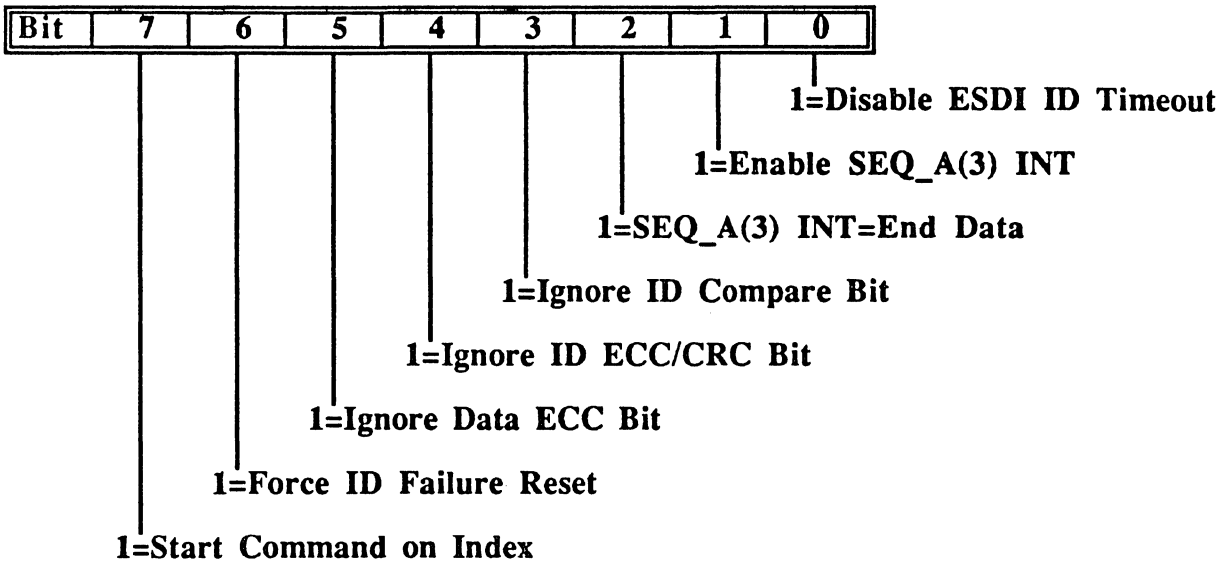
Bit	7	6	5	4	3	2	1	0
Byte	Channel 1 0X-FXh				Channel 0 X0-XFh			

Bits 0-3 select the memory (RAM buffer) bank for Channel 0; Bits 4-7 select the memory bank for Channel 1.

Note: These bits are actually used as Address Bits 16-19 in DRAM mode to provide 20-bit addressing; that is, addresses 0-15 are input via registers WR00 and WR01 (Channel 0) or WR04 and WR05 (Channel 1) and are incremented by internal counters, while addresses 16-19 (called "Bank Selects") are input by writing to WR33 and are not automatically incremented. These additional bits (16-19) allow addressing of DRAMs greater than 64K, and they are irrelevant unless the user has more than 64K of memory and DRAM mode is used.

See Appendix C for DRAM configurations and pin out.

Write Register 34--Optional Control



BIT 0 = ID Timeout Control

Setting this bit =1 will disable the ESDI ID 256 RD_REF_CLK ID timeout.

BIT 1 = Sector Interrupt Control

This bit enables an interrupt (INT SEQ) when SEQA3 goes from 0 to 1 or 1 to 0 as discussed below. If set=1, enable interrupt (SEQA3). If set=0, disable interrupt (SEQA3).

BIT 2 = Sector Interrupt Enable

If this bit is set=1 (and Bit 1 is set=1), the interrupt occurs when SEQA3 goes from 0 to 1; i.e., on State 8. This indicates the beginning of the Data Segment. If this bit is set=0 (and Bit 1 is set=1), then the interrupt occurs when SEQA3 goes from 1 to 0, thus indicating, in normal operation the end of the Data Segment in a multi-sector operation.

BITS 3-5 = Ignore Error Control

Bits 3, 4, and 5 allow the firmware to override some of the embedded control logic. Respectively, these bits allow ignoring of the ID Compare, ID CRC/ECC, and Data CRC/ECC Bits. Bit 3=Ignore ID Compare, Bit 4= Ignore ID CRC/ECC, and Bit 5=Ignore Data CRC/ECC.

With Bit 3 set=1, the firmware can read or write the first sector that it encounters with valid Sync and CRC/ECC fields.

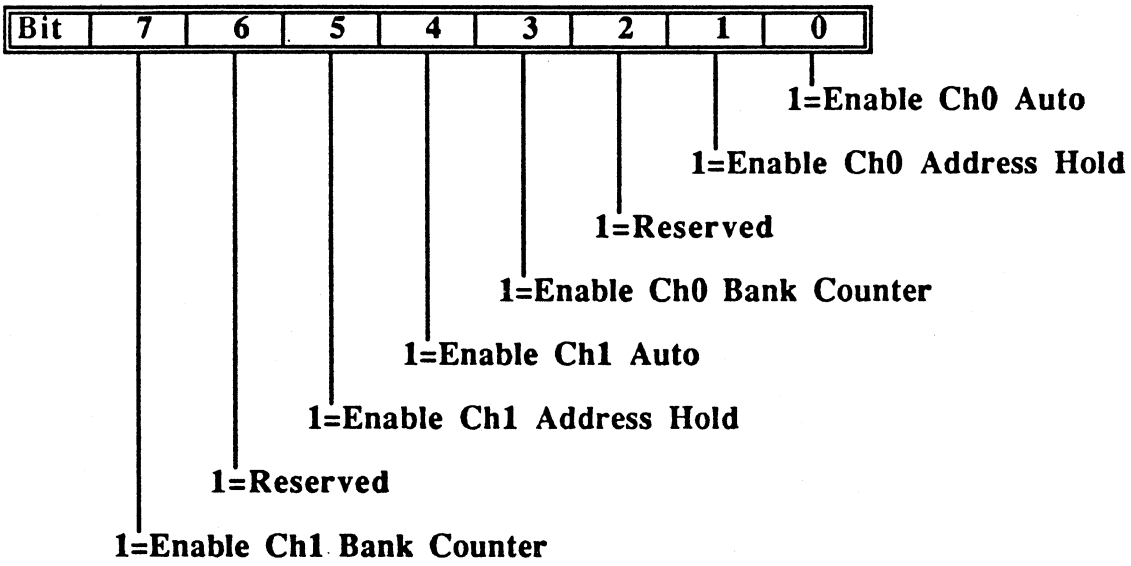
BIT 6 = ID Failure Control

With Bit 6 set=1, the sequencer behaves as if an ID failure has occurred; therefore it does not process the data in the sector.

BIT 7 = Start On Index Control

With Bit 7 set=1, the sequencer will not start any command until the leading edge of INDEX. **This option may be useful in a CHECK TRACK FORMAT Command.**

Write Register 35--Additional DMA Control



The Additional DMA Control Register is cleared on Power-on or a SCSI Reset to provide backward compatibility with the CHIPS 5055B device. This register is used to enable new features in both DMA Channel 0 and 1 for greater flexibility and higher performance.

BIT 0 and 4 = Enable Auto Channel

Setting Bit 0=1 for Channel 0 or Bit 4=1 for Channel 1 enables the respective channel to continue operation after the Transfer Count has expired. This option is useful for a multi-sectored operation. If the interrupt for the appropriate channel is enabled, an interrupt will be generated after the last transfer from that channel has occurred but, the channel will remain enabled and further transfers will occur. It is the responsibility of the firmware to re-issue a command to the interrupting channel to clear the interrupt so firmware can maintain sector interlock.

BIT 1 and 5 = Enable Channel Address Hold Register

Setting Bit 1=1 for Channel 0 or Bit 5=1 for Channel 1 enables the respective channel Address Holding Register. This option is useful for a non-contiguous buffer data with a multi-sectored operation. If the firmware updates either the low or high address register for a channel, when the transfer count has expired for that channel, the new updated address will be used as a reference for the next sector's buffer address. If the Low or High Address Registers are not updated while a transfer is in progress, the next sector's address will only be incremented from the previous sector's last byte transferred address.

BIT 2 and 6 = Reserved

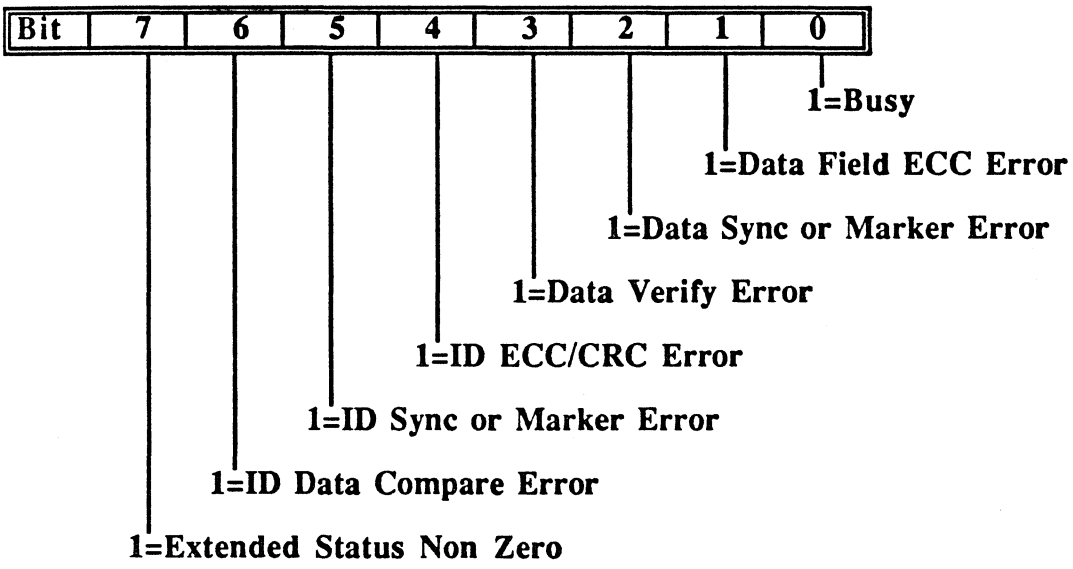
Bits 2 and 6 are reserved and Must be loaded with a 0.

BIT 3 and 7 = Bank Address Control

Setting Bit 3=1 for Channel 0 or Bit 7=1 for Channel 1 enables the respective channel bank address as a counter and not just a holding register. If this bit is set, the bank address will increment as the lower 16 bit address counter increments from FFFFh to 0000h.

2.2 Read Registers

Read Register 16--Sequencer Status



This register contains sequencer status information. It is read at the completion of every command to determine whether execution was successful. During command execution it may be read by the microprocessor to examine specific status information on a sector-by-sector, real-time basis. For example, when a timeout has occurred, the microprocessor can determine whether or not an ID was read successfully (even though the ID did not compare); or whether any IDs were read successfully. If it is determined an ID was not read successfully it means the disk may be improperly formatted or incompatible with the controller.

BIT 0 = Busy

Bit 0 is set=1 when a command is in progress. It is cleared when the sequencer is inactive.

BIT 1 = Data ECC

Bit 1 is set=1 during read operations when the sequencer detects a CRC/ECC error in the data field.

BIT 2 = Data Sync

Bit 2 is set=1 in External Sync mode when the Address Mark is detected (AMF is true) but the byte value of either the Sync Field or the Address Mark Field, as read from the disk, does not compare with the value in the Format RAM. This applies to a read operation on the Data Segment.

BIT 3 = Data Verify

Bit 3 is set=1 when an error is detected during any VERIFY command.

BIT 4 = ID ECC/CRC

Bit 4 is set=1 when the CRC/ECC Bits in the ID Field do not match those generated by the CRC/ECC generator.

BIT 5 = ID Sync

Bit 5 is set=1 during execution of read/write operations if the sector's ID Sync and/or ID Address Mark were in error. The number of disk revolutions that may occur before this bit is set is determined by the value of Index Timeout (WR18).

BIT 6 = ID Compare

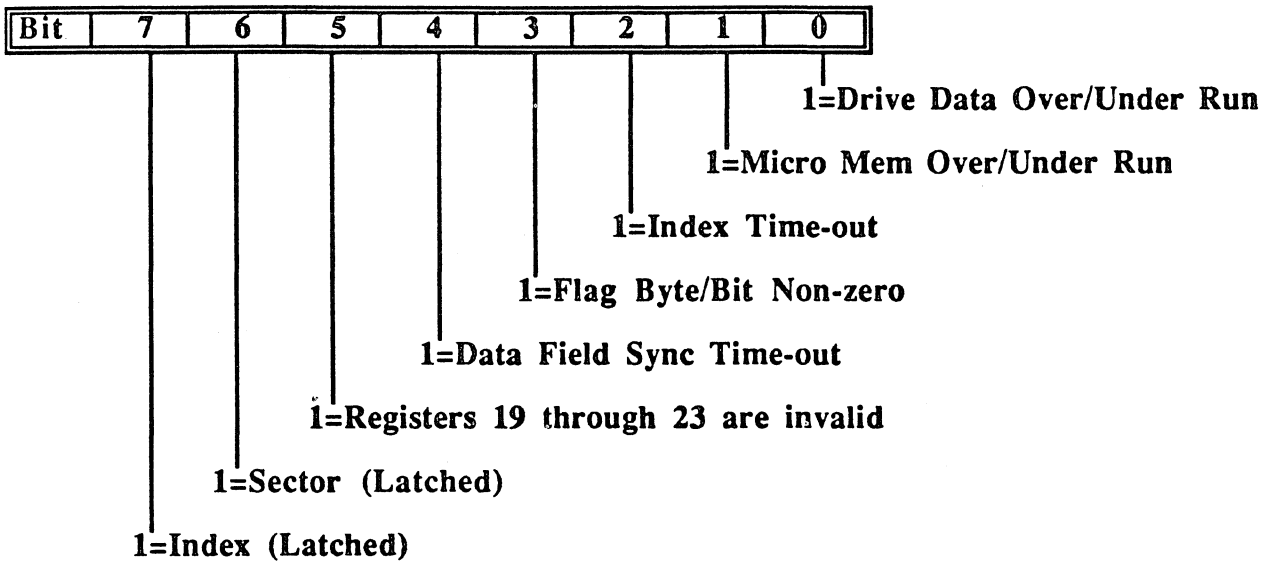
Bit 6 is set=1 when the sequencer detects that the 4-byte ID Header does not correspond to the contents of WR20 to WR23. Bit 6 is cleared when a matching ID Header is found.

BIT 7 = Extended Non-Zero

Bit 7 is set=1 whenever specific bits in the Extended Status Register (RR17) are set.

When any command other than ABORT is issued to the sequencer, RR16 is preset. Refer to Table 3-4, Status Registers.

Read Register 17--Extended Status



The Extended Status Register contains additional sequencer status information regarding command execution.

BIT 0 = Over/Under Run 0

Bit 0 is set=1 when DMA Channel 0 does not respond within one byte time with acknowledge (ACK0) to a data sequencer request (REQ0) for a data transfer. If memory parity is enabled (Bit 4 of WR27 is set), see note under Bit 1 below.

BIT 1 = Over/Under Run 1

Bit 1 is set=1 whenever DMA Channel 0 does not respond after the microprocessor reads RR24 or writes WR24.

Note: If memory parity is enabled (Bit 4 of WR27 is set), then the functions of Bit 0 and 1 in RR17 (Drive Data Over/Under Run and Micro Memory Over/Under Run) will be OR'd in Bit 0 of RR17, and Bit 1 of RR17 will be used to indicate a parity error.

BIT 2 = Index Timeout

Bit 2 is set=1 because of an index time-out function. This occurs when a valid ID has not been detected within the programmable number of revolutions.

BIT 3 = Flag Non-Zero

Bit 3 is set=1 on a read or write command after the sequencer has found the proper ID but there is non-zero flag information in the Head/Flag Byte or the Flag Byte.

BIT 4 = Data Sync Timeout

Bit 4 is set=1 on a read command if the sequencer finds the proper ID but the Data Sync Field has not been detected after 512 or 32 bit times (choice determined by Bit 6 or WR10)--assuming Data Sync Field Timeout has been enabled (Bit 7 of WR28 is set).

BIT 5 = ID Register Valid

Bit 5 is initially set=1 by any command to the sequencer but is cleared (set=0) after the sequencer has processed any valid ID and RR19-RR23 have a valid ID stored. If this bit is cleared (set=0) after an Index timeout, RR19-RR23 hold the last valid ID processed.

BIT 6 = Sector

Bit 6 is a means for the microprocessor to poll a SECTOR/AMF pulse from the disk. **This bit is latched so that a narrow pulse from the disk may be captured.**

BIT 7 = Index

Bit 7 is a means for the microprocessor to poll for an INDEX pulse from the disk. **This bit is latched so that a narrow pulse from the disk may be captured.**

When any command is issued to the Sequencer, RR16 and RR17 are preset as follows:

Table 3-5. Status Registers

STATUS REGISTER

BIT VALUE	NAME	BIT
0	Busy	1
1	Data ECC Error	0
2	Data Sync + Marker Error	0
3	Data Verify Error	0
4	ID ECC/CRC Error	1
5	ID Sync + Marker Error	1
6	ID Compare Error	1
7	Extended Status Non Zero	X

Note: X - Indicates an OR Condition from specific extended status bits.

Table 3-6. Extended Status Registers

EXTENDED STATUS REGISTER BIT

BIT BIT 7	NAME	BIT VALUE	OR STATUS
0	Disk Data Over/Under-run	X	YES
1	Micro Memory Over/Under-run	X	YES
2	Index Time-out	0	YES
3	Flag Bit/Byte Non Zero	X	YES
4	Data Field Sync Time-out	0	YES
5	Invalid ID	1	NO
6	Sector	X	NO
7	Index	X	NO

Notes: YES - Indicates that it is an OR condition for RR16 status bit 7.
X- Indicates that a previous setting remains.

Read Register 18--Sequencer State/Retry Count

Bit	7	6	5	4	3	2	1	0
Byte	0X-FXh=Sequencer State				X0-XFh=Retry Count			

BITS 0-3 = Retry Count

Bits 0 through 3 contain the number of disk revolutions counted to find a requested sector on a read or write type command.

BITS 4-7 = Sequencer State

Bits 4-7 of this register contain the real-time state number of the sequencer. This number ranges from 0 to 15, and as noted earlier, **it is also the address of the Format RAM.** This information is useful for synchronizing the microprocessor firmware to the sequencer. **Note: It is necessary to de-bounce this data, since the internal state machine runs asynchronously to the microprocessor.**

Read Register 19--Flag Byte (ID Byte 4)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh=Flag Byte							

This register contains the fifth byte of ID Header information read from the disk in real time. If the format of the disk does not use five bytes of ID Header, then this register will not contain any valid information. If the sequencer is configured in Flag Byte mode (Bit 2 of WR29 is set) and the Flag Byte/Nibble Bit in the Extended Status Register is set (Bit 3 of RR17), then this register will contain the flag information.

Read Register 20 through Read Register 23--ID Header

These four registers contain the current ID Header bytes read from the disk. They are updated for every sector that has a valid ID Sync Byte-- regardless of the results of checking the ID CRC/ECC Bits. RR20 is the first ID Header Byte; RR23 is the fourth. If the sequencer is configured in Head/Flag mode (Bit 2 of WR29 is cleared), then the high nibble of RR22 will contain the flag information; otherwise, the flag information will be contained in RR19 as noted above.

Read Register 20--CYLINDER HIGH (ID BYTE 0)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 21--CYLINDER LOW (ID BYTE 1)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 22--Head/Flag Byte (ID BYTE 2)

Bit	7	6	5	4	3	2	1	0
Byte	Flag				Head Address			

If Head/Flag mode has been selected (Bit 2 of WR29 is set=0), then Bits 4-7 of this register contain flag information, and Bits 3-0 will contain the Head number. If Flag Byte mode has been selected (Bit 2 of WR29 is set), then Bits 0-7 will contain the Head number, Byte 2 of the ID Header Field.

Read Register 23--Sector Number (ID BYTE 3)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

Read Register 24--Memory to Micro/Peripheral

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used to transfer data from the RAM buffer to the microprocessor or to a peripheral device on the microprocessor bus.

RAM Buffer to Microprocessor Transfers

When the microprocessor reads RR24, the data in the register is transferred to the microprocessor. The sequencer then does a Channel 0 DMA request (REQ0) in preparation for the next microprocessor request.

Note: Before beginning a RAM buffer read sequence, it is necessary to configure DMA Channel 0 to be in read memory/write peripheral mode. Also, the microprocessor should discard the first read of RR24, as it will contain old information. If the DMA does not respond to the Channel 0 request (REQ0), the Micro Memory Over/Under Run Bit in the Extended Status Register (Bit 1 of RR17) will be set along with the Extended Status Non-Zero Bit in the Sequencer Status Register (Bit 7 or RR16).

RAM Buffer to Peripheral Transfer

The sequencer can also transfer data from the RAM buffer to a peripheral device that is connected to the microprocessor address/data bus (AD0-7). To transfer from the RAM buffer to the peripheral, the microprocessor reads RR11. **Note: As above, DMA Channel 0 must be initialized before starting the transfer. Also, the first transfer will contain old information and so should be discarded.**

When the microprocessor reads RR11, the sequencer generates the write strobe signal -GRPWRT for writing the data from the RR24 into the peripheral device. On the trailing edge of the strobe, a Channel 0 DMA cycle is initiated, using REQ0 and ACK0 to read the next RAM buffer location into RR24 in preparation for the next transfer.

An alternative is to first read RR24, which causes a request for new data but does not strobe data into the peripheral; thus data does not have to be discarded.

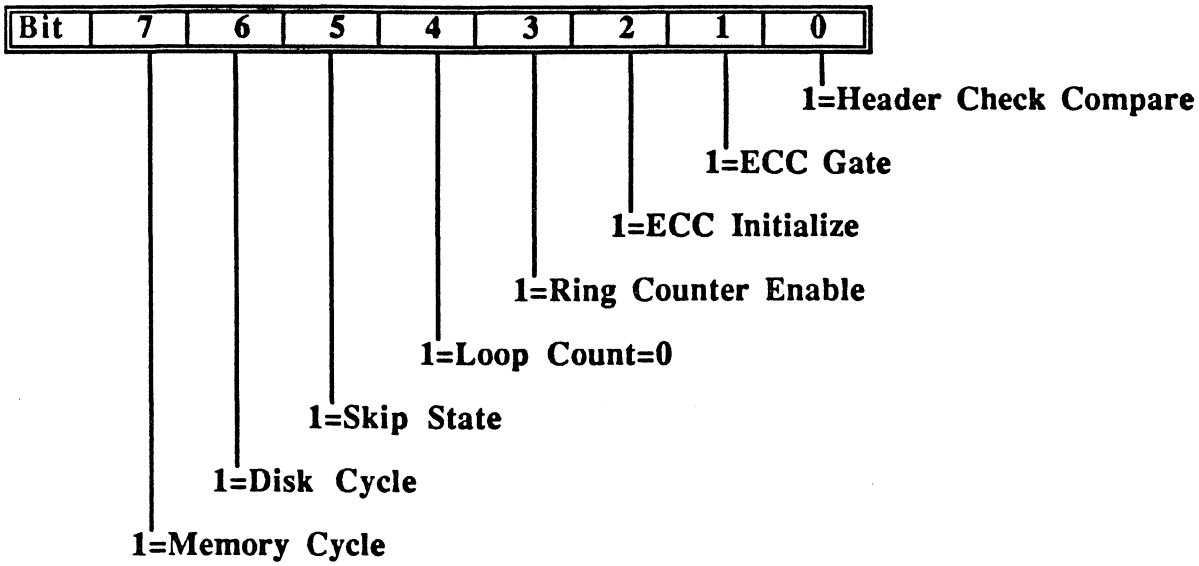
Read Register 25--Sequencer Loop Count

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register contains the real-time value of the Sequencer Loop Count, which is initially set to the number of sectors to be read or written--or in the case of a format-type command, to the number of sectors on the disk--and then is decremented each time the sequencer goes from the Sequencer Loop State to the Restart State.

This information is valuable for synchronization of the microprocessor and the sequencer in commands that involve more than one sector. **Note: It is necessary to debounce this data since the internal state machine runs asynchronously to the microprocessor.**

Read Register 26--Test Register



This register allows access to various internal signals for test purposes.

Read Register 27--Force INDEX

Bit	7	6	5	4	3	2	1	0
Byte	XXh							

Whenever the microprocessor reads this register an internal INDEX signal is generated with the same timing as the -IORD input signal.

Note: There is no information provided to the microprocessor by reading this register.

Read Register 28--Force Sequencer Reset

Bit	7	6	5	4	3	2	1	0
Byte	XXh							

Whenever the microprocessor reads this register an internal RESET signal is generated with the same timing as the -IORD input signal. This function is useful for the firmware to ABORT the sequencer and preserve the status and loop-count information.

Note: There is no information provided to the microprocessor by reading this register.

Read Register 30--Value Register @ Sequencer Start

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register returns the Value Byte in the Format RAM as indexed by WR25.

Read Register 31--Count Register @ Sequencer Start

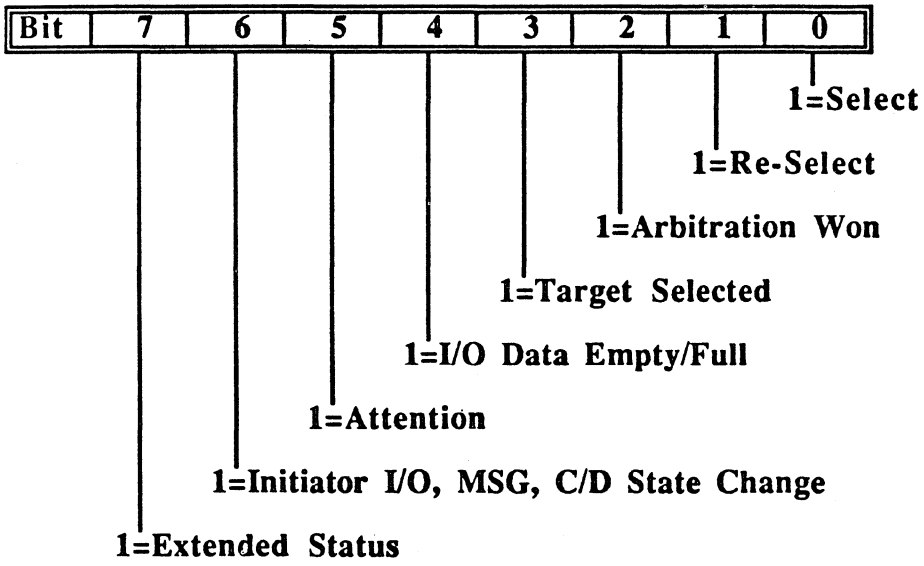
Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register returns the Count Byte in the Format RAM as indexed by WR25.

3. SCSI INTERFACE REGISTERS

3.1 Write Registers

Write Register 64--SCSI Interrupt Mask



This register gives the firmware control over the condition(s) that cause a SCSI interrupt from this device to the firmware. The bit conditions for the mask are disabled when the mask bit is cleared (0) and enabled when the bit for the mask is set = 1.

Power-on or Reset have no effect on this interrupt mask register so it is the responsibility of the firmware to initialize this register to correspond with the flow of the firmware.

BIT 0 = Select

When Bit 0 is set=1, the SCSI interrupt will be enabled for a Selection phase interrupt.

BIT 1 = Re-Select

When Bit 1 is set=1, the SCSI interrupt will be enabled for a Re-Selection phase interrupt.

BIT 2 = Arbitration Won

When Bit 2 is set=1, the SCSI interrupt will be enabled for a Arbitration Won interrupt.

BIT 3 = Target Selected

When Bit 3 is set=1, the SCSI interrupt will be enabled for a Target Selected interrupt.

BIT 4 = I/O Empty/Full

When Bit 4 is set=1, the SCSI interrupt will be enabled for a I/O Data Empty/Full interrupt.

BIT 5 = Attention

When Bit 5 is set=1, the SCSI interrupt will be enabled for a Attention interrupt.

BIT 6 = Initiator State Change

When Bit 6 is set=1, the SCSI interrupt will be enabled for a Initiator State Change interrupt.

BIT 7 = Extended Non-Zero

When Bit 7 is set=1, the SCSI interrupt will be enabled for a Extended Status interrupt.

Write Register 65--SCSI Bus Control

This register allows the firmware control of the SCSI Bus Interface Control signals. It is the responsibility of the firmware to configure this device for the proper SCSI bus phase for any Data, Command, Status or Message transfer phase.

Power-on or Reset clears all bits in this register.

See the following table for SCSI bus control and their mode and driver requirements.

Table 3-7. SCSI Bus Control Requirements

HEX	BITS 7654	BITS 3210	COMMAND			MODE	DRIVER
00	0000	0000	Clear REQ				
01	0000	0001	Clear ACK				
02	0000	0010	Clear SEL				
03	0000	0011	Clear BSY				
04	0000	0100	Clear I/O				
05	0000	0101	Clear C/D				
06	0000	0110	Clear MSG				
07	0000	0111	Clear ATN				
80	1000	0000	Set REQ			Target&I/O	Enabled
81	1000	0001	Set ACK			Initiator&I/O	Enabled
82	1000	0010	Set SEL				
83	1000	0011	Set BSY				
84	1000	0100	Set I/O			Target&I/O	Enabled
85	1000	0101	Set C/D				Enabled
86	1000	0110	Set MSG				Enabled
87	1000	0111	Set ATN				
40	0100	0000	Clear MSG	Clear C/D	Clear I/O		
41	0100	0001	Clear MSG	Clear C/D	Set I/O		
42	0100	0010	Clear MSG	Set C/D	Clear I/O		
43	0100	0011	Clear MSG	Set C/D	Set I/O		
44	0100	0100	Set MSG	Clear C/D	Clear I/O		
45	0100	0101	Set MSG	Clear C/D	Set I/O		
46	0100	0110	Set MSG	Set C/D	Clear I/O		
47	0100	0111	Set MSG	Set C/D	Set I/O		

Write Register 66--SCSI INTERFACE COMMAND

This is the main Command Register for the SCSI interface portion of this device. A write to this register allows the firmware to select the modes and conditions for the applications desired.

Power-on clears all bits in this register while RESET only clears selected bits.

See the following table for all commands and their relationship to RESET.

Table 3-8. SCSI Interface Commands and Reset

HEX	BITS 7654 3210	COMMAND	RESET	POWER-ON
00	0000 0000	Arbitration Complete	Clear	Clear
01	0000 0001	Target Mode	Clear	Clear
02	0000 0010	I/O Mode	Clear	Clear
03	0000 0011	Select Arbitration	Clear	Clear
04	0000 0100	Bus Driver Disable	Clear	Clear
05	0000 0101	Async DMA Data Transfer	Clear	Clear
06	0000 0110	Interrupt Active High		Clear
07	0000 0111	No SCSI Parity Check		Clear
08	0000 1000	Memory Parity Disable		Clear
09	0000 1001	Reset-Out Enable		Clear
0A	0000 1010	SCSI -RST Disable		Clear
0B	0000 1011	1-Shot Delay Normal		Clear
0C	0000 1100	Arbitration w/Attn Disable	Clear	Clear
0D	0000 1101	Latch I/O Control Disable		Clear
0E	0000 1110	Disable Differential Drive		Clear
0F	0000 1111	Reset POR Status		Set
80	1000 0000	Start Arbitration	Clear	Clear
81	1000 0001	Initiator Mode	Clear	Clear
82	1000 0010	DMA Mode	Clear	Clear
83	1000 0011	Re-Select Arbitration	Clear	Clear
84	1000 0100	Bus Driver Enable	Clear	Clear
85	1000 0101	Sync DMA Data Transfer	Clear	Clear
86	1000 0110	Interrupt Active Low		Clear
87	1000 0111	SCSI Parity Check		Clear
88	1000 1000	Memory Parity Enable		Clear
89	1000 1001	Reset-Out Disable		Clear
8A	1000 1010	SCSI -RST Enable		Clear
8B	1000 1011	1-Shot Delay Short		Clear
8C	1000 1100	Arbitration w/Attn Enable	Clear	Clear
8D	1000 1101	Latch I/O Control Enable		Clear
8E	1000 1110	Enable Differential Drive		Clear

00 = Arbitration Complete

This command is used after an Arbitration Won and Target Selected Status has occurred during an Arbitration phase to disable the arbitration mode within this device. As this command is executed, both SEL along with the initiator's and target ID's will be de-asserted from the SCSI bus.

01 = Target Mode

This command configures this device for a Target Role in the SCSI protocol and enables both REQ and I/O and disables ACK on the SCSI bus (if the driver is enabled).

02 = I/O Mode

This command configures this device in I/O mode of information transfer. In this mode, the microprocessor has direct control of the SCSI data bus and the information will not be directed to the memory buffer. In this mode, the firmware also has control of the SCSI I/O control signal along with REQ if the target mode is configured or ACK if the initiator mode is configured.

03 = Select Arbitration

This command configures this device to not assert I/O during an Arbitration phase thus a normal Selection will occur.

04 = Driver Disable

This command disables all SCSI interface signals with the exception of SEL, BSY and ATN if the respective bit is set in the SCSI Bus Control Register.

05 = Async DMA Data Transfer

This command enables the Async DMA data transfer mode within this device if both DMA and drivers are enabled in this register along with the SCSI Req/Ack protocol mode in the Channel 1 Control WR09.

06 = Interrupt Active High

This command configures the SCSI interrupt output to be an Active High response.

07 = SCSI Parity Check Disable

This command disables all SCSI interface parity checking for all information transfer and also for valid parity during Arbitration phase.

08 = Memory Parity Check Disable

This command disables all memory interface parity checking for all information transfer to or from the buffer memory in DMA mode.

09 = Reset Out Enable

This command enables the RESET_OUT signal to reset the microprocessor at power-on or during a SCSI bus Reset State.

0A = SCSI Reset Disable

This command de-asserts the SCSI bus Reset signal. This command must be issued 25 microseconds after a SCSI Reset Enable (8A) command.

0B = 1-Shot Delay Normal

This command makes the R-C time constant of the RESET_CAP a function of the external capacitor and an internal 25 microamp current source.

0C = Arbitration Without Attention

This command configures this device to not assert ATN during an Arbitration phase thus a normal Selection without a Message In phase will occur.

0D = Latch I/O Control Disable

This command configures this device in DMA mode to allow bit 1 of Channel 1 Control to determine the assertion or de-assertion of the SCSI Control Signal I/O.

0E = Differential Drivers Disable

This command configures this device to be in normal single ended driver/receiver mode.

0F = Reset Power-On Status

This command clears the Power-on/Reset status in the SCSI Status Register RR66. This feature is convenient for a closed loop control of this status bit. If firmware is in the midst of any initial diagnostic or configuration while a SCSI bus Reset condition occurs, the POR status bit will remain asserted flagging firmware to reexecute all the diagnostics and configuration followed by clearing the Power-on status.

80 = Start Arbitration

This command is used to start an arbitration sequence. As this command is executed, both BSY and SEL along with the initiator's and target ID's will be asserted on the SCSI bus. The relative time between SCSI bus phases in controlled by the values programmed in arbitration timing registers WR67 and WR68 along with the device ID in WR69 and the targets ID for selection or the initiator ID for re-selection in WR70.

81 = Initiator Mode

This command configures this device for an initiator role in the SCSI protocol and enables ACK and disables both REQ and I/O on the SCSI bus (if the driver is enabled).

82 = DMA Mode

This command configures this device in DMA mode of information transfer. In this mode, the DMA controller has direct control of the SCSI data bus and the information will be directed to the memory buffer. In this mode the SCSI I/O control signal (if target mode is configured) is a direct function of Bit 1 of the Channel 1 Control WR09 (unless the Latch I/O Control command was issued) along with REQ if the target mode is configured or ACK if the initiator mode is configured. If the Latch I/O Control command was issued and the device is configured in the target mode, the SCSI bus signal I/O will be a function of WR65 the SCSI Bus Control Register.

83 = Re-Select Arbitration

This command configures this device to assert I/O during an Arbitration phase thus a Re-Selection phase will occur.

84 = Driver Enable

This command enables all SCSI interface signals with the exception of SEL, BSY and ATN which have the capability of always being asserted, if the respective bit is set in the SCSI Bus Control Register.

85 = Sync DMA Data Transfer Enable

This command enables the Sync DMA data transfer mode within this device if both DMA and drivers are enabled in this register along with the channel Req/Ack protocol mode in the Channel 1 Control WR09.

86 = Interrupt Active Low

This command configures the SCSI interrupt output to be an Active Low response.

87 = SCSI Parity Check Enable

This command enables all SCSI interface parity checking for all information transfer and also for valid parity during Arbitration phase.

88 = Memory Parity Check Enable

This command enables all memory interface parity checking for all information transfer to or from the buffer memory in DMA mode.

89 = Reset Out Disable

This command disables the RESET_OUT signal to reset the microprocessor during a SCSI bus Reset state. This command must be issued if this device is to assert the SCSI bus signal RST by the command SCSI RESET ENABLE to this register if the RESET_OUT signal is connected to the microprocessor or the microprocessor will be reset as it tries to reset the SCSI bus.

8A = SCSI Reset Enable

This command asserts the SCSI Bus signal RST. This command must be followed by the command SCSI Reset Disable (0A) 25 microseconds after the SCSI RESET ENABLE command.

8B = 1-Shot Delay Short

This command makes the R-C time constant of the RESET_CAP a function of the external capacitor and an internal 1600 microamp current source. This feature is to provide a long R-C time period for Power-On and a short R-C time period for just a SCSI bus Reset function.

8C = Arbitration With Attention

This command configures this device to assert ATN during an Arbitration phase thus a Selection with a Message In phase will occur. The firmware must set the ATN bit in the SCSI Bus Control Register before issuing the Arbitration Complete command to this register.

8D = Latch I/O Control Enable

This command configures this device in DMA mode to allow the SCSI Bus Control of I/O onto the SCSI bus instead of bit 1 of Channel 1 Control to determine the assertion or de-assertion of the SCSI Control Signal I/O.

8E = Differential Drivers Enable

This command configures this device to be in differential driver/receiver mode. In this mode, the Inport 1 configuration pins are used to control the external differential driver and receivers.

Write Register 67--Arbitration Timing 1

Bit	7	6	5	4	3	2	1	0
Byte XFh	Delay to Enable Busy 0X-FXh				Bus Free Phase X0-			

Write Register 68--Arbitration Timing 2

Bit	7	6	5	4	3	2	1	0
Byte	Delay to Enable Select 0X-FXh				Arbitration Delay X0-XFh			

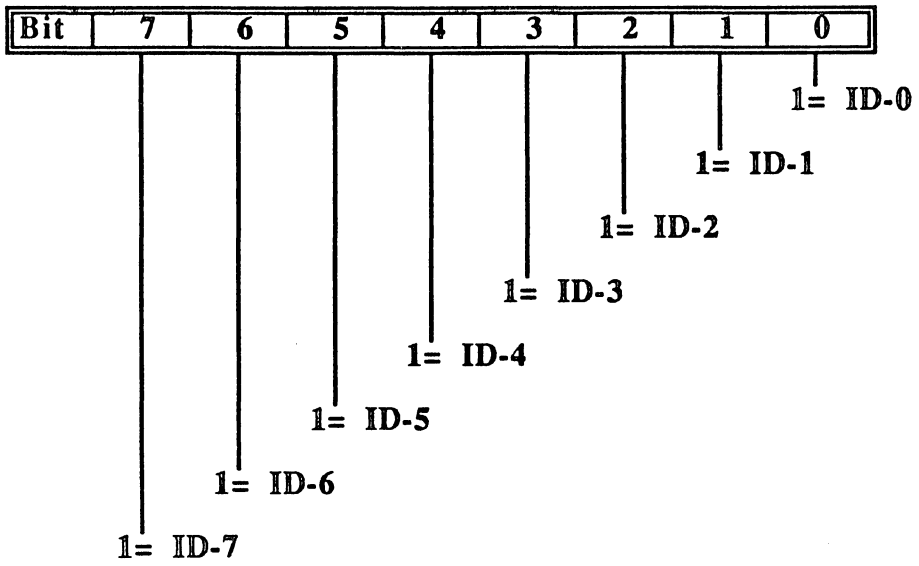
These registers allow the firmware control of the timing of the SCSI Bus Interface Control signals during Arbitration phase. It is the responsibility of the firmware to configure this register for the proper timing before a Start Arbitration command is issued to WR66. The following table reflects the number or clock cycles for each of the phases in the Arbitration phase. For absolute timing, the XTAL_IN period and the SCSI Arbitration Reference Clock selection WR11 bit 6 must be considered.

These two registers are not affected by Power-on or Reset.

Table 3-9. Clock Cycles for Arbitration Phases

HEX	Bus Free Phase WR67 X1-XFh	Delay to Busy WR67 1X-FXh	Arbitration Delay WR68 X1-XFh	Delay to Select WR68 1X-FXh
0	Invalid	Invalid	Invalid	Invalid
1	2 Clocks	2 Clocks	4 Clocks	4 Clocks
2	3 Clocks	3 Clocks	6 Clocks	6 Clocks
3	4 Clocks	4 Clocks	8 Clocks	8 Clocks
4	5 Clocks	5 Clocks	10 Clocks	10 Clocks
5	6 Clocks	6 Clocks	12 Clocks	12 Clocks
6	7 Clocks	7 Clocks	14 Clocks	14 Clocks
7	8 Clocks	8 Clocks	16 Clocks	16 Clocks
8	9 Clocks	9 Clocks	18 Clocks	18 Clocks
9	10 Clocks	10 Clocks	20 Clocks	20 Clocks
A	11 Clocks	11 Clocks	22 Clocks	22 Clocks
B	12 Clocks	12 Clocks	24 Clocks	24 Clocks
C	13 Clocks	13 Clocks	26 Clocks	26 Clocks
D	14 Clocks	14 Clocks	28 Clocks	28 Clocks
E	15 Clocks	15 Clocks	30 Clocks	30 Clocks
F	16 Clocks	16 Clocks	32 Clocks	32 Clocks

Write Register 69--SCSI DEVICE ID



This register gives the firmware control over the SCSI device ID. It is the responsibility of the firmware to initialize this register to correspond with the desired ID. The value written to this register is typically the result of reading RR68 input configuration register followed by masking off all but the three least significant bits of that register and rotating a bit the number of times the masked value reflects. The hardware only used the value in this register for Select/Re-Select or Arbitration Phased. On a Selection/Re-Selection phase this register may be written with more than one bit if one physical device requires more than one logical ID.

Power-on or Reset have no effect on this register.

Write Register 70--SCSI DATA I/O OUT (No Handshake)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register gives the firmware control over the SCSI data bus in an I/O out configuration with no automatic SCSI REQ/ACK handshake. This register is also used to hold the target ID during a Selection phase or the initiator ID during a Re-Selection phase.

Power-on or Reset have no effect on this register.

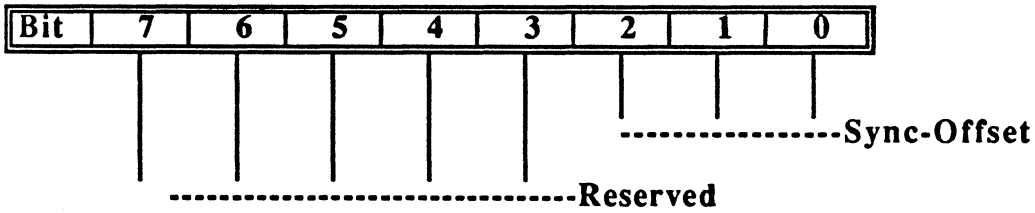
Write Register 71--SCSI DATA I/O OUT (With Handshake)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register gives the firmware control over the SCSI data bus in an I/O out configuration with automatic SCSI REQ/ACK handshake. If the device is configured in target and I/O out mode, when the firmware writes to this register, the SCSI data bus will reflect the value (inverted) written and the SCSI signal REQ will be asserted. When the initiator responded by asserting ACK, this device will de-assert REQ, as the initiator de-asserts ACK, the I/O Data Empty/Full interrupt (if enabled) will be asserted. As the firmware writes a new value to this register, the I/O Data Empty/Full status bit will be de-asserted and the SCSI signal REQ will be asserted for the next byte of data handshake.

Power-on or Reset have no effect on this register.

Write Register 72--Synchronous Offset Control



BIT 0-2 = Synchronous Offset

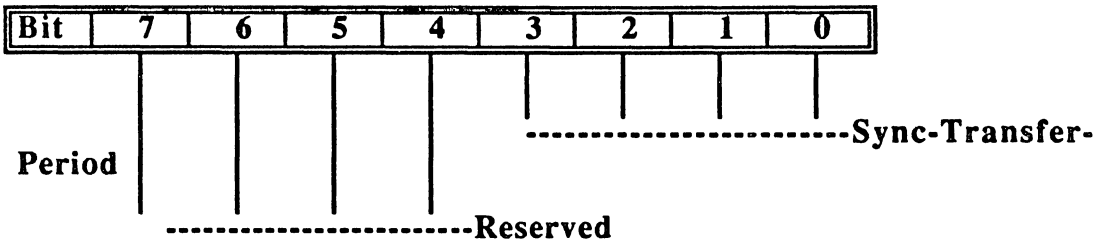
Bits 0-2 set the maximum offset between -REQ output from this device and -ACK input to this device when in synchronous data transfer mode. The valid options are 1 through 7.

BITS 3-7 = Reserved

These bits are reserved and must be set to 0.

Power-on or Reset have no effect on this register.

Write Register 73--Synchronous Transfer Period



BIT 0-3 = Transfer Period

Bits 0-3 set the synchronous transfer period of -REQ deasserted to -REQ asserted while in synchronous data transfer mode. The valid options are 2 through 0Fh. If the value to this register is less than 04, the -REQ output will be asserted for two clock cycles, if the value is greater than 03, the -REQ output will be asserted for three clock cycles.

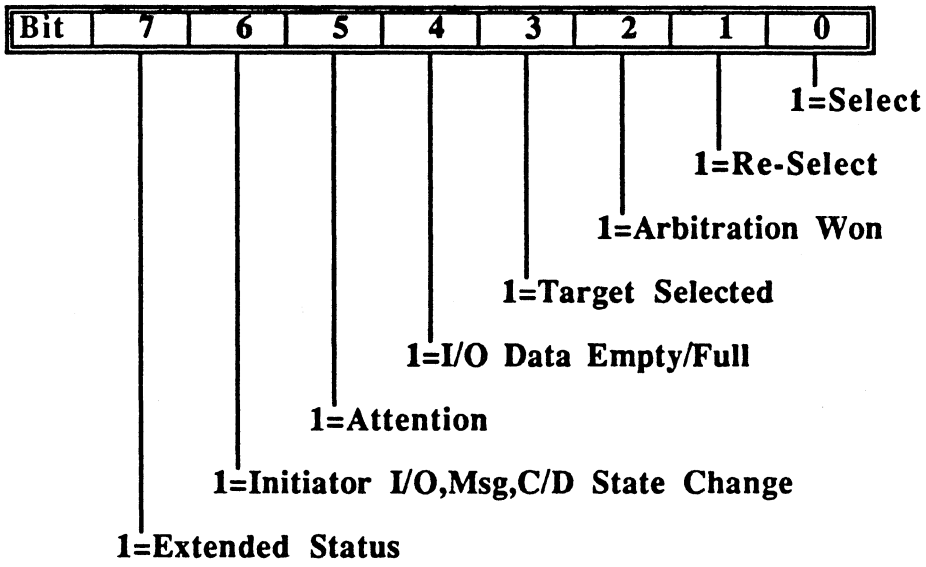
BITS 4-7 = Reserved

These bits are reserved and must be set to 0.

Power-on or Reset have no effect on this register.

3.2 Read Registers

Read Register 64--SCSI Interrupt Status



This read register gives the firmware status over condition(s) that cause a SCSI interrupt from this device to the firmware. If the respective SCSI interrupt Mask Bit is set, the SCSI interrupt will be asserted if the Status Bit is set. If firmware is configured for a polling only mode, any bit in this Interrupt Status Register may be polled for the appropriate status.

BIT 0 = Select

If Bit 0 is set=1, this device is in the SCSI Bus Selection phase and the following conditions exist:

-SEL is asserted.
-BSY is de-asserted.
-I/O is de-asserted.
The target ID on the SCSI data bus completes a logical AND with t h e I D programmed in WR69.

BIT 1 = Re-Select

If Bit 1 is set=1, this device is in the SCSI Bus Re-Selection phase and the following conditions exist:

-SEL is asserted.
-BSY is de-asserted.
-I/O is asserted.
The target ID on the SCSI data bus completes a logical AND with the ID programmed in WR69.

BIT 2 = Arbitration Won

If Bit 2 is set=1, it indicates this bus device has completed the Arbitration phase and has won arbitration. The following conditions exist:

-SEL is asserted.
-BSY is de-asserted (by this device).
-I/O is de-asserted (If Select).
-I/O is asserted (If Re-Select).
The SCSI data bus is driven to a state that completes a logical OR with the ID programmed in WR69 and the initiator ID programmed in WR70 and the resulting ODD parity of the SCSI data bus.

BIT 3 = Target Selected

If Bit 3 is set=1, it indicates this bus device has completed the Arbitration phase and has won arbitration and the target has responded to the Selection phase. The following conditions exist:

-SEL is asserted.
-BSY is asserted (by the target).
-I/O is de-asserted (If Select).
-I/O is asserted (If Re-Select).
The SCSI data bus is driven to a state that completes a logical OR with the ID programmed in WR69 and the initiator ID programmed in WR70 and the resulting ODD parity of the SCSI data bus.

BIT 4 = I/O Data Empty/Full

If Bit 4 is set=1, it indicates the status of the I/O information transferred during a SCSI REQ/ACK handshake has been completed. The following configuration must exist:

Driver I/O Enable
I/O mode

If this device is configured in target mode, this bit is set when the initiator de-asserts ACK. In initiator mode, this bit is set when the target asserts REQ. This status bit or interrupt will be cleared by any of the following conditions:

A microprocessor read of the SCSI data bus RR70 (with no handshake for the last byte) or RR71 (with handshake for more data to transfer with the REQ/ACK handshake).

A microprocessor write to the SCSI Data Bus WR71 (with handshake for more data to transfer with the REQ/ACK handshake).

BIT 5 = Attention

If Bit 5 is set=1, it indicates SCSI Control signal ATN is asserted on the SCSI bus.

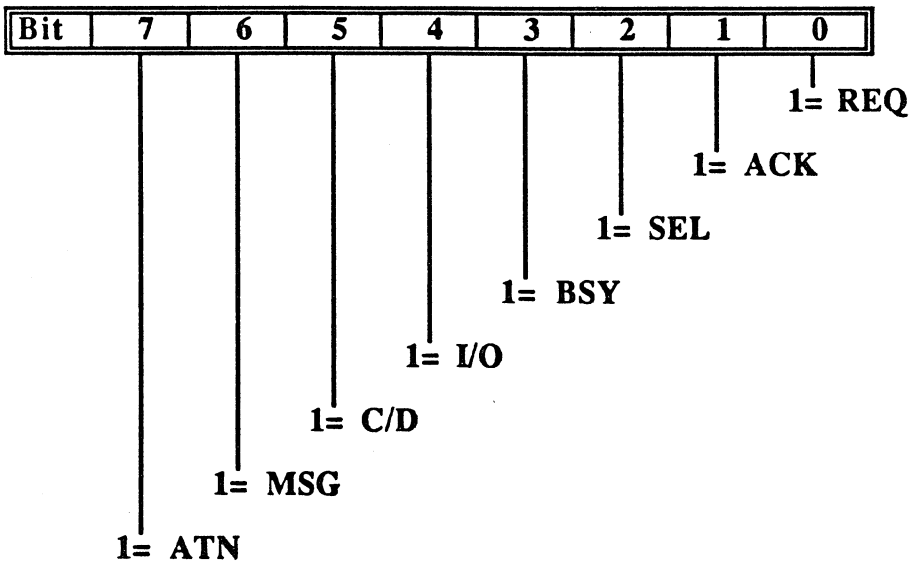
BIT 6 = Initiator I/O, MSG or C/D State Change

If Bit 6 is set=1, it indicates the status of the SCSI Bus Control signals have changed state. Initiator mode must be configured and a pulse or level change on either the SCSI Control signal I/O or MSG or C/D occurred. If this condition occurs while this device is in DMA mode, this state change will reset DMA mode back to I/O mode so firmware can reconfigure either its memory addresses or respond to the proper new SCSI state. This status bit is cleared on the trailing edge of the read status of this register.

BIT 7 STATUS NON-ZERO

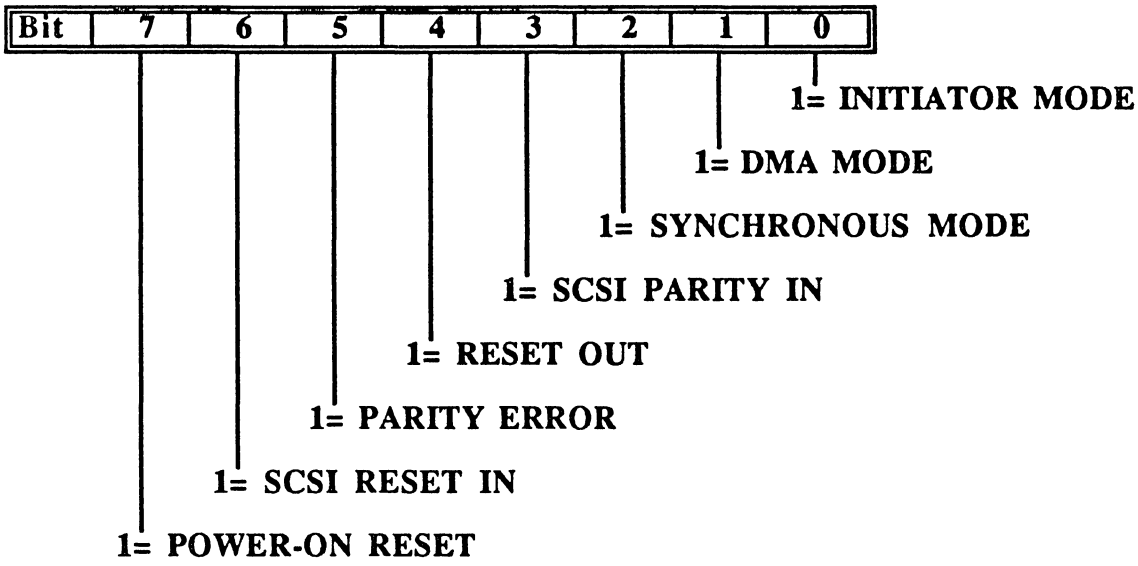
If Bit 7 is set=1, the Extended Status RR66 Bits 5 thru 7 are not zero. **Bit 5 of RR66 is set if there is a SCSI bus parity error or a memory parity error or if either of these paritys are enabled.** Bit 6 of RR66 is set if there is a SCSI Reset condition on the bus. Bit 7 of RR66 is set because of a Power-on Reset condition.

Read Register 65--SCSI Bus Status



This read register gives the firmware status over the current status of the SCSI Control Bus. Each of these status bits directly reflect the condition of their respective control signal. If the SCSI Control signal is asserted, the respective status bit will be set=1.

Read Register 66--SCSI Interface Device Status



BIT 0 = Initiator Mode

If Bit 0 is set=1, this device is configured in the Initiator mode and if set=0 it is configured in the Target mode.

BIT 1 = DMA Mode

If Bit 1 is set=1, this device is configured in the DMA Data Transfer mode and if set=0 it is configured in the I/O Data Transfer mode.

BIT 2 = Synchronous Mode

If Bit 2 is set=1, this device is configured in the Synchronous DMA Data Transfer mode and if set=0 it is configured in the Asynchronous DMA Data Transfer mode or I/O Transfer mode.

BIT 3 = SCSI Parity In

If Bit 3 is set=1, the SCSI Data Parity Bit is asserted and if set=0 the SCSI Data Parity Bit is de-asserted.

BIT 4 = Reset Out

If Bit 4 is set=1, this device would be driving the microprocessor RESET OUT signal (if it were enabled).

BIT 5 = Parity Error

If Bit 5 is set=1, if this device has detected a SCSI data bus parity error on a Data In handshake if SCSI parity is enabled or it detects a memory parity error on a read from buffer memory cycle if memory parity is enabled. This status bit is cleared on the trailing edge of the read status of this register.

BIT 6 = SCSI Reset In

If Bit 6 is set=1, if this device has detected a SCSI Bus Reset State. This function is edge triggered and a very short SCSI RESET pulse will set this status bit (and also cause the Reset one-shot to fire). This status bit is cleared on the trailing edge of the read status of this register.

BIT 7 = Power-On Reset

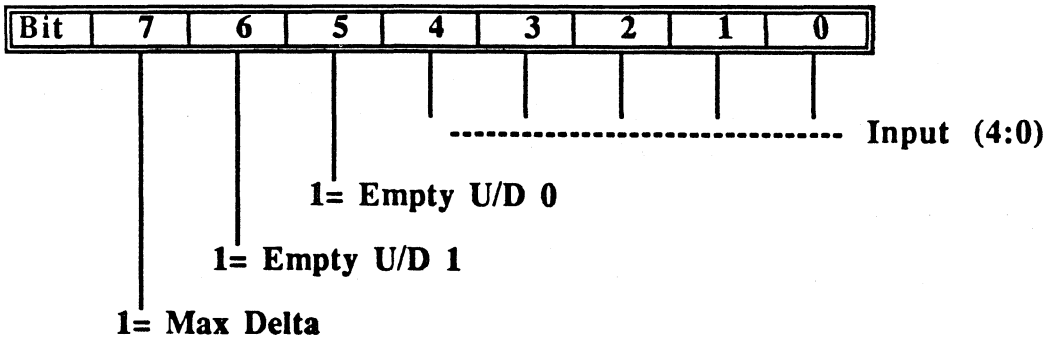
If Bit 7 is set=1, if this device has detected a Power-On Reset condition. This status bit is cleared only by writing to WR66 with a 0Fh value.

Read Register 67--RESERVED

Bit	7	6	5	4	3	2	1	0
Byte	XXh							

This register is reserved and no information provided to the microprocessor by reading this register.

Read Register 68--Input Port 1



BIT 0-4 = Input_1(4:0)

These five bits directly reflect the state of the configuration jumpers 0 - 4.

BIT 5 = Empty U/D 0

If Bit 5 is set=1, the up/down counter that counts the Synchronous Data Transfer FIFO is empty.

BIT 6 = Empty U/D 1

If Bit 6 is set=1, the up/down counter that counts the REQ/ACK Offset for Synchronous Data Transfer FIFO is zero.

BIT 7 = Max Delta

If Bit 7 is set=1, the up/down counter that counts the REQ/ACK Offset for Synchronous Data Transfer FIFO is at the limit as by programming the Max Offset in WR72.

Read Register 69--SCSI Data I/O In (Direct)

Bit	7	6	5	4	3	2	1	0
Byte	00h-FFh							

This register is is used by the firmware to provide a direct snapshot of the SCSI data bus present (inverted) value. The main functional usage of this read register is for the firmware to assure that only two bits of the SCSI data bus are asserted during a Selection phase to this device and also to save the initiator's ID.

Read Register 70--SCSI Data I/O In (Latched, No handshake)

Bit	7	6	5	4	3	2	1	0
Byte	00h-FFh							

This register is used by the firmware to provide data to the microprocessor without performing a SCSI REQ/ACK handshake protocol. See the following definition of RR71 below.

Read Register 71--SCSI Data I/O In (Latched, With handshake)

Bit	7	6	5	4	3	2	1	0
Byte	00-FFh							

This register is used by the microprocessor during all firmware direct I/O transfers (except the last byte) of Commands or Messages In from the initiator to the target using the SCSI REQ/ACK handshake protocol.

The following is an example of how the flow would be for the target (this device) to receive a command (in I/O mode) from an initiator.

First, the firmware would perform an initial read of this register just to assert the SCSI Control signal REQ on the SCSI bus and then discard the information provided by this read operation. The initiator would respond by providing the SCSI data bus with the first byte of the command then assert the SCSI Control signal ACK. This device would automatically de-assert REQ by this device. When the initiator de-asserts ACK, the Interrupt Status I/O Data Empty/Full (RR64 Bit 4) would be set (a SCSI interrupt would also be asserted if the Interrupt Mask for this status bit was set). The firmware would respond to this I/O Data Empty/Full status by again reading this register RR71 which now contains the first byte of the command. As stated before, as this register is read, REQ would again be asserted. This process is followed until the last byte of the command is in this register. The firmware would then read register RR70 to get the last byte of the command but **not** assert REQ on the SCSI bus.

4. FORMAT RAM

The details of the media format for an application depend on the disk drive and some system considerations. The precise definition of the format is required by the 82C5058 both for writing format information on the media and for reading and writing the disk. The 82C5058 provides great flexibility in the definition of the format, supporting a wide variety of drive parameters and system requirements.

Format information is stored in the 82C5058 in an internal RAM viewed as a set of register pairs. Before any commands are issued to access the disk the **parameter RAM** must be loaded by the microprocessor with the format information. The loading must be performed when the controller is initialized, or when the track format is changed.

The parameter RAM is organized as 16 pairs of bytes, each pair consisting of a Value Byte and a Count Byte. The series of byte pairs describes the entire sequence of information recorded on a single track of the drive, beginning at INDEX. For every field on the physical disk track, a corresponding register pair holds the bit pattern for each byte of the field in the Value Byte register--assuming that a certain bit pattern is expected in the bytes of that field--and the length of the field in bytes (i.e., the number of bytes in the field) in the Count Byte Register. Note that only certain fields have expected bit patterns in them; e.g., the ID Sync Field has an expected pattern, the Data Field portion of the data segment does not. As the data sequencer moves from media field to media field, it indexes through the register pairs, using each pair to determine the byte pattern (if applicable) and the number of bytes in each field.

Table 3-6 shows typical register pair values for a soft-sectored MFM ST506 drive using MFM encoding/decoding. **This is intended as an example only.**

See Appendix A for examples of other drive types and formats.

Following the table is a general description of each register pair.

Table 3-10. Example Register Pairs for MFM ST506 Drive

Register Pair	Name	Value	Count	Sequencer State
0	ESDI Sector Gap	00h	01	0
1	Post-Index Gap	4Eh	16	1
2	ID Preamble	00h	13	2
3	ID Sync	A1h	01	3
4	ID Address Mark	FEh	01	4
5	ID Header	00h	04	5
6	ID CRC/ECC	00h	04	6
7	ID Postamble	00h	02	7
8	Data Preamble	00h	13	8
9	Data Sync	A1h	01	9
10	Data Address Mark	F8h	01	A
11	Data Field	E5h	16	B
12	Data CRC/ECC	00h	04	C
13	Data Postamble	00h	02	D
14	Inter-Sector Gap	4Eh	14	E
15	Pre-Index/Sector Gap	4Eh	01	F

Register Pair 0--ESDI Sector Gap

This pair is used only for ESDI type interfaces. It specifies the bit pattern that is expected in the bytes that are placed between sectors, and the number of those bytes.

Register Pair 1--Post-Index Gap

This speed tolerance gap provides space between a write splice (any time WRT GATE is asserted or deasserted) at the end of the track and the first sector's preamble. It also allows for variation in the mechanical detection of the physical drive index. The value used for this field is typically non-zero to prevent confusing it with the Preamble field.

The fields that correspond to the next six register pairs relate to the ID Segment of the disk. They are written once for each sector on a track. The Header portion of the ID Segment contains the Cylinder, Head, and Sector numbers that identify the unique sector.

Register Pair 2--ID Preamble

The ID Preamble field is provided to allow a stream of well controlled data from the disk read channel to be used by the controller PLL to gain frequency and phase synchronization before reading ID data. The Value and Count bytes set for this field are determined by the encoding scheme used and system dynamics. In systems that use MFM encoding, this field generally uses a Value Byte of 00h and a Count Byte of 10-12.

Register Pair 3--ID Sync

For a hard-sectored disk, byte alignment begins with this field. The bytes in this field (usually just one) constitute a bit pattern that enables control circuitry to determine the byte boundaries of the incoming data. The value for this field is normally chosen so that the first bit of this field may be differentiated from the last bit of the preamble. The Count byte for this field is typically 1. Since this field is the first field actively processed by the 82C5058 on read or write commands, its State Number (3) is commonly written to WR25 as the Start State or the Restart State.

For soft-sectored drives, the output pin AM ENABLE is asserted during this field to signal the Encode/Decode circuitry to process Address Mark information. For MFM encoded data, this processing will typically include an illegal (missing) clock scheme used to uniquely define the beginning of ID or Data Segments. For these drives, an illegal MFM pattern of A1h Data/0Ah Clock Byte is very commonly used.

Register Pair 4--ID Address Mark

The ID Address Mark field is required on soft-sectored drives (with the exception of ESDI soft-sectored drives). Its Value is used to differentiate between the ID Segment and the Data Segment. Generally the Count is 1.

Register Pair 5--ID Header

The ID Header varies from drive to drive. Its main purpose is to identify or locate the sector within the drive. Typically the Header has two Cylinder Number Bytes, a Head Number Byte, and a Sector Number Byte. The ID Header may also contain flag information for bad track or bad sector recognition.

In the 82C5058, the Header consists of information written into a series of registers by the user firmware. A typical Header consists of four bytes:

Cylinder Address High Byte	(WR20)
Cylinder Address Low Byte	(WR21)
Head Address/Flag Byte	(WR22)
Sector Address Byte	(WR23)

Note: If Bit 2 of WR29 is set=0, then only the low nibble of the Head byte is used for the Head Number. The high nibble is then available for flag information. If Bit 2 of WR29 is set=1, however, the entire byte contains the Head number, and a fifth byte will contain flag information, which can be read via RR19.

Register Pair 6--ID CRC/ECC

This field contains the CRC or ECC remainder computed for the ID Header if a "1 Field Sync" is used (Bit 1 of WR29 is cleared), or the ID Address Mark and the ID Header if a "2 Field Sync" is used (Bit 1 of WR 29 is set). Count should be set to match the polynomial that is used; i.e., Count = 2 for CRC, Count = 6 for 48-bit ECC, etc. The computed CRC or ECC remainder is supplied by the 82C5058 whenever a format-type command writes the ID.

Register Pair 7--ID Postamble

This final field in the sector ID sequence is used to space the beginning of the Data Segment Preamble away from the ID Segment. This allows the write splice from a sector write operation to occur in an area where no recoverable data is present. As was the case for the Post-Index Gap, the Value used for this field is typically non-zero to prevent confusing it with preamble fields.

The fields that correspond to the next six register pairs relate to the Data Segment of the disk. Like the ID Segment, there are Preamble, Sync, Address Mark, CRC/ECC, and Postamble fields. Corresponding to the Header field is the Data field, which is used for actual user data. Note that for a write operation all fields in the Data Segment are rewritten--not just the Data field.

Register Pair 8--Data Preamble

The Data Preamble has the same function in the Data Segment as does the ID Preamble in the ID Segment. Generally, both preambles will be programmed with the same Value and Count bytes.

Register Pair 9--Data Sync

The Data Sync has the same function as the ID Sync. Typically, they use the same Value and Count bytes.

Register Pair 10--Data Address Marker

The Data Address Marker functions much the same as the ID Address Marker. **Note: The Data Address Mark will have a different Value from the ID Address Mark, thus allowing these two fields to be differentiated.**

Register Pair 11--Data Field

Actual user data is written in this field. **Note: The length of this field is the product of the Sub-block Count (WR19) + 1 and Data Count from the Format RAM. (Note: This is an exception; the number of bytes in other fields is simply the Count for those fields without multipliers.)** For a Format TRACK or FORMAT SECTOR command, this field is written to with a fill character.

Register Pair 12--Data CRC/ECC

This field contains the CRC or ECC remainder computed for the Data field. Count should be set to match the polynomial that is used; i.e., Count = 2 for CRC, Count = 6 for 48-bit ECC, etc. The computed CRC or ECC remainder is supplied by the 82C5058 whenever the data field is formatted or re-written.

Register Pair 13--Data Postamble

The Data Postamble spaces the write splice at the end of a sector re-write away from the CRC/ECC field. A short gap of one or two bytes is typical.

The final two fields are gaps which, on a soft-sectored disk, space the sectors evenly around the track and provide buffer space for the physical field length changes which occur with variations in both instantaneous and long-term rotation speed.

Register Pair 14--Inter-Sector Gap

This gap provides space between the end of one sector and the beginning of another. The value chosen is typically the same as for other gaps.

Register Pair 15--Pre-Index/Sector Gap

On soft-sectored drives, this last field fills space from the end of the last Sector to the drive Index. The Count field is the number of byte times the sequencer remains Busy and continues formatting after the Index pulse. (Typically the Count is 1.) As with other gaps, the value used for this gap should be chosen so that it is not confused with preamble fields.

INITIALIZATION

The broad flexibility of the 82C5058 requires that various parameter control registers be initialized before commands are issued to access the disk. **Once initialized for an application, many of these registers never need to be changed. Typically, the following registers require infrequent initialization:**

WR10--Memory Cycle Timing
WR11--CRC/ECC Polynomial Selection
WR18--Index Timeout
WR19--Sub-Block Count
WR27--Bit Ring Start Count
WR28--CRC/ECC Control (most bits)
WR29--Configuration Control
WR67--Arbitration Timing 1
WR68--Arbitration Timing 2
WR69--SCSI Device ID
Media Format Registers (RAM)

Note: Write Registers WRXX are all directly accessible, as described in Chapter 3 (Registers), and that the Media Format Registers (RAM) are indirectly accessed via WR30, WR31, and WR25, as described in the same chapter

ISSUING COMMANDS

1. Command Overview

A specific command is issued by writing WR16 (Sequencer Command Register), but before writing WR16 other parameters specific to that command must be programmed by writing of the appropriate registers. Thus each access to the disk consists of a sequence of register write operations that leads up to issuing the specific command by writing WR16.

The particular sequence of registers written before issuing the specific command varies with each application. The registers commonly written before most commands include:

Memory Controller Registers for data block transfers:
WR00-09

Sequencer Registers:
WR17--Sequencer Loop Count with number of sectors
WR20-23--Header with Cylinder, Head, and Sector
WR25--Sequencer Start/Restart State
(Note: WR25 should be initialized with 33h and does not need to be changed except for a format type command.)
WR26--Sequencer Loop State
(Note: WR26 should be initialized with a 0Eh and does not need to be changed except for a format-type command.)

Access to these registers is discussed in Chapter 3 (Registers). It is reiterated below.

2. How to Issue a Command

Issuing a command is synonymous with writing WR16. (Note: Only certain combinations of writing WR16, as described below, are valid.) To write WR16 (or any other register in the sequence leading up to writing WR16), the processor must put the appropriate register address on the Address/Data bus (A/D0-7), assert ALE (8051 mode) or -AS (Z8 mode) to latch the address, then with appropriate control signals, transfer the data to the register. (See Chapter 2 for timing details for writing a 82C5058 internal register.)

3. Command Descriptions

Table 4-1 lists all possible command bytes which may be issued to the 82C5058 via the WR16, the Sequencer Command Register. For other values written to WR16, results are undefined.

Table 4-1. Sequencer Command Register

HEX	BITS 7654 3210	COMMAND
00	0000 0000	ABORT
01	0000 0001	NORMAL READ
02	0000 0010	NORMAL WRITE
05	0000 0101	READ ID
06	0000 0110	FORMAT TRACK
09	0000 1001	READ LONG
0A	0000 1010	WRITE LONG
0E	0000 1110	FORMAT TRACK LONG
19	0001 1001	READ SYNDROME LONG
1D	0001 1101	READ ID SYNDROME LONG
21	0010 0001	READ--IGNORE FLAG
22	0010 0010	WRITE--IGNORE FLAG
26	0010 0110	FORMAT SECTOR
29	0010 1001	READ LONG--IGNORE FLAG
2A	0010 1010	WRITE LONG--IGNORE FLAG
39	0011 1001	READ SYNDROME LONG--IGNORE FLAG
41	0100 0001	VERIFY
49	0100 1001	VERIFY LONG
59	0101 1001	VERIFY SYNDROME LONG
61	0110 0001	VERIFY--IGNORE FLAG
69	0110 1001	VERIFY LONG--IGNORE FLAG
79	0111 1001	VERIFY SYNDROME LONG--IGNORE FLAG
81	1000 0001	CHECK DATA CRC/ECC
85	1000 0101	CHECK TRACK FORMAT
A1	1010 0001	CHECK DATA CRC/ECC--IGNORE FLAG

00h ABORT

Issuing an ABORT to the Sequencer Command Register (WR16) when the sequencer is busy will abort the command that is executing. The status (read in Bit 0 or RR16) goes from Busy to Not-Busy. If interrupts are enabled (Bit 7 of WR29 is set), the sequencer interrupt (INTSEQ) will be asserted.

01h NORMAL READ

This is the normal command to read the disk. It is used to transfer one or more blocks of data from the disk to the RAM buffer. The starting disk address for the transfer is taken from WR20 through WR23, and the number of sectors to be transferred is taken from WR17.

02h NORMAL WRITE

This is the normal write to the disk. It is used to transfer one or more blocks of data from the RAM buffer to the disk. Its operation is much the same as the NORMAL READ command except that the direction of data flow is reversed and no data error checking occurs.

05h READ ID

The READ ID command is used for sequentially reading ID Segments (ID Header only) from the disk and transferring them to the RAM buffer. The transfer begins with the first ID that is encountered after the command is issued; the number of sectors (ID Segments) to be transferred is taken from WR17. The READ ID command is useful for verifying disk addressing errors such as seek positioning and head selection errors. It is also valuable for determining instantaneous disk rotational position. **Note: If this command is used, the firmware should be synchronized to the disk; that is, the firmware must know where it is located on the disk.**

06h FORMAT TRACK

The FORMAT command is used to format a single track on the disk. It may be used for either hard- or soft-sectored disks. When the command is issued, the sequencer waits for the next INDEX pulse. On the rising edge of INDEX, the sequencer turns on WRTGATE, and WRTGATE stays on until the Sequencer Loop Count (written via WR17, read via RR25) has counted down to zero. If, as in a normal FORMAT TRACK command, the Sequencer Loop State (written in WR26) is 0Eh (soft sector), WRTGATE is turned off on the next rising edge of INDEX and, if interrupts are enabled (Bit 7 or WR29 is set), an interrupt occurs (INTSEQ is asserted). If Enable Write Gate Edge is set (Bit 5 of WR29), then WRTGATE is disabled for 2 bit times preceding each Data Preamble field. The latter feature is an option for some ESDI-type formats.

The Sequencer Loop Count sets the number of sectors on a track; i.e., the number of loops that the sequencer state machine will execute. For each sector on the track, the size of the fields within the sector is determined by the Count Byte for that field in the Format RAM. With the exception of the ID Header, ID CRC/ECC, and Data CRC/ECC fields, all fields are determined by the related Value Bytes in the Format RAM.

The ID Header field is read by the sequencer from the RAM buffer using DMA Channel 0. It is the responsibility of the firmware to configure DMA Channel 0 properly and to point to a location in the RAM buffer where a table of sequential ID Header fields is located. The sequencer generates the ID CRC/ECC and Data CRC/ECC fields based on the contents of the CRC/ECC polynomial. Selection Register (WR11) and the CRC/ECC Control Register (WR28).

For format commands with Non-ESDI configuration, unlike data read or write commands, the Sequencer Start/Restart Register (WR25) should be loaded with 21h and the Sequencer Loop State Register should be loaded with 0Eh for soft-sectored disks and 0Fh for hard-sectored disks.

09h READ LONG

The READ LONG command is used to transfer one or more blocks of data to the RAM buffer as in the NORMAL READ command except that the Data CRC/ECC field is read as data. This command is sometimes used together with the WRITE LONG command described below to test CRC/ECC operation: a normal sector is written; it is transferred to the RAM buffer, along with its CRC/ECC bytes, using READ LONG; contents are modified in the buffer; then it is written back to the disk using WRITE LONG. This process allows the microprocessor to introduce an error of arbitrary type, length, and location into the data sector for subsequent reading and error detection and recovery.

0Ah WRITE LONG

The WRITE LONG command is used to transfer one or more blocks of data from the external RAM buffer to the disk as in the NORMAL WRITE command except that the CRC/ECC bytes are taken from the RAM buffer instead of from computed values from the sequencer.

0Eh FORMAT TRACK LONG

The FORMAT TRACK LONG command is equivalent to the FORMAT TRACK command except that ID Header and ID CRC/ECC bytes are fetched from the RAM buffer; i.e., ID CRC/ECC bytes are not internally generated by the CHIPS 82C5058.

19h READ SYNDROME LONG

The READ SYNDROME LONG command is equivalent to the READ LONG command except that CRC/ECC syndrome bytes are transferred to the external RAM buffer instead of the actual CRC/ECC bytes.

Note: The syndrome bytes are computed from the Data portion of the Data Segment and the Data CRC/ECC field. The syndrome bytes may be used to correct bad data.

1Dh READ ID SYNDROME LONG

This command is equivalent to the READ ID command except that the syndrome bytes from reading the ID Segment are also transferred to the external RAM buffer.

21h READ--IGNORE FLAG

The READ--IGNORE FLAG command is equivalent to the NORMAL READ command except it is not aborted by a non-zero flag. (Note: **The non-zero flag would be in the high nibble of byte 3 of the ID Header field if Bit 2 of WR29 is set=0, or it would be in byte 5 of the ID Header if Bit 2 is set.)**

22h WRITE--IGNORE FLAG

This command is equivalent to the NORMAL WRITE command except that it is not aborted by a non-0 flag nibble or byte.

26h FORMAT SECTOR

The FORMAT SECTOR command is used exclusively for hard-sectored disks to format one or more sectors. After the command is issued, the sequencer will start the format on the next SECTOR or INDEX pulse and format for the number of sectors specified in the Sequencer Loop Counter Register (WR17).

It is the responsibility of the microprocessor to issue the command during the sector just before the sector to be formatted. The microprocessor can count the number of sectors since INDEX by polling the Extended Status Register Index and Sector Bits (Bits 7 and 6 of RR17). This command allows the controller to easily map out bad sectors even after the disk has been formatted and used.

29h READ LONG--IGNORE FLAG
2Ah WRITE LONG--IGNORE FLAG
39h READ SYNDROME LONG--IGNORE FLAG

These commands are equivalent to READ LONG, WRITE LONG, and READ SYNDROME LONG except that they are not aborted by a non-zero flag nibble or byte.

41h VERIFY

A VERIFY command is a convenience for checking data written to disk. A VERIFY command (1) reads data from the disk into the 82C5058; (2) reads data out of the RAM buffer; and (3) performs a byte-by-byte comparison. Unlike the various read commands, this command does not destroy data in the RAM buffer.

49h VERIFY LONG
59h VERIFY SYNDROME LONG
61h VERIFY--IGNORE FLAG
69h VERIFY LONG--IGNORE FLAG
79h VERIFY SYNDROME LONG--IGNORE FLAG

Each of these commands operates like the equivalent READ command except that data is compared as in the VERIFY command.

81h CHECK DATA CRC/ECC

The CHECK DATA CRC/ECC command is equivalent to the NORMAL READ command except that no data is transferred to the RAM buffer. This command is useful as a check of the data and CRC/ECC written on the disk.

85h CHECK TRACK FORMAT

This command performs the same function for the Header field of the ID Segment as the CHECK DATA CRC/ECC command does for the Data portion of the Data Segment.

A1h CHECK DATA CRC/ECC--IGNORE FLAG

This command is equivalent to the CHECK DATA CRC/ECC command except that it is not aborted by a non-zero Flag Byte/Nibble.

Data Transfer

Once the CHIPS 82C5058 has been initialized (including writing the Format RAM) and a disk has been formatted (see below), commands can be issued to transfer data.

Note: The Sector Number Register (WR23) gets incremented automatically after each error free block is transferred; thus it is unnecessary to reinitialize it for sequential block transfers.

Part of a command to transfer data consists of searching for a valid ID with the correct Header field.

1. **ID Search.** In non-ESDI mode, after a read/write-type command is issued to the sequencer, RDGATE is asserted. Three bit times after the AMFOUND signal goes active the sequencer first compares the Sync byte found on the disk with the Sync Byte in the Format RAM; then it compares the Address Marker found on the disk with the Address Marker in the Format RAM. Next the sequencer reads the ID Header, which it latches into the registers RR19-23, and compares the ID Header with the contents of WR20-23.

If the Sync Byte, Address Mark Byte, and the ID Header compare with the expected values, then the sequencer clears the ID Data Compare Error in the Sequencer Status Register (Bit 6 of RR16) and the ID Sync and Marker Error Bit (Bit 5 of RR 16). If the ID Data Compare Error Bit is set=0, the sequencer next checks the Flag Byte (RR19) or the high nibble of the Head/Flag Byte (RR22)--depending on the scheme chosen for storing flag information (see Bit 2 of WR29). If Bit 5 of WR16 is set (to abort on non-zero flag information) and the flag byte or nibble is non-zero, then the command is aborted and the Flag Byte/Nibble Non-Zero Bit in the Extended Sequencer Status Register is set (Bit 3, RR17).

Next, the ID CRC/ECC is read and checked. If it is good, the ID CRC/ECC Bit in the Sequencer Status Register (Bit 4, RR16) is cleared.

If there are any errors in the ID Sector (Sync does not compare, Address Mark does not compare, ID Data does not compare, or CRC/ECC error), the sequencer automatically deasserts RDGATE and loops back to the Start State to retry the desired Sector. The sequencer searches until it finds the valid ID or until it has reached the number of revolutions specified in the Index Timeout Register (WR18).

In ESDI mode, after a read/write-type command is issued to the sequencer, AM ENABLE is asserted. This tells the drive to search for an Address Mark. The drive will respond with AM FOUND on the SECTOR/AMF pin when it detects the Address Mark. The sequencer will deassert the AM ENABLE signal when the drive responds with the AM FOUND function. As the sequencer deasserts AM ENABLE, the drive will deassert AM FOUND, which completes the handshake.

If the drive is in hard-sectored mode and the sequencer is configured for hard-sectored mode, the sequencer still asserts AM ENABLE. This has no effect on the hard-sectored ESDI drive but the drive will still provide a pulse on the SECTOR/AM FOUND pin (interpreted as an AM FOUND).

After the SECTOR/AMF is detected, the sequencer will delay for the State 3 Count, then it will assert RD GATE. After RD GATE is asserted, the sequencer will look for the NRZ IN serial-to-parallel converter (SERDES) to compare with the value in State 4. If this compare doesn't occur within 256 RD_REF_CLK cycles, the sequencer will time-out, deassert RD GATE, and retry the Address Mark search sequence. If the compare does occur, the sequencer will start the internal Byte Clock and compare the first four bytes of the ID with the contents of WR20-WR23.

Note: The value for the ID Sync byte must be shifted three bits from the written Sync value to compensate for the internal delay from the Sync compare function to the desired byte synchronization. The above description assumes the sequencer is configured in Internal Sync mode with "1 Field Sync" in ESDI mode and that ID Sync Timeout is not disabled (Bit 0 of WR 34 not set).

The ID Compare with CRC/ECC check is the same as in a non-ESDI configuration.

2. **Data Transfer.** If the ID search was successful, the RDGATE signal is deasserted, then reasserted to read the data field.

In the External Sync mode (Bit 4 of WR29 is set for non-ESDI type), after the Sync field is detected (AMFOUND from the external data separator goes active), the Data Sync byte from the disk is compared to the value in the Format RAM, followed by the comparison of the Address Mark byte. If either of these comparisons fail, then the command is aborted and the Data Sync or Address Mark Error Bit in the Sequencer Status Register is set (Bit 2, RR16).

If AMFOUND is not detected (that is, if the data separator does not detect the Sync field and assert AMFOUND, an input to the 82C5058 within 512 or 32 bit times (see Bit 6 of WR10) after RDGATE is activated), the command is aborted and, if the Enable Data Sync Timeout Bit is set in the CRC/ECC Control Register (Bit 7 or WR28), the Data Sync Field Timeout Bit in the Extended Status Register (Bit 4 of RR17) will be set.

If AMFOUND is detected by the 82C5058 and Data Sync and Data Address Mark fields are valid, the sequencer then uses REQ0 and ACK0 to request the DMA Controller to transfer the data to the buffer memory.

During the data transfer, if the DMA Controller does not respond within one byte time to the sequencer request (REQ0), the Drive Data Over/Under Run Bit is set in the Sequencer Extended Status Register (Bit 0, RR17).

After the data transfer is complete, the data ECC is read and checked. If it is good, the sequencer will increment WR23 (the Sector Register) and decrement WR17 (the Sequencer Loop Count Register). If WR17 is Non-Zero, the sequencer will loop back to the Start State and start the sequencing over again for the next sector in a multi-sector operation.

If the loop count is zero, the sequencer will stop and will clear (RR16 Bit 0=0) and assert the INT SEQ if it is enabled. (Bit 7 of WR29 is set.)

When the command is complete or has aborted, the Sequencer Status will go to not Busy (Bit 0 of RR16 will be cleared). If sequencer interrupts are enabled (Bit 7 of WR29 is set), the INTSEQ line will also go active.

If the ID search was successful, RD GATE is deasserted and reasserted to read the Data field. In Internal Sync mode, the sequencer will (as above) look for the NRZ IN serial-to-parallel converter (SERDES)to compare with the value in State 10. If this compare does not occur within 512 or 32 RD_REF_CLK cycles, the sequencer will time-out and issue a Data Sync Field Timeout (Bit 4 of RR17 set). If the compare is successful, the sequencer will react from this state as it does in non-ESDI mode.

Note: The Value for the Data Sync byte must be shifted three bits from the written Sync Value to compensate for the internal delay from the Sync compare function to the desired byte synchronization.

For data transfer in write mode, if the ID search was successful, the RD GATE signal is deasserted and the WRT GATE signal is asserted. If a "1 Field Sync" has been programmed (Bit 1 of WR29 cleared), then the Data Sync field is written just as it is programmed in the Format RAM. If a "2 Field Sync" has been programmed (Bit 1 of WR29 set), then the Data Sync and the Data Address Mark fields are written just as they are programmed in the Format RAM. If the sequencer is in ST506/412 mode ("2 Field Sync"), then AM ENABLE is asserted for State 9 (Data Sync field), which tells the Encode/Decode device to insert the illegal pattern violation for the Data Sync field.

From this point on, data is fetched from memory and converted from parallel to serial form and CRC/ECC is calculated for the data. At the end of the data transfer, the CRC/ECC remainder is written out, followed by the postamble as programmed for the Postamble in the Value and Count fields of the Format RAM. WRT GATE is then deasserted. From this point on the write operation is complete. For multiple-sector write operations, the ID search would be performed again just as it would for a read operation. Write splices occur at the end of the ID Postamble and beginning of the Data Preamble, and at the end of the Data Postamble and beginning of the Inter-Sector Gap.

Reading Status

As a command is issued to the CHIPS 82C5058, one of the immediate responses is the setting of the Busy Bit (Bit 0) of the Sequencer Status Register (RR16). When the command is completed, the Busy Bit is cleared and an interrupt (INTSEQ) is generated if the interrupt is enabled (Bit 7 of WR29 set). At this point, status related to the command execution is available in the Sequencer Status Register. If the Extended Status Non-Zero Bit (Bit 7) of the Sequencer Status Register is set, then status information is also available in the Extended Sequencer Status Register (RR17).

These registers are accessed, as explained in Chapter 3, by the microprocessor driving the selected I/O addresses for the register onto the A/D0 -7 bus, then generating the address latch, ALE (for 8051 type microprocessor) or -AS (for Z8 type microprocessor).

Error Processing

The 82C5058 performs no error processing explicitly except for ID retries. However, a wide spectrum of its capabilities are valuable in the microprocessor implementation of this phase of controller operation. Among these capabilities are the ability to recover ECC remainders, read sector IDs, etc.

The 82C5058 error detection and correction (EDAC) capability relative to disk data and buffer memory is limited to CRC 16 (error detection only), three computer generated ECC polynomials, and odd parity check/generation for the DMA Buffer RAM data.

In the case of ECC, the 82C5058 generates and checks the serial NRZ data stream for errors. These errors are flagged by a non-zero syndrome. Location and length information is obtained from the syndrome byte(s) returned in case of an error. The 82C5058 does not make corrections by itself. The microprocessor through a specific algorithm will determine:

1. The location of the error.
2. The length of the error.
3. Whether the error length is within correctable range.

It will then make the correction (if length is < MAX).

The ECC polynomials used by the 82C5058 have associated algorithms available for use. Contact CHIPS Mass Storage Operations, Marketing for information concerning this firmware.

Disk Formatting

Three commands are available for formatting disks: FORMAT TRACK, FORMAT TRACK LONG, and FORMAT SECTOR. (Note that FORMAT TRACK and FORMAT TRACK LONG are equivalent except that for the latter, command ID Header and ID CRC/ECC bytes are fetched from the external RAM buffer.) The FORMAT TRACK command can be used for both hard and soft sectored disks, and it is typically used to format an entire track. Formatting begins with the detection of an INDEX pulse, and when used with hard-sectored disks, the SECTOR pulse is used to divide the disk track n Sectors, n being the number of Sector pulses per track.

The FORMAT SECTOR command is used only with hard-sectored disks. The command can be used to format one or more sectors, as specified by the Sequencer Loop Count (WR17).

For the details of these three commands, see their description under "Issuing Commands" and "Command Descriptions" in this chapter. Note: The size of each field formatted by these commands is determined by its Count byte in the Format RAM (see Chapter 3) with the exception of the Data Segment Data field, whose size in bytes is equal to the Count byte in the Format RAM times the Sub-Block Count (set by writing WR19). (Note that Sub-Block Count is merely a multiplier for the Count byte in the Format RAM, since the Sector Size would be limited to 256 bytes if only the Count byte in the Format RAM were used.) Note that all fields will be written during a format operation. The Data field will, of course, be written with fill characters. Thus, before issuing any format-type command, the user firmware must have written the appropriate Value and Count bytes into the Format RAM.

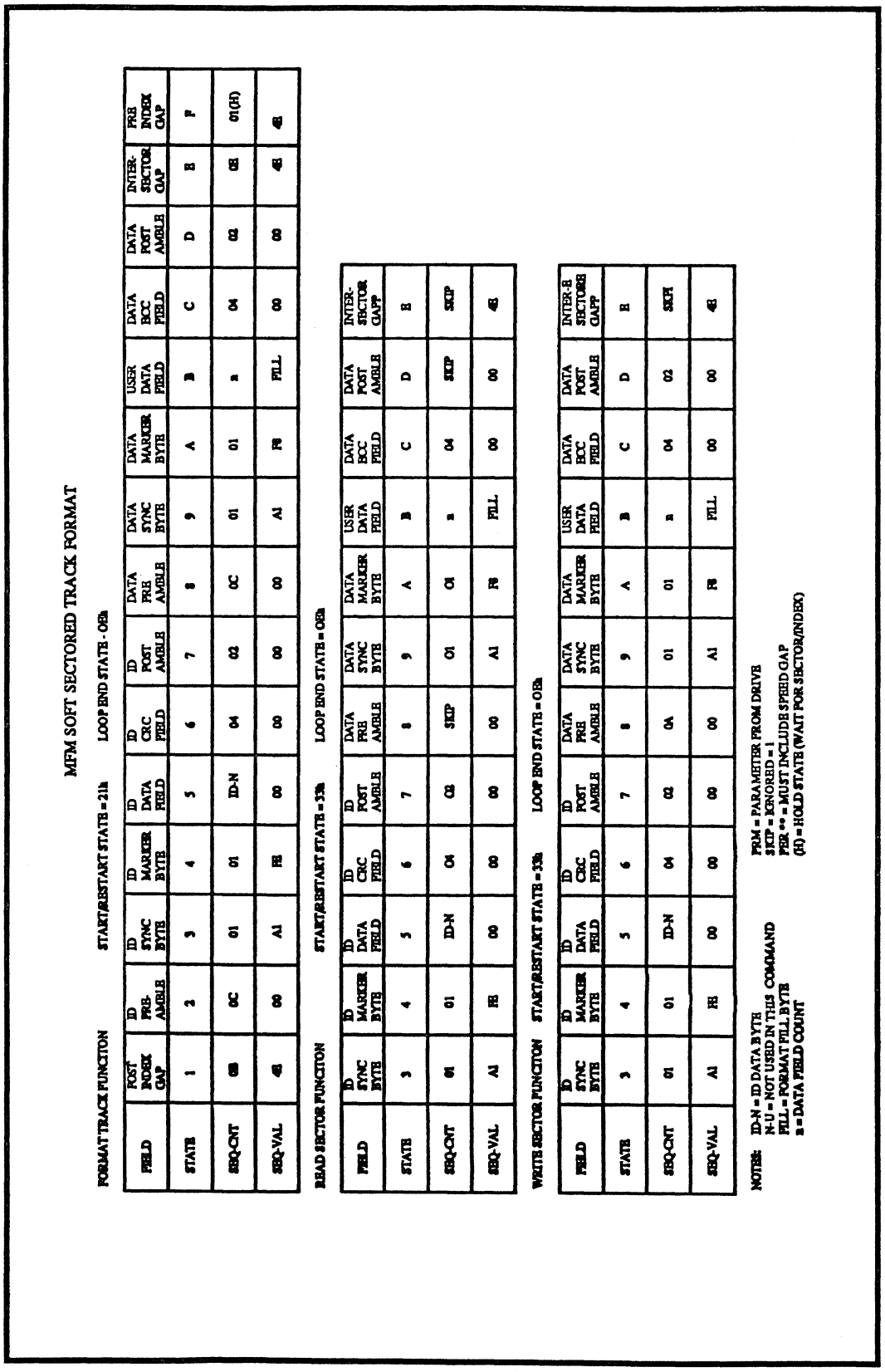
APPENDIX A

TRACK FORMAT

The following four tables provide the track format options for MFM Soft Sectored Format, RLL 2,7 Soft Sectored Format, ESDI Soft Sectored Format, and ESDI Hard Sectored Format.

The recommended Sequencer values and byte counts associated with a sequencer state is given in each table.

In addition, diagrams are provided for the Read/Write data sequencer operation on these track formats. The sequencer Start/Restart and Loop End State values are also noted for format, Read and Write commands.



MFM SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTION START/RESTART STATE = 21h LOOP END STATE = 05h

FIELD	POST INDEX GAP	ID PRE-AMBLE	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP	PRE INDEX GAP
STATE	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	00	00	01	01	ID-N	04	02	00	01	01	n	04	02	00	01(01)
SEQ-VAL	4E	00	A1	FE	00	00	00	00	A1	FB	FILL	00	00	4E	4E

READ SECTOR FUNCTION START/RESTART STATE = 33h LOOP END STATE = 05h

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	04	02	SKIP	01	01	n	04	SKIP	SKIP
SEQ-VAL	A1	FE	00	00	00	00	A1	FB	FILL	00	00	4E

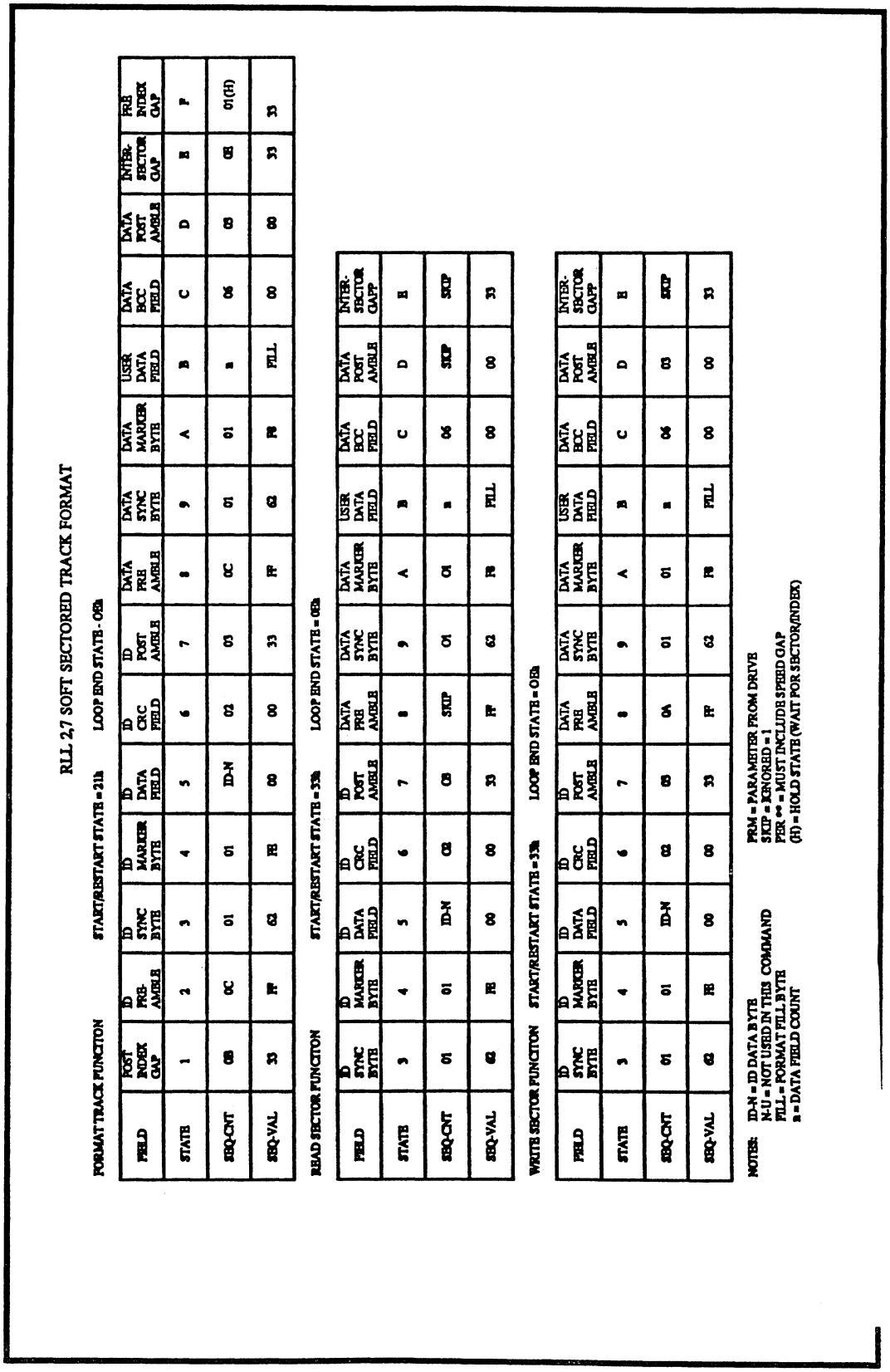
WRITE SECTOR FUNCTION START/RESTART STATE = 33h LOOP END STATE = 05h

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	04	02	04	01	01	n	04	02	SKIP
SEQ-VAL	A1	FE	00	00	00	00	A1	FB	FILL	00	00	4E

NOTES: ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT

PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

Table A-1. MFM SOFT SECTORED FORMAT



RLL 2,7 SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTION — START/RESTART STATE = 21h — LOOP END STATE = 05h

FIELD	POST INDEX GAP	ID PRE-AMBLE	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAP	PRE INDEX GAP
STATE	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	00	0C	01	01	ID-N	02	03	0C	01	01	n	06	05	0E	01(H)
SEQ-VAL	33	FF	02	FE	00	00	33	FF	02	FB	FILL	00	00	33	33

READ SECTOR FUNCTION — START/RESTART STATE = 33h — LOOP END STATE = 05h

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	02	03	SKIP	01	01	n	06	SKIP	SKIP
SEQ-VAL	02	FB	00	00	33	FF	02	FB	FILL	00	00	33

WRITE SECTOR FUNCTION — START/RESTART STATE = 33h — LOOP END STATE = 05h

FIELD	ID SYNC BYTE	ID MARKER BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	DATA MARKER BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	01	01	ID-N	02	03	0A	01	01	n	06	03	SKIP
SEQ-VAL	02	FB	00	00	33	FF	02	FB	FILL	00	00	33

NOTES: ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT

PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

Table A-2. RLL 2,7 SOFT SECTORED TRACK FORMAT

Table A-3. ESDI SOFT SECTORED TRACK FORMAT

ESDI SOFT SECTORED TRACK FORMAT

FORMAT TRACK FUNCTION START/RESTART STATE = 10h LOOP END STATE - 0Eh

FIELD	POST INDEX GAP	AM ENABL TIME	ID PRE-AMBLE	ID PRE-AMBLE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAP	PRE INDEX GAP
STATE	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	PRM	03	PRM-1	01	01	ID-N	02	04	01	PRM	01	n	06	04	PRM**	01(H)
SEQ-VAL	00	00	00	00	C3	00	00	00	00	00	C3	FILL	00	00	00	00

READ SECTOR FUNCTION START/RESTART STATE = 33h LOOP END STATE = 0Eh

FIELD	AMP TO BGAT	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	02	01	ID-N	02	02	SKIP	SKIP	01	n	06	SKIP	SKIP
SEQ-VAL	00	19	00	00	00	00	00	19	FILL	00	00	00

WRITE SECTOR FUNCTION START/RESTART STATE = 53h LOOP END STATE = 0Fh

FIELD	AMP TO BGATE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	WGATE-SAM DELAY	PRE INDEX GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	02	01	ID-N	02	02	01	PRM	01	n	06	04	0A	00
SEQ-VAL	00	19	00	00	00	00	00	C3	FILL	00	00	00	00

NOTES:
ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT
PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT FOR SECTOR/INDEX)

Table A-4. ESDI HARD SECTORED TRACK FORMAT

ESDI HARD SECTORED TRACK FORMAT

FORMAT TRACK FUNCITON START/RESTART STATE = 1Fh LOOP END STATE - 0Fh

FIELD	POST INDEX GAP	AM ENABL TIME	ID PRE-AMBLE	ID PRE-AMBLE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER SECTOR GAP	PRE INDEX GAP
STATE	F	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	01(H)	PRM	PRM-1	01	01	ID-N	02	04	01	PRM	01	n	06	04	01	01(H)
SEQ-VAL	00	00	00	00	C3	00	00	00	00	00	C3	FILL	00	00	00	00

READ SECTOR FUNCITON START/RESTART STATE = 33h LOOP END STATE = 0Eh

FIELD	AMP TO RGAT	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	INTER-E SECTORX GAPP
STATE	3	4	5	6	7	8	9	A	B	C	D	E
SEQ-CNT	PRM	01	ID-N	02	02	SKIP	SKIP	01	n	06	SKIP	SKIP
SEQ-VAL	00	19	00	00	00	00	00	19	FILL	00	00	00-U

WRITE SECTOR FUNCITON START/RESTART STATE = 33h LOOP END STATE = 0Fh

FIELD	AMP TO RGATE	ID SYNC BYTE	ID DATA FIELD	ID CRC FIELD	ID POST AMBLE	DATA PRE AMBLE	DATA PRE AMBLE	DATA SYNC BYTE	USER DATA FIELD	DATA BCC FIELD	DATA POST AMBLE	WGATE-SAM DELAY	PRE INDEX GAP
STATE	3	4	5	6	7	8	9	A	B	C	D	E	F
SEQ-CNT	PRM	01	ID-N	02	02	01	PRM	01	N	06	04	01	00
SEQ-VAL	00	19	00	00	00	00	00	C3	FILL	00	00	00	00

NOTES: ID-N = ID DATA BYTE
N-U = NOT USED IN THIS COMMAND
FILL = FORMAT FILL BYTE
n = DATA FIELD COUNT

PRM = PARAMETER FROM DRIVE
SKIP = IGNORED = 1
PER ** = MUST INCLUDE SPEED GAP
(H) = HOLD STATE (WAIT POR SECTOR/INDEX)

APPENDIX B

FORMAT PARAMETER REGISTER FILE

In order to initialize the Format Parameter Register File, a table must first be setup (typically in ROM) containing the values to be written. Each of the following define byte (DB) directives specify the contents of a value or count. An example for soft sectored ST506/412 Track Format is given in Figure B-1 and Table B-1 is as follows:

```
SEQTBL:  DB    001H    ;; STATE 0 COUNT
         DB    000H    ;; STATE 0 VALUE
         DB    00FH    ;; POST-INDEX BYTE COUNT
         DB    04EH    ;; POST-INDEX BYTE VALUE
         DB    00CH    ;; 10 PREAMBLE BYTE COUNT
         DB    000H    ;; 10 PREAMBLE BYTE VALUE
         DB    001H    ;; ID SYNC BYTE COUNT
         DB    0A1H    ;; ID SYNC BYTE VALUE
         DB    001H    ;; ID MARKER BYTE COUNT
         DB    0FEH    ;; ID MARKER BYTE VALUE
         DB    004H    ;; ID DATA FIELD COUNT
         DB    000H    ;; ID DATA FIELD VALUE (NO CARE)
         DB    004H    ;; ID ECC FIELD COUNT
         DB    000H    ;; ID ECC FIELD VALUE (NO CARE)
         DB    003H    ;; ID POSTAMBLE COUNT
         DB    000H    ;; ID POSTAMBLE BYTE VALUE
         DB    00CH    ;; DATA FIELD PREAMBLE BYTE COUNT
         DB    000H    ;; DATA FIELD PREAMBLE BYTE VALUE
         DB    001H    ;; DATA FIELD SYNC BYTE COUNT
         DB    0A1H    ;; DATA FIELD SYNC BYTE VALUE
         DB    001H    ;; DATA FIELD MARKER BYTE COUNT
         DB    0F8H    ;; DATA FIELD MARKER BYTE VALUE
         DB    004H    ;; DATA FIELD BYTE COUNT
         DB    0E5H    ;; DATA FIELD BYTE VALUE (FORMAT VALUE)
         DB    004H    ;; DATA FIELD ECC BYTE COUNT
         DB    000H    ;; DATA FIELD ECC VALUE (NO CARE)
         DB    003H    ;; DATA FIELD POSTAMBLE COUNT
         DB    000H    ;; DATA FIELD POSTAMBLE VALUE
         DB    017H    ;; INTER-RECORD GAP BYTE COUNT
         DB    04EH    ;; INTER-RECORD GAP BYTE VALUE
         DB    001H    ;; PRE-INDEX GAP BYTE COUNT
         DB    04EH    ;; PRE-INDEX GAP BYTE VALUE
TBLEND:  EQU   $       ;; END OF TABLE
```

Table B-1. Format Parameter Register File for ST506/412 Track Format

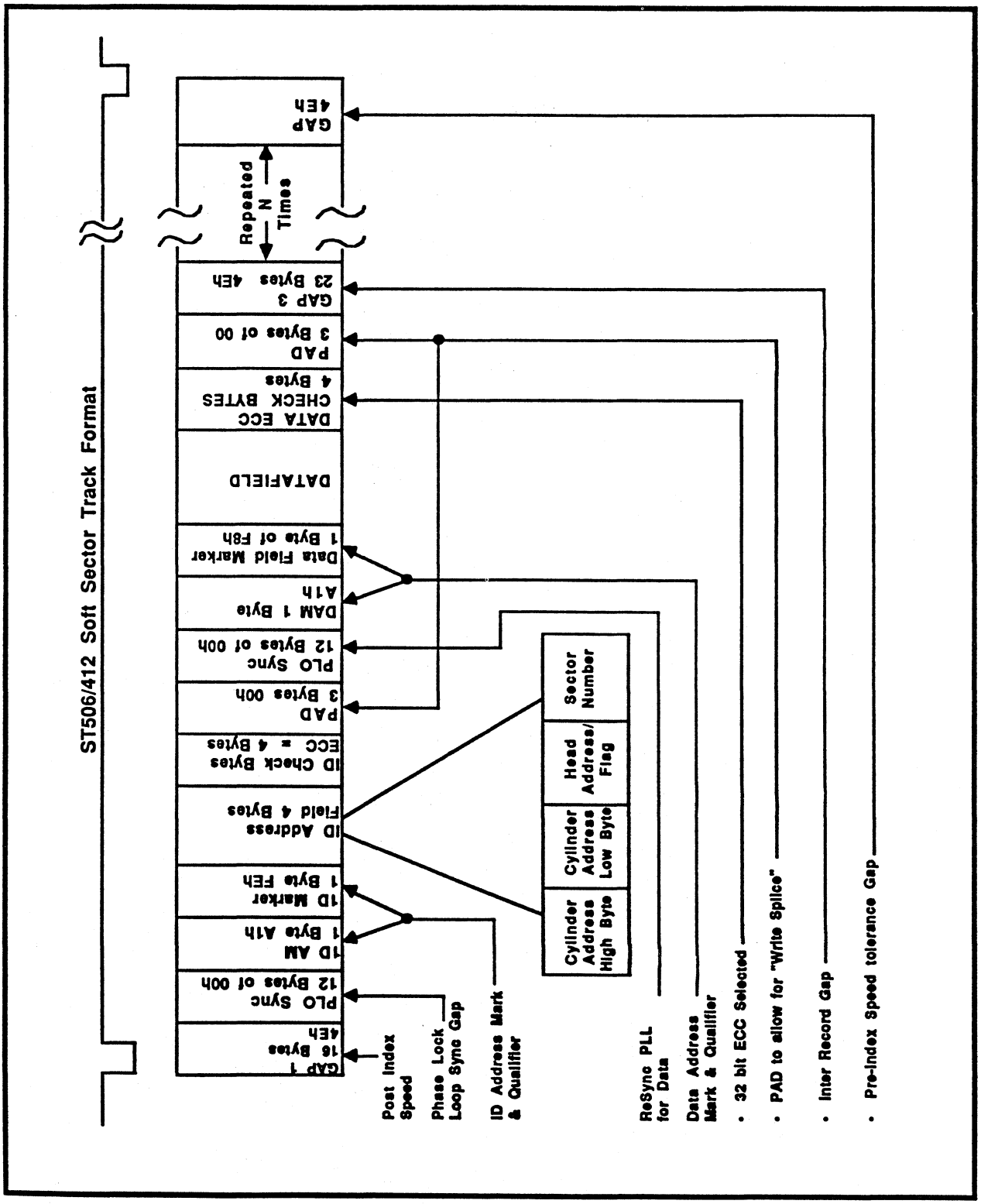


Figure B-1. ST 506/412 Soft Sector Track Format Diagram

APPENDIX C

Table C-1. DRAM From SRAM Pin Conversion (8/16 Bit, 64/128K, 256/512K, 1M)

MEMORY ARRAY CONFIGURATIONS		64K x 8B	64K x 16B	256K x 8 B	256K x 16B	1M x 8B
SRAM PIN FUNCTION	DRAM PIN FUNCITONS	ADDRESS	ADDRESS	ADDRESS	ADDRESS	ADDRESS
MEM_A(0)	MUX_A(0)	0 & 8	———	0 & 8	———	0 & 8
MEM_A(1)	MUX_A(1)	1 & 9	1 & 9	1 & 9	1 & 9	1 & 9
MEM_A(2)	MUX_A(2)	2 & 10	2 & 10	2 & 10	2 & 10	2& 10
MEM_A(3)	MUX_A(3)	3 & 11	3 & 11	3 & 11	3 & 11	3 & 11
MEM_A(4)	MUX_A(4)	4 & 12	4 & 12	4 & 12	4 & 12	4 & 12
MEM_A(5)	MUX_A(5)	5 & 13	5 & 13	5 & 13	5 & 13	5 & 13
MEM_A(6)	MUX_A(6)	6 & 14	6 & 14	6 & 14	6 & 14	6 & 14
MEM_A(7)	MUX_A(7)	7 & 15	7 & 15	7 & 15	7 & 15	7 & 15
MEM_A(8)	MUX_A(8)	———	8 & 16	———	8 & 16	———
MEM_A(9)	MUX_A(A)	———	———	16 & 17	———	16 & 17
MEM_A(10)	MUX_A(B)	———	———	———	17 & 18	———
MEM_A(11)	MUX_A(C)	———	———	———	———	18 & 19
MEM_A(12)	-REFSH	-REFSH	-REFSH	-REFSH	-REFSH	-REFSH
MEM_A(13)	-CAS	-CAS	-CAS	-CAS	-CAS	-CAS
MEM_A(14)	-OE	-OE	-OE	-OE	-OE	-OE
-MEM_CE(0)	-RAS(0)	-RAS	-RAS(0)	-RAS	-RAS(0)	-RAS
-MEM_CE(1)	-RAS(1)	———	-RAS(1)	———	-RAS(1)	———
-MEM_WRT	-WE	-WE	-WE	-WE	-WE	-WE

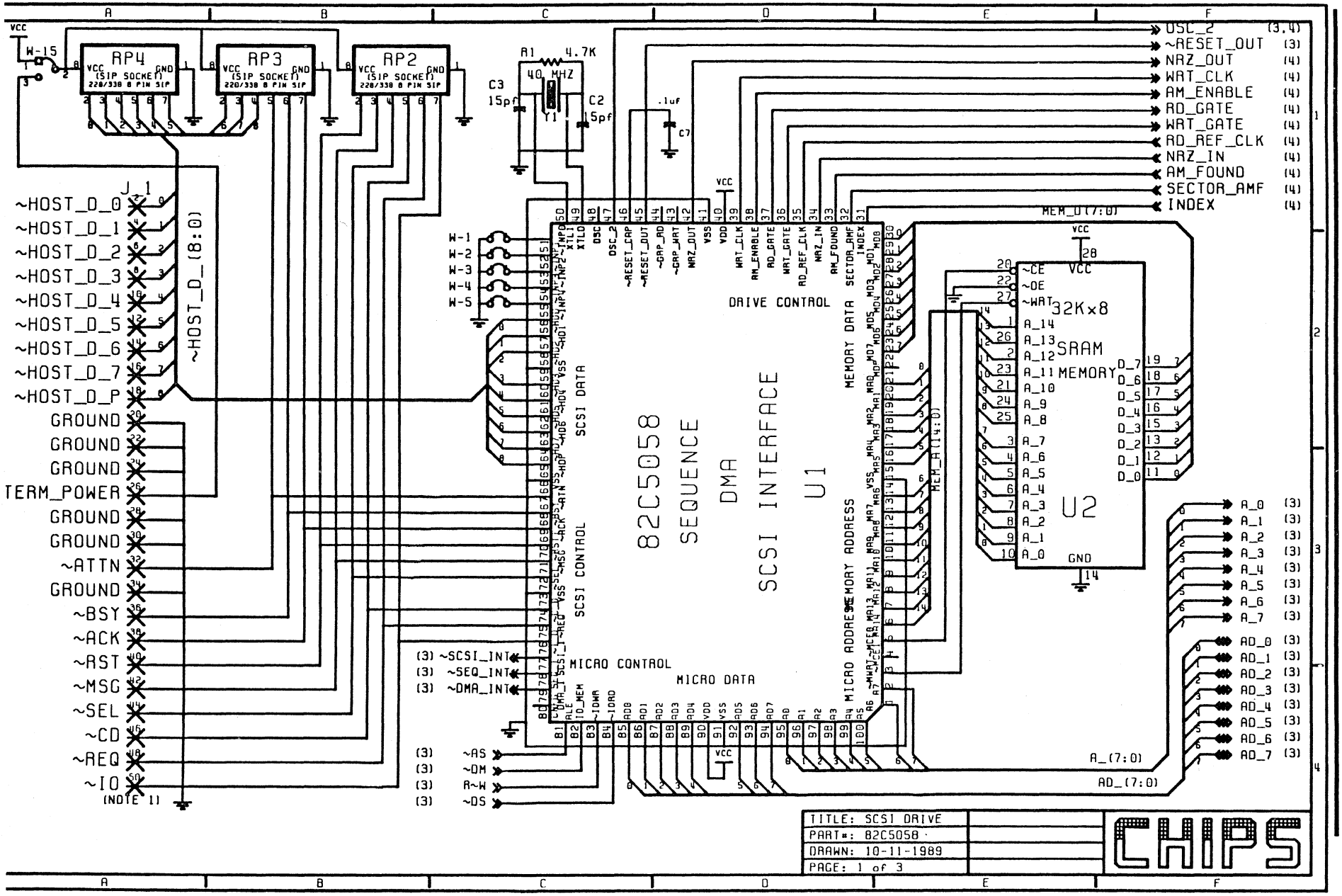
APPENDIX D

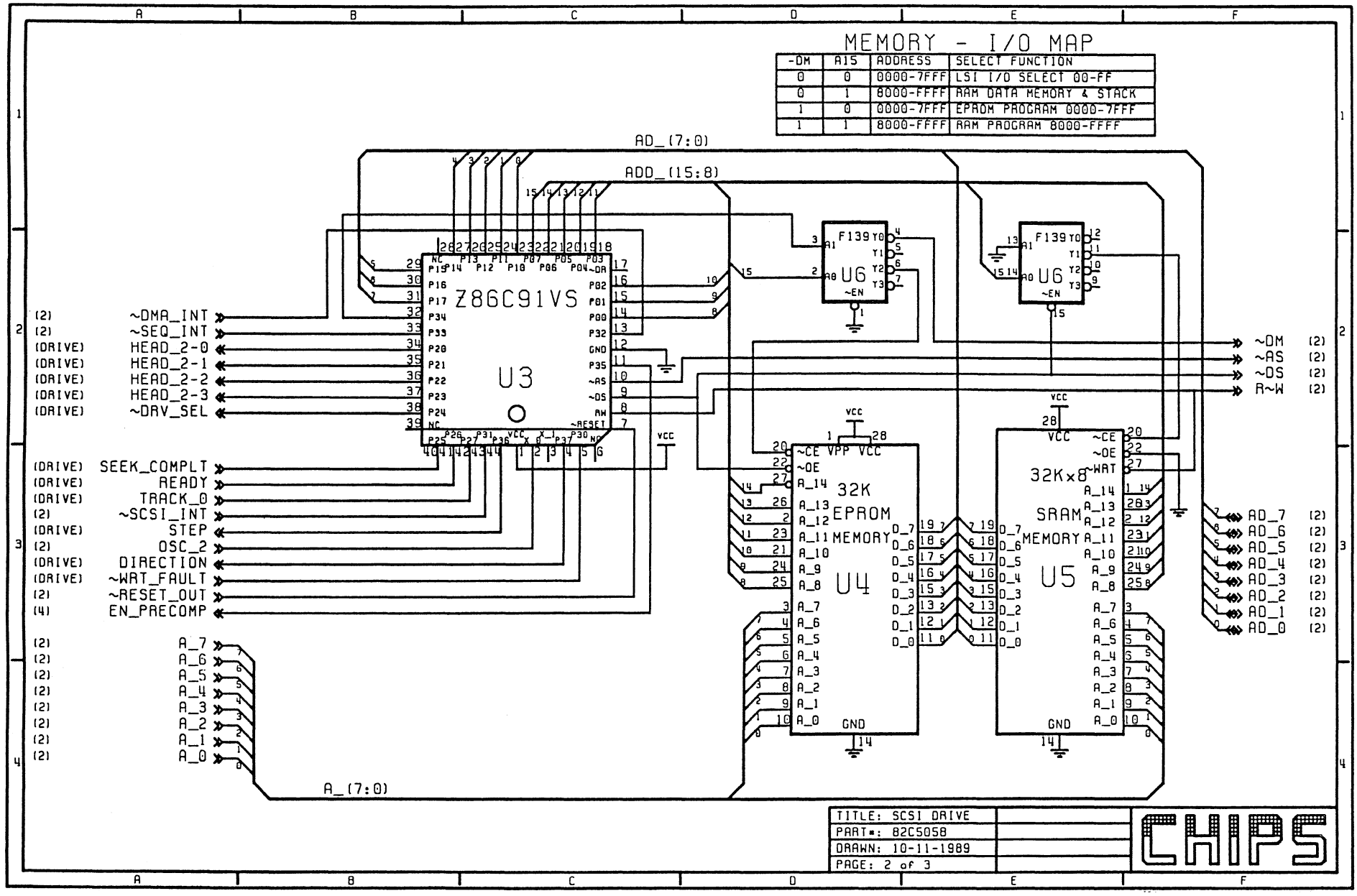
TYPICAL SYSTEM SCHEMATICS

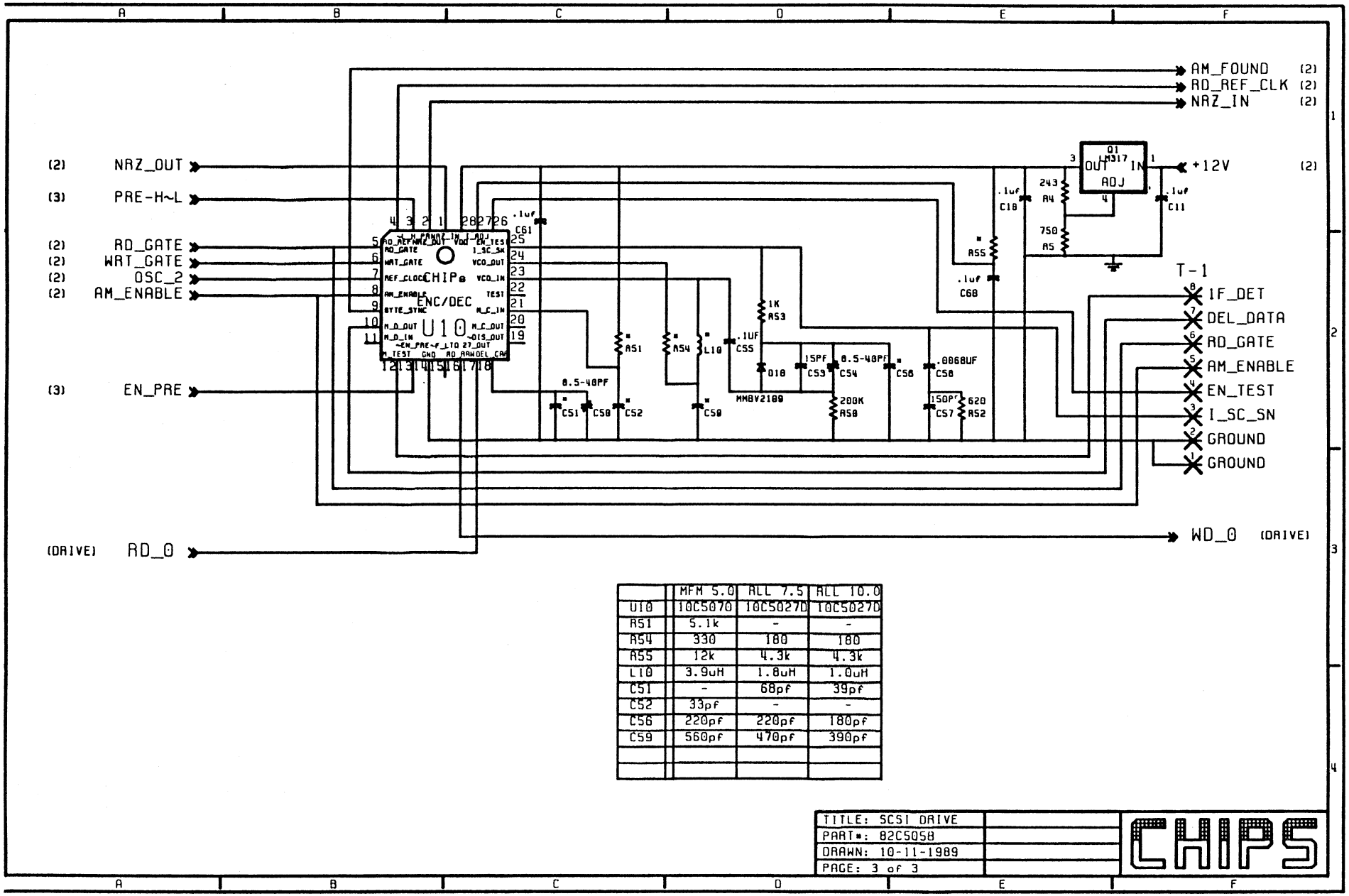
The following five pages are a set of schematics for a typical system configuration using the OMTI 5058 Memory Controller and Programmable Data Sequencer and SCSI-Bus Interface device with a RAM buffer, an OMTI data separator device , and a microcomputer with a (P)ROM and RAM.

There are three RAM buffer option configurations provided, a 64K x 9 DRAM,256K x 9 DRAM, and 64K x 8 SRAM configuration.

Figures D-1 thru D-3 appear on the following three pages.


82C5058
SEQUENCE
DMA
SCSI INTERFACE
U1
SCSI DATA
SCSI CONTROL
MICRO CONTROL
MICRO DATA
MICRO ADDRESS
MEMORY ADDRESS
MEMORY DATA
DRIVE CONTROL
32K×8
SRAM
MEMORY
U2
RP4
RP3
RP2
(SIP SOCKET)
220/330 8 PIN SIP
W-15
A1 4.7K
40 MHZ
Y1
C3 15pf
C2 15pf
.1uf
C7
J_1
~HOST_D_(8:0)
~HOST_D_0
~HOST_D_1
~HOST_D_2
~HOST_D_3
~HOST_D_4
~HOST_D_5
~HOST_D_6
~HOST_D_7
~HOST_D_P
GROUND
TERM_POWER
~ATTN
~BSY
~ACK
~RST
~MSG
~SEL
~CD
~REQ
~IO
(NOTE 1)
W-1
W-2
W-3
W-4
W-5
OSC_2 (3,4)
~RESET_OUT (3)
NRZ_OUT (4)
WRT_CLK (4)
AM_ENABLE (4)
RD_GATE (4)
WRT_GATE (4)
RD_REF_CLK (4)
NRZ_IN (4)
AM_FOUND (4)
SECTOR_AMF (4)
INDEX (4)
MEM_D(7:0)
MEM_A(14:0)
A_(7:0)
AD_(7:0)
(3) ~SCSI_INT
(3) ~SEQ_INT
(3) ~DMA_INT
(3) ~AS
(3) ~DM
(3) R~W
(3) ~DS
TITLE: SCSI DRIVE
PART#: 82C5058
DRAWN: 10-11-1989
PAGE: 1 of 3
CHIPS


MEMORY - I/O MAP
-DM | A15 | ADDRESS | SELECT FUNCTION
0 | 0 | 0000-7FFF | LSI I/O SELECT 00-FF
0 | 1 | 8000-FFFF | RAM DATA MEMORY & STACK
1 | 0 | 0000-7FFF | EPROM PROGRAM 0000-7FFF
1 | 1 | 8000-FFFF | RAM PROGRAM 8000-FFFF
AD_(7:0)
ADD_(15:8)
Z86C91VS
U3
F139
U6
~EN
32K EPROM MEMORY
U4
32K x 8 SRAM MEMORY
U5
VCC
GND
(2) ~DMA_INT
(2) ~SEQ_INT
(DRIVE) HEAD_2-0
(DRIVE) HEAD_2-1
(DRIVE) HEAD_2-2
(DRIVE) HEAD_2-3
(DRIVE) ~DRV_SEL
(DRIVE) SEEK_COMPLT
(DRIVE) READY
(DRIVE) TRACK_0
(2) ~SCSI_INT
(DRIVE) STEP
(2) OSC_2
(DRIVE) DIRECTION
(DRIVE) ~WRT_FAULT
(2) ~RESET_OUT
(4) EN_PRECOMP
(2) A_7
(2) A_6
(2) A_5
(2) A_4
(2) A_3
(2) A_2
(2) A_1
(2) A_0
A_(7:0)
~DM (2)
~AS (2)
~DS (2)
R~W (2)
AD_7 (2)
AD_6 (2)
AD_5 (2)
AD_4 (2)
AD_3 (2)
AD_2 (2)
AD_1 (2)
AD_0 (2)
TITLE: SCSI DRIVE
PART#: 82C5058
DRAWN: 10-11-1989
PAGE: 2 of 3
CHIPS



	MFM 5.0	RLL 7.5	RLL 10.0
U10	10C5070	10C5027D	10C5027D
R51	5.1k	-	-
R54	330	180	180
R55	12k	4.3k	4.3k
L10	3.9uH	1.8uH	1.0uH
C51	-	68pf	39pf
C52	33pf	-	-
C56	220pf	220pf	180pf
C59	560pf	470pf	390pf

TITLE: SCSI DRIVE	
PART#: 82C5058	
DRAWN: 10-11-1989	
PAGE: 3 of 3	

CHIPS

APPENDIX E

CRYSTAL CIRCUIT APPLICATION NOTES

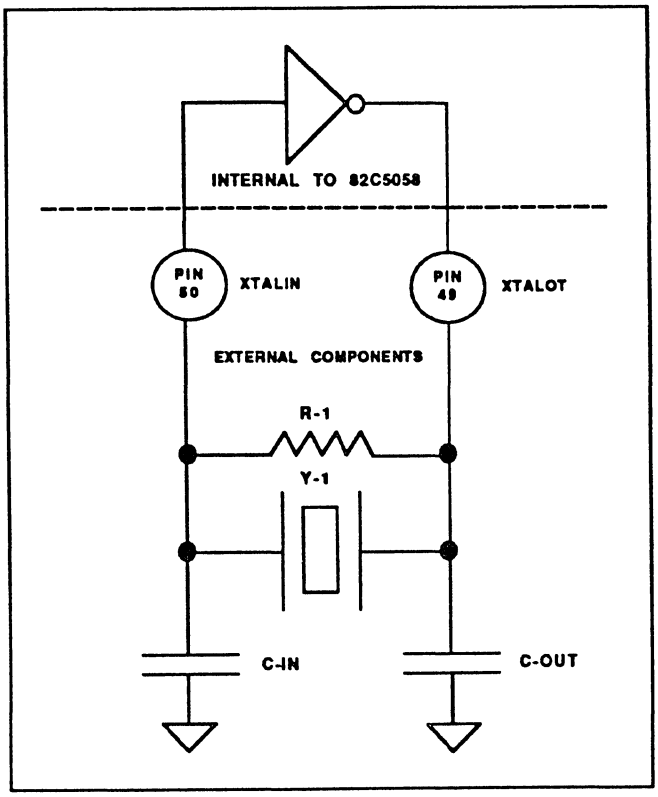


Figure E-1. 82C5058 Crystal Circuit

The crystal Y-1 should be a Series Resonance "AT" cut with an effective series resistance of less than 30 ohms.

For frequenceies less than 24 MHz, a Fundamental Crystal should be used with a R-1 value of 10 Megaohms with a C-IN and C-OUT value of typically 15pF.

For frequencies greater than 24 MHz, a Third Harmonic Crystal should be used with an R-1 value of 4.7 Kohms. The C-IN and C-OUT values are a function of the Crystal used. The most important aspect of the the capacitors are to insure a voltage out swing of at least 3.5 volts. The value of C-IN and C-OUT and their ratio control the gain of the oscillator loop.

As with all analog circuits, printed circuit board layout is very important to minimize both noise and crosstalk. The external components should be located as close as possible to the pins of the device.

A_D	address/data
address	1. a specific location in memory where a unit of data is stored. 2. A disk drive address generally specifies cylinder, head and sector.
address mark	a value used to differentiate between the ID segment and the data segment of the sector.
ANSI	American National Standard for Information Systems.
ASIC	Application Specific Integrated Circuit.
bit	an abbreviation of binary digit, of which there are two possibilities (0 and 1). A bit is the basic data unit of most digital computers. A bit is usually part of a data byte or word, but bits may be used singly to control read logic "on-off" functions.
buffer	a temporary data storage area that compensates for a difference in data transfer rates and /or data processing rates between sender and receiver.
Bus	a length of parallel conductors that forms a major interconnection route between the computer system CPU and its peripheral subsystems.
Byte	a set of binary digits (bits) handled as a unit, usually 8 bits long. One byte is necessary to define an alphanumeric character.
C	centigrade.
CAS	Column Address Strobe. A dynamic RAM input used to store the column address of the RAM matrix.
Channel	a DMA path for access to a memory device.
CMOS	Complementary Metal-Oxide Semiconductor. A technology used in the manufacture of integrated circuits.

CRC	Cyclic Redundancy Check. CRC codes are used for error detection only. Generally, redundancy for these codes is calculated by dividing the data bit stream by a polynomial with binary coefficients which is selected to provide the desired detection capability.
cylinder	a set of disk tracks that are simultaneously under a set of read/write heads. The 3-dimensional storage volume can be accessed with a single head-positioning movement.
data transfer rate	in a disk or tape drive it is the rate at which data is transferred to or from the storage media. It is usually given in thousands of bits per second (kbit/sec.) or millions of bits per second (mbit/sec.).
disk	a flat, circular piece of metal or plastic with a magnetic coating upon which information can be recorded and stored.
DMA	Direct Memory Access.
DRAM	Dynamic Random Access Memory.
ECC	Error Correction Code. Codes used for error detection.
EDAC	Error Detection And Correction.
ESDI	Enhanced Small Device Interface.
FDC	Floppy Disk Controller.
format	in a disk drive, the arrangement of data on a storage media.
head	the electromagnetic device that writes (records), reads (plays back), and erases data on magnetic media.
I/O	input/output.
ID	indentifier.
ID Header	that portion of an ID segment that identifies the cylinder head and sector.
index	usually a mechanical sensor, or an output of a mechanical sensor, on a disk drive to generate one pulse per revolution. It is utilized as a reference point on the track format.

mA	milliamp.
MAX	maximum.
MFM	Modified Frequency Modulation. A method of encoding a digital data signal for recording on magnetic media.
MHz	megahertz.
MIN	minimum.
NRZ	Non-Return to Zero.
ns	nanosecond.
parity	a computer data checking method using an extra bit in which the total number of binary 1's (or 0's) in a byte is always odd or always even; thus, in an odd parity scheme, every byte has eight bits of data and one parity bit. If using odd parity and the number of 1 bits comprising the byte of data is not odd, the 9th or parity bit is set to 1 to create the odd parity. In this way, a byte of data can be checked for accurate transmission by simply counting the bits for an odd parity indication. If the count is ever even, an error has occurred.
PIO	Parallel Input/Output .
PLCC	Plastic Leaded Chip Carrier. The 84-pin version of the 5055B is available in PLCC.
PLL	Phase Lock Loop.
postamble	the field on the track format to position a write splice.
preamble	the field on the track format used by the controller PLL to gain frequency and phase synchronization.
PROM	Programmable Read Only Memory.
QFP	Quad-plastic Flat Package.
RAM	Random Access Memory.
RAS	Row Address Strobe. Dynamic RAM input used to store the row address of the RAM matrix.
read	to access a storage location and obtain previously recorded data.

RLL2,7	Run-Length Limited. An encoding process that repositions data bits and limits the length of a string of zero bits in order to compress information being stored on disks.
ROM	Read Only Memory.
RR	Read Register.
SCSI	Small Computer System Interface.
Schmidt trigger input signal	an input device that has hysteresis to prevent a slow rise time or noise on a signal causing a glitch.
sector	one segment of a disk.
SERDES	serial to parallel and parallel to serial converter.
SRAM	Static Random Access Memory.
syndrome	1. A symbol or set of symbols containing information about an error or errors. 2. The remainder of a read long operation used to correct an error in the data field.
TA	temperature ambient.
track	recording path formed when magnetic media moves past a head. Disk tracks are shaped like concentric rings.
transfer count	a counter used to keep track of the number of bytes per sector when reading or writing data.
V	voltage.
VCO	variable control oscillator.
Vdd	drain DC voltage.
Vss	Ground.
WR	Write Register.
write	to access a storage location and store data on the magnetic surface.
-	a minus sign prefix to a signal name indicates an active low polarity.
+	a plus sign prefix to a signal name indicates an active high polarity.

INDEX I