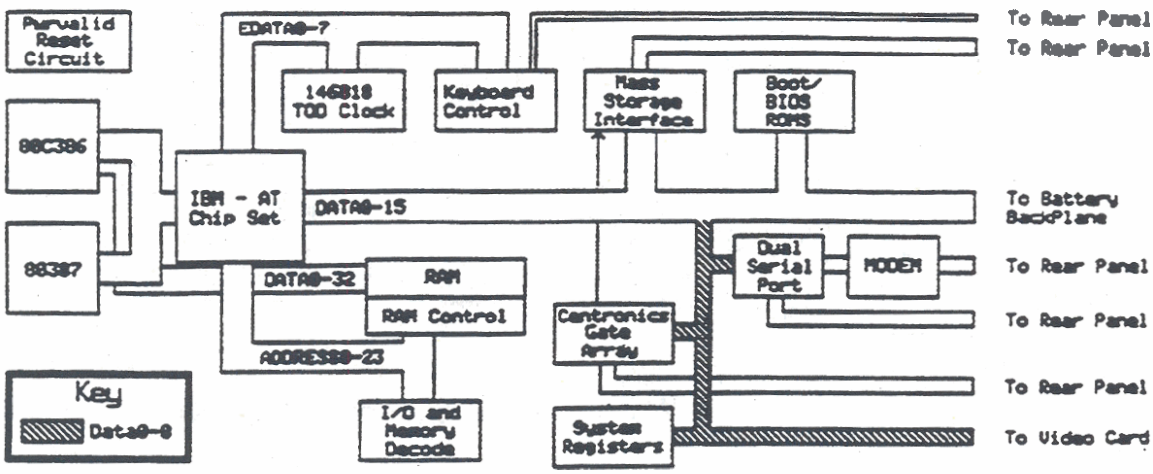
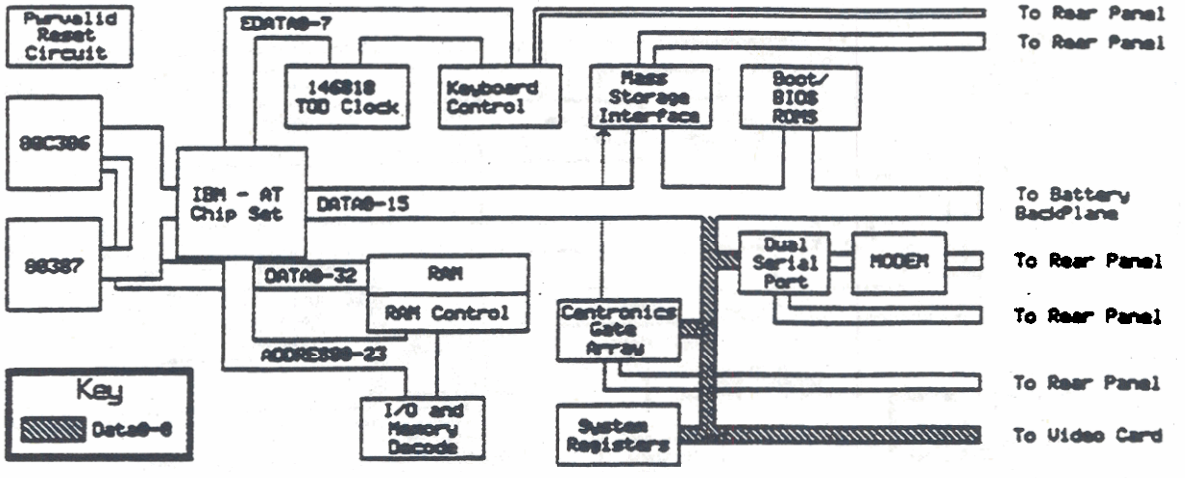
GRiDCASE 1500 Theory of Operations

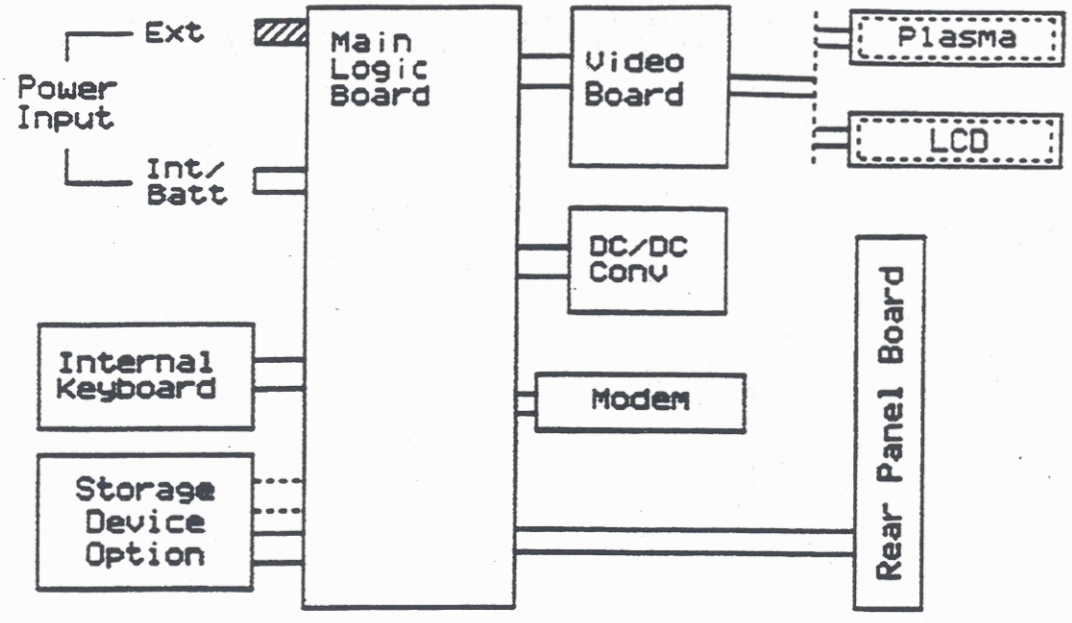
GRiDCASE 1520 Main Logic Board Block Diagram



GRiDCASE 1530 Main Logic Board Block Diagram



GRiDCASE 1500 Sub-assembly Block Diagram



Key

- Direct part to part connection
- Cable
- Optional connection

The Main Logic Board's Most Important Circuits

1. Clocks
2. Powervalid circuit
3. Microprocessors
4. IBM AT VLSI chip set
5. Decode and system registers
6. Boot ROMs
7. RAM control
8. RAM
9. 146818 time-of-day clock

Clocks

- 14.318 MHz crystal oscillator for timer/counter functions in the IBM-AT chip set
- 20 MHz clock (1520) or 25 MHz clock (1530) system clock for CPU clock generation on the IBM-AT chip set and RAM control

Powervalid Circuit

- **Purposes:**
  - **To allow system operation if the +5 and +12 volt supplies have stabilized**
  - **To initiate reset at power-on**
- **Reset is generated by the IBM AT chip set and used to initialize the CPU and other circuitry**

Microprocessors

- 80C286:
  - 16-bit data bus
  - 24-bit address bus
- 80386:
  - 32-bit data bus
  - 32-bit address bus
- After reset, the 80C86 executes the code at address FFFF0h

IBM AT Chip Set

- 4 VLSI gate arrays:
  - FE 3000 CPU controller
  - FE 3010 peripheral functions
  - FE 3020 address buffer
  - FE 3030 data buffer

FE 3000 CPU Controller

- Generates CPU clock
- Controls wait state generation
- Controls CPU cycle interruption for interrupts and DMA
- Generates CPU READY line

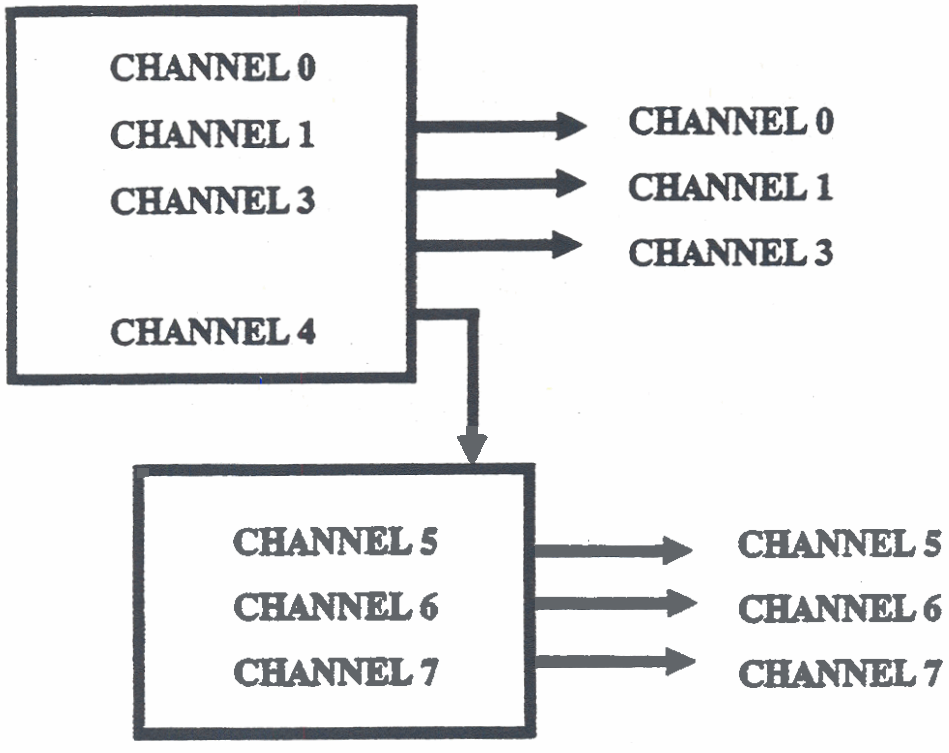
FE 3010 Peripheral Functions

- Consists of the DMA, interrupt and memory refresh generation circuitry

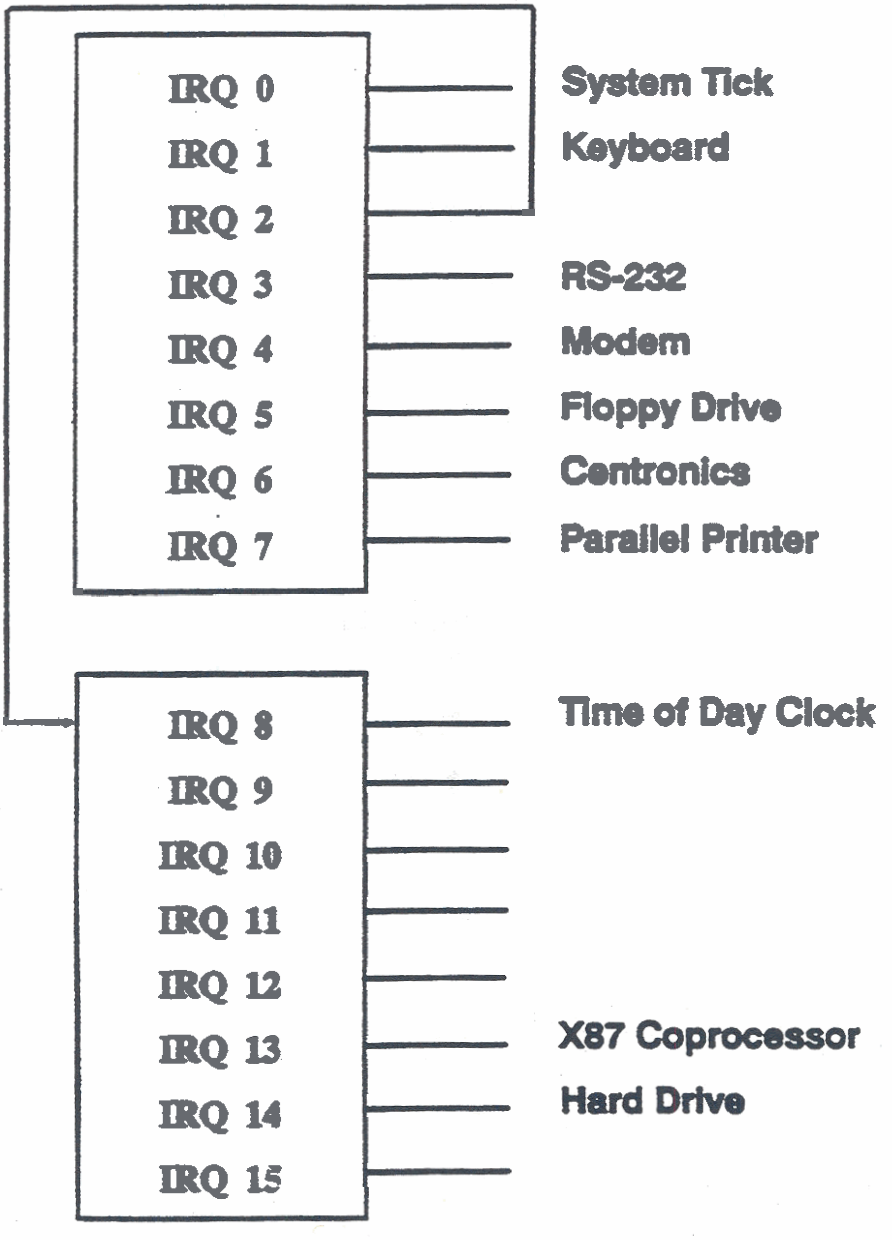
  Contains the equivalent of two 8237 DMA controllers, two 8259 interrupt controllers, and one 8254 timer/counter

- Timer/counter provides 2 functions:
  - TC1: Refresh
  - TC2: Speaker tone
- I/O ports, and interconnections of the DMA, interrupt, and timer functions emulates the same circuitry in the IBM AT.

DMA Function



Interrupt Functions



FE 3030 Data Buffer

- **Bi-directional buffered data lines DATA0-15**
- **Partially active (during I/O addressing 0-100h) buffered data lines EDATA0-7**

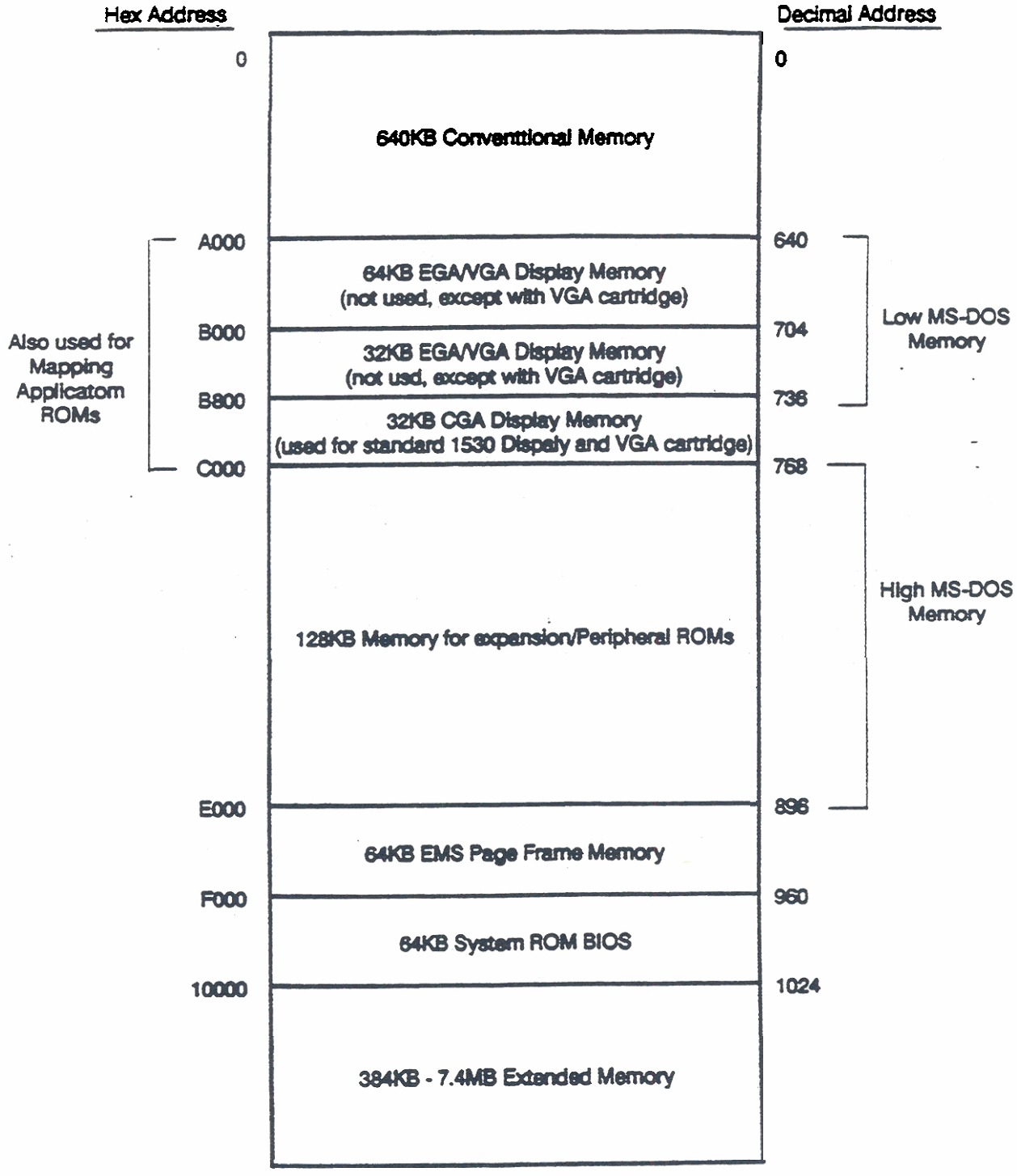
Decode/System Registers

- Decode generates chip select signals from address bus for memory and I/O activity
- The system registers are used to control some system functions:
  - serial port reset
  - applications ROM enable

System I/O MAP

000-01F	DMA control, channels 0-3
020-021h	Interrupt control, channels 0-7
040-043h	Timer/counter
060-063h	Kayboard controller
070h	NMI mask register
080-08Fh	DMA page registers
0A0-0BFh	Inrerrupt control, channels 8-15
0C0-0DFh	DMA control, channel 5-7
0F0-0FFh	80287/387 coprocessor control ports
FB-2FEh	COM2 (RS-232) serial interface
378-37Ah	Centronics parallel interface
3D0-3DFh	Video Control
3F2-3F5h	Intenal floppy disk control
3F8-3FEh	COM1 (modem) serial interface
440h	Application ROM mapping

System Memory Map



System Registers

- Control of non-AT standard system options
- On/Off condition only (DATA 0)
- I/O ports affected:

402h- application ROM size select

405h- Memsize 0

406h- Memsize 1

407h- AT or EMS

416h- CPU clock speed select (slow or fast)

420h- Modem: analog loopback mode

421h- Modem: RSSIGS

423h- Centronics port:read enable

424h- Modem: Analog to speaker enable

426h- Modem reset

427h- Modem on

Boot ROMs

- Located at F0000h to FFFFFh (conventional mode) and F0000h to FFFFFFh (virtual/protected mode) in the system memory map
- Contain the system boot/Power-On-Self-Test (POST) diagnostics firmware
- Contain the BIOS: subroutines or calls used to perform basic software functions in the system
- Contain the bootstrap loader routine
- 150ns or faster chips

System RAM

- Dynamic RAM
- 256KX8 or 1MX8 RAMsticks, 120ns or faster
- Multiplexed addressing onto the chips
- Address multiplexing and chip selects generated by RAM controller
- 1520 has 16-bit memory bus
- 1530 has 32-bit memory bus

RAM Controller

- Generates RAS and CAS address strobes and chip selects
- Facilitates refresh
- Restructures RAM access to fit IBM AT memory map
- 1520:
  - 256K RAM controller for 256K RAMsticks
  - 1M RAM controller for 1M RAM sticks
- 1530:
  - Sheppard RAM controller for either type of RAMstick

Interfaces to the Real World

- 8741 keyboard controller
- Centronics interface
- RS-232 and modem serial port s
- 146818 time of day clock chip

8741 Keyboard Controller

- Micro-controller technology
- Scans internal keyboard matrix
- Accepts input from IBM AT compatible external keyboard
- Controls EL backlight in LCD units
- Controls speaker

Centronics Interface

- Centronics parallel data I/O
- Primarily used for printer output
- Provides pocket floppy configuration information
- Gate array technology

RS-232 and Modem Serial Controller

- Asynchronous communications via the RS-232 port and Hayes compatible modem

COM1: Modem

COM2: RS-232 IBM AT compatible 9-pin port

- 1520: two 82C50 UARTs
- 1530: one VLSI dual UART

146818 Time of Day Clock Chip

- Provide time of day, date and system configuration information
- Powered by 3.6 V lithium cell when system is off

Mass Storage Interfaces

- Application ROM control
- 72065 floppy disk drive control
- Hard disk drive control

Application ROM Control

- Up to 256KB of application ROM software
- 28 - or 32-pin chips can be used
- All control circuitry on the video card

72065 Floppy Disk Drive Control

- 72065 controls the following:
  - head positioning and selection
  - drive read/write
  - DMA to and from system memory
- 72065 controller supports 3.5 and 5.25 inch, DD and HD IBM formats internally
- Disk drive selection and motor enable occurs outside the 72065
- Gate array technology provides drive and motor selection

Initialization Sequence

1. Test CMOS components (IBM AT chip set and time of day clock chip registers)

2. Test first 64KB of RAM

3. Checks video card

4. Initializes and starts hard disk drive if present

5. Determines size of RAM

6. Beeps (end of POST)

7. Scans storage devices for a valid bootstrap

Boot Sequence

System searches for DOS bootstrap in following order:

1. Application ROMs
2. Internal floppy disk drive
3. Internal hard disk drive
4. Pocket/pouch floppy drive

Theory of Operation:Other Sub-Assemblies

What are the Sub-assemblies?

- Video card
- DC/DC converter
- Display
- Keyboard
- Mass storage assembly
- Expansion bus/battery backplane

Video Card

- CGA compatible
- Consists of:
  - Video controller chip
  - 32KB video RAM
  - 32KB character generator ROM with four fonts in normal and intensity modes
  - 2 32-pin JEDEC compatible application ROM sockets

Display Modes

- Alphanumeric mode:
  - 80X25 or 40X25
  - 2 bytes/charater: 1st byte character, 2nd byte attribute
  - Monochrome on internal monitir with underline available
  - Character generator is used in this mode
- Default mode for MS-DOS/COMMAND.COM
- 320x200 Graphics mode
  - 4 color graphics
  - 4 pixels per byte (2 bits/pixel)
  - video RAM divided into two blocks
  - 1st block: even scan lines
  - 2nd block: odd scan lines
- 640X200 Graphics Mode

- Each bit of each video memory byte displayed:left to right, MSB to LSB
- Video RAM divided into two blocks...
- 1st block: even scan lines
- 2nd block: odd scan lines

- 640X400 graphics mode:
  - Each bit of each vidieo memory byte displayed:
  - -left to right
  - -MSB to LSB
- Video RAM divided into four blocks:
  - 1st block: scan lines 0, 4, 8, 12
  - 2nd block: scan lines 1, 5, 9, 13
  - 3rd block: scan lines 2, 6, 10, 14
  - 4th block: scan lines 3, 7, 11, 15
  - IBM, AT&T, and Toshiba 640X400 display modes supported

DC/DC Converter

- 2 types of DC/DC converter used to support LCD and plasma displays
- Input 9 to 20 volts
- 4 inputs:

LCD/4-OUTPUT	
For Hard Drive	+ 12V
Logic Board, Hard Drive	+ 5V
LCD, Modem	- 24V
El Backlite	- 100V
PLASMA/4-OUTPUT	
Plasma	+ 33V
Hard Drive	+ 12V
Logic Board, Hard Drive	+ 5V
Modem, Display	- 15V

Display

- 640 by 400 pixel
- 1:1 pixel aspect ratio
- EL backlit in LCD models

Internal Keyboard

- Internal keyboard is a switch matrix
- Completely passive

Mass Storage Assembly

- 1 of the 5 following options:
  - Two 1.44MB FDDs
  - One 1.44MB and one 20MB HDD
  - One 40MB HDD
  - One 1.44MB FDD and 1/2 height 40MB HDD
  - One 100MB HDD
- Each configuration reqires an appropriate backplane

Application ROMs

- User accessable application ROMs
- 28-pin or 32-pin ROMs:
  - 32KB, 64KB or 128KB EPROMs
  - 128KB masked ROMs

Expansion Bus/Battery Backplane

Supply IBM XT and AT expansion buses

- Provide for user OEM cartridge peripherals